RL78/G23

Hardware Design Guide

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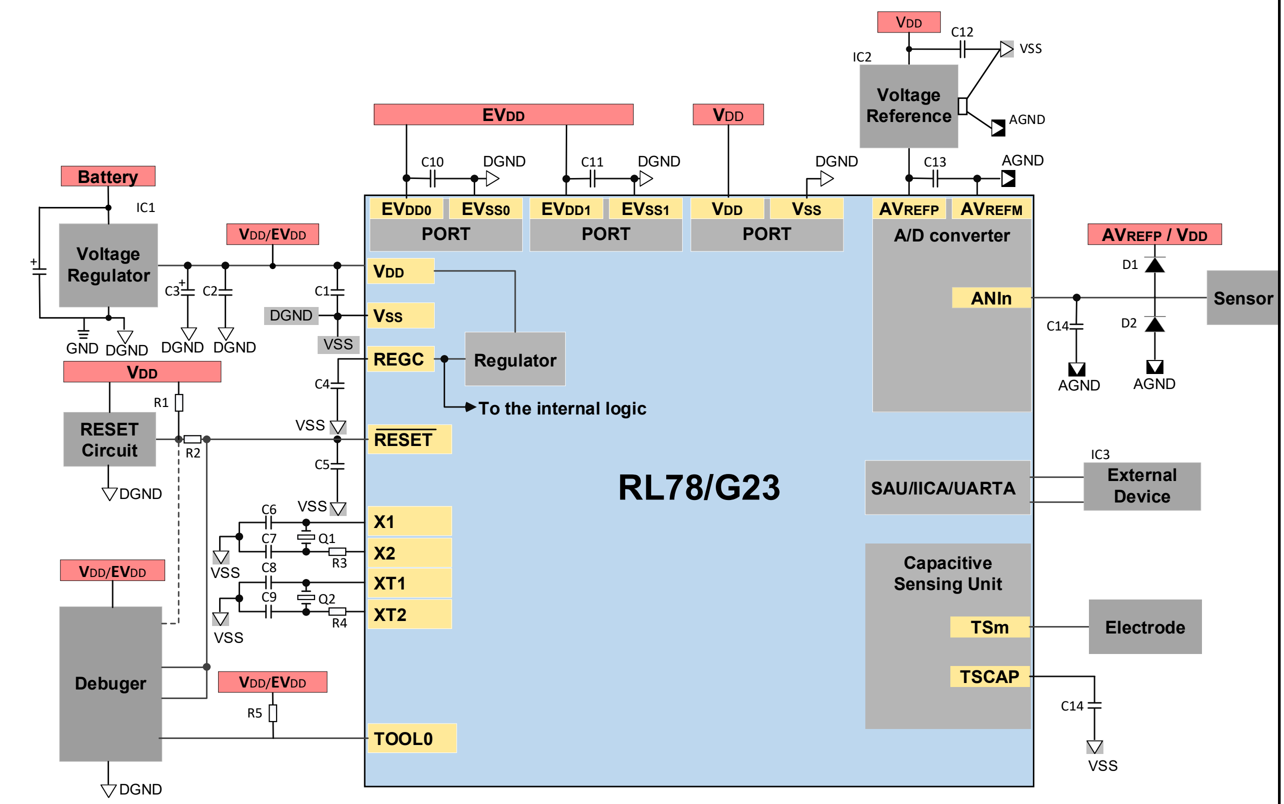
Introduction

This document is intended to provide the hardware specific information and recommendations on RL78/G23 usage. It should be used in conjunction with the Hardware User's Manual (includes the electrical characteristics).

Contents

1. Typical Circuit Schematic

Figure 1 shows the typical circuit schematic for the RL78/G23. And Table 1 shows the minimum external components list on Figure 1.



Caution 1. The above figure illustrates the major circuit schematic for the target device (RL78/G23). For unused pins, follow the section related to recommended connection of unused pins in each hardware user's manual.

Caution 2. For the QFN package product, solder the exposed die pad to the PCB.

Caution 3. Available functions depend on the product. For details, check RL78/G23 hardware user's manual.

Figure 1: Typical Circuit Schematic for the RL78/G23

Table 1: Minimum External Components List

Category	Components	Value (Typ.)	Purpose	Remark	Supplement
Power supply	IC1	No recommended IC	Generating power supply for V_{DD}	Depends on the user system.	1.1
	C1	0.1 μF	Bypass capacitor	Reference value. Place it as short and equidistant from the V_{DD} and V_{SS} pins as possible.	
	C2, C3	No recommended value	Stabilizing the output voltage of the voltage regulator	Follow the recommendation of the data sheet of the voltage regulator IC.	
	C4	0.47 μF to 1.0 μF	Stabilizing the internal regulator output voltage	Place REGC and V_{DD} pins as short as possible.	1.2
	C10	0.1 μF	Bypass capacitor	Reference value. Place it as short and equidistant from the EV_{DD0}, EV_{SS0} pins as possible.	–
	C11	0.1 μF	Bypass capacitor	Reference value. Place it as short and equidistant from the EV_{DD1}, EV_{SS1} pins as possible.	
RESET	R1	1.0 kΩ	Pull-up resistor	Depends on the external reset circuit.	1.3
	C5	0.1 μF	Stabilizing the reset output voltage level	Reference value. Place RESET and V_{SS} pins as short as possible.	
Oscillator circuit (Main system clock)	Q1	1.0 MHz to 20.0 MHz	Generating clock signal source for the main system clock	Customers are requested to consult the resonator manufacturer to select an appropriate resonator and to determine the proper oscillation constant. Connect the GND side of C6 and C7 to the V_{SS} pin as short as possible.	1.4.1 1.4.2
	C6, C7	No recommended value			
	R3	No recommended value			
Oscillator circuit (Subsystem clock)	Q2	32.768 kHz	Generating clock signal source for the subsystem clock	Customers are requested to consult the resonator manufacturer to select an appropriate resonator and to determine the proper oscillation constant. Connect the GND side of C8 and C9 to the V_{SS} pin as short as possible.	1.4.1 1.4.3
	C8, C9	No recommended value			
	R4	No recommended value			
A/D converter	IC2	No recommended IC	Voltage reference	Depends on the user system.	1.6
	C12	No recommended value	Bypass capacitor	Depends on the external voltage reference IC.	
	C13	0.1 μF	Bypass capacitor	Place AV_{REFP} and AV_{REFM} pins as short as possible.	
	D1, D2	$V_F \leq 0.3$ V	Noise protection	Depends on the user system.	
	C14	10 pF to 0.1 μF	Stabilizing the sampling operation	Depends on the user system. Place the ANIn and V_{SS} pins as short as possible.	
Debug	R2	10 kΩ	Current limit between Reset circuit and Debugger	Depends on the external reset circuit.	1.7
	R5	1.0 kΩ	Pull-up resistor	Be sure to pull-up this pin externally when on-chip debugging is enabled (pulling it down is prohibited).	
SAU/IICA	IC3	No recommended IC	Controlling external device	Depends on the user system.	–
Capacitive Sensing Unit	C14	10 nF	Stabilizing the measurement secondary power	Place TSCAP and V_{DD} pins as short as possible.	–

1.1 Power Supply Circuit

1.1.1 Power Supply Pin

Connect the power supply pin to GND via a bypass capacitor. For the bypass capacitor, use a capacitor with good frequency characteristics such as a ceramic capacitor. Also, wire the power supply pin (+ side), bypass capacitor, and paired power supply pin (- side) as short and equidistant as possible. Bypass capacitors should always be connected to pairs of power supply pins. For example, the V_{DD} and V_{SS} pins, the EV_{DD0}/EV_{DD1} and EV_{SS0}/EV_{SS1} pins, and the AV_{REFP} and AV_{REFM} pins form a pair. Wire the pattern of the power supply pin with a pattern that is thicker than the other signal lines. Also, please design this product as EV_{DD0} = EV_{DD1} and V_{SS} = EV_{SS0}/EV_{SS1} as shown in "Figure 1 Typical Circuit Schematic for the RL78/G23".

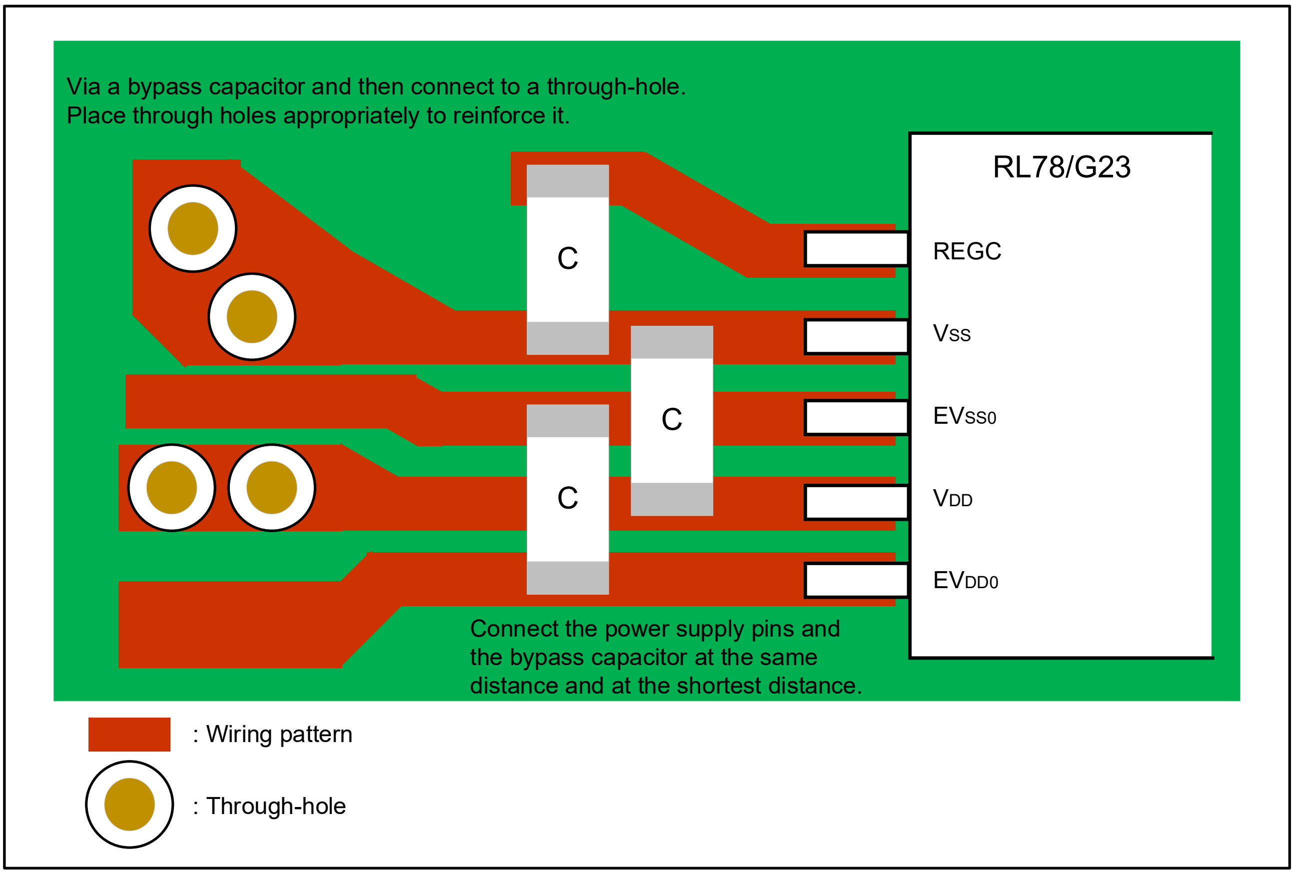
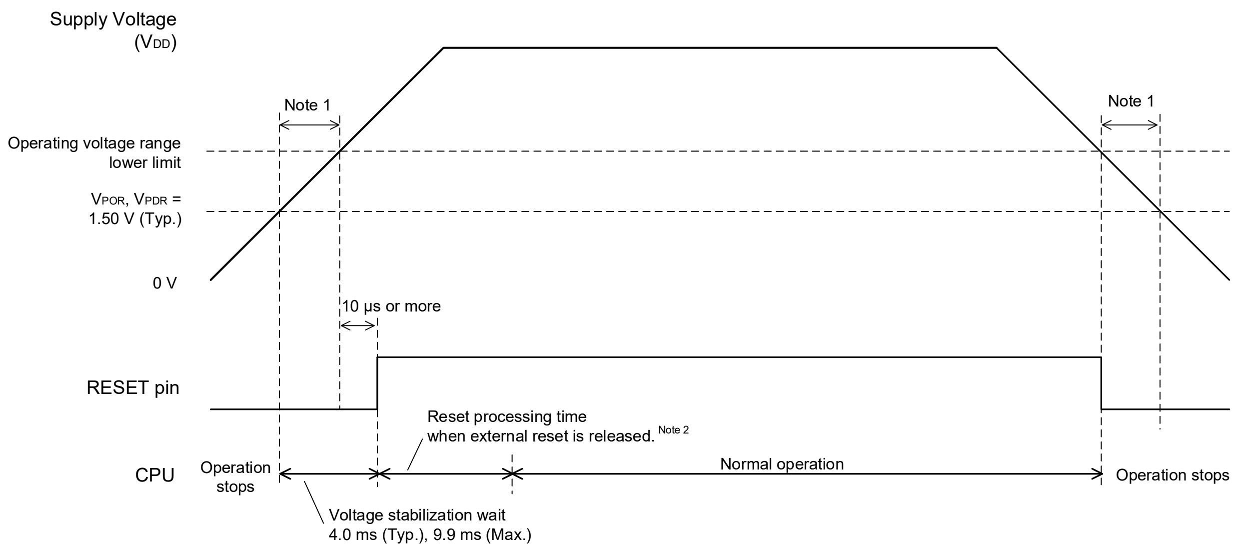


Figure 2: Connection Example of Power Supply Pin and Bypass Capacitor

1.1.2 Power Supply Timing

Please note that power supply timing according to the following use case.

(1) When the externally input reset signal on the RESET pin is used.



Note 1. After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in the AC characteristics in the ELECTRICAL SPECIFICATIONS of the Hardware User's Manual. This is done by controlling the externally input reset signal. After power supply is turned off, this LSI should be placed in the STOP mode, or in the reset state by utilizing the voltage detection circuit or externally input reset signal, before the voltage falls below the operating range. When restarting the operation, make sure that the operation voltage has returned within the range of operation.

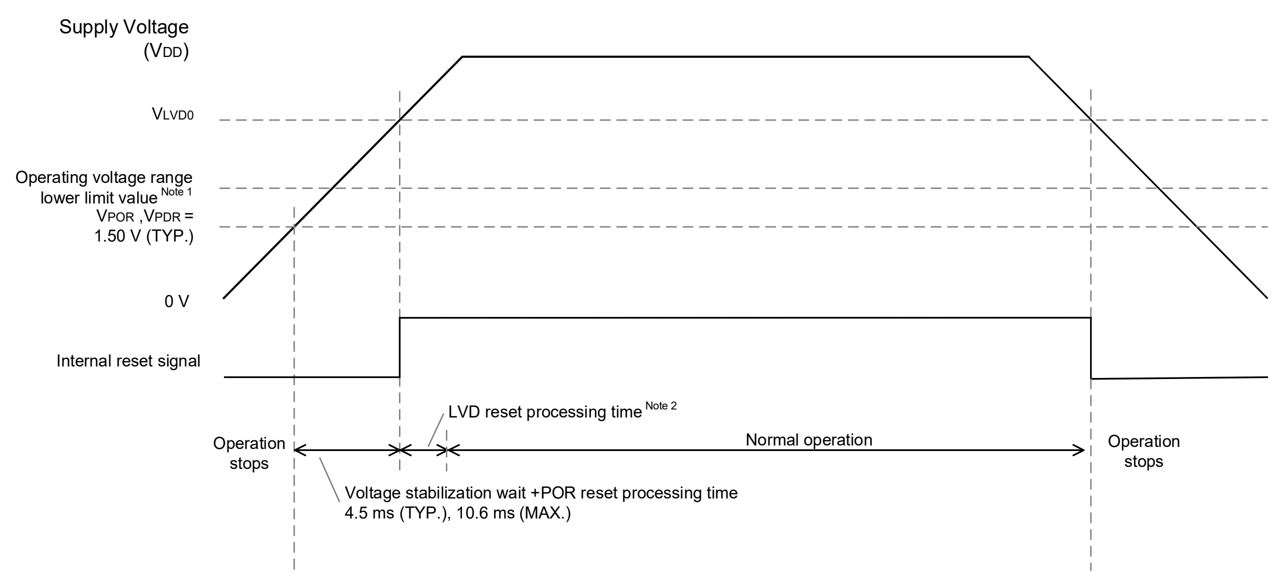
Note 2. The time until normal operation starts includes the following reset processing time when the external reset is released (after the first release of POR) after the RESET signal is driven high (1) as well as the voltage stabilization wait time after V_{POR} (1.50 V, TYP.) is reached. Reset processing time when the external reset is released is shown below.

Release from the first external reset following release from the POR state:
0.506 ms (TYP.), 0.694 ms (MAX.) (when the LVD is in use)
0.201 ms (TYP.), 0.335 ms (MAX.) (when the LVD is off)

Remarks V_{POR}: POR power supply rise detection voltage, V_{PDR}: POR power supply fall detection voltage

Figure 3: Power Supply Timing using the Externally RESET Circuit

(2) When LVD0 is in use (reset mode).



Note 1. The operating voltage range is determined by the operating frequency and flash operating mode. Only proceed with normal operations after V_{DD} has reached the operating voltage range. If an operation may be generated at outside the operating voltage range when the supply voltage falls or power-on, use the reset function of the voltage detector 0, or input the low level to the RESET pin.

Note 2. LVD reset processing time: 0 ms to 0.041 ms (MAX.)

Remarks V_{LVD0}: LVD0 detection voltage
V_{POR}: POR power supply rise detection voltage, V_{PDR}: POR power supply fall detection voltage

Figure 4: Power Supply Timing using LVD0

1.2 REGC Pin

RL78/G23 contain a circuit for operating the device with a constant voltage. At this time, in order to stabilize the regulator output voltage, connect the REGC pin to V_{SS} via a capacitor (0.47 μF to 1 μF). Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage. The REGC pin can be used as a reference voltage for an external circuit. An external circuit for connection to the REGC pin for this purpose must have an input impedance of at least 1.5 MΩ.

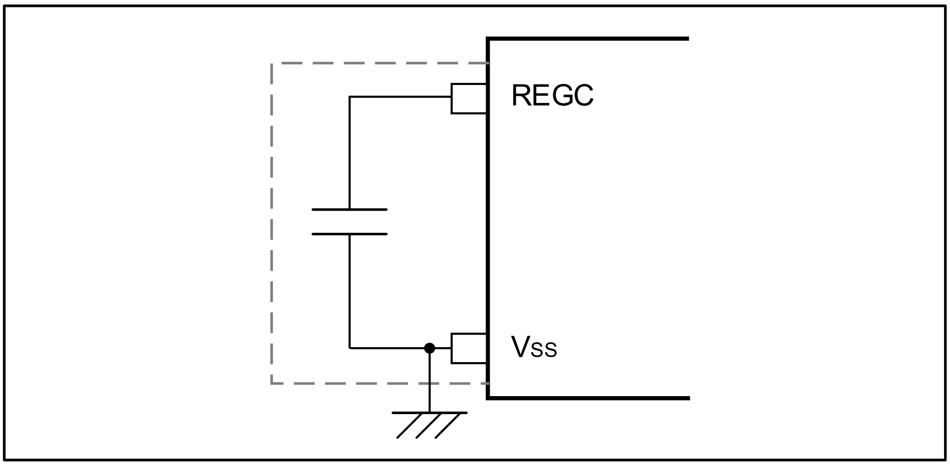


Figure 5: REGC Pin Connection

Caution Keep the wiring length as short as possible for the broken-line part in the above figure.

1.3 RESET Pin

RL78/G23 has the on-chip voltage detection circuit. Therefore, a specific external RESET circuit is not required, and the minimum requirement of the RESET circuit is a pull-up resistor R1 (1 kΩ to 10 kΩ) to V_{DD}. When using the hot plug-in, place a ceramic capacitor C5 (about 0.1 μF) close to the RESET pin to suppress noise to the RESET pin when the emulator is connected.

It depends on user system if RESET IC with external WDT function is necessary for a safety reason.

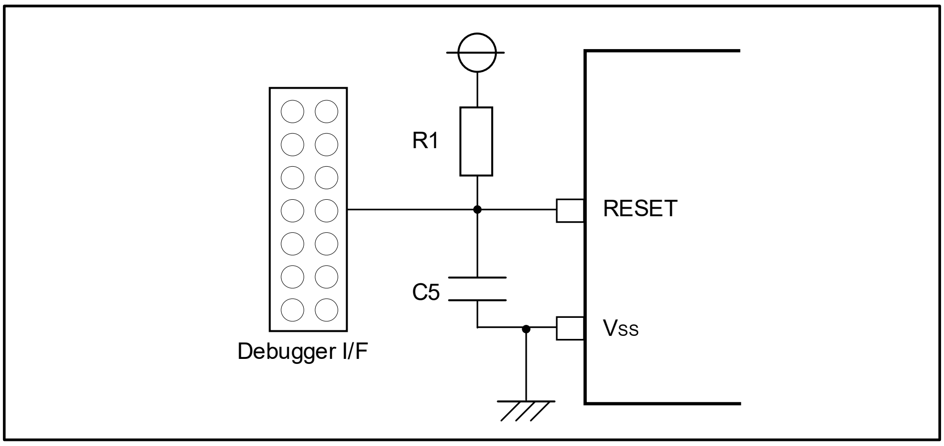


Figure 6: Minimum RESET Pin Connection (Minimum Circuit Image)

1.4 Oscillator Circuit

1.4.1 Oscillator Input/Output Pin

Wire the oscillator input/output pins (X1, X2, XT1, XT2) as short as possible, including the peripheral circuits. Also, guard the oscillator input/output pin pattern with a stable Vss pattern so that it is not adjacent to other patterns (signal lines that carry high alternating current or signal lines that switch at high speed). See “1.4.4 Common Note for Oscillator Circuit” for details.

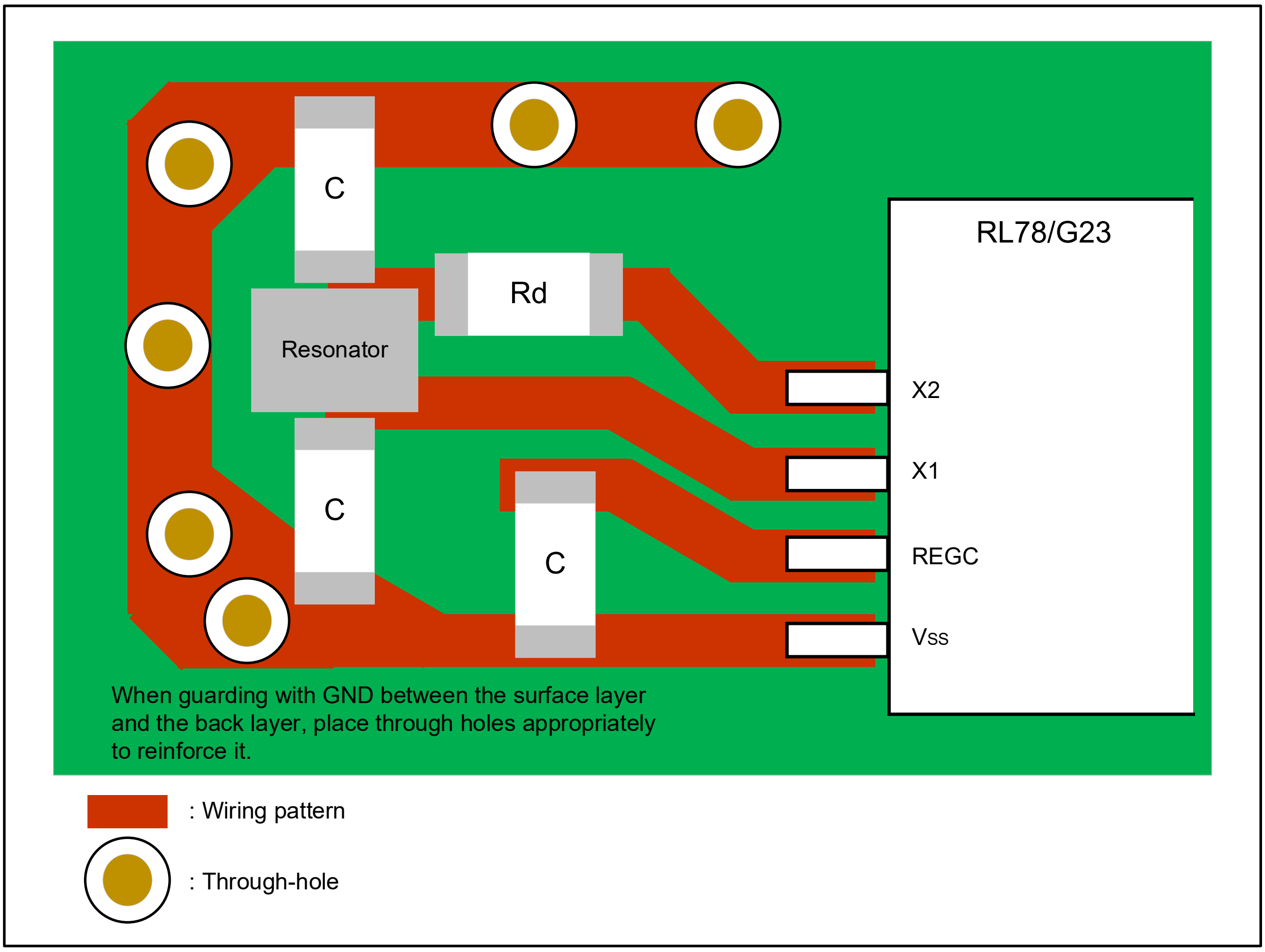


Figure 7: Connection Example of Oscillator Input/Output Circuit

1.4.2 Main System Clock

Typical circuit for the external oscillator circuit of the main system clock is illustrated below. The X1 oscillator oscillates with a crystal resonator or ceramic resonator (2 MHz to 20 MHz) connected to the X1 and X2 pins.

Please check with the manufacturer of the resonator used for the resistance and capacitance values that make up the circuit.

An external clock can also be input. In this case, input the clock signal to the EXCLK pin.

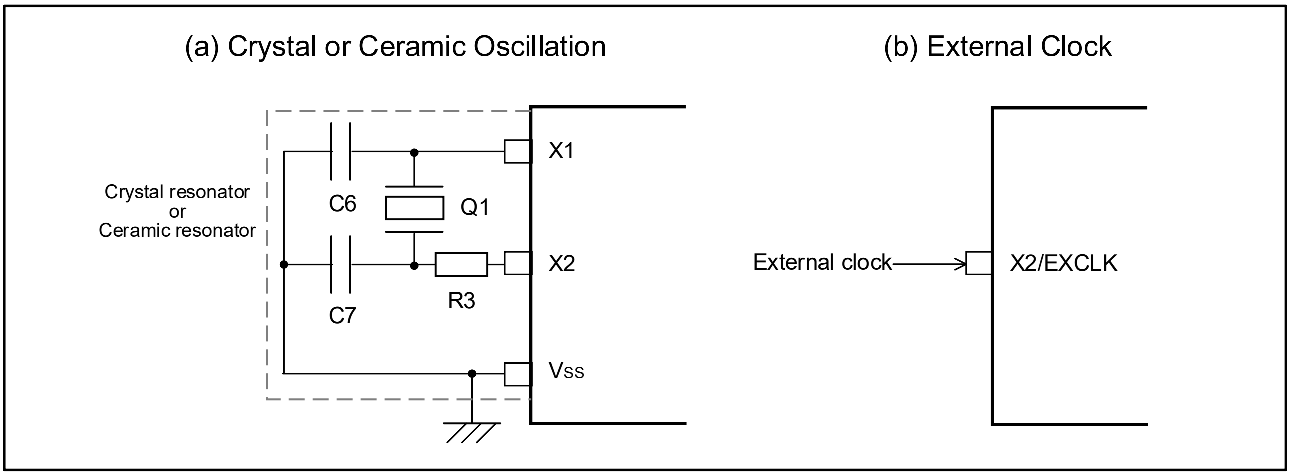


Figure 8: Main System Clock Connection

1.4.3 Subsystem Clock

Typical circuit for the external oscillator circuit of the subsystem clock is illustrated below. The XT1 oscillator oscillates with a crystal resonator (standard: 32.768 kHz) connected to the XT1 and XT2 pins.

Please check with the manufacturer of the resonator used for the resistance and capacitance values that make up the circuit.

An external clock can also be input. In this case, input the clock signal to the EXCLKS pin.

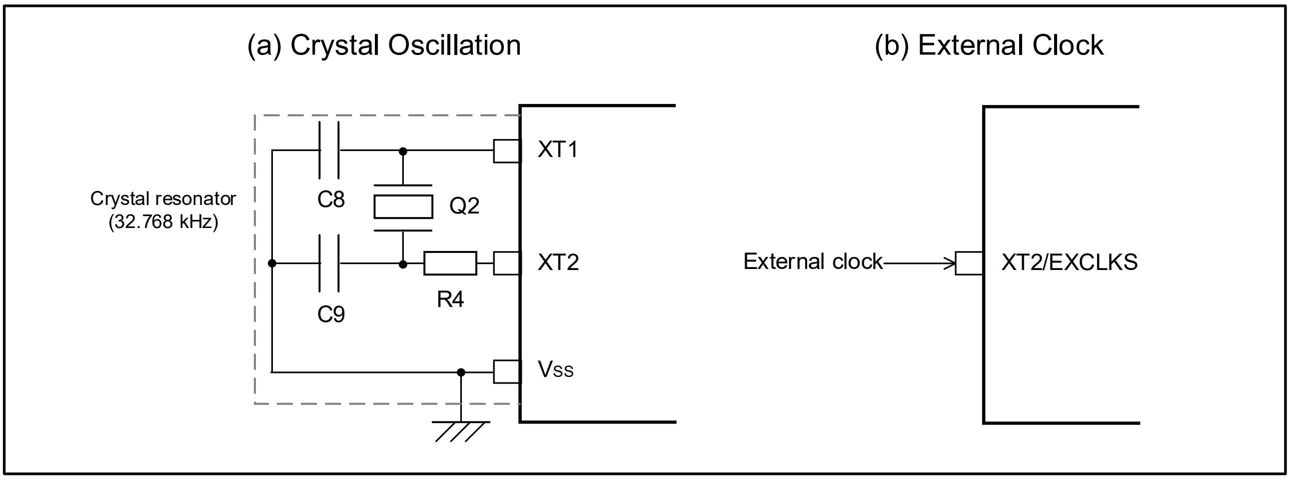


Figure 9: Subsystem Clock Connection

1.4.4 Common Note for Oscillator Circuit

Customers are requested to consult the resonator manufacturer to select an appropriate resonator and to determine the proper oscillation constant.

When using the X1 oscillator and XT1 oscillator, wire as follows in the area enclosed by the broken lines in Figure 8 and Figure 9 to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flow.
- Always make the ground point of the oscillator capacitor the same potential as V_{SS}. Do not ground the capacitor to a ground pattern through which a high current flow.
- Do not fetch signals from the oscillator.

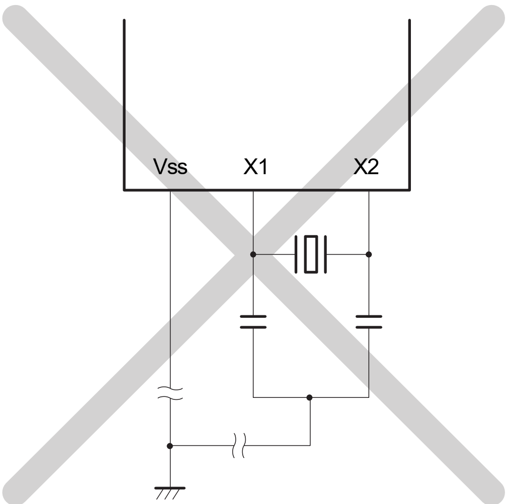
The XT1 oscillator is a circuit with low amplification in order to achieve low-power consumption.

Note the following points when designing the circuit.

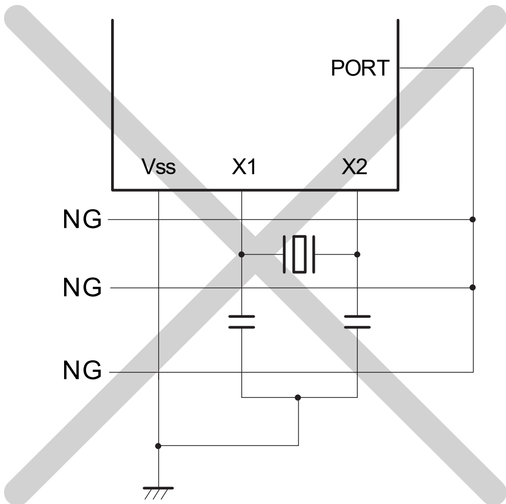
- Pins and circuit boards include parasitic capacitance. Therefore, perform oscillation evaluation using a circuit board to be actually used and confirm that there are no problems.
- Make the wiring between the XT1 and XT2 pins and the resonators as short as possible, and minimize the parasitic capacitance and wiring resistance. Note this particularly when the low power consumption oscillation 2 (AMPHS1, AMPHS0 = 1, 0) or low power consumption oscillation 3 (AMPHS1, AMPHS0 = 1, 1) is selected.
- Configure the circuit of the circuit board, using material with little wiring resistance.
- Place a ground pattern that has the same potential as VSS as much as possible near the XT1 oscillator.
- Be sure that the signal lines between the XT1 and XT2 pins, and the resonators do not cross with the other signal lines.
  Do not route the wiring near a signal line through which a high fluctuating current flow.
- The impedance between the XT1 and XT2 pins may drop and oscillation may be disturbed due to moisture absorption of the circuit board in a high-humidity environment or dew condensation on the board. When using the circuit board in such an environment, take measures to damp-proof the circuit board, such as by coating.
- When coating the circuit board, use material that does not cause capacitance or leakage between the XT1 and XT2 pins.

Examples of bad connection in oscillator circuit are shown below.

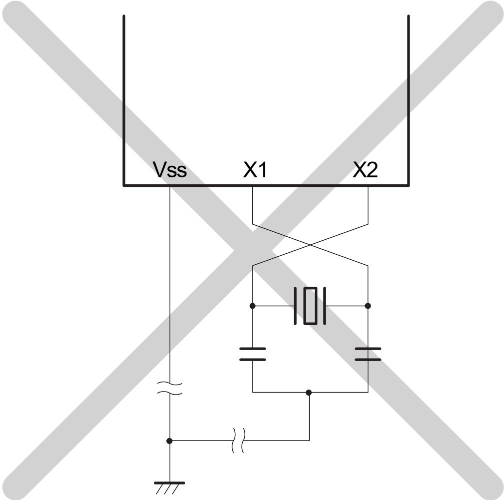
(a) Too long wiring



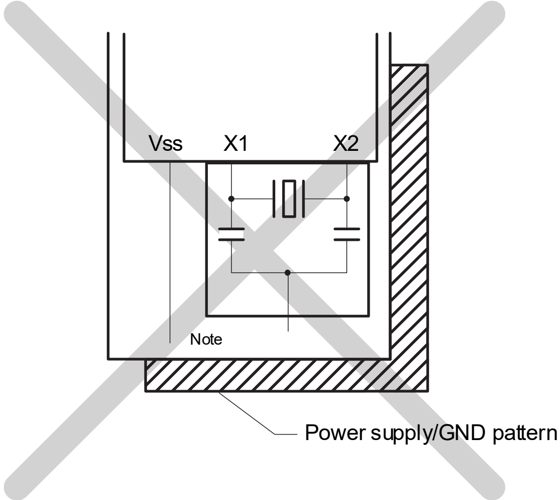
(b) Closed signal line



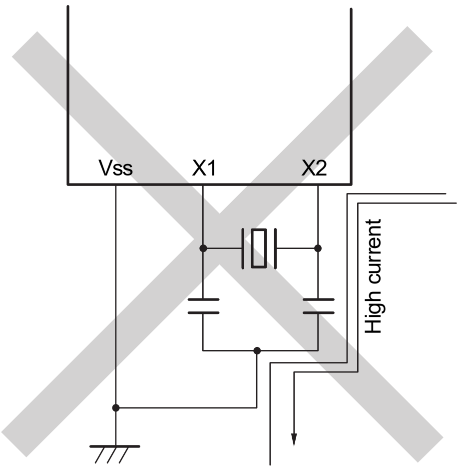
(c) The X1 and X2 signal line wires cross



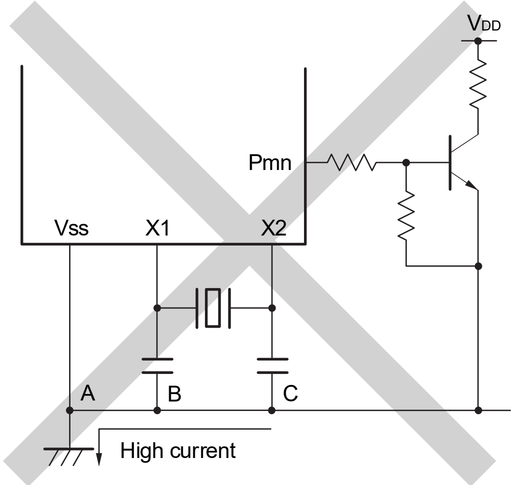
(d) A power supply/GND pattern exists under the X1 and X2 wires



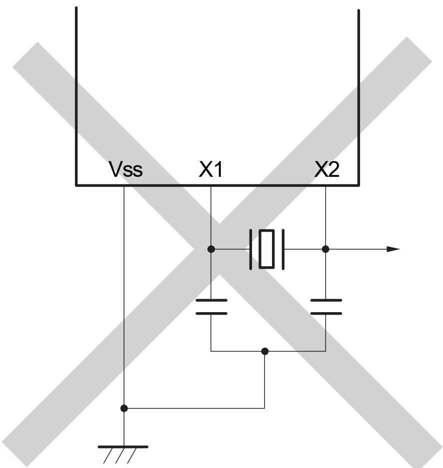
(e) Wiring near high alternating current



(f) Current flowing through ground of oscillator (potential at points A, B, and C fluctuates)



(g) Signals are fetched



Caution When X2 and XT1 are wired in parallel, the crosstalk noise of X2 may increase with XT1, resulting in malfunctioning.

Remark When using the subsystem clock, replace X1 and X2 with XT1 and XT2, respectively. Also, insert resistors in series on the XT2 side.

1.5 Note for I/O Port

1.5.1 Output Characteristics of I/O Port

The general purpose I/O of RL78/G23 products have VDD-type I/O and EVDD-type I/O.
Note that port drive current capability is different according to I/O type.

Table 2. IOH and IOL Characteristics

- Consumer application products

Port Type	Applicable General Purpose I/O	Conditions	Port Characteristics (IOH and IOL)
VDD-type	Per pin for P20-P27, P121, P122, P150-P156	4.0V ≤ V_{DD} ≤ 5.5V	IOH2: -3.0 mA IOL2: 8.5 mA
		2.7V ≤ V_{DD} < 4.0V	IOH2: -1.0 mA IOL2: 1.5 mA
		1.8V ≤ V_{DD} < 2.7V	IOH2: -1.0 mA IOL2: 0.6 mA
		1.6V ≤ V_{DD} <1.8V	IOH2: -0.5 mA IOL2: 0.4 mA
	Total of all VDD-type pins (when duty ≤ 70%)	4.0V ≤ V_{DD} ≤ 5.5V	IOH2: -20.0 mA IOL2: 20 mA
		2.7V ≤ V_{DD} < 4.0V	IOH2: -10.0 mA IOL2: 20 mA
		1.8V ≤ V_{DD} < 2.7V	IOH2: -5.0 mA IOL2: 15 mA
		1.6V ≤ V_{DD} <1.8V	IOH2: -5.0 mA IOL2: 10 mA
EVDD-type	Per pin for P00-P07, P10-P17, P30-P37, P40-P47, P50-P57, P64-P67, P70-P77, P80-P87, P90-P97, P100-P106, P110-P117, P120, P125-P127, P130, P140-P147	1.6V ≤ V_{DD} ≤ 5.5V	IOH1: -10.0 mA IOL1: 20 mA
	Per pin for P60-P63	1.6V ≤ V_{DD} ≤ 5.5V	IOL1: 15 mA
	Total of P00-P04, P07, P32-P37, P40-P47, P102-P106, P120, P125-P127, P130, P140-P145 (when duty ≤ 70%)	4.0V ≤ V_{DD} ≤ 5.5V	IOH1: -55.0 mA IOL1: 70.0 mA
		2.7V ≤ V_{DD} < 4.0V	IOH1: -10.0 mA IOL1: 15.0 mA
		1.8V ≤ V_{DD} < 2.7V	IOH1: -5.0 mA IOL1: 9.0 mA
		1.6V ≤ V_{DD} <1.8V	IOH1: -2.5 mA IOL1: 4.5 mA
	Total of P05, P06, P10-P17, P30, P31, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100, P101, P110-P117, P146, P147 (when duty ≤ 70%)	4.0V ≤ V_{DD} ≤ 5.5V	IOH1: -80.0 mA IOL1: 80.0 mA
		2.7V ≤ V_{DD} < 4.0V	IOH1: -19.0 mA IOL1: 35.0 mA
		1.8V ≤ V_{DD} < 2.7V	IOH1: -10.0 mA IOL1: 20.0 mA
		1.6V ≤ V_{DD} <1.8V	IOH1: -5.0 mA IOL1: 10.0 mA
	Total of all EVDD-type pins (when duty ≤ 70%)	1.6V ≤ V_{DD} ≤ 5.5V	IOH1: -135.0 mA IOL1: 150.0 mA

- Industrial application products (T_A = -40 to +85℃)

Port Type	Applicable General Purpose I/O	Conditions	Port Characteristics (IOH and IOL)
VDD-type	Per pin for P20-P27, P121, P122, P150-P156	4.0V ≤ V_{DD} ≤ 5.5V	IOH2: -3.0 mA IOL2: 8.5 mA
		2.7V ≤ V_{DD} < 4.0V	IOH2: -1.0 mA IOL2: 1.5 mA
		1.8V ≤ V_{DD} < 2.7V	IOH2: -1.0 mA IOL2: 0.6 mA
		1.6V ≤ V_{DD} <1.8V	IOH2: -0.5 mA IOL2: 0.4 mA
	Total of all VDD-type pins (when duty ≤ 70%)	4.0V ≤ V_{DD} ≤ 5.5V	IOH2: -20.0 mA IOL2: 20 mA
		2.7V ≤ V_{DD} < 4.0V	IOH2: -10.0 mA IOL2: 20 mA
		1.8V ≤ V_{DD} < 2.7V	IOH2: -5.0 mA IOL2: 15 mA
		1.6V ≤ V_{DD} <1.8V	IOH2: -5.0 mA IOL2: 10 mA
EVDD-type	Per pin for P00-P07, P10-P17, P30-P37, P40-P47, P50-P57, P64-P67, P70-P77, P80-P87, P90-P97, P100-P106, P110-P117, P120, P125-P127, P130, P140-P147	1.6V ≤ V_{DD} ≤ 5.5V	IOH1: -10.0 mA IOL1: 20 mA
	Per pin for P60-P63	1.6V ≤ V_{DD} ≤ 5.5V	IOL1: 15 mA
	Total of P00-P04, P07, P32-P37, P40-P47, P102-P106, P120, P125-P127, P130, P140-P145 (when duty ≤ 70%)	4.0V ≤ V_{DD} ≤ 5.5V	IOH1: -55.0 mA IOL1: 70.0 mA
		2.7V ≤ V_{DD} < 4.0V	IOH1: -10.0 mA IOL1: 15.0 mA
		1.8V ≤ V_{DD} < 2.7V	IOH1: -5.0 mA IOL1: 9.0 mA
		1.6V ≤ V_{DD} <1.8V	IOH1: -2.5 mA IOL1: 4.5 mA
	Total of P05, P06, P10-P17, P30, P31, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100, P101, P110-P117, P146, P147 (when duty ≤ 70%)	4.0V ≤ V_{DD} ≤ 5.5V	IOH1: -80.0 mA IOL1: 80.0 mA
		2.7V ≤ V_{DD} < 4.0V	IOH1: -19.0 mA IOL1: 35.0 mA
		1.8V ≤ V_{DD} < 2.7V	IOH1: -10.0 mA IOL1: 20.0 mA
		1.6V ≤ V_{DD} <1.8V	IOH1: -5.0 mA IOL1: 10.0 mA
	Total of all EVDD-type pins (when duty ≤ 70%)	1.6V ≤ V_{DD} ≤ 5.5V	IOH1: -100.0 mA IOL1: 150.0 mA

- Industrial application products (T_A = -40 to +105℃)

Port Type	Applicable General Purpose I/O	Conditions	Port Characteristics (IOH and IOL)
VDD-type	Per pin for P20-P27, P121, P122, P150-P156	4.0V ≤ V_{DD} ≤ 5.5V	IOH2: -3.0 mA IOL2: 8.5 mA
		2.7V ≤ V_{DD} < 4.0V	IOH2: -1.0 mA IOL2: 1.5 mA
		1.8V ≤ V_{DD} < 2.7V	IOH2: -1.0 mA IOL2: 0.6 mA
		1.6V ≤ V_{DD} <1.8V	IOH2: -0.5 mA IOL2: 0.4 mA
	Total of all VDD-type pins (when duty ≤ 70%)	4.0V ≤ V_{DD} ≤ 5.5V	IOH2: -20.0 mA IOL2: 20 mA
		2.7V ≤ V_{DD} < 4.0V	IOH2: -10.0 mA IOL2: 20 mA
		1.8V ≤ V_{DD} < 2.7V	IOH2: -5.0 mA IOL2: 15 mA
		1.6V ≤ V_{DD} <1.8V	IOH2: -5.0 mA IOL2: 10 mA
EVDD-type	Per pin for P00-P07, P10-P17, P30-P37, P40-P47, P50-P57, P64-P67, P70-P77, P80-P87, P90-P97, P100-P106, P110-P117, P120, P125-P127, P130, P140-P147	1.6V ≤ V_{DD} ≤ 5.5V	IOH1: -10.0 mA IOL1: 20 mA
	Per pin for P60-P63	1.6V ≤ V_{DD} ≤ 5.5V	IOL1: 15 mA
	Total of P00-P04, P07, P32-P37, P40-P47, P102-P106, P120, P125-P127, P130, P140-P145 (when duty ≤ 70%)	4.0V ≤ V_{DD} ≤ 5.5V	IOH1: -30.0 mA IOL1: 40.0 mA
		2.7V ≤ V_{DD} < 4.0V	IOH1: -10.0 mA IOL1: 15.0 mA
		1.8V ≤ V_{DD} < 2.7V	IOH1: -5.0 mA IOL1: 9.0 mA
		1.6V ≤ V_{DD} <1.8V	IOH1: -2.5 mA IOL1: 4.5 mA
	Total of P05, P06, P10-P17, P30, P31, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100, P101, P110-P117, P146, P147 (when duty ≤ 70%)	4.0V ≤ V_{DD} ≤ 5.5V	IOH1: -50.0 mA IOL1: 40.0 mA
		2.7V ≤ V_{DD} < 4.0V	IOH1: -19.0 mA IOL1: 35.0 mA
		1.8V ≤ V_{DD} < 2.7V	IOH1: -10.0 mA IOL1: 20.0 mA
		1.6V ≤ V_{DD} <1.8V	IOH1: -5.0 mA IOL1: 10.0 mA
	Total of all EVDD-type pins (when duty ≤ 70%)	1.6V ≤ V_{DD} ≤ 5.5V	IOH1: -60.0 mA IOL1: 80.0 mA

Remarks: Some general purpose I/O may not be mounted depending on the product.
P123 to P124 and P137 are input-only pins.

1.5.2 Recommended Connection of Unused Pins

Table 3 shows the recommended connections of unused pins for RL78/G23 products.

Table 3: Recommended Connection of Unused Pins

Port Type	Pin Name	Recommended Connection of Unused Pin
VDD-type	P123 to P124 (Input-only pin)	Independently connect V_{DD} or V_{SS} via a resistor. Alternatively, set the EXCLKS and OSCSELS bits in the clock operation mode control register (CMC) to 0 and 1, respectively. Set the XTSTOP bit in the clock operation status control register (CSC) to 1, and leave the pins open-circuit [Note1].
	P137 (Input-only pin)	Independently connect V_{DD} or V_{SS} via a resistor. Alternatively, set the PDIDIS137 bit in the port digital input disable register (PDIDIS13) to 1, and leave the pin open-circuit.
	All VDD-type pins except P123 to P124 and P137	Input: Independently connect to V_{DD} or V_{SS} via a resistor. [Reference resistance value: Pull-up with 20 kΩ resistor] Output: Leave open.
	RESET	Connect to V_{DD} directly or via a resistor.
EVDD-type	P40 [Note2]	Input: Independently connect to EV_{DD} via a resistor. [Reference resistance value: 1.0 kΩ] Output: Leave open.
	P130 (Output-only pin)	Leave open.
	All EVDD-type pins except P40 and P130	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. [Reference resistance value: 10 kΩ] Output: Leave open.

Note 1: When the low-speed on-chip oscillator clock (fIL) is selected for the CPU/peripheral hardware clock frequency (fCLK), the current may increase approximately by 1 μA.

Note 2: TOOL0 (On-chip debugger/Flash memory programmer interface pin) function is assigned to P40. When using TOOL0 function on the board, select an input mode and connect to EV_{DD} via a resistor (1.0 kΩ).

1.5.3 Peripheral I/O Redirection Function

Peripheral I/O pin of RL78/G23 products can be assigned using the PIOR register.

Table 4: Peripheral I/O Redirection Function

Register	Bit Symbol	Assignable Peripheral I/O Function
PIOR	PIOR5	INTP1, INTP3, INTP4, INTP6 to INTP9 (External interrupt input pin)
		SI10/SDA10/RXD1, SO10/TXD1, SCK10/SCL10 (Serial array unit I/O pin)
	PIOR4	INTP5 (External interrupt input pin)
		PCLBUZ1 (Clock output/buzzer output pin)
	PIOR3	PCLBUZ0 (Clock output/buzzer output pin)
	PIOR2	SCLA0, SDAA0 (Serial interface IICA I/O pin)
	PIOR1	INTP10, INTP11 (External interrupt input pin)
		SI00/SDA00/RXD0, SO00/TXD0, SCK00/SCL00, SI20/SDA20/RXD2, SO20/TXD2, SCK20/SCL20 (Serial array unit I/O pin)
	PIOR0	TI02/TO02 to TI07/TO07 (I/O pin of timer array unit)

1.6 Note for A/D Converter

1.6.1 Input Range of ANIn Pins

Observe the rated range of the ANIn pins input voltage. If a voltage higher than V_{DD} and AV_{REFP} and less than V_{SS} and AV_{REFM} (even in the range of absolute maximum ratings) is input to an analog input channel, the converted value of that channel becomes undefined. In addition, the converted values of the other channels may also be affected.

When internal reference voltage (1.48 V) is selected reference voltage source for the + side of the A/D converter, do not input a voltage higher than the internal reference voltage to a pin selected by the ADS register. However, it is no problem that a voltage higher than the internal reference voltage is input to a pin not selected by the ADS register.

1.6.2 Notes on Board Design

- Separate the digital power supply pattern (V_{DD}, EV_{DD0}, EV_{DD1}, V_{SS}, EV_{SS0}, EV_{SS1}) and the analog reference power supply pattern (AV_{REFP}, AV_{REFM}) and layout them with the possible thick wiring patterns.
- By preparing separate analog power supply sources (AV_{REFP}, AV_{REFM}) and digital power supply sources (V_{DD}, EV_{DD0}, EV_{DD1}, V_{SS}, EV_{SS0}, EV_{SS1}), the effects of digital power supply noise can be reduced.
- When using the analog power (AV_{REFP}, AV_{REFM}) and digital power (V_{DD}, EV_{DD0}, EV_{DD1}, V_{SS}, EV_{SS0}, EV_{SS1}) as a common power supply, separate the analog and digital power supplies at the output section of the power supply source.
- Connect the analog ground (AV_{REFM}) pattern to the stable digital ground (V_{SS}) pattern on the board at only one point to prevent a noise from the digital ground.

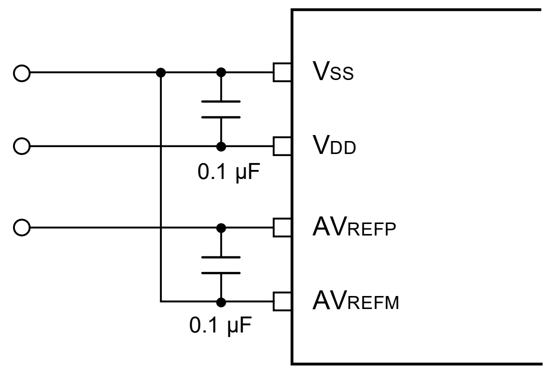


Figure 10: Power Supply Pin Connection Example

1.6.3 Noise Countermeasures

To maintain the 10-bit resolution, attention must be paid to noise input to the AV_{REFP}, V_{DD}, ANIn pins.

(1) Connect a capacitor with a low equivalent resistance and a good frequency response to the power supply.

(2) The higher the output impedance of the analog input source, the greater the influence. To reduce the noise, connecting external capacitor as shown in Figure 10 is recommended.

(3) Do not switch these pins with other pins during conversion.

(4) The accuracy is improved if the HALT mode is set immediately after the start of conversion.

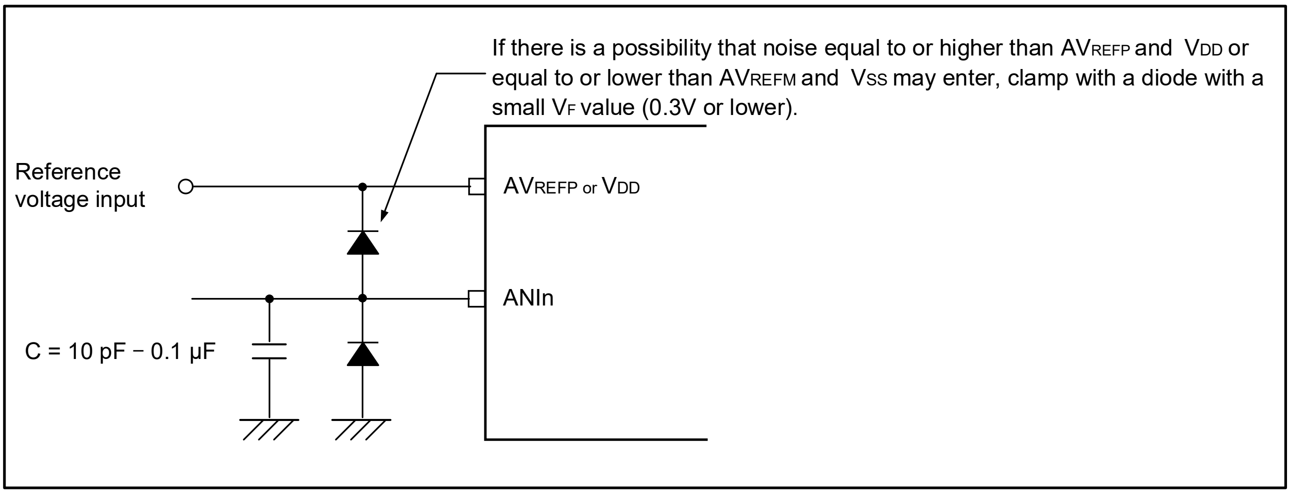


Figure 11: Sample Protection Circuit for Analog Inputs

1.6.4 Analog Input Pins (ANIn)

(1) The analog input pins (ANIn) are shared with input port pins.

Do not change the output values for the shared port-pin functions while A/D conversion of the signals on the ANIn pins is selected and conversion is in progress, since doing so may lower the precision of the results of conversion.

(2) When a pin adjacent to one on which A/D conversion is in progress is used as a digital I/O port pin, coupling may lead to noise that causes the results of A/D conversion to differ from the expected values. Be sure to prevent the input or output of pulses on such pins while conversion is in progress.

1.6.5 Input Impedance of Analog Input (ANIn) Pins

This A/D converter charges a sampling capacitor for sampling during sampling time. Therefore, only a leakage current flows when sampling is not in progress, and a current that charges the capacitor flows during sampling. Consequently, the input impedance fluctuates depending on whether sampling is in progress, and on the other states.

To make sure that sampling is effective, however, it is recommended to keep the output impedance of the analog input source to within 1 kΩ, and to connect a capacitor of about 0.1 µF to the ANIn pins (Figure 11).

1.6.6 Internal Equivalent Circuit

The equivalent circuit of the analog input section is shown below.

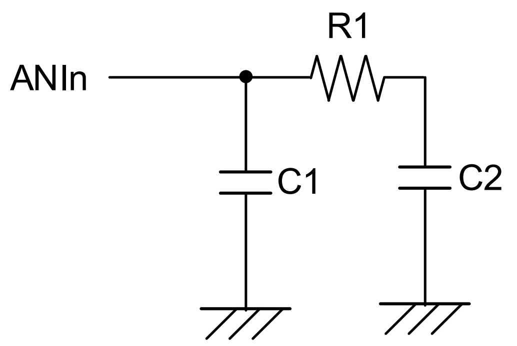


Figure 12: Equivalent Circuit of ANIn Pins

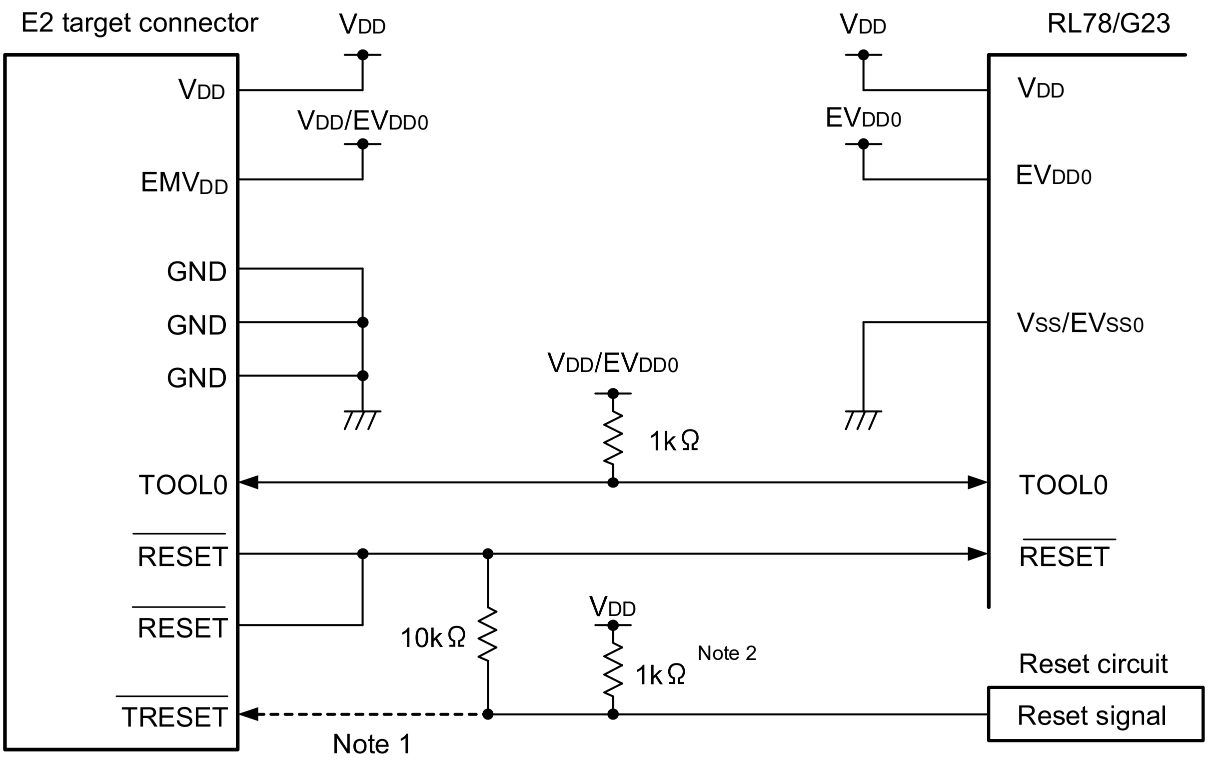
Table 5: Example of the Specifications of the Internal Equivalent Circuit

AV_{REFP}, V_{DD}	ANIn	R1 [kΩ]	C1 [pF]	C2 [pF]
2.4 V ≤ VDD ≤ 5.5 V	ANI0 to ANI14	11	8	9
	ANI16 to ANI26	12	8	10
1.8 V ≤ VDD < 2.4 V	ANI0 to ANI14	55	8	9
	ANI16 to ANI26	60	8	10
1.6 V ≤ VDD < 1.8 V	ANI0 to ANI14	110	8	9
	ANI16 to ANI26	120	8	10

Note: The values of these parameters are for reference only and are not guaranteed.

1.7 On-chip Debug Circuit

RL78/G23 uses the V_{DD}, EV_{DD0}, RESET, TOOL0, and V_{SS} pins to communicate with the host machine via an E2/E2 LITE on-chip debugging emulator. Serial communication is performed by using a single-line UART that uses the TOOL0 pin. For detail, refer “E1/E20/E2 Emulator, E2 Emulator Lite Additional Document for User’s Manual (Notes on Connection of RL78)” (Document No. R20UT1994EJ).



Note 1. Connecting the dotted line is not necessary during flash programming.

Note 2. If the reset circuit on the target system does not have a buffer and generates a reset signal only with resistors and capacitors, this pull-up resistor is not necessary.

Caution This circuit diagram is assumed that the reset signal outputs from an N-ch O.D. buffer (output resistor: 100 Ω or less).

Figure 13: Connection Example of E2 On-chip Debugging Emulator

Related Documents

Document Name	Document No
RL78/G23 User’s Manual: Hardware	R01UH0896E
E1/E20/E2 Emulator, E2 Emulator Lite Additional Document for User’s Manual (Notes on Connection of RL78)	R20UT1994E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar 13, 2024	–	First issue

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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