

RL78/G1H, RAA604S00

Control method of RF front-end components

Introduction

This document describes the control method when using RL78/G1H (LSI chip for sub-GHz-band wireless communications) and RF front-end components such as switches and amplifiers, and the parameter setting method using the RF driver.

Although it describes RL78/G1H, RAA604S00 can control RF front-end components by the same method.

Note: The contents of this document are provided as an example for reference and do not guarantee the signal quality in systems. When implementing this example into an existing system, thoroughly evaluate the product in the overall system and apply the contents of this document at your own responsibility.

Target Device

RL78/G1H

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1. Overview

When designing a board using RL78 / G1H and RF front-end components, RF front-end components must be properly controlled.

The RF driver provided by our company has parameters (<u>I</u>nformation <u>B</u>ase) for controlling the RF front-end components. In order to properly control the RF front-end components, the user should set the IB value according to the RF front-end components to be used.

This document explains the IB of the RF driver and introduces connection examples between the RL78/G1H and RF front-end components.

2. IB Setting

Table 1 shows IB parameters for controlling the RF front-end components implemented in the RF driver.

IB name	Related Pin	Description	Settable range(%)	Initial value(※) (No IB setting)
phyAgcWaitGainOffset	_	RX waiting gain adjustment RX level threshold adjustment	Decimal 0 to 31 [dB]	0
		(When using external LNA)	Hexadecimal 0x00 to 0x1F [dB]	0x00
phyCcaVth	-	CCA level threshold setting (When using external LNA)	Hexadecimal only 0x0100 to 0x01FF [dBm] (-256 to -1dBm)	0x01AA (-86 dBm)
nhu(Cca)/thOffset	yCcaVthOffset - CCA level threshold adjustment (When using external LNA)		Decimal 0 to 31 [dB]	0
phyocavitionset			Hexadecimal 0x00 to 0x1F [dB]	0x00
phyAntennaSwitchEna	yAntennaSwitchEna GPIO4 ANTSW function enable External transmit amplifier		Decimal 0 or 1	0
	(ANTSW)	enable signal	Hexadecimal 0x00 or 0x01	0x00
	witchEnaTiming GPIO4 Timing adjust of external (ANTSW) transmit amplifier enable signal		Decimal 1 to 340 [us]	300
phyAntennaSwitchEnaTiming			Hexadecimal 0x0001 to 0x0154 [us]	0x012C
phyAntennaSelectTx	phyAntennaSelectTx GPIO1/2 GPIO1/2		Decimal 0 or 1	la sut se de
		RF switch control signal	Hexadecimal 0x00 or 0x01	Input mode
phyGpio0Setting	GPIO0	GPIO0 output setting	Decimal 0 or 1	Input mode
phyopiolocially			Hexadecimal 0x00 or 0x01	
nhu/Chio3Sotting	GPIO3	CPIO2 output setting	Decimal 0 or 1	
phyGpio3Setting	GFIUS	GPIO3 output setting	Hexadecimal 0x00 or 0x01	Input mode

Table 1 IB parameters



phyRssiOutputOffset	-	RSSI and ED value adjustment	Decimal 0 to 31 [dB]	0
		(When using external LNA)	Hexadecimal 0x00 to 0x1F [dB]	0x00

(※) Refer to the API specification for the settable range and initial value.



2.1 phyAgcWaitGainOffset

This is the IB for setting RX waiting gain and RX level threshold, and it is the parameter that needs to be adjusted when an external receive LNA is used.

When using this IB, set in decimal or hexadecimal. The settable range is 0 to 31 / 0x00 to 0x1F [dB].

RX waiting gain is the receiver gain when waiting for a signal. RX waiting gain is optimized so that even low power signals can be detected. If the receiver gain increases due to the use of LNA, adjustment to lower RX waiting gain of RL78/G1H is necessary.

RX level threshold is a judgment value to compare the RSSI of the received signal with this threshold (register setting value) and discard the signal below the set value. When the receiver gain increases due to the use of LNA, an offset occurs in the RSSI value, so "RX level threshold" adjustment is required.

When the value is set in this IB, this offset is automatically corrected to RX waiting gain and RX level threshold.

Refer to section 3.1 and 3.2 of the application note (R01AN3849) for details on the adjustment method.

2.2 phyCcaVth

This is the IB for setting CCA level threshold, and it is the parameter that needs to be adjusted when an external receive LNA is used.

When using this IB, set in hexadecimal . The settable range is 0x0100 to 0x01FF (-256 to -1) [dBm]. Set the CCA level threshold in bits [8: 0] (set by 2's complement). Set bit [15: 9] to 0.

CCA is a function that performs receive power detection before starting transmission and is used to judge whether or not transmission should be performed when power exceeding the CCA level threshold exists.

When the value is set in this IB, CCA level threshold offset value in Chapter 2.3 is automatically corrected. For example, if CCA level threshold is set to -86dBm and the offset is 17dB, -69dBm is set as CCA level threshold for RL78/G1H. CCA level threshold of the antenna terminal is -86dBm.

CCA level threshold for RL78/G1H : -86(dBm) + 17(dB) = -69dBm

2.3 phyCcaVthOffset

This is the IB for setting CCA level threshold offset, and it is the parameter that needs to be adjusted when an external receive LNA is used.

When using this IB, set in decimal or hexadecimal. The settable range is 0 to 31 / 0x00 to 0x1F [dB].

When the receiver gain increases due to the use of LNA, an offset occurs in the CCA/ED value, so CCA level threshold adjustment is required. The gain of the external LNA is this offset.

Refer to section 3.3 of the application note (R01AN3849) for details on the adjustment method.

2.4 phyAntennaSwitchEna

This is the IB for enable ANTSW function, and it is the parameter that must be set when an external transmission amplifier is used.

When using this IB, set in decimal or hexadecimal. The settable range is 0 or 1 / 0x00 or 0x01.

By using this IB, GPIO4 can be controlled to "TX = High" and "RX = Low". Therefore, it can be used for ON / OFF control of an external amplifier.



2.5 phyAntennaSwitchEnaTiming

This is the IB for adjusts the GPIO4 start-up timing described in Chapter 2.5. This parameter must be set when an external transmission amplifier is used.

When using this IB, set in decimal or hexadecimal. The settable range is 1 to 340 / 0x0001 to 0x0154 [us].

In order to turn on the external transmission amplifier immediately before the frame, it is necessary to adjust the startup timing.

2.6 phyAntennaSelectTx

This is the IB for sets the GPIO1 / 2 output, and it is the parameter that must be set when an external RF switch is used.

When using this IB, set in decimal or hexadecimal. The settable range is 0 or 1 / 0x00 or 0x01.

By using this IB, GPIO1 / 2 can be controlled to "TX = High / RX = Low" or "TX = Low / RX = High". Therefore, it can be used to control an external RF switch. GPIO1 and GPIO2 are in reverse operation.

2.7 phyGpio0Setting

This is the IB for sets the GPIO0 output.

When using this IB, set in decimal or hexadecimal. The settable range is 0 or 1 / 0x00 or 0x01.

By using this IB, GPIO0 can be fixed to High or Low regardless of the TX / RX mode. Therefore, it can be used as a single antenna by fixing the control of the external RF switch for diversity.

2.8 phyGpio3Setting

This is the IB for sets the GPIO3 output.

When using this IB, set in decimal or hexadecimal. The settable range is 0 or 1 / 0x00 or 0x01.

By using this IB, GPIO3 can be fixed to High or Low regardless of the TX / RX mode. Therefore, it can be used as a single antenna by fixing the control of the external RF switch for diversity.

2.9 phyRssiOutputOffset

This is the IB for setting RSSI value and ED value offset, and it is the parameter that needs to be adjusted when an external receive LNA is used.

When using this IB, set in decimal or hexadecimal. The settable range is 0 to 31 / 0x00 to 0x1F [dB].

When the receiver gain increases due to the use of LNA, an offset occurs in the RSSI value and ED value, so when using as the RSSI value and ED value of the antenna terminal, adjustment is required. The gain of the external LNA is this offset.



3. Description example of program code

Figure 1 shows an example of program code for using the IB. This is a description example using the RF front-end module (SE2435L).

uint8 t wk8; uint16 t wk16; wk8 = 0x0D;// (13)[dB] RpSetPibReg(RP PHY AGC WAIT GAIN OFFSET, sizeof(uint8 t), &(wk8)); wk16 = 0x01AA; // (-86)[dBm] RpSetPibReq(RP_PHY_CCA_VTH, sizeof(uint16_t), &(wk16)); wk8 = 0x11: // (17)[dB] RpSetPibReq(RP PHY CCA VTH OFFSET, sizeof(uint8 t), &(wk8)); wk8 = 0x01: RpSetPibReq(RP_PHY_ANTENNA_SWITCH_ENA, sizeof(uint8_t), &(wk8)); wk16 = 0x012C: // (300)[usec] RpSetPibReg(RP PHY ANTENNA SWITCH ENA TIMING, sizeof(uint8 t), &(wk16)); wk8 = 0x00: RpSetPibReq(RP PHY ANTENNA SELECT TX, sizeof(uint8 t), &(wk8)); wk8 = 0x00: RpSetPibReq(RP_PHY_GPIO0_SETTING, sizeof(uint8_t), &(wk8)); wk8 = 0x00: RpSetPibReq(RP_PHY_GPIO3_SETTING, sizeof(uint8_t), &(wk8)); wk8 = 0x11: // (17)[dB] RpSetPibReq(RP_PHY_RSSI_OUTPUT_OFFSET, sizeof(uint8_t), &(wk8));

Figure 1 Description example of program code



4. IB setting value and GPIO operation

This chapter shows GPIO operation and GPIO operation timing according to the IB setting value.

4.1 phyAntennaSelectTx

Table 2 shows phyAntennaSelectTx setting value and GPIO1 / 2 operation, and Figure 2 shows GPIO1 / 2 timing.

phyAntennaSelectTx	GPIO0		GPIO1		GPIO2		GPIO3		GPIO4	
	TX	RX	TX	RX	TX	RX	TX	RX	TX	RX
0	-	-	High	Low	Low	High	-	-	-	-
1	-	-	Low	High	High	Low	-	-	-	-
No setting	-	-	Х	Х	Х	Х	-	-	-	-

Table 2 phyAntennaSelectTx setting value and GPIO1 / 2 operation



Figure 2 phyAntennaSelectTx setting value and GPIO1 / 2 timing



4.2 phyAntennaSwitchEna

Table 3 shows phyAntennaSwitchEna setting value and GPIO4 operation. Figure 3 shows GPIO4 timing.

Table 3 phyAntennaSwitchEna setting value and GPIO4 operation



Figure 3 phyAntennaSwitchEna setting value and GPIO4 timing



4.3 phyGpio0Setting

Table 4 shows phyGpio0Setting setting value and GPIO0 operation. Figure 4 shows GPIO0 timing.



Figure 4 phyGpio0Setting setting value and GPIO0 timing

4.4 phyGpio3Setting

Table 5 shows phyGpio3Setting setting value and GPIO3 operation. Figure 5 shows GPIO3 timing.

Та	ble 5											
phyGpio3Setting		GP	GPIO0		GPIO1		GPIO2		GPIO3		GPIO4	
phyopiosetting		TX	RX	TX	RX	TX	RX	TX	RX	TX	RX	
0		-	-	-	-	-	-	Low	Low	-	-	
1		-	-	-	-	-	-	High	High	-	-	
No setting		-	-	-	-	-	-	Х	X	-	-	
	Initial register setting											
RF mode SLEEP	IDLE	RX		IDLE	CCA	(RX)	IDLE		ТΧ	IC	DLE	
(Set to "0") GPIO3 High-Z												
(Set to "1")												
GPIO3 High-Z												

Figure 5 phyGpio3Setting setting value and GPIO3 timing



5. Connection example with RF front-end components

5.1 SPDT (2-control)

Table 6 shows the IB settings when using SPDT (2-control), and Figure 6 shows the connection example.

Table 6	IB setting value (SPDT_2-control)
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IB name	Setting value	Comment
phyAgcWaitGainOffset	No setting	
phyCcaVth	0x01AA (※)	-86 [dBm]
phyCcaVthOffset / phyRssiOutputOffset	No setting	
phyAntennaSwitchEna	No setting	
phyAntennaSwitchEnaTiming	No setting	
phyAntennaSelectTx	0x00	
phyGpio0Setting	No setting	
phyGpio3Setting	No setting	

(※) Please set an appropriate CCA threshold by the customer.



Figure 6 Connection with RL78 / G1H (SPDT_2-control)

5.2 SPDT (1-control)

Table 7 shows the IB settings when using SPDT (1-control), and Figure 7 shows the connection example.

IB name	Setting value	Comment
phyAgcWaitGainOffset	No setting	
phyCcaVth	0x01AA (※)	-86 [dBm]
phyCcaVthOffset / phyRssiOutputOffset	No setting	
phyAntennaSwitchEna	No setting	
phyAntennaSwitchEnaTiming	No setting	
phyAntennaSelectTx	0x00	
phyGpio0Setting	No setting	
phyGpio3Setting	No setting	

Table 7 IB setting value (SPDT_1-control)

(※) Please set an appropriate CCA threshold by the customer.



Figure 7 Connection with RL78 / G1H (SPDT_1-control)



5.3 DPDT (ANT1 port)

Table 8 shows the IB settings when using DPDT (ANT1 port), and Figure 8 shows the connection example.

Setting value	Comment
No setting	
0x01AA (※)	-86 [dBm]
No setting	
No setting	
No setting	
0x00	
No setting	
No setting	
	0x01AA (%) No setting No setting No setting 0x00 No setting

Table 8 IB setting value (DPDT_ANT1 port)

(※



Figure 8 Connection with RL78 / G1H (DPDT_ANT1 port)

5.4 DPDT (ANT2 port)

Table 9 shows the IB settings when using DPDT (ANT2 port), and Figure 9 shows the connection example.

IB name	Setting value	Comment
phyAgcWaitGainOffset	No setting	
phyCcaVth	0x01AA (※)	-86 [dBm]
phyCcaVthOffset / phyRssiOutputOffset	No setting	
phyAntennaSwitchEna	No setting	
phyAntennaSwitchEnaTiming	No setting	
phyAntennaSelectTx	0x01	
phyGpio0Setting	No setting	
phyGpio3Setting	No setting	
	(※	

Table 9 IB setting value (DPDT_ANT2 port)



Figure 9 Connection with RL78 / G1H (DPDT_ANT2 port)



5.5 Front-end module_SE2435L (ANT1 port) / case1

Table 10 shows the IB settings when using front-end module_SE2435L (ANT1 port), and Figure 10 shows the connection example.

	Table 10	IB setting value (SE2435L_ANT1 / case1)	
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IB name	Setting value	Comment
phyAgcWaitGainOffset	0x0D	13 [dB]
phyCcaVth	0x01AA (※)	-86 [dBm]
phyCcaVthOffset / phyRssiOutputOffset	0x11	17 [dB]
phyAntennaSwitchEna	0x01	
phyAntennaSwitchEnaTiming	0x012C	300 [us]
phyAntennaSelectTx	No setting	
phyGpio0Setting	0x00	
phyGpio3Setting	No setting	

(※



Figure 10 Connection with RL78 / G1H (SE2435L_ANT1 port / case1)

5.6 Front-end module_SE2435L (ANT1 port) / case2

Table 11 shows the IB settings when using front-end module_SE2435L (ANT1 port), and Figure 11 shows the connection example. This connection is an example of fixing ANT_SEL pin of SE2435L with H / W (GND).

Table 11IB setting value (SE2435L_ANT1 / case2)

IB name	Setting value	Comment
phyAgcWaitGainOffset	0x0D	13 [dB]
phyCcaVth	0x01AA (※)	-86 [dBm]
phyCcaVthOffset / phyRssiOutputOffset	0x11	17 [dB]
phyAntennaSwitchEna	0x01	
phyAntennaSwitchEnaTiming	0x012C	300 [us]
phyAntennaSelectTx	No setting	
phyGpio0Setting	No setting	
phyGpio3Setting	No setting	

(※) Please set an appropriate CCA threshold by the customer.





5.7 Front-end module_SE2435L (ANT2 port) / case1

Table 12 shows the IB settings when using front-end module_SE2435L (ANT2 port), and Figure 12 shows the connection example.

Table 12	IB setting value ((SE2435L_ANT2 / case1)	
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IB name	Setting value	Comment
phyAgcWaitGainOffset	0x0D	13 [dB]
phyCcaVth	0x01AA (※)	-86 [dBm]
phyCcaVthOffset / phyRssiOutputOffset	0x11	17 [dB]
phyAntennaSwitchEna	0x01	
phyAntennaSwitchEnaTiming	0x012C	300 [us]
phyAntennaSelectTx	No setting	
phyGpio0Setting	0x01	
phyGpio3Setting	No setting	

(※



Figure 12 Connection with RL78 / G1H (SE2435L_ANT2 port / case1)

5.8 Front-end module_SE2435L (ANT2 port) / case2

Table 13 shows the IB settings when using front-end module_SE2435L (ANT2 port), and Figure 13 shows the connection example. This connection is an example of fixing ANT_SEL pin of SE2435L with H / W (VDD).

Table 13	IB setting value (SE2435L_ANT2 / case2)	

IB name	Setting value	Comment	
phyAgcWaitGainOffset	0x0D	13 [dB]	
phyCcaVth	0x01AA (※)	-86 [dBm]	
phyCcaVthOffset / phyRssiOutputOffset	0x11	17 [dB]	
phyAntennaSwitchEna	0x01		
phyAntennaSwitchEnaTiming	0x012C	300 [us]	
phyAntennaSelectTx	No setting		
phyGpio0Setting	No setting		
phyGpio3Setting	No setting		
(※			



Figure 13 Connection with RL78 / G1H (SE2435L_ANT2 port / case2)



5.9 Front-end module_RFFM6907 (ANT1 port)

Table 14 shows the IB settings when using front-end module_RFFM6907 (ANT1 port), and Figure 14 shows the connection example.

Table 14 IB s	setting value ((RFFM6907_	_ANT1)
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IB name	Setting value	Comment
phyAgcWaitGainOffset	No setting	
phyCcaVth	0x01AA (※)	-86 [dBm]
phyCcaVthOffset / phyRssiOutputOffset	No setting	
phyAntennaSwitchEna	0x01	
phyAntennaSwitchEnaTiming	0x012C	300 [us]
phyAntennaSelectTx	0x00	
phyGpio0Setting	No setting	
phyGpio3Setting	No setting	

(※



Figure 14 Connection with RL78 / G1H (RFFM6907_ANT1 port)

5.10 Front-end module_RFFM6907 (ANT2 port)

Table 15 shows the IB settings when using front-end module_RFFM6907 (ANT2 port), and Figure 15 shows the connection example.

IB name	Setting value	Comment
phyAgcWaitGainOffset	No setting	
phyCcaVth	0x01AA (※)	-86 [dBm]
phyCcaVthOffset / phyRssiOutputOffset	No setting	
phyAntennaSwitchEna	0x01	
phyAntennaSwitchEnaTiming	0x012C	300 [us]
phyAntennaSelectTx	0x00	
phyGpio0Setting	No setting	
phyGpio3Setting	No setting	

Table 15	IB setting value (RFFM6907_ANT2)
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(※



Figure 15 Connection with RL78 / G1H (RFFM6907_ANT2 port)



5.11 SPDT (2-control) + external AMP

Table 16 shows the IB settings when using SPDT (2-control) + external amplifier, and Figure 16 shows the connection example.

Table 16	IB setting value (SPDT_2-control + external AMP)
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IB name	Setting value	Comment
phyAgcWaitGainOffset	0x0D (※1)	13 [dB]
phyCcaVth	0x01AA (※2)	-86 [dBm]
phyCcaVthOffset / phyRssiOutputOffset	0x11 (※1)	17 [dB]
phyAntennaSwitchEna	0x01	
phyAntennaSwitchEnaTiming	0x012C	300 [us]
phyAntennaSelectTx	0x00	
phyGpio0Setting	No setting	
phyGpio3Setting	No setting	

(X1) This value varies depending on the LNA gain and NF.

(X



Figure 16 Connection with RL78 / G1H (SPDT_2-control + external AMP)

5.12 SPDT (1-control) + external AMP

Table 17 shows the IB settings when using SPDT (1-control) + external amplifier, and Figure 17 shows the connection example.

IB name	Setting value	Comment
phyAgcWaitGainOffset	0x0D (※1)	13 [dB]
phyCcaVth	0x01AA (※2)	-86 [dBm]
phyCcaVthOffset / phyRssiOutputOffset	0x11 (※1)	17 [dB]
phyAntennaSwitchEna	0x01	
phyAntennaSwitchEnaTiming	0x012C	300 [us]
phyAntennaSelectTx	0x00	
phyGpio0Setting	No setting	
phyGpio3Setting	No setting	

Table 17 IB setting value (SPDT_1-control + external AMP)

(※1) This value varies depending on the LNA gain and NF.





Figure 17 Connection with RL78 / G1H (SPDT_1-control + external AMP)



6. Control method when using test program

This chapter explains how to control RF front-end components and how to set parameters when using a test program. Table 18 shows the test program commands corresponding to the IB setting values.

For details of the test program commands, refer to the application note of the following RF evaluation program.

RF Characteristic Evaluation Program for Renesas Sub-GHz Transceiver

IB name	Test program command	Comment	
phyAgcWaitGainOffset	tagcwgo X	Use "tagcwgo" command.	
phyCcaVth	tccavt X	Use "tccavt" command.	
phyCcaVthOffset	tccavto X	Use "tccavto" command.	
phyAntennaSwitchEna	tantsw X	Use "tantsw" command.	
phyAntennaSwitchEnaTiming	tantswti X	Use "tantswti" command.	
phyAntennaSelectTx	tantsel X	Use "tantsel" command.	
phyGpio0Setting	tgpio0 X	Use "tgpio0" command.	
phyGpio3Setting	tgpio3 X	Use "tgpio3" command.	
phyRssiOutputOffset	trssio X	Use "trssio" command.	

Table 18Test command for IB setting values

Table 19 shows a setting example when using the front-end module (configuration described in Chapter 5.7).

IB name	IB setting value	Test program command
phyAgcWaitGainOffset	0x0D	tagcwgo 0x0D
phyCcaVth	0x01AA	tccavt 0x01AA
phyCcaVthOffset / phyRssiOutputOffset	0x11	tccavto 0x11
		trssio 0x11
phyAntennaSwitchEna	0x01	tantsw 0x01
phyAntennaSwitchEnaTiming	0x012C	tantswti 0x012C
phyAntennaSelectTx	No setting	-
phyGpio0Setting	0x01	tgpio0 0x01
phyGpio3Setting	No setting	-

Table 19Test command setting example



Revision History

		Description	
Rev.	Date	Page	Summary
1.00	Dec.13.2019	-	First edition issued
2.00	Nov.30.2021	Chapter 2	Added "phyRssiOutputOffset" as IB
		Chapter 3	Added "trssio" as test program command
		Chapter 5	
		Chapter 6	



General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power is supplied until the power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

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8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a systemevaluation test for the given product.

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