

RL78/G15

Temperature Alarm Device Utilizing Comparator Function

Introduction

This application note describes how to use the comparator function of RL78/G15 to sound a buzzer (via the clock output/buzzer output control circuit) when a set temperature is exceeded by comparing the analog input voltage at the IVCMP pin with an internal reference voltage.

Target Device

RL78/G15

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

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1. Specifications

1.1 Overview of Specifications

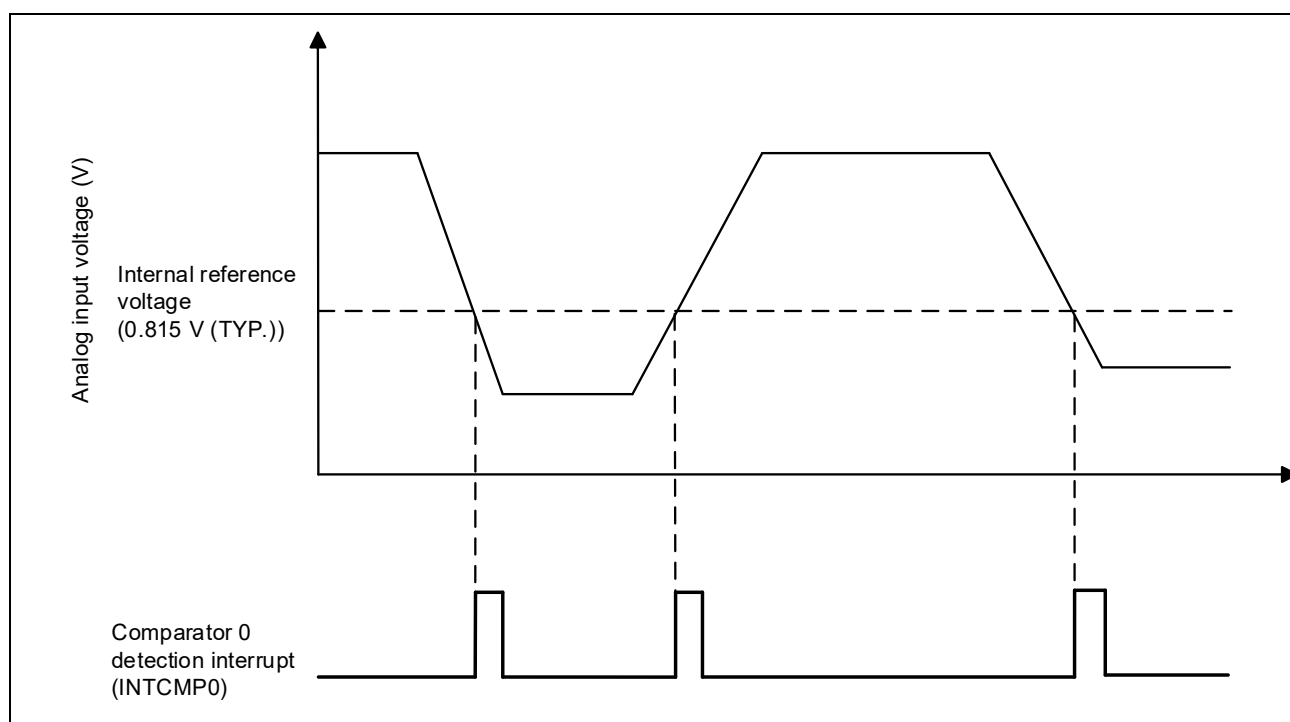
The temperature alarm is implemented by using comparator 0 in RL78/G15.

If the analog input voltage at the IVCMP0 pin drops below the internal reference voltage (0.815 V (TYP.)), the buzzer sounds. The buzzer stops when the analog input voltage exceeds the internal reference voltage.

Table 1-1 Required Peripheral Functions and Their Use

Peripheral function	Use
Comparator	Comparing input voltage and reference voltage
Buzzer output	Sounding and stopping the buzzer

Figure 1-1 Overview of Comparator 0 Operation



1.2 Overview of Operation

The comparator 0 reference voltage specified for the internal reference voltage is compared with the analog input voltage at the IVCMP0 pin.

In addition, buzzer output from the PCLBUZ0 pin is controlled by changing the PCLOE0 bit value of the clock output select register 0 according to the comparison result.

Table 1-2 Overview of Operation According to Comparison Result

Input voltage		PCLOE0
Rising	Falling	
Higher than the comparator 0 reference voltage	--	Set to 0 (output disabled)
—	Lower than the comparator 0 reference voltage	Set to 1 (output enabled)

(1) Initialize the buzzer output.

<Setting conditions>

- Use the P06 pin as the PCLBUZ0 pin.
- Set the output clock to $f_{\text{MAIN}}/2^{11} = 7.81 \text{ kHz}$.

(2) Initialize the comparator.

<Setting conditions>

- Input the analog voltage via the IVCMP0 pin.
- Set the operation mode to the comparator high-speed mode.
- Use the internal reference voltage (0.815 V (TYP.)) for the reference voltage.
- For detection, select "Comparator 0 both-edge detection".
- Set the digital filter to ON and the sampling clock to $f_{\text{CLK}}/8 = 2000 \text{ kHz}$.
- Specify "Enable comparator 0 interrupt request".
- For the interrupt priority level, select "Level 3 lowest priority (default)".
- Specify "Disable comparator 0 VCOUT0 pin output".

(3) Operation when a comparator 0 interrupt occurs

When a comparator 0 interrupt (INTCMP0) occurs, the setting value of the PCLOE0 bit of the clock output select register 0 (CKS0) changes according to the value of the comparator 0 monitor flag (COMON).

- If COMON is 0 (input voltage < comparator 0 reference voltage), PCLOE0 is set to 1 (output enabled).
- If COMON is 1 (input voltage > comparator 0 reference voltage), PCLOE0 is set to 0 (output disabled).

2. Operation Evaluate Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2-1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G15 (R5F12608ASP)
Board to be used	RL78/G15-20p Fast Prototyping Board (RTK5RLG150C00000BJ)
Operating frequency	HOCO(f_{IH}) : 16MHz
Operating voltage	5.0V (Operation is possible over a voltage range of 2.4 to 5.5V.)
Integrated development environment(CS+)	CS+ for CC V8.09.00 from Renesas Electronics Corp.
Assembler (CS+)	CC-RL V1.12.00 from Renesas Electronics Corp.
Integrated development environment (e2studio)	e2studio V2023-04(23.4.0) from Renesas Electronics Corp.
Assembler(e2studio)	CC-RL V1.12.00 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V5.10.1 from IAR Systems.
Assembler(IAR)	IAR C/C++ Compiler for Renesas RL78 V5.10.1 from IAR Systems.
Smart Configurator (SC)	V1.6.0
Board Support Package(BSP)	V1.60

3. Description of the Hardware

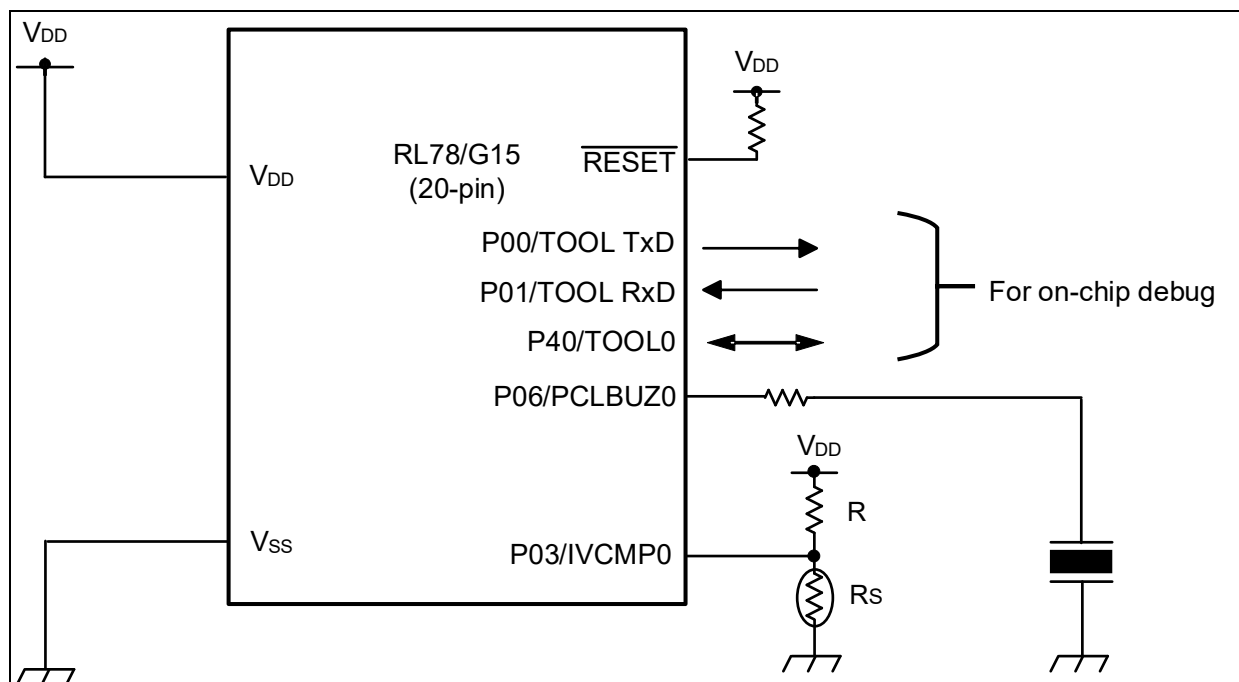
3.1 Hardware Configuration Example

Figure 3-1 shows an example hardware configuration used in this application note.

To detect temperature, an NTC thermistor is used. The voltage divider value V_t between the resistance value R_s of the thermistor and the resistance value R is input to the IVCMP0 terminal. The resistance value R can be calculated from the resistance value R_s of the thermistor for the detected temperature using the following equation.

$$0.815(V) = V_{DD} \times \{R_s / (R + R_s)\}$$

Figure 3-1 Hardware Configuration



Note. This simplified circuit diagram was created to show an overview of connections only. When actually designing your circuit, make sure the design includes appropriate pin handling and meets electrical characteristic requirements (connect each input-only port to V_{DD} or V_{SS} through a resistor).

3.2 List of Pins to be Used

Table 3-1 lists the pins to be used and their functions.

Table 3-1 Pins to be Used and their Functions

Pin Name	I/O	Description
P03/IVCMP0	Input	Analog Input for Comparator0.
P06/PCLBUZ0	Output	Buzzer Output

Note. This application note only demonstrates the handling of the used pins. When creating an actual circuit, please ensure appropriate pin handling and design the circuit to meet electrical characteristics.

4. Description of the Software

4.1 List of Option Byte Settings

Table 4-1 summarizes the settings of the option bytes.

Table 4-1 Option Byte Settings

Address	Value	Description
000C0H	11101111B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H	11110111B	At Rising: TYP. 2.90V At Falling: TYP.2.84V
000C2H	11111001B	HOCO : 16MHz
000C3H	10000101B	Enables the on-chip debugger

4.2 Function Specifications

This section describes the specifications for the functions that are used in the sample code.

r_Config_COMP0_interrupt

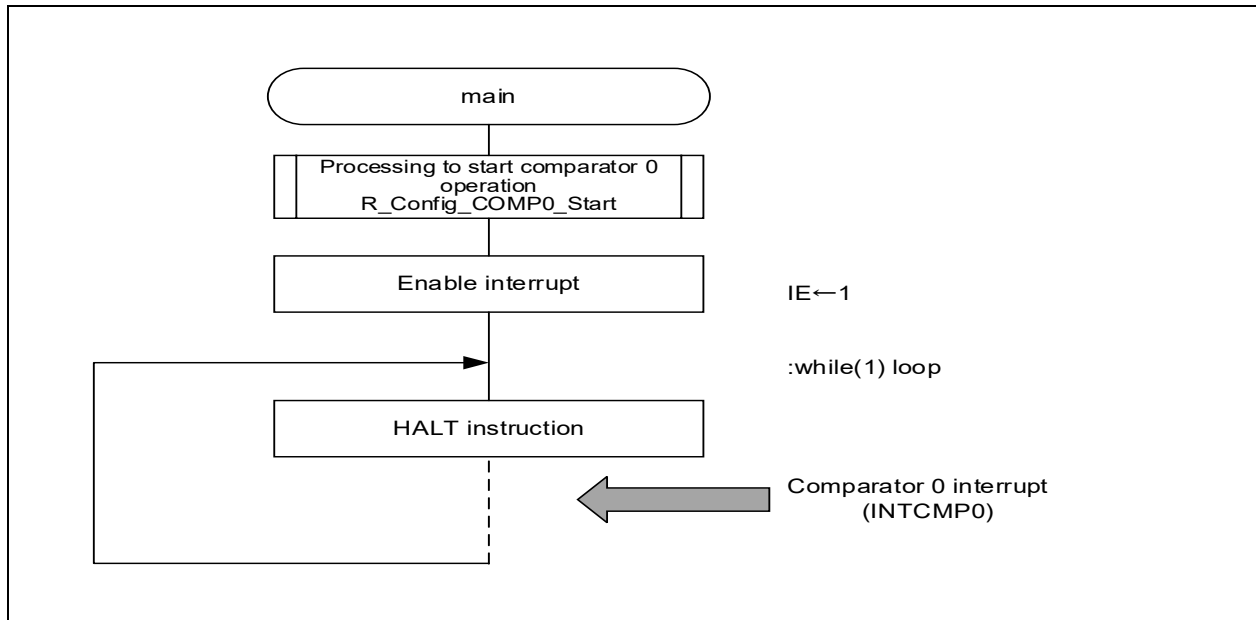
Synopsis	The interrupt handling for Comparator0.
Header	Config_COMP0.h
Declaration	static void __near r_Config_COMP0_interrupt(void);
Explanation	Based on the value of the monitor flag of Comparator0, modify the value of the PCLOE0 bit.
Argument	None
Return value	None

4.3 Flowchart

4.3.1 Main Processing

Figure 4-1 shows the main processing flowchart.

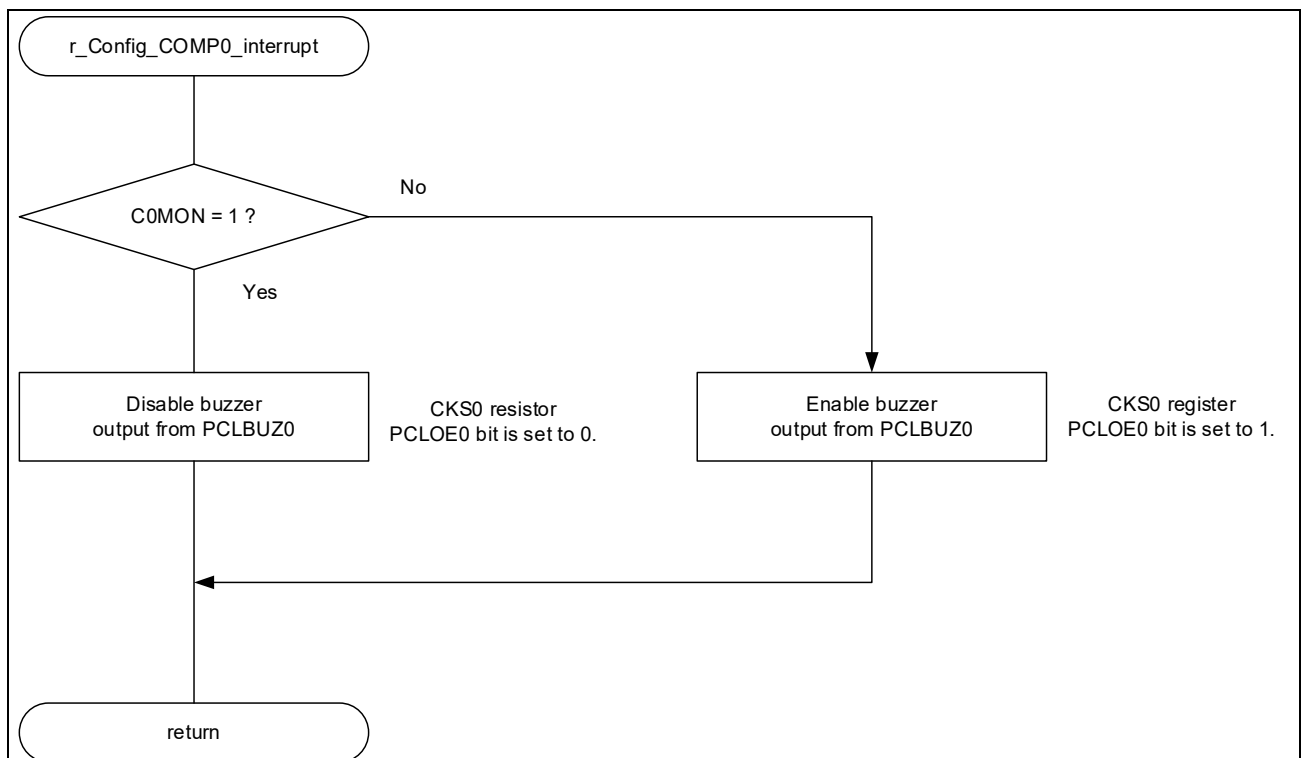
Figure 4-1 Main Processing



4.3.2 Comparator 0 Interrupt Processing

Figure 4-2 shows the flowchart for comparator 0.

Figure 4-2 Comparator 0 Interrupt processing



5. Sample Code

Please obtain the sample code from the Renesas Electronics website.

6. Documents for Reference

User's Manual:

RL78/G15 User's Manual: Hardware (R01UH0959EJ)

RL78 Family User's Manual: Software(R01US0015JJ)

The latest version can be downloaded from the Renesas Electronics website.

Technical Updates/Technical News

The latest information can be downloaded from the Renesas Electronics website.

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00		—	First edition issued

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1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

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5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

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