# RL78/G15, G16

## COM Port Connection Recovery Application for Fast Prototyping Board

### Introduction

Fast Prototyping Boards (FPB) for RL78/G15 and G16 prohibit using the reset pin as an I/O port through the option byte settings.

In this application, the dedicated recovery tool and procedure allow you to erase the flash memory and restore the option bytes to their state before the prohibited setting.

### Target Device

RL78/G15 Fast Prototyping Board (RTK5RLG150C00000BJ)
RL78/G16 Fast Prototyping Board (RTK5RLG160C00000BJ)

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# 1. Regarding the Occurrence of being unable to write.

## 1.1 Conditions for Occurrence

When writing the relevant program using the FPB of RL78/G15 or G16 via the COM port connection, subsequent debugging and writing via the COM port become impossible.

・Relevant program
Program configured with PORTSELB = 0 in the option byte settings.

| PORTSELB | P125/$\overline{\text{RESET}}$/INTP1/(VCOUT0)/(VCOUT1)/(SI01)Note 1 pin control |
|---|---|
| 0 | Port function (P125/INTP1/(VCOUT0)/(VCOUT1)/(SI01)Note 1 |
| 1 | $\overline{\text{RESET}}$ input (internal pull-up resistor can be always connected.) |

Note 1. For 20-pin products

Remark. When using the E2 Emulator or E2 Emulator Lite (E2, E2 Lite) for debugging or writing, this phenomenon does not occur.

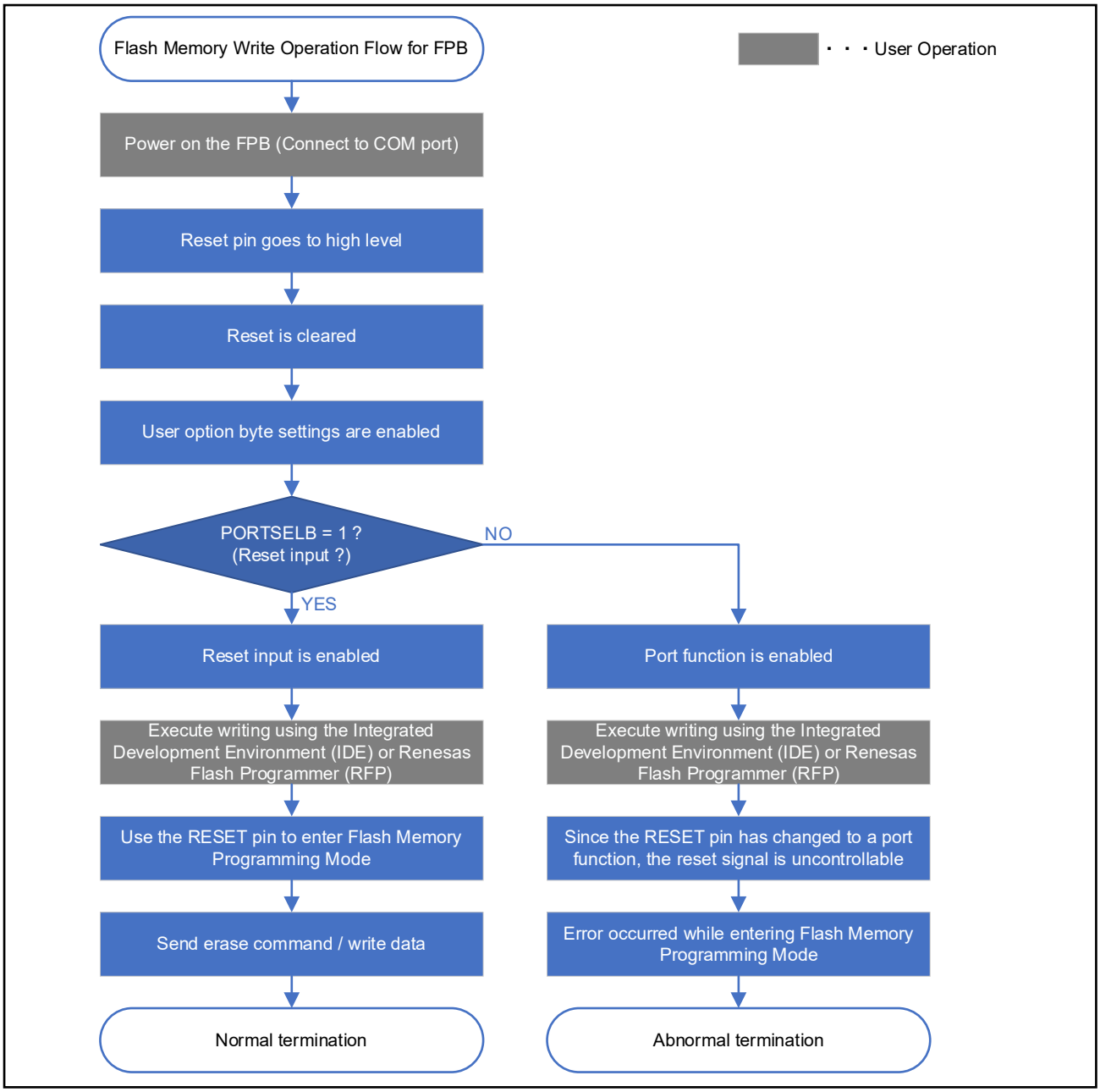
## 1.2 Mechanism of Occurrence

This phenomenon is due to the inability to enter Flash Memory Programming Mode when performing writing operations via the COM port connection using the FPB with the relevant program written.

The ability to enter Flash Memory Programming Mode is determined by the state of the RESET pin. However, when using the FPB with a COM port connection, the specification is such that the reset is released at the time of COM port connection. As a result, during debugging and writing, the RESET pin operates as a port, leading to this phenomenon.

Figure 1-1 shows the flow of Flash Memory writing operations with the FPB when PORTSELB is set to 1 and 0.

Figure 1-1 Hardware Configuration



# 2. Recovery Method

It is possible to recover by using an Integrated Development Environment (IDE) or Renesas Flash Programmer (RFP) to rewrite the option bytes to their pre-restriction state (PORTSELB = 1).

## 2.1 When Using E2 Emulator or E2 Emulator Lite

When using the E2 or E2 Lite, immediately after connecting the FPB to the PC, the E2 or E2 Lite applies a low level to the shared pins and maintains this state. This allows the reset input to remain active without being released after power-up, enabling rewriting.

## 2.2 When Using the Recovery Application

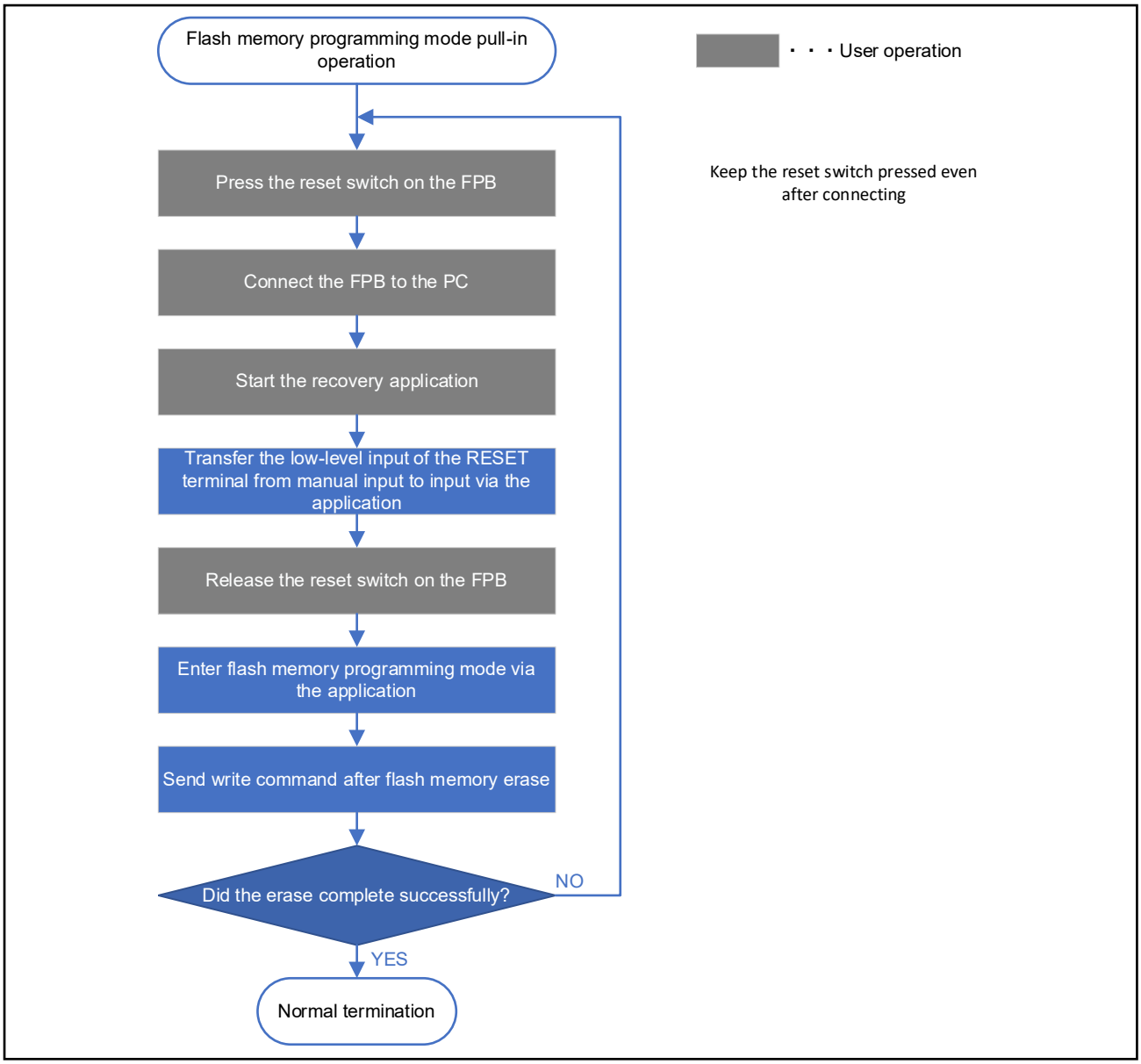
### 2.2.1 Recovery Flow

After connecting the FPB to the COM port, to enable the reset input, connect it to the PC while pressing the reset switch on the FPB (GND connection) and use the recovery application to maintain the low level.

Then, use the recovery application to enter flash memory programming mode, send erase and write commands to clear the flash memory, and restore the user option bytes to their pre-restriction state (PORTSELB = 1).

Figure 2-1 shows the recovery flow when the recovery application is used.

Figure 2-1 Recovery flow when using the recovery application



### 2.2.2 Operation Confirmation Conditions

The recovery application has been verified to operate under the following conditions.

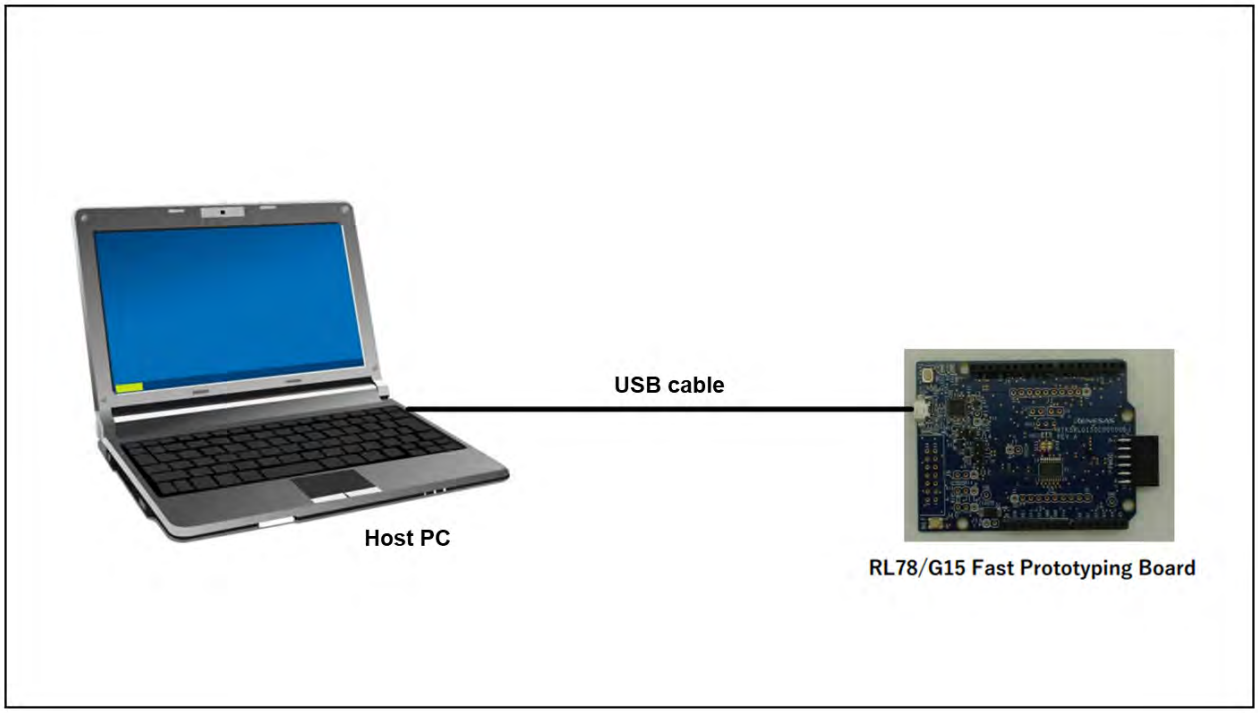
Table 2-1 Operation Confirmation Conditions

| | |
|---|---|
| Board used | RL78/G15 Fast Prototyping Board (RTK5RLG150C00000BJ)<br>RL78/G16 Fast Prototyping Board (RTK5RLG160C00000BJ) |
| Debug tool | COM port |
| Flash programming tool | Recovery application (RL78/G15G16 Flash Eraser) |
| Option Byte (000C1H) | PORTSELB = 1 ($\overline{\text{RESET}}$ input) |

### 2.2.3 Operation Confirmation Conditions

Figure 2-2 shows an example of the hardware configuration used in this application note. Recovery can be performed using the same hardware configuration as for COM port debugging.

Figure 2-2 Hardware configuration

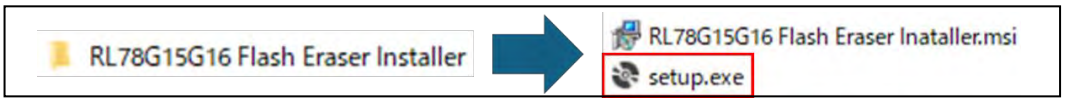


### 2.2.4 Installation Procedure for the Recovery Application

Please obtain the installer for the recovery application from the Renesas Electronics website. The installation procedure for the recovery application is outlined below in steps (1) through (6).

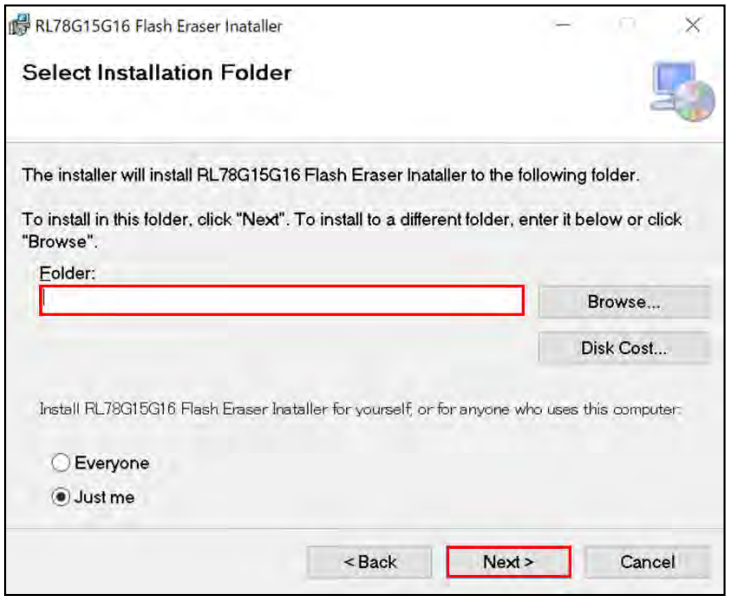
(1) Extract the r01an7363.zip.

(2) Open the file 'RL78G15G16 Flash Eraser Installer' and select 'setup.exe' to launch the installer.

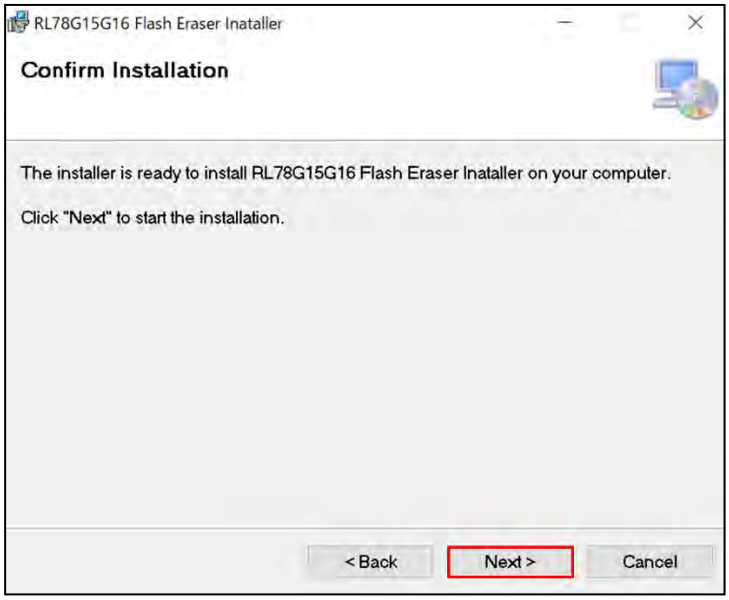



(3) Select “Next”.

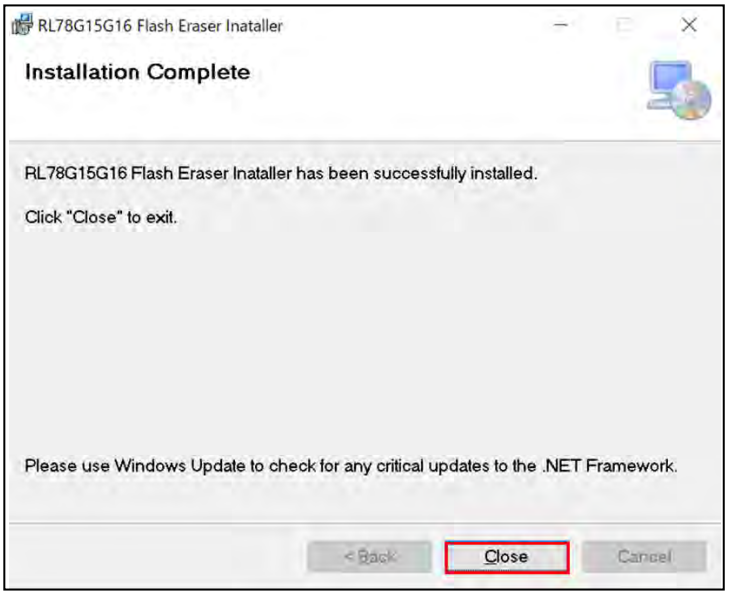

(4) Specify the installation folder and select “Next”.



(5) Selecting “Next” will begin the installation.




(6) Select “Close” to exit the installer.



### 2.2.5 User Interface (UI)

Figure 2-3 shows a description of the UI of the recovery application.

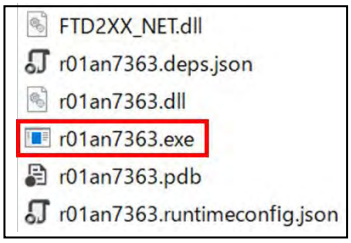
Figure 2-3 UI of the recovery application


① Help button・・・Allows you to check the application version and access the Renesas official
② SW1, SW2 ・・・ Buttons that users operate during the FPB recovery procedure.
③ Message box・・・Displays operation instructions, cautions, and execution results.

### 2.2.6 Operation procedure

The operation procedure for the recovery application is outlined below in steps (1) through (5).

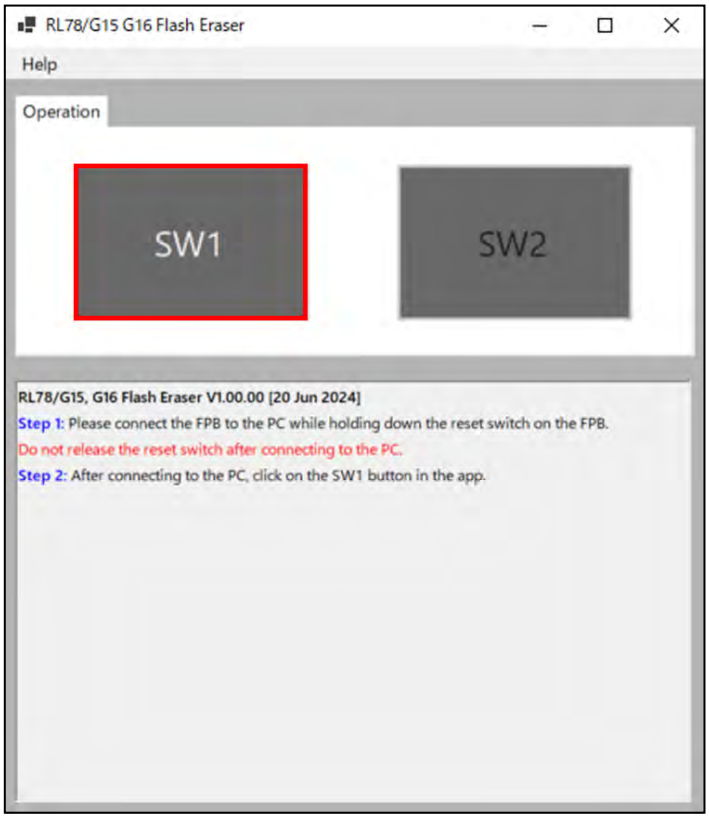
(1) Select “r01an7363.exe” to launch the application.




(2) Press the reset switch on the FPB before connecting the FPB to the PC.

(3) While continuing to press the reset switch, connect the FPB to the PC. Keep the reset switch pressed even after connecting.

(4) After launching the application, press SW1 on the application interface.



(5) After confirming the message box displays “OK: Reset signal is low.” release the reset switch on the FPB that you have been pressing. Then, press SW2 on the application interface. If an error occurs after pressing SW1, an error message will be displayed for 3 seconds, after which the process will automatically return to step (4). Please repeat the procedure if needed.

(6) When the flash memory is successfully erased, “OK: The flash memory has been erased.” will be displayed. Press “×” to exit the application. If an error occurs after pressing SW2, an error message will be displayed for 3 seconds, after which the process will automatically return to step (4). Please repeat the procedure if needed.


### 2.2.7 Notes

Do not connect multiple boards (including FPBs) that use FTDI chips simultaneously. There may be a risk of failing to erase the flash memory correctly.

## 3. Reference Documents

RL78/G15 User’s Manual: Hardware (R01UH0959E)
RL78/G16 User’s Manual: Hardware (R01UH0980E)
RL78 family user's manual software (R01US0015E)
RL78 Flash Programmer (RL78 Protocol B) (R01AN6782E)
RL78 Microcontroller (RL78 Protocol B) Serial Programming Guide (R01AN6332E)

The latest versions can be downloaded from the Renesas Electronics website.

Technical update
The latest versions can be downloaded from the Renesas Electronics website.

## Revision History

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | 2024.9.2 | - | First Edition |
| | | | |

# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

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1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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