RL78/G14

Using the DTC to Perform Continuous Clock Synchronous Serial Communication

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Abstract

This document describes how to perform continuous clock synchronous serial communication using the serial array unit (3-wire serial I/O) and DTC in the RL78/G14.

Products

RL78/G14

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

In this application note, the serial array unit (SAU) and DTC are used to successively transmit and receive 8-bit data. The SAU is used as a 3-wire serial I/O interface to output a transfer clock from the SCK00 pin, output transmit data from the SO00 pin, and input receive data to the SI00 pin.

The DTC transfers transmit data and receive data from the transmission source address to the destination address. The DTC is activated by the 3-wire serial I/O interface transfer end.

Table 1.1 lists the peripherals functions and their applications. Figure 1.1 shows the timing and communication format.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
SAU (unit 0, channel 0)	Performs clock synchronous serial communication
DTC	Transfers transmit data and receive data

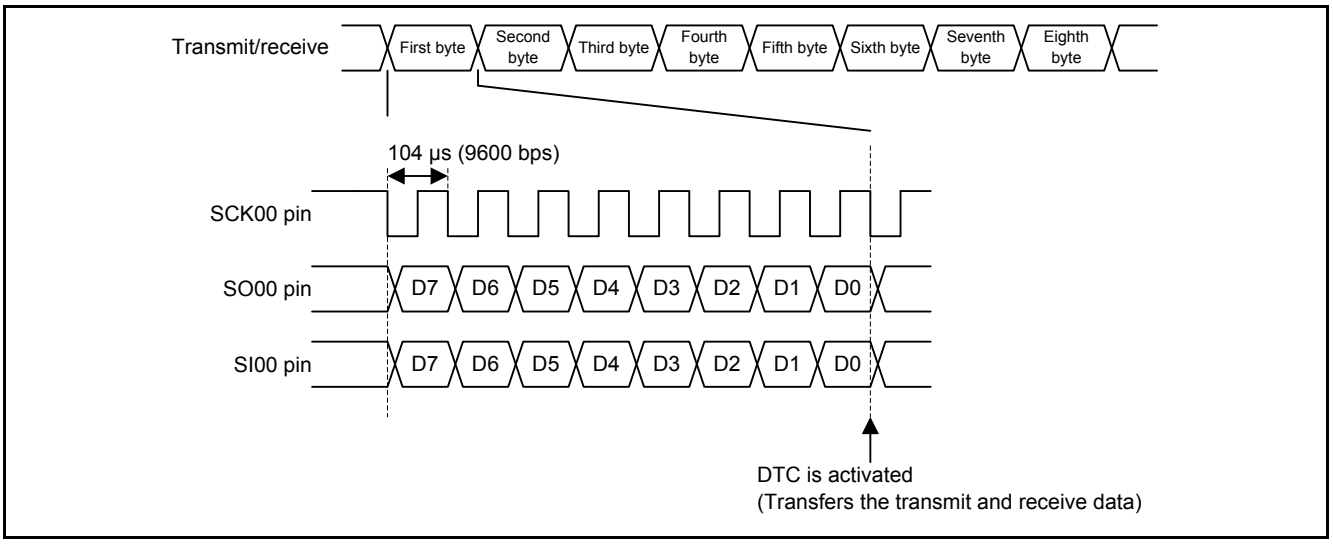


Figure 1.1 Timing and Communication Format

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

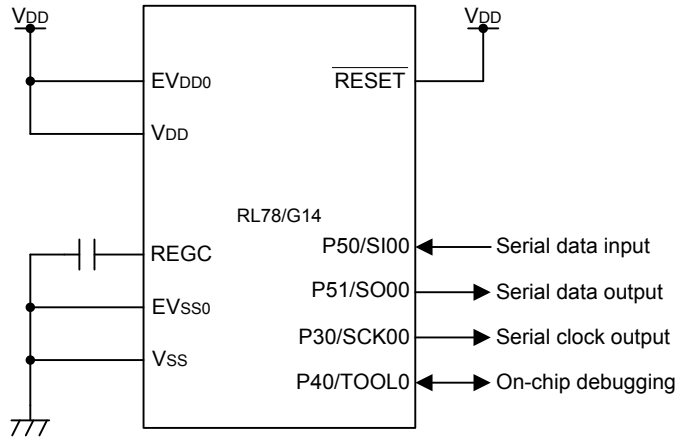
Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	RL78/G14 (R5F104PJA)
Operating frequencies	• High-speed on-chip oscillator clock (f_{HOCO}): 32 MHz (typical) • CPU/peripheral hardware clock (f_{CLK}): 32 MHz
Operating voltage	5.0 V (operation enabled from 2.9 to 5.5 V) LVD operation (V_{LVI}): 2.81 V at the rising edge or 2.75 V at the falling edge in reset mode
Integrated development environment	Renesas Electronics Corporation CubeSuite+ V1.03.00
C compiler	Renesas Electronics Corporation CA78K0R V1.60
RL78/G14 code library	Renesas Electronics Corporation CodeGenerator for RL78/G14 V1.01.03.06

3. Hardware

3.1 Hardware Configuration

Figure 3.1 shows a connection example.



Notes:
1. The above figure is simplified to show an overview of the hardware connection. When designing circuits, make sure to handle unused pins appropriately to satisfy the electrical characteristics. Connect input-only ports independently to either V_{DD} or V_{SS} via resistors.
2. Connect pins with names that begin with EV_{SS} to V_{SS}, and pins with names that begin with EV_{DD} to V_{DD}.
3. Make sure to set VDD greater than the detection voltage (V_{LVI}) specified by the LVD.

Figure 3.1 Connection Example

3.2 Pins Used

Table 3.1 lists the pins used and their functions.

Table 3.1 Pins Used and Their Functions

Pin Name	I/O	Function
P50/SI00	Input	Serial data input
P51/SO00	Output	Serial data output
P30/SCK	Output	Serial clock output

4. Software

As the sample code is created by editing the functions generated by the RL78/G14 code library, the code generator property has been modified. Figure 4.1 shows the code generator property setting.

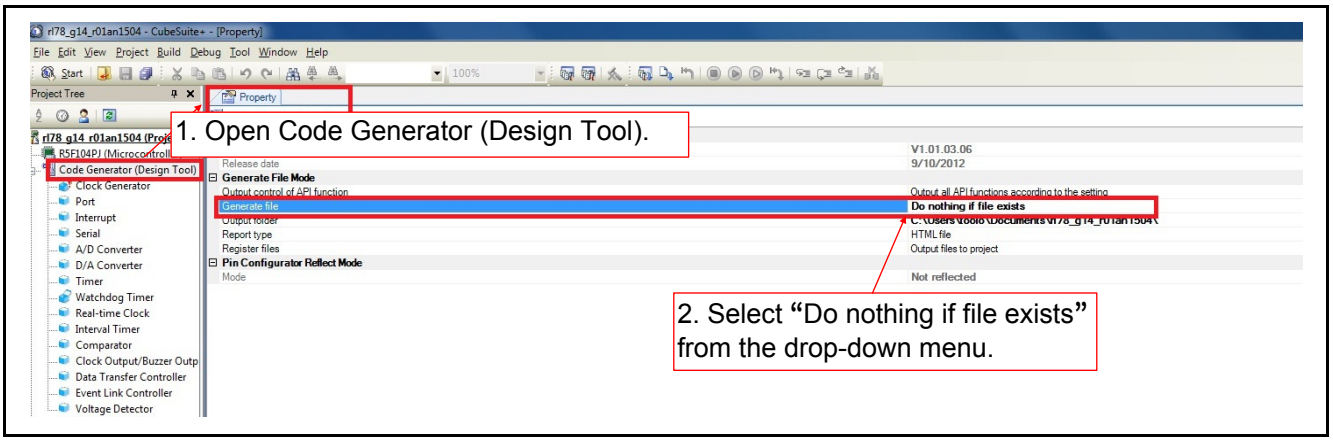


Figure 4.1 Code Generator Property Setting

4.1 Operation Overview

RL78/G14 transfers the receive data using the DTC control data 0 (DTCD0), and transfers the transmit data using the DTC control data 1 (DTCD1), and thus successively transmits and receives 8-byte data. Note that the program transfers the first byte of transmit data and the eighth byte of receive data.

Settings for the peripheral functions are listed below.

SAU

- Use single transfer mode
- Set the data length to 8 bits
- Set the data transfer sequence to MSB first
- Set the data transmit/receive timing to type 1
- Set the baud rate to 9600 bps
- Set the interrupt priority to low

DTCD0

- Set the activation source to CSI00 transfer end
- Enable the chain transfer
- Set the transfer mode to normal mode
- Set the data length to 8 bits
- Set the transfer source to FFF10H (SIO00 register address), fixed
- Set the transfer destination to FE900H, incremented
- Set the number of transfers to seven
- Set the transfer block size to 1 byte

DTCD1

- Set the activation source to DTC0 transfer end
- Disable the chain transfer
- Set the transfer mode to normal mode
- Set the data length to 8 bits
- Set the transfer source to FE911H, incremented
- Set the transfer destination to FFF10H (SIO00 register address), fixed
- Set the transfer block size to 1 byte

Figure 4.2 shows transmit and receive timing, and DTC activation. Figure 4.3 shows the operation of DTCD0. Figure 4.4 shows the operation of DTCD1.

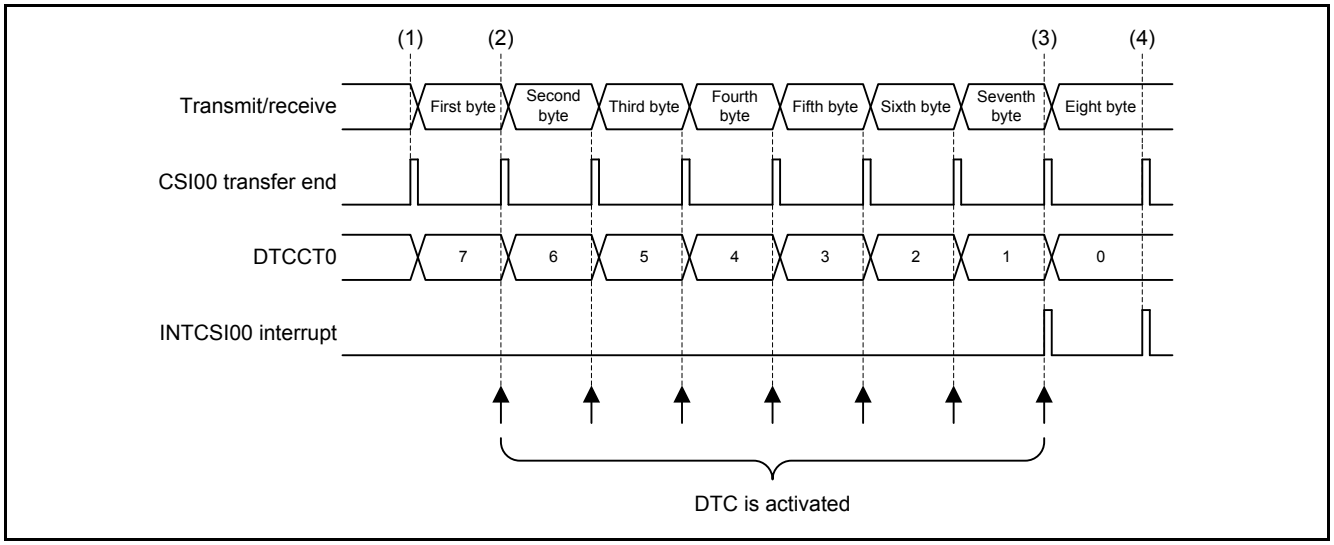


Figure 4.2 Timing of Transmission/Reception and DTC Activation

(1) Transmission/reception start

RL78/G14 starts transmission and reception after the DTC is configured.

Transmission is performed by the program writing the first byte of transmit data to the SIO00 register.

(2) DTC activation

After the first byte of data has been transmitted and received, DTC0 is activated. The first byte of receive data is transferred from the SIO00 register to the transfer destination address.

When transfer of the receive data is completed, DTC1 is activated. The second byte of transmit data from the transmit source address is transferred to the SIO00 register.

When the transmit data is written to the SIO00 register, the next transmission and reception start. The DTC is activated every time when the transmission and reception are completed and the same procedure is repeated until the transmission and reception of the eighth byte data is started. The DTCCT0 register value decrements each time the DTC transfer is activated.

(3) INTCSI00 interrupt generated by the DTC transfer end

When the DTCCT0 register becomes 0, the INTCSI00 interrupt occurs.

Preparations to complete transmission and reception are performed in the program.

(4) INTCSI00 interrupt generated by transmission/reception end

When the transmission and reception of the eighth byte of data is completed, the INTCSI00 interrupt occurs. The program reads and copies the eighth byte of receive data.

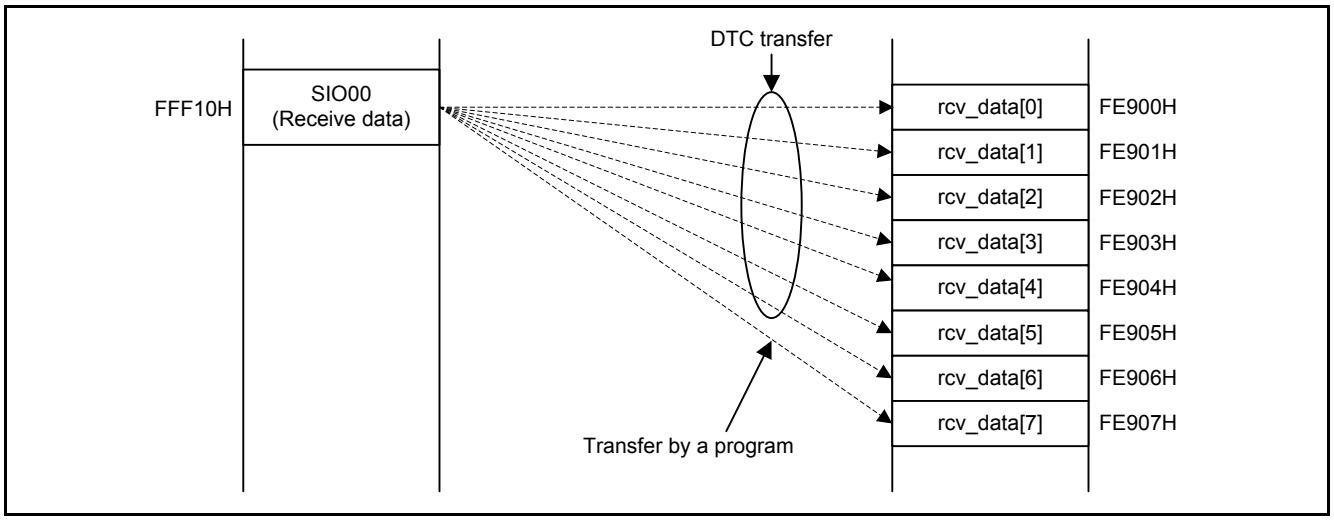


Figure 4.3 DTCD0 Operation

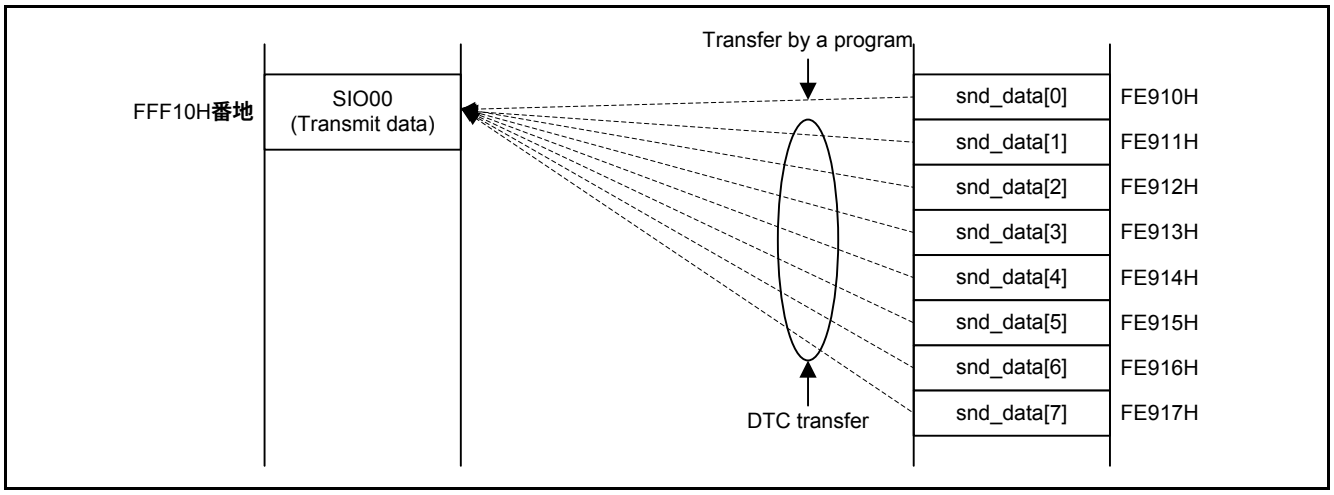


Figure 4.4 DTCD1 Operation

4.2 Section Composition

Table 4.1 lists the sections used in the sample code.

Table 4.1 Sections Used in the Sample Code

Section Name	Address	Reference Variable	Description
DTC0DST	0FE900H	rcv_data[]	DTCD0 transfer destination address
DTC1SRC	0FE910H	snd_data[]	DTCD1 transfer source address

4.3 Option Byte Settings

Table 4.2 lists the option byte settings.

Table 4.2 Option Byte Settings

Address	Setting Value	Contents
000C0H/010C0H	11101111B	Stops the watchdog timer (counting is stopped when a reset is canceled)
000C1H/010C1H	01111111B	Sets the LVD in reset mode Detection voltage: 2.81 V at the rising edge, 2.75 V at the falling edge
000C2H/010C2H	11101000B	Sets the HOCO clock as 32 MHz in high-speed main (HS) mode
000C3H/010C3H	10000100B	Enables on-chip debugging

4.4 Constant

Table 4.3 lists the constant used in the sample code.

Table 4.3 Constant Used in the Sample Code

Constant Name	Setting Value	Contents
TX_RX_DATA_SIZE	8 bytes	Transmit/receive data size

4.5 Variables

Table 4.4 lists the global variables, and Table 4.5 lists the static variable.

Table 4.4 Global Variables

Type	Variable Name	Contents	Function Used
uint8_t	rcv_data[]	Receive data	R_MAIN_UserInit r_csi00_interrupt r_csi00_callback_receiveend
uint8_t	snd_data[]	Transmit data	R_CSI00_Send_Receive transmit_data_set
uint8_t	set_rcv_data[]	Store the receive data	r_csi00_callback_receiveend
uint8_t	csi_status	Transmission/reception end status	main R_MAIN_UserInit r_csi00_callback_receiveend

Table 4.5 static Variable

Type	Variable Name	Contents	Function Used
MD_STATUS	md_status	Status flag	main

4.6 Functions

Table 4.6 lists the functions.

Table 4.6 Functions

Function Name	Outline
hdwinit	Initialization
R_Systeminit	Peripheral function initialization
R_CGC_Create	CPU clock initialization
R_SAU0_Create	SAU0 initialization
R_CSI00_Create	CSI00 initialization
R_CSI00_Start	CSI00 operation start
R_CSI00_Send_Receive	CSI00 transmission/reception start
r_csi00_interrupt	CSI00 transfer end interrupt
r_csi00_callback_receiveend	CSI00 receive end callback function
r_csi00_callback_error	CSI00 error callback function
R_DTC_Create	DTC initialization
R_DTCD0_Start	DTCD0 operation start
R_DTCD0_Stop	DTCD0 operation stop
main	Main processing
R_MAIN_UserInit	Main initialization
transmit_data_set	Transmit data setting

4.7 Function Specifications

The following tables list the sample code function specifications.

hdwinit	
Outline	Initialization
Header	None
Declaration	void hdwinit(void)
Description	Initializes the peripheral functions.
Arguments	None
Return Value	None

R_Systeminit	
Outline	Peripheral function initialization
Header	None
Declaration	void R_Systeminit(void)
Description	Initializes the peripheral functions used in this application note.
Arguments	None
Return Value	None

R_CGC_Create	
Outline	CPU clock initialization
Header	r_cg_cgc.h
Declaration	void R_CGC_Create(void)
Description	Initializes the CPU clock.
Arguments	None
Return Value	None

R_SAU0_Create	
Outline	SAU0 initialization
Header	r_cg_serial.h
Declaration	void R_SAU0_Create(void)
Description	Initializes SAU0.
Arguments	None
Return Value	None

R_CSI00_Create	
Outline	CSI00 initialization
Header	r_cg_serial.h
Declaration	void R_CSI00_Create(void)
Description	Initializes CSI00.
Arguments	None
Return Value	None

R_CSI00_Start	
Outline	CSI00 operation start
Header	r_cg_serial.h
Declaration	void R_CSI00_Start(void)
Description	Starts CSI00 operation.
Arguments	None
Return Value	None

R_CSI00_Send_Receive		
Outline	CSI00 transmit/receive start	
Header	r_cg_serial.h	
Declaration	MD_STATUS R_CSI00_Send_Receive(uint8_t * const tx_buf, uint16_t tx_num, uint8_t * const rx_buf)	
Description	Prepares the data buffer for CSI00 communication (transmission/reception) and sets the first byte of the transmit data.	
Arguments	uint8_t * const tx_buf	: Transmit data buffer pointer
	uint16_t tx_num	: Transmit data size
	uint8_t * const rx_buf	: Receive data buffer pointer
Return Value	MD_OK	: Setting is completed, operation started
	MD_ARGERROR	: Argument is incorrect

r_csi00_interrupt	
Outline	CSI00 transfer end interrupt
Header	None
Declaration	__interrupt static void r_csi00_interrupt(void)
Description	Performs CSI00 transfer end interrupt handling.
Arguments	None
Return Value	None

r_csi00_callback_receiveend	
Outline	CSI00 receive end callback function
Header	r_cg_serial.h
Declaration	static void r_csi00_callback_receiveend(void)
Description	This function is called when receiving the specified number of bytes of data is completed. 8 bytes of receive data are copied to set_rcv_data[TX_RX_DATA_SIZE].
Arguments	None
Return Value	None

r_csi00_callback_error	
Outline	CSI00 error callback function
Header	r_cg_serial.h
Declaration	static void r_csi00_callback_error(uint8_t err_type)
Description	This function is called when the CSI00 error occurs.
Arguments	uint8_t err_type : Error type
Return Value	None
Remarks	The sample code does not include the error processing. Add processing to the user program as needed.

R_DTC_Create	
Outline	DTC initialization
Header	r_cg_dtc.h
Declaration	void R_DTC_Create(void)
Description	Initializes the DTC.
Arguments	None
Return Value	None

DTCD0_Start	
Outline	DTCD0 operation start
Header	r_cg_dtc.h
Declaration	void R_DTCD0_Start(void)
Description	Starts the DTCD0 operation.
Arguments	None
Return Value	None

R_DTCD0_Stop	
Outline	DTCD0 operation stop
Header	r_cg_dtc.h
Declaration	void R_DTCD0_Stop(void)
Description	Stops the DTCD0 operation.
Arguments	None
Return Value	None

main	
Outline	Main processing
Header	None
Declaration	void main(void)
Description	Performs the main processing.
Arguments	None
Return Value	None

R_MAIN_UserInit	
Outline	Main initialization
Header	None
Declaration	void R_MAIN_UserInit(void)
Description	Performs processing required to initialize the main processing.
Arguments	None
Return Value	None

transmit_data_set	
Outline	Transmit data setting
Header	None
Declaration	static void transmit_data_set(void)
Description	Sets the transmit data.
Arguments	None
Return Value	None

4.8 Flowcharts

4.8.1 Overall Flow

Figure 4.5 shows the overall flow.

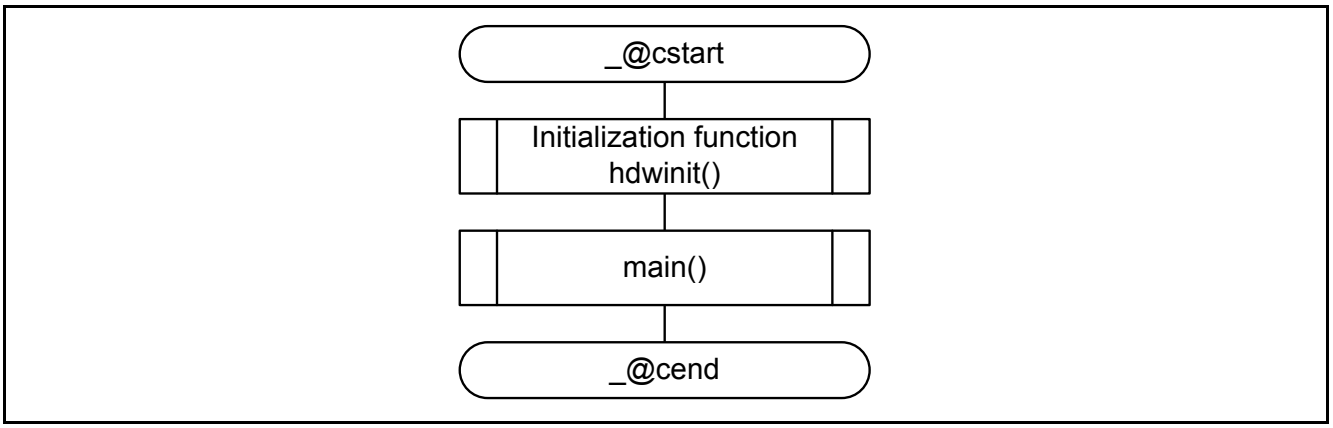


Figure 4.5 Overall Flow

4.8.2 Initialization

Figure 4.6 shows the initialization.

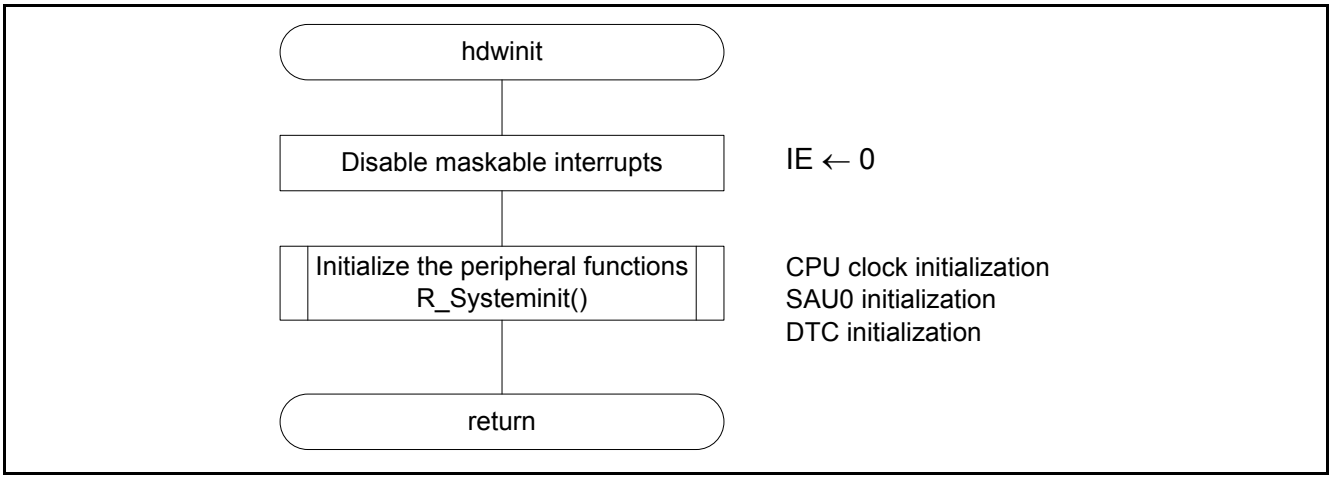


Figure 4.6 Initialization

4.8.3 Peripheral Function Initialization

Figure 4.7 shows the peripheral function initialization.

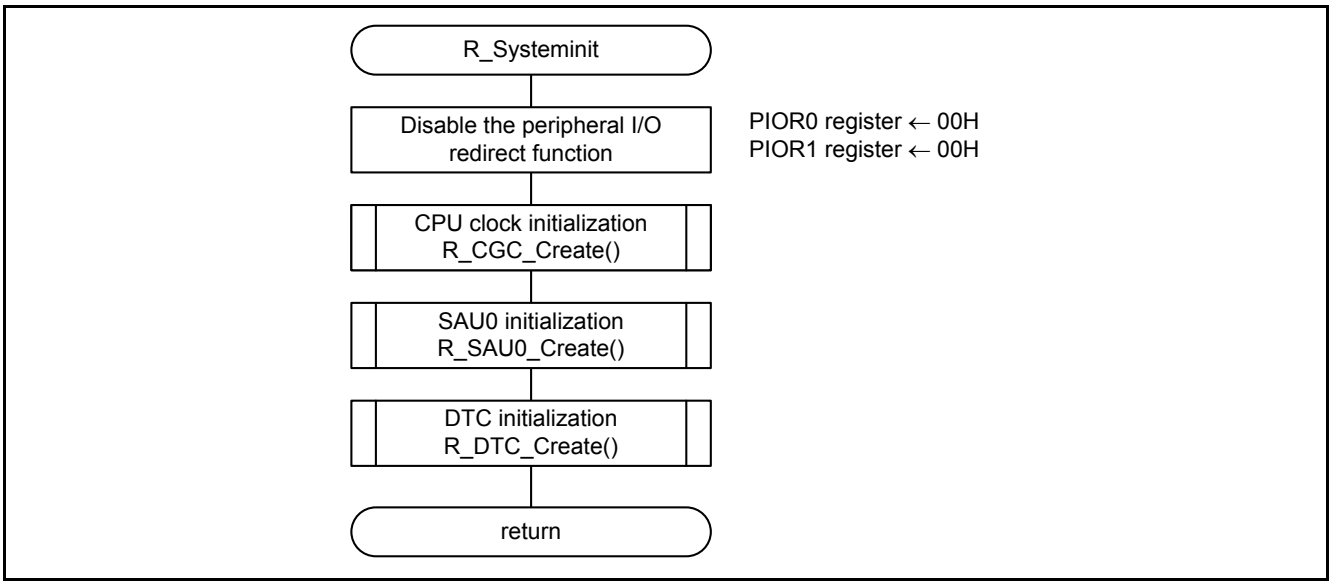


Figure 4.7 Peripheral Function Initialization

4.8.4 CPU Clock Initialization

Figure 4.8 shows the CPU clock initialization

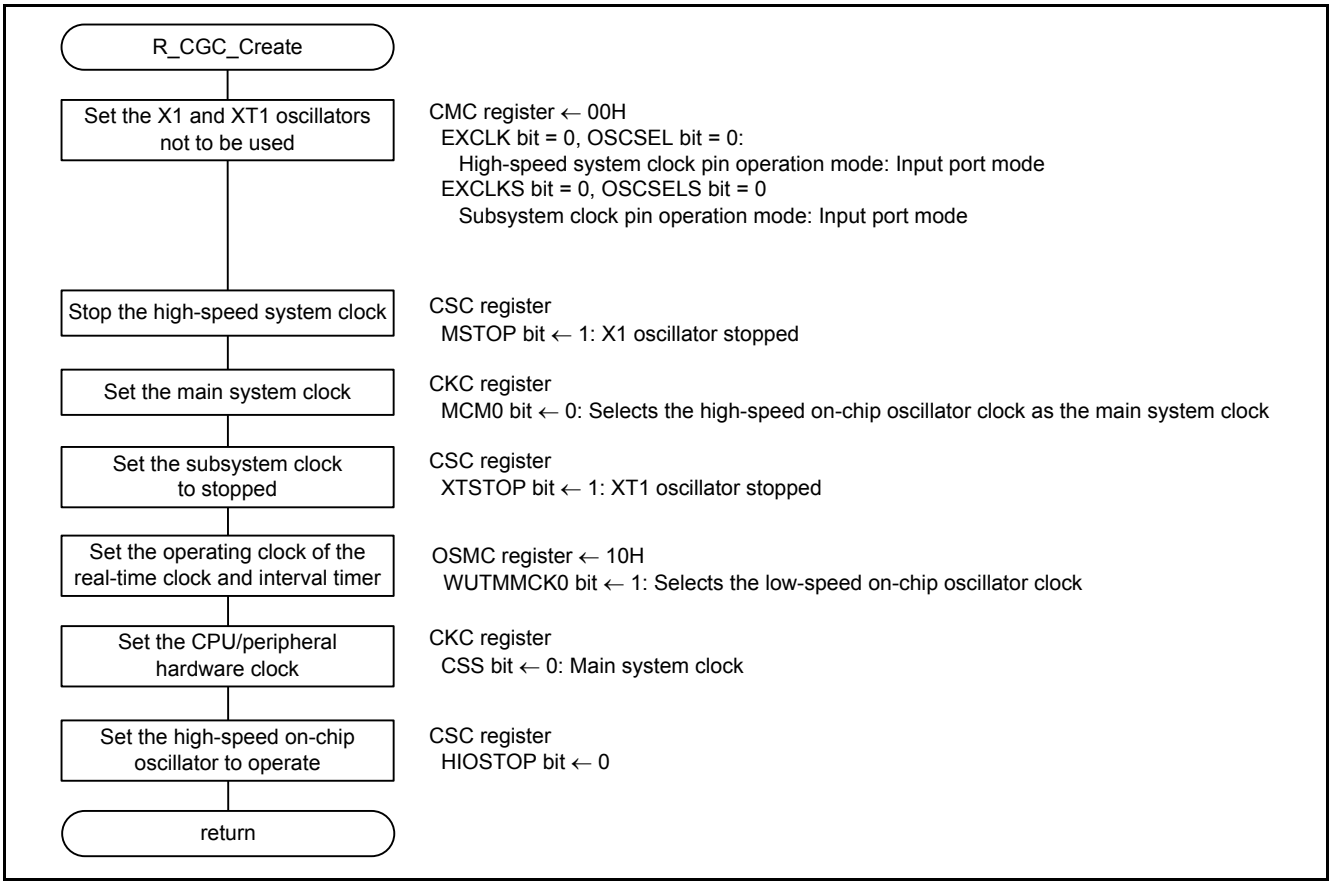


Figure 4.8 CPU Clock Initialization

4.8.5 SAU0 Initialization

Figure 4.9 shows the SAU0 initialization.

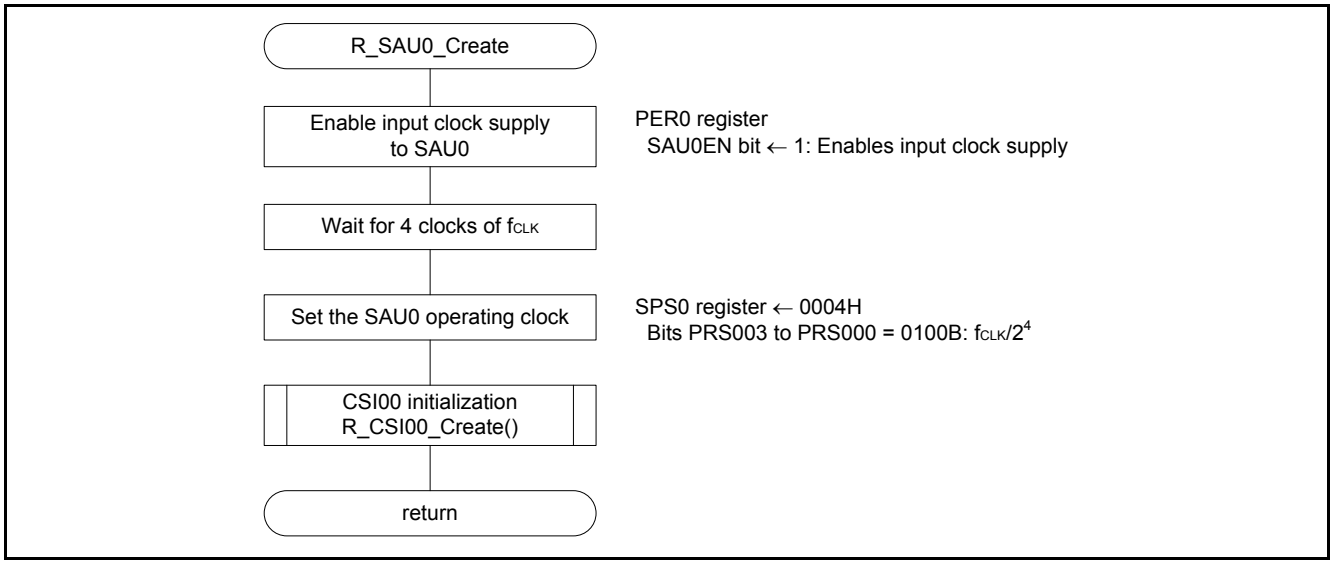


Figure 4.9 SAU0 Initialization

Enabling input clock supply to SAU0

- Peripheral enable register 0 (PER0)

Symbol	7	6	5	4	3	2	1	0
PER0	RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	**SAU0EN**	TAU1EN	TAU0EN
Value	×	×	×	×	×	**1**	×	×

- Bit 2

SAU0EN bit	Control of serial array unit 0 input clock supply
0	Stops supply of input clock • SFR used by serial array unit 0 cannot be written. • Serial array unit 0 is in the reset status.
1	Enables input clock supply • SFR used by serial array unit 0 can be read/written.

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting the SAU0 operating clock

- Serial clock select register 0 (SPS0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPS0	0	0	0	0	0	0	0	0	PRS 013	PRS 012	PRS 011	PRS 010	**PRS 003**	**PRS 002**	**PRS 001**	**PRS 000**
Value	–	–	–	–	–	–	–	–	×	×	×	×	**0**	**1**	**0**	**0**

- Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000	Select the operating clock (CK00)					
					f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz	f_{CLK} = 32 MHz
0	0	0	0	f_{CLK}	2 MHz	5 MHz	10 MHz	20 MHz	32 MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	16 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	8 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	4 MHz
0	**1**	**0**	**0**	**$f_{CLK}/2^4$**	125 kHz	313 kHz	625 kHz	1.25 MHz	**2 MHz**
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156 kHz	313 kHz	625 kHz	1 MHz
0	1	1	0	$f_{CLK}/2^6$	31.3 kHz	78.1 kHz	156 kHz	313 kHz	500 kHz
0	1	1	1	$f_{CLK}/2^7$	15.6 kHz	39.1 kHz	78.1 kHz	156 kHz	250 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	125 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.77 kHz	19.5 kHz	39.1 kHz	62.5 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.77 kHz	19.5 kHz	31.3 kHz
1	0	1	1	$f_{CLK}/2^{11}$	977 Hz	2.44 kHz	4.88 kHz	9.77 kHz	15.6 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	7.8 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	3.9 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.95 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	977 Hz

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

4.8.6 CSI00 Initialization

Figure 4.10 shows the CSI00 initialization.

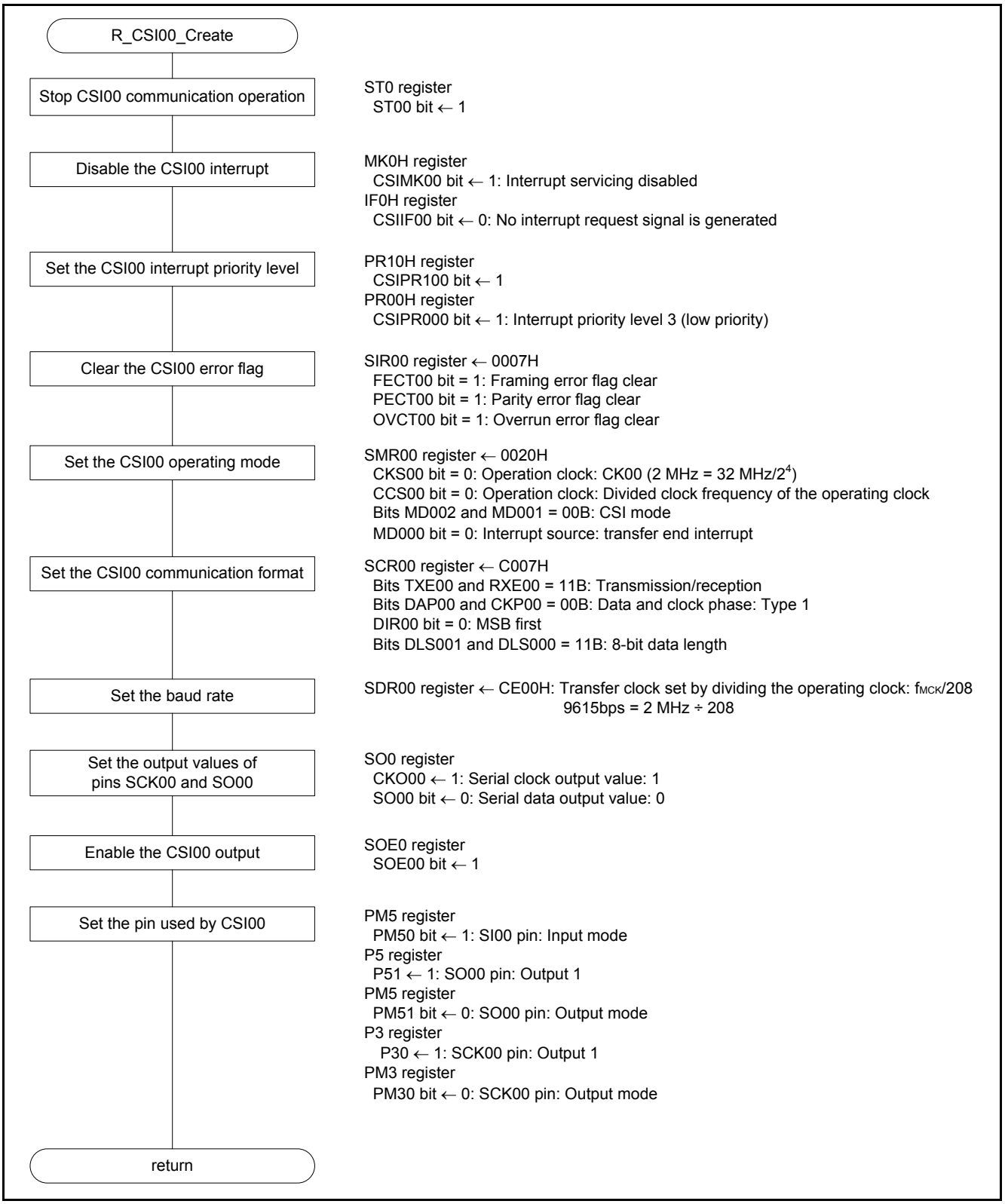


Figure 4.10 CSI00 Initialization

Stopping the CSI00 communication operation

- Serial channel stop register 0 (ST0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ST0	0	0	0	0	0	0	0	0	0	0	0	0	ST03	ST02	ST01	**ST00**
Value	–	–	–	–	–	–	–	–	–	–	–	–	×	×	×	**1**

- Bit 0

ST00 bit	Operation stop trigger of channel 0
0	No trigger operation
1	Clears the SE00 bit to 0 and stops the communication operation

Disabling the CSI00 interrupt

- Interrupt mask flag register (MK0H)

Symbol	7	6	5	4	3	2	1	0
MK0H	SREMK0 TMMK01H	SRMK0 CSIMK01 IICMK01	STMK0 **CSIMK00** IICMK00	1	1	SREMK2 TMMK11H	SRMK2 CSIMK21 IICMK21	STMK2 CSIMK20 IICMK20
Value	×	×	**1**	–	–	×	×	×

- Bit 5

CSIMK00 bit	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

- Interrupt request flag register (IF0H)

Symbol	7	6	5	4	3	2	1	0
IF0H	SREIF0 TMIF01H	SRIF0 CSIIF01 IICIF01	STIF0 **CSIIF00** IICIF00	0	0	SREIF2 TMIF11H	SRIF2 CSIIF21 IICIF21	STIF2 CSIIF20 IICIF20
Value	×	×	**0**	–	–	×	×	×

- Bit 5

CSIIF00 bit	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request signal is generated, interrupt request status

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting the CSI00 interrupt priority level

- Priority specification flag registers (PR10H, PR00H)

Symbol	7	6	5	4	3	2	1	0
PR00H	SREPR00 TMPR001H	SRPR00 CSIPR001 IICPR001	STPR00 **CSIPR000** IICPR000	1	1	SREPR02 TMPR011H	SRPR02 CSIPR021 IICPR021	STPR02 CSIPR020 IICPR020
Value	×	×	**1**	–	–	×	×	×

Symbol	7	6	5	4	3	2	1	0
PR10H	SREPR10 TMPR101H	SRPR10 CSIPR101 IICPR101	STPR10 **CSIPR100** IICPR100	1	1	SREPR12 TMPR111H	SRPR12 CSIPR121 IICPR121	STPR12 CSIPR120 IICPR120
Value	×	×	**1**	–	–	×	×	×

- Bit 5

CSIPR100 bit	CSIPR000 bit	Priority level selection
0	0	Specify level 0 (high priority)
0	1	Specify level 1
1	0	Specify level 2
1	1	Specify level 3 (low priority)

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Clearing the CSI00 error flag

- Serial flag clear trigger register (SIR00)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIR00	0	0	0	0	0	0	0	0	0	0	0	0	0	FECT00	PECT00	OVCT00
Value	–	–	–	–	–	–	–	–	–	–	–	–	–	1	1	1

- Bit 2

FECT00 bit	Clear trigger of framing error of channel 0
0	Not cleared
1	Clears the FEF00 bit of the SSR00 register to 0

- Bit 1

PECT00 bit	Clear trigger of parity error of channel 0
0	Not cleared
1	Clears the PEF00 bit of the SSR00 register to 0

- Bit 0

OVCT00 bit	Clear trigger of overrun error of channel 0
0	Not cleared
1	Clears the OVF00 bit of the SSR00 register to 0

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting the CSI00 operating mode

- Serial mode register 00 (SMR00)
  Operating clock (f_{MCK}): CK00
  Transfer clock (f_{TCLK}): Divided f_{MCK}
  Operating mode: CSI mode

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMR00	**CKS 00**	**CCS 00**	0	0	0	0	0	STS 00	0	SIS 000	1	0	0	**MD 002**	**MD 001**	**MD 000**
Value	**0**	**0**	–	–	–	–	–	0	–	0	1	–	–	**0**	**0**	**0**

- Bit 15

CKS00 bit	Selection of operating clock (f_{MCK}) of channel 0
0	Operating clock CK00 set by the SPS0 register
1	Operating clock CK01 set by the SPS0 register
Operating clock (f_{MCK}) is used by the edge detector. In addition, depending on the setting of the CCS00 bit and the higher 7 bits of the SDR00 register, a transfer clock (f_{TCLK}) is generated.	

- Bit 14

CCS00 bit	Selection of transfer clock (f_{TCLK}) of channel 0
0	Divided operating clock f_{MCK} specified by the CKS00 bit
1	Clock input f_{SCK} from the $\overline{SCK00}$ pin (slave transfer in CSI mode)
Transfer clock f_{TCLK} is used for the shift register, communication controller, output controller, interrupt controller, and error controller. When CCS00 = 0, the division ratio of operating clock (f_{MCK}) is set by the higher 7 bits of the SDR00 register.	

- Bits 2 and 1

MD002 bit	MD001 bit	Setting of operating mode of channel 0
0	0	CSI mode
0	1	UART mode
1	0	Simplified I^2C mode
1	1	Setting prohibited

- Bit 0

MD000 bit	Selection of interrupt source of channel 0
0	Transfer end interrupt
1	Buffer empty interrupt (Occurs when data is transferred from the SDR00 register to the shift register)

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting the CSI00 communication format

- Serial communication operation setting register 00 (SCR00)
  Operating mode: Enable transmission/reception
  Clock phase: Type 1
  Data transfer sequence: MSB first
  Data length: 8-bit data length

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCR00	**TXE 00**	**RXE 00**	**DAP 00**	**CKP 00**	0	EOC 00	PTC 001	PTC 000	**DIR 00**	0	SLC 001	SLC 000	0	1	**DLS 001**	**DLS 000**
Value	**1**	**1**	**0**	**0**	–	×	×	×	**0**	–	×	×	–	–	**1**	**1**

- Bits 15 and 14

TXE00 bit	RXE00 bit	Selection of operating mode of channel n
0	0	Disable communication
0	1	Reception only
1	0	Transmission only
1	1	Transmission/reception

- Bits 13 and 12

DAP00 bit	CKP00 bit	Selection of data and clock phase in CSI mode
0	0	Type 1
0	1	Type 2
1	0	Type 3
1	1	Type 4

- Bit 7

DIR00 bit	Selection of data transfer sequence in CSI and UART modes
0	Inputs/outputs data with MSB first
1	Inputs/outputs data with LSB first

- Bits 1 and 0

DLS001 bit	DLS000 bit	Setting of data length in CSI and UART modes
0	0	9-bit data length (stored in bits 0 to 8 of the SDR00 register) (settable in UART mode only)
1	0	7-bit data length (stored in bits 0 to 6 of the SDR00 register)
1	1	8-bit data length (stored in bits 0 to 7 of the SDR00 register)
Other than above		Setting prohibited

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting the baud rate

- Serial data register 00 (SDR00)
  Sets the transfer clock to 9600 bps (9600 bps = fMCK ÷ 208 = 2 MHz ÷ 208)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDR00	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Value	**1**	**1**	**0**	**0**	**1**	**1**	**1**	–								

- Bits 15 to 9

SDR00[15:9]							Transfer clock set by dividing the operating clock (fMCK)
0	0	0	0	0	0	0	fMCK/2
0	0	0	0	0	0	1	fMCK/4
…	…	…	…	…	…	…	…
1	1	0	0	1	1	1	fMCK/208 (=fMCK/[(103+1) × 2])

Setting the output values from pins SCK00 and SO00

- Serial output register 0 (SO0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO0	0	0	0	0	CKO03	CKO02	CKO01	**CKO00**	0	0	0	0	SO03	SO02	SO01	SO00
Value	–	–	–	–	×	×	×	**1**	–	–	–	–	×	×	×	

- Bit 8

CKO00 bit	Serial clock output of channel 0
0	Serial clock output value is “0”
1	Serial clock output value is “1”

- Serial output register 0 (SO0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO0	0	0	0	0	CKO03	CKO02	CKO01	CKO00	0	0	0	0	SO03	SO02	SO01	**SO00**
Value	–	–	–	–	×	×	×		–	–	–	–	×	×	×	**0**

- Bit 0

SO00 bit	Serial data output of channel 0
0	Serial clock output value is “0”
1	Serial clock output value is “1”

For details on register setting, refer to the RL78/G14 User’s Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Enabling the CSI00 output

- Serial output enable register 0 (SOE0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOE0	0	0	0	0	0	0	0	0	0	0	0	0	SOE03	SOE02	SOE01	**SOE00**
Value	–	–	–	–	–	–	–	–	–	–	–	–	×	×	×	**1**

- Bit 0

SOE00 bit	Serial output enable/stop of channel 0
0	Stops output by serial communication operation
1	Enables output by serial communication operation

Setting the pin used by CSI00

- Port mode register 5 (PM5)

Symbol	7	6	5	4	3	2	1	0
PM5	PM57	PM56	PM55	PM54	PM53	PM52	PM51	**PM50**
Value	×	×	×	×	×	×		**1**

- Bit 0

PM50 bit	P50 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

- Port register 5 (P5)

Symbol	7	6	5	4	3	2	1	0
P5	P57	P56	P55	P54	P53	P52	**P51**	P50
Value	×	×	×	×	×	×	**1**	

- Bit 0

P51 bit	Output data control (in output mode)
0	Output 0
1	Output 1

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

- Port mode register 5 (PM5)

Symbol	7	6	5	4	3	2	1	0
PM5	PM57	PM56	PM55	PM54	PM53	PM52	**PM51**	PM50
Value	×	×	×	×	×	×	**0**	

  - Bit 1

PM51 bit	P51 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

- Port register 3 (P3)

Symbol	7	6	5	4	3	2	1	0
P3	0	0	0	0	0	0	P31	**P30**
Value	–	–	–	–	–	–	×	**1**

  - Bit 0

P30 bit	Output data control (in output mode)
0	Output 0
1	Output 1

- Port mode register 3 (PM3)

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	1	1	1	PM31	**PM30**
Value	×	×	×	×	×	×	×	**0**

  - Bit 0

PM30 bit	P30 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

4.8.7 CSI00 Operation Start

Figure 4.11 shows the CSI00 operation start.

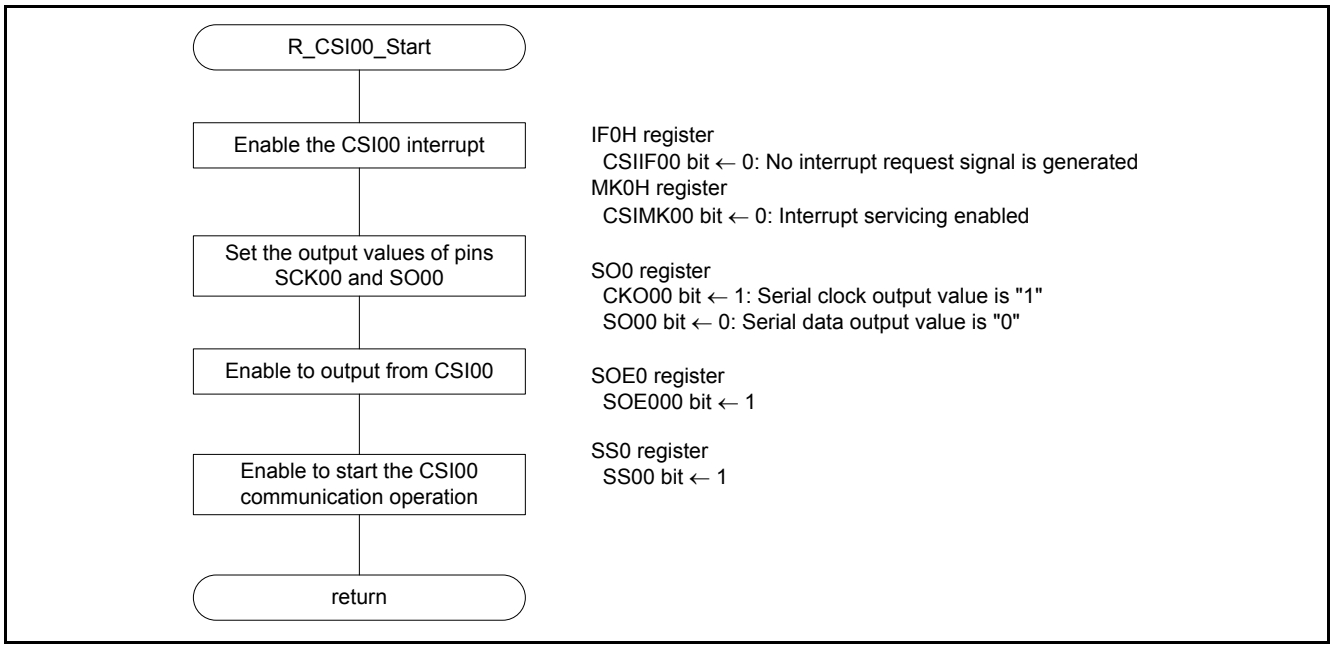


Figure 4.11 CSI00 Operation Start

Enabling the CSI00 interrupt

- Interrupt request flag register (IF0H)

Symbol	7	6	5	4	3	2	1	0
IF0H	SREIF0 TMIF01H	SRIF0 CSIIF01 IICIF01	STIF0 **CSIIF00** IICIF00	0	0	SREIF2 TMIF11H	SRIF2 CSIIF21 IICIF21	STIF2 CSIIF20 IICIF20
Value	×	×	**0**	–	–	×	×	×

- Bit 5

CSIIF00 bit	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request signal is generated, interrupt request status

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

- Interrupt mask flag register (MK0H)

Symbol	7	6	5	4	3	2	1	0
MK0H	SREMK0 TMMK01H	SRMK0 CSIMK01 IICMK01	STMK0 **CSIMK00** IICMK00	1	1	SREMK2 TMMK11H	SRMK2 CSIMK21 IICMK21	STMK2 CSIMK20 IICMK20
Value	×	×	**0**	–	–	×	×	×

- Bit 5

CSIMK00 bit	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Setting the output values from pins SCK00 and SO00

- Serial output register 0 (SO0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO0	0	0	0	0	CKO03	CKO02	CKO01	**CKO00**	0	0	0	0	SO03	SO02	SO01	SO00
Value	–	–	–	–	×	×	×	**1**	–	–	–	–	×	×	×	

- Bit 8

CKO00 bit	Serial clock output of channel 0
0	Serial clock output value is “0”
1	Serial clock output value is “1”

- Serial output register 0 (SO0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO0	0	0	0	0	CKO03	CKO02	CKO01	CKO00	0	0	0	0	SO03	SO02	SO01	**SO00**
Value	–	–	–	–	×	×	×		–	–	–	–	×	×	×	**0**

- Bit 0

SO00 bit	Serial data output of channel 0
0	Serial clock output value is “0”
1	Serial clock output value is “1”

For details on register setting, refer to the RL78/G14 User’s Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Enabling the CSI00 output

- Serial output enable register 0 (SOE0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOE0	0	0	0	0	0	0	0	0	0	0	0	0	SOE03	SOE02	SOE01	**SOE00**
Value	–	–	–	–	–	–	–	–	–	–	–	–	×	×	×	**1**

- Bit 0

SOE00 bit	Serial output enable/stop of channel 0
0	Stops output by serial communication operation
1	Enables output by serial communication operation

Enabling to start the CSI00 communication operation

- Serial channel start register 0 (SS0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SS0	0	0	0	0	0	0	0	0	0	0	0	0	SS03	SS02	SS01	**SS00**
Value	–	–	–	–	–	–	–	–	–	–	–	–	×	×	×	**1**

- Bit 0

SS00 bit	Operation start trigger of channel 0
0	No trigger operation
1	Sets the SE00 bit to 1 and enters the communication wait status

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

4.8.8 CSI00 Transmission/Reception Start

Figure 4.12 shows the CSI00 transmission/reception start.

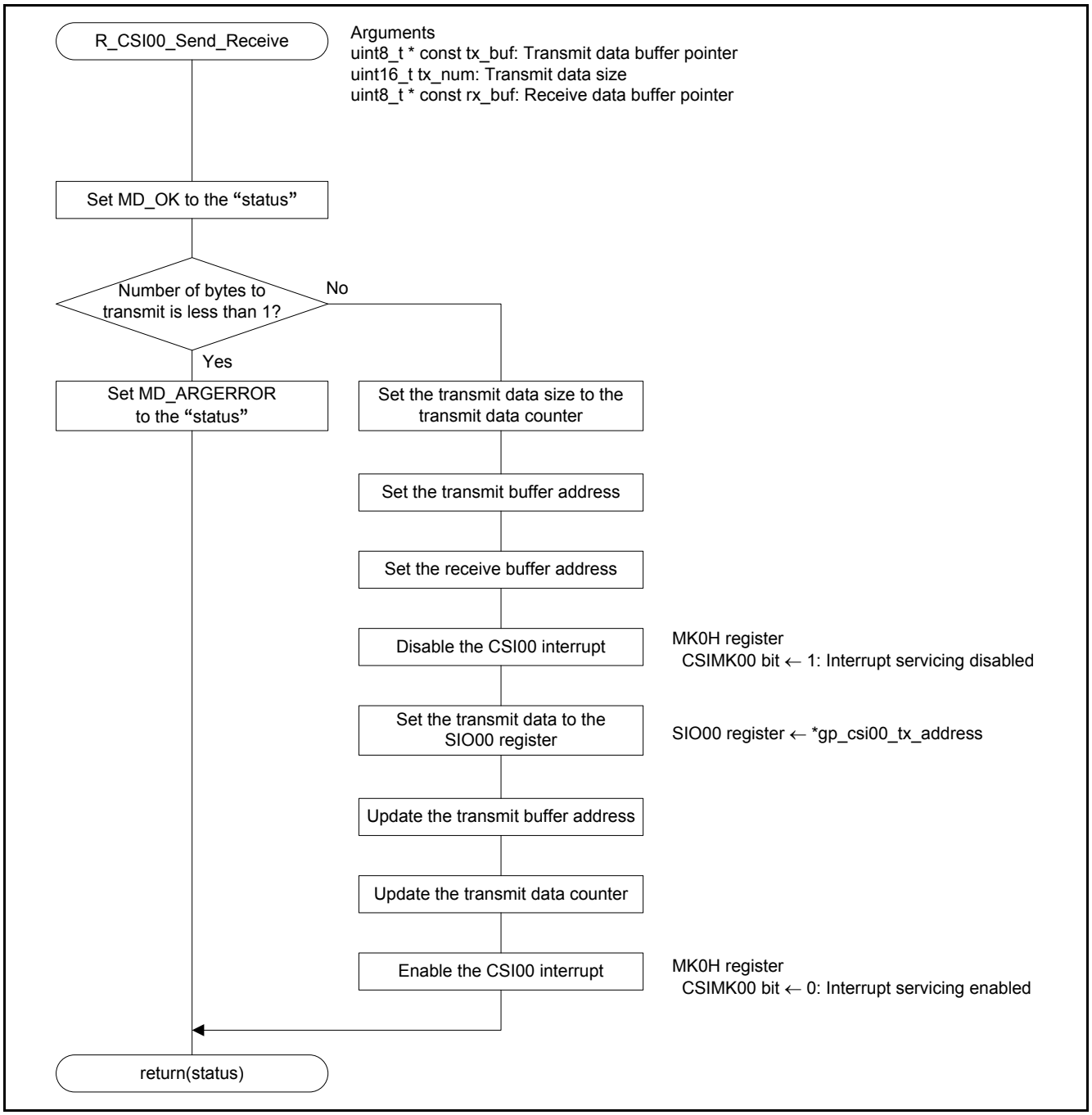


Figure 4.12 CSI00 Transmission/Reception Start

Disabling the CSI00 interrupt

- Interrupt mask flag register (MK0H)

Symbol	7	6	5	4	3	2	1	0
MK0H	SREMK0 TMMK01H	SRMK0 CSIMK01 IICMK01	STMK0 **CSIMK00** IICMK00	1	1	SREMK2 TMMK11H	SRMK2 CSIMK21 IICMK21	STMK2 CSIMK20 IICMK20
Value	×	×	**1**	–	–	×	×	×

- Bit 5

CSIMK00 bit	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Setting the transmit data

- CSI00 data register (SIO00)

Symbol	7	6	5	4	3	2	1	0
SIO00	–	–	–	–	–	–	–	–
Value	**00H to FFH**							

Enabling the CSI00 interrupt

- Interrupt mask flag register (MK0H)

Symbol	7	6	5	4	3	2	1	0
MK0H	SREMK0 TMMK01H	SRMK0 CSIMK01 IICMK01	STMK0 **CSIMK00** IICMK00	1	1	SREMK2 TMMK11H	SRMK2 CSIMK21 IICMK21	STMK2 CSIMK20 IICMK20
Value	×	×	**0**	–	–	×	×	×

- Bit 5

CSIMK00 bit	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

4.8.9 CSI00 Transfer End Interrupt

Figure 4.13 shows the CSI00 transfer end interrupt.

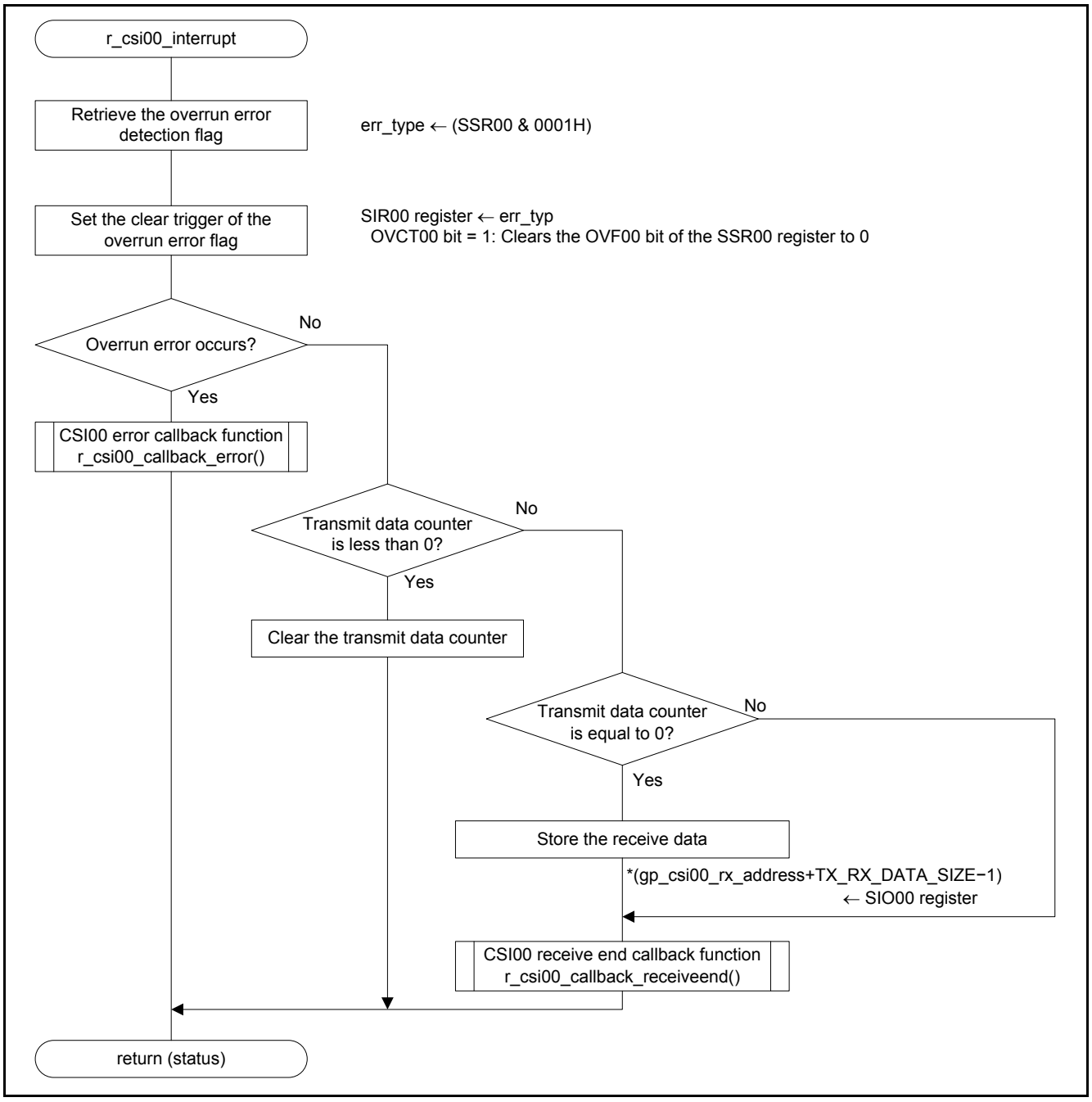


Figure 4.13 CSI00 Transfer End Interrupt

Retrieving the overrun error detection flag status

- Serial status register 00 (SSR00)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSR00	0	0	0	0	0	0	0	0	0	TSF 00	BFF 00	0	0	FEC 00	PEC 00	**OVC 00**

- Bit 0

OVC00 bit	**Overrun error detection flag of channel 0**
0	No error occurs
1	An error occurs

Setting the clear trigger of the overrun error flag

- Serial flag clear trigger register (SIR00)
  Clears an overrun error flag when an overrun error occurs.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIR00	0	0	0	0	0	0	0	0	0	0	0	0	0	FECT00	PECT00	**OVCT00**
Value	–	–	–	–	–	–	–	–	–	–	–	–	–	×	×	**1**

- Bit 0

OVCT00 bit	**Clear trigger of overrun error flag of channel 0**
0	Not cleared
1	Clears the OVF00 bit of the SSR00 register to 0

Storing the receive data

- CSI00 data register 00 (SIO00)
  Reads the receive data

Symbol	7	6	5	4	3	2	1	0
SIO00	–	–	–	–	–	–	–	–

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

4.8.10 CSI00 Receive End Callback Function

Figure 4.14 shows the CSI00 receive end callback function.

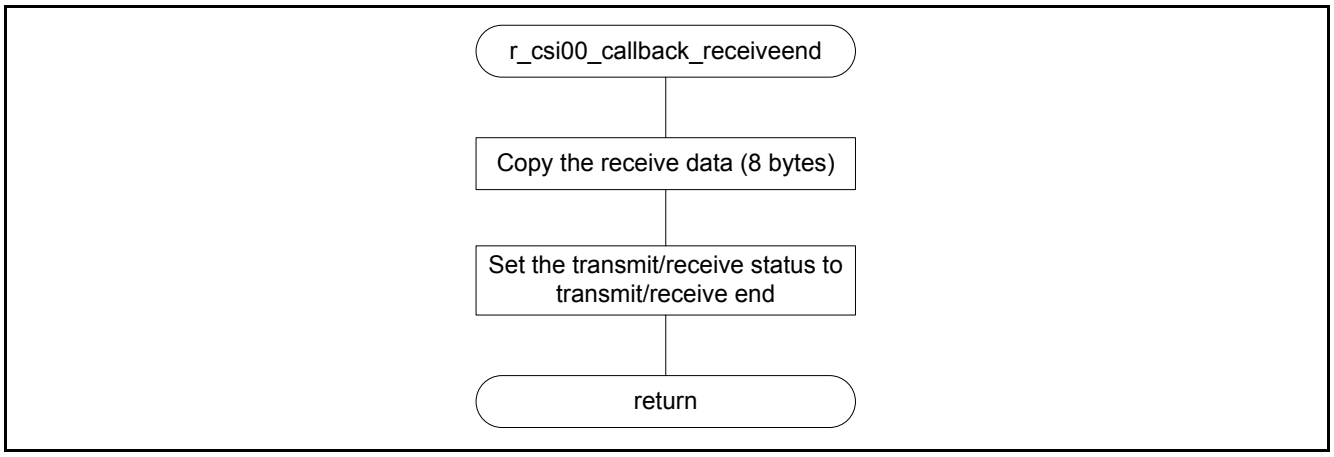


Figure 4.14 CSI00 Receive End Callback Function

4.8.11 CSI00 Error Callback Function

Figure 4.15 shows the CSI00 error callback function.

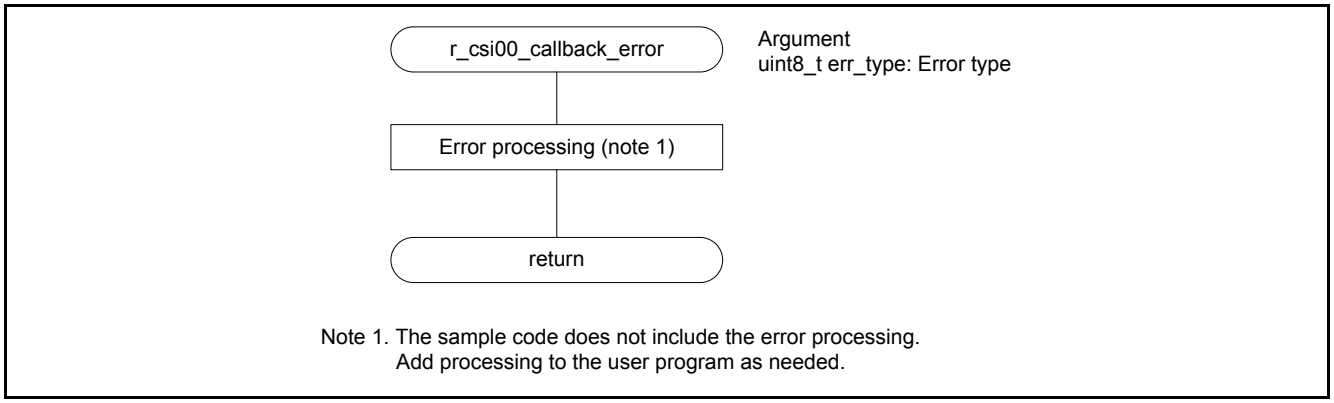


Figure 4.15 CSI00 Error Callback Function

4.8.12 DTC Initialization

Figure 4.16 shows the DTC initialization.

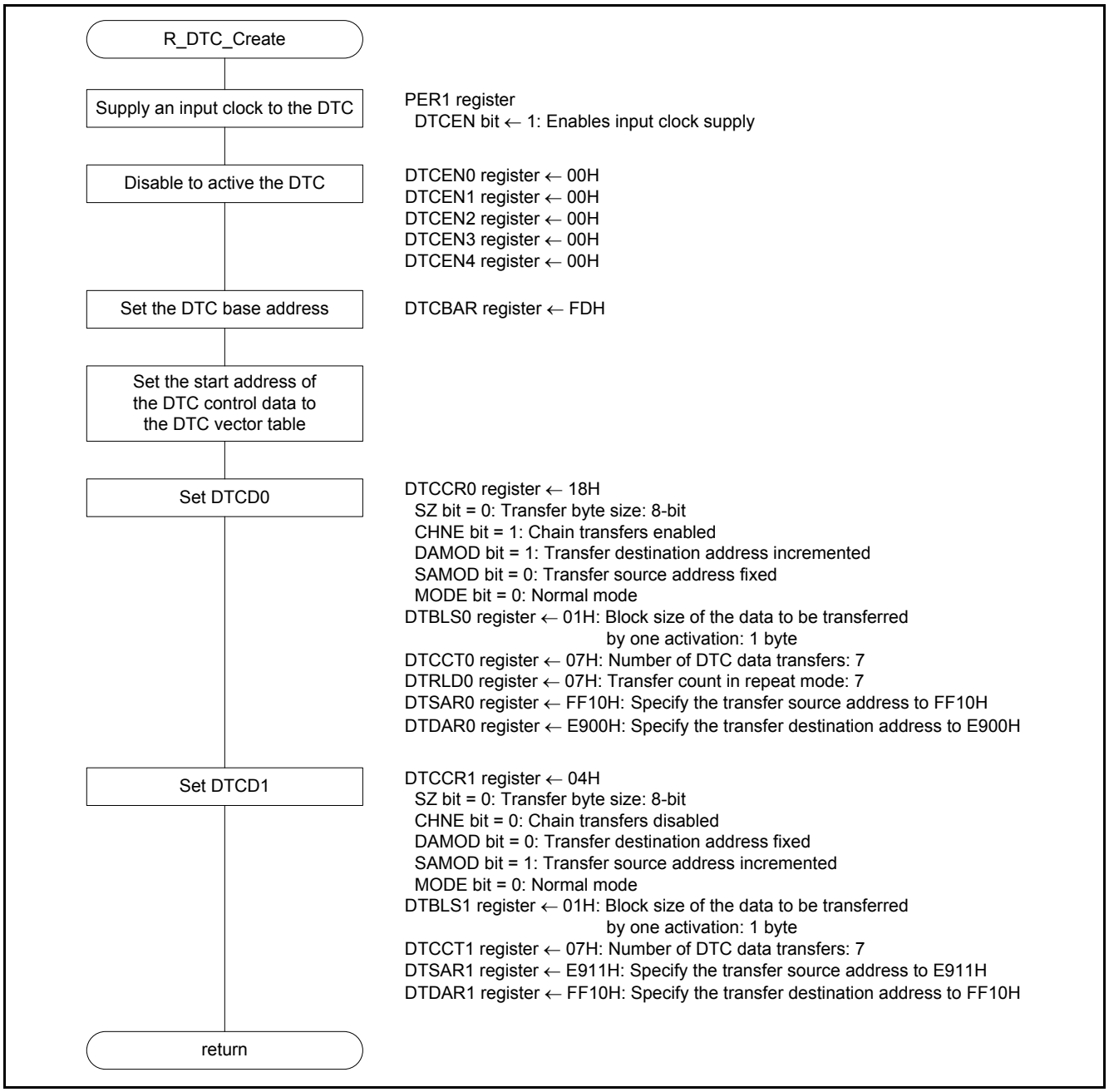


Figure 4.16 DTC Initialization

Supplying an input clock to the DTC

- Peripheral enable register 1 (PER1)

Symbol	7	6	5	4	3	2	1	0
PER1	DACEN	TRGEN	CMPEN	TRD0EN	**DTCEN**	0	0	TRJ0EN
Value	×	×	×	×	**1**	–	–	×

- Bit 3

DTCEN bit	Control of DTC input clock supply
0	Stops input clock supply • DTC cannot run.
1	Enables input clock supply • DTC can run.

Disabling to activate DTC0

- DTC activation enable register i (DTCENi, i = 0 to 4)

Symbol	7	6	5	4	3	2	1	0
DTCENi	**DTCENi7**	**DTCENi6**	**DTCENi5**	**DTCENi4**	**DTCENi3**	**DTCENi2**	**DTCENi1**	**DTCENi0**
Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

- Bit 7

DTCENi7 bit	DTC activation enable i7
0	Activation disabled
1	Activation enabled

- Bit 6

DTCENi6 bit	DTC activation enable i6
0	Activation disabled
1	Activation enabled

- Bit 5

DTCENi5 bit	DTC activation enable i5
0	Activation disabled
1	Activation enabled

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

- Bit 4

DTCENi4 bit	DTC activation enable i4
0	Activation disabled
1	Activation enabled

- Bit 3

DTCENi3 bit	DTC activation enable i3
0	Activation disabled
1	Activation enabled

- Bit 2

DTCENi2 bit	DTC activation enable i2
0	Activation disabled
1	Activation enabled

- Bit 1

DTCENi1 bit	DTC activation enable i1
0	Activation disabled
1	Activation enabled

- Bit 0

DTCENi0 bit	DTC activation enable i0
0	Activation disabled
1	Activation enabled

Setting the DTC base address

- DTC base address register (DTCBAR)
  Sets the start address of the DTC control data area.

Symbol	7	6	5	4	3	2	1	0
DTCBAR	DTCBAR7	DTCBAR6	DTCBAR5	DTCBAR4	DTCBAR3	DTCBAR2	DTCBAR1	DTCBAR0
Value	FDH							

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting the DTCD0

- DTC control register 0 (DTCCR0)
  Data size: 8 bits
  Chain transfer: Enabled
  Transfer destination address: Incremented
  Transfer source address: Fixed
  Transfer mode: Normal mode

Symbol	7	6	5	4	3	2	1	0
DTCCR0	0	**SZ**	RPTINT	**CHNE**	**DAMOD**	**SAMOD**	RPTSEL	**MODE**
Value	–	**0**	×	**1**	**1**	**0**	×	**0**

- Bit 6

SZ bit	Data size selection
0	8 bits
1	16 bits

- Bit 4

CHNE bit	Enabling/disabling chain transfers
0	Chain transfers disabled
1	Chain transfers enabled

- Bit 3

DAMOD bit	Transfer destination address control
0	Fixed
1	Incremented

- Bit 2

SAMOD bit	Transfer source address control
0	Fixed
1	Incremented

- Bit 0

MODE bit	Transfer mode selection
0	Normal mode
1	Repeat mode

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

- DTC block size register 0 (DTBLS0)
  Set the DTC0 block size to 1 byte.

Symbol	7	6	5	4	3	2	1	0
DTBLS0	DTBLS07	DTBLS06	DTBLS05	DTBLS04	DTBLS03	DTBLS02	DTBLS01	DTBLS00
Value	01H							

- DTC transfer count register 0 (DTCCT0)
  Set the number of transfers by DTC0 to 7.

Symbol	7	6	5	4	3	2	1	0
DTCCT0	DTCCT07	DTCCT06	DTCCT05	DTCCT04	DTCCT03	DTCCT02	DTCCT01	DTCCT00
Value	07H							

- DTC transfer count reload register 0 (DTRLD0)
  Set the number of transfers in repeat mode to 7 (This register can be used in repeat mode).

Symbol	7	6	5	4	3	2	1	0
DTRLD0	DTRLD07	DTRLD06	DTRLD05	DTRLD04	DTRLD03	DTRLD02	DTRLD01	DTRLD00
Value	07H							

- DTC source address register 0 (DTSAR0)
  Specify the transfer source address for data transfer to FF10H.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTSAR0	DTSAR015	DTSAR014	DTSAR013	DTSAR012	DTSAR011	DTSAR010	DTSAR09	DTSAR08	DTSAR07	DTSAR06	DTSAR05	DTSAR04	DTSAR03	DTSAR02	DTSAR01	DTSAR00
Value	FF10H															

- DTC destination address register 0 (DTDAR0)
  Specify the transfer destination address for data transfer to E900H.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTDAR0	DTDAR015	DTDAR014	DTDAR013	DTDAR012	DTDAR011	DTDAR010	DTDAR09	DTDAR08	DTDAR07	DTDAR06	DTDAR05	DTDAR04	DTDAR03	DTDAR02	DTDAR01	DTDAR00
Value	E900H															

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

Setting the DTCD1

- DTC control register 1 (DTCCR1)
  Data size: 8 bits
  Chain transfer: Disabled
  Transfer destination address: Fixed
  Transfer source address: Incremented
  Transfer mode: Normal mode

Symbol	7	6	5	4	3	2	1	0
DTCCR1	0	**SZ**	RPTINT	**CHNE**	**DAMOD**	**SAMOD**	RPTSEL	**MODE**
Value	–	**0**	×	**0**	**0**	**1**	×	**0**

- Bit 6

SZ bit	Data size selection
0	8 bits
1	16 bits

- Bit 4

CHNE bit	Enabling/disabling chain transfers
0	Chain transfers disabled
1	Chain transfers enabled

- Bit 3

DAMOD bit	Transfer destination address control
0	Fixed
1	Incremented

- Bit 2

SAMOD bit	Transfer source address control
0	Fixed
1	Incremented

- Bit 0

MODE bit	Transfer mode selection
0	Normal mode
1	Repeat mode

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

- DTC block size register 1 (DTBLS1)

Sets the DTC1 block size to 1 byte.

Symbol	7	6	5	4	3	2	1	0
DTBLS1	DTBLS17	DTBLS16	DTBLS15	DTBLS14	DTBLS13	DTBLS12	DTBLS11	DTBLS10
Value	01H							

- DTC transfer count register 1 (DTCCT1)
  Set the number of transfers by DTC1 to 7.

Symbol	7	6	5	4	3	2	1	0
DTCCT1	DTCCT17	DTCCT16	DTCCT15	DTCCT14	DTCCT13	DTCCT12	DTCCT11	DTCCT10
Value	07H							

- DTC source address register 1 (DTSAR1)
  Specify the transfer source address for data transfer to E911H.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTSAR1	DTSAR115	DTSAR114	DTSAR113	DTSAR112	DTSAR111	DTSAR110	DTSAR19	DTSAR18	DTSAR17	DTSAR16	DTSAR15	DTSAR14	DTSAR13	DTSAR12	DTSAR11	DTSAR10
Value	E911H															

- DTC destination address register 1 (DTDAR1)
  Specify the transfer destination address for data transfer to FF10H.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTDAR1	DTDAR115	DTDAR114	DTDAR113	DTDAR112	DTDAR111	DTDAR110	DTDAR19	DTDAR18	DTDAR17	DTDAR16	DTDAR15	DTDAR14	DTDAR13	DTDAR12	DTDAR11	DTDAR10
Value	FF10H															

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

4.8.13 DTCD0 Operation Start

Figure 4.17 shows the DTCD0 operation start.

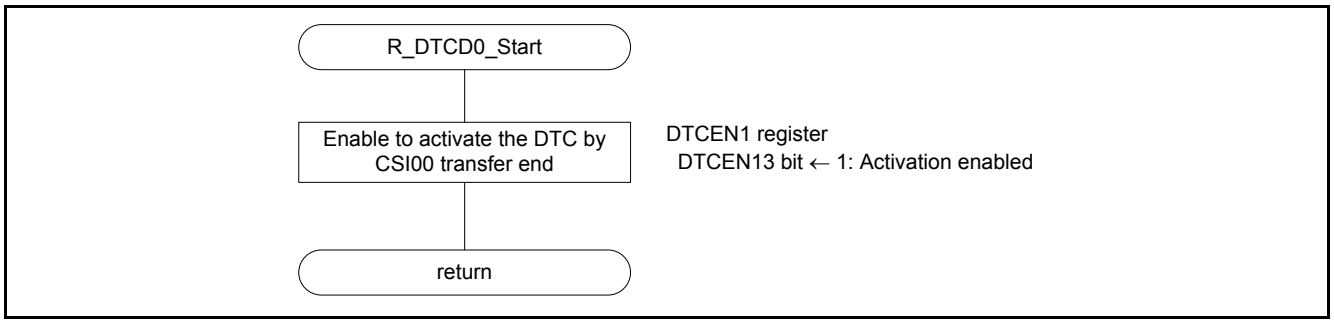


Figure 4.17 DTCD0 Operation Start

Enabling to activate the DTC by CSI00 transfer end

- DTC activation enable register 1 (DTCEN1)

Symbol	7	6	5	4	3	2	1	0
DTCEN1	DTCEN17	DTCEN16	DTCEN15	DTCEN14	**DTCEN13**	DTCEN12	DTCEN11	DTCEN10
Value	×	×	×	×	**1**	×	×	×

- Bit 3

DTCEN13 bit	DTC activation enable 13
0	Activation disabled
1	Activation enabled

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

4.8.14 DTCD0 Operation Stop

Figure 4.18 shows DTCD0 operation stop.

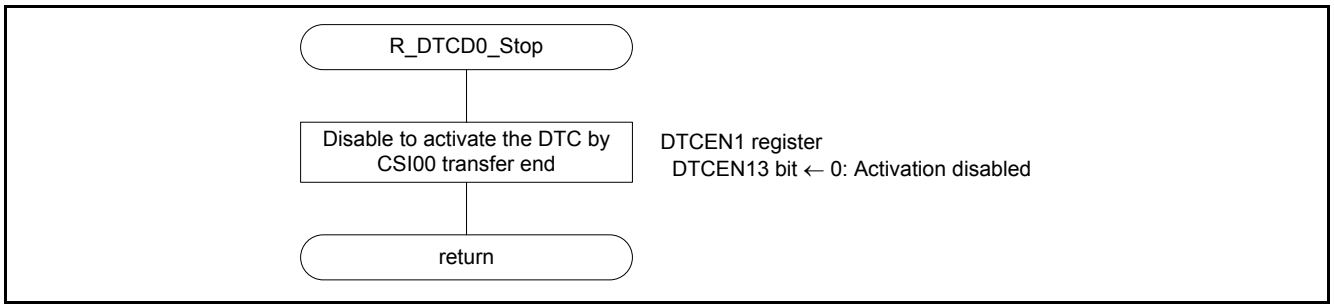


Figure 4.18 DTCD0 Operation Stop

Disabling to activate the DTC by CSI00 transfer end

- DTC activation enable register 1 (DTCEN1)

Symbol	7	6	5	4	3	2	1	0
DTCEN1	DTCEN17	DTCEN16	DTCEN15	DTCEN14	**DTCEN13**	DTCEN12	DTCEN11	DTCEN10
Value	×	×	×	×	**0**	×	×	×

- Bit 3

DTCEN13 bit	DTC activation enable 13
0	Activation disabled
1	Activation enabled

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit; blank cell: unchanged bit; –: reserved bit or unallocated bit

4.8.15 Main Processing

Figure 4.19 shows the main processing.

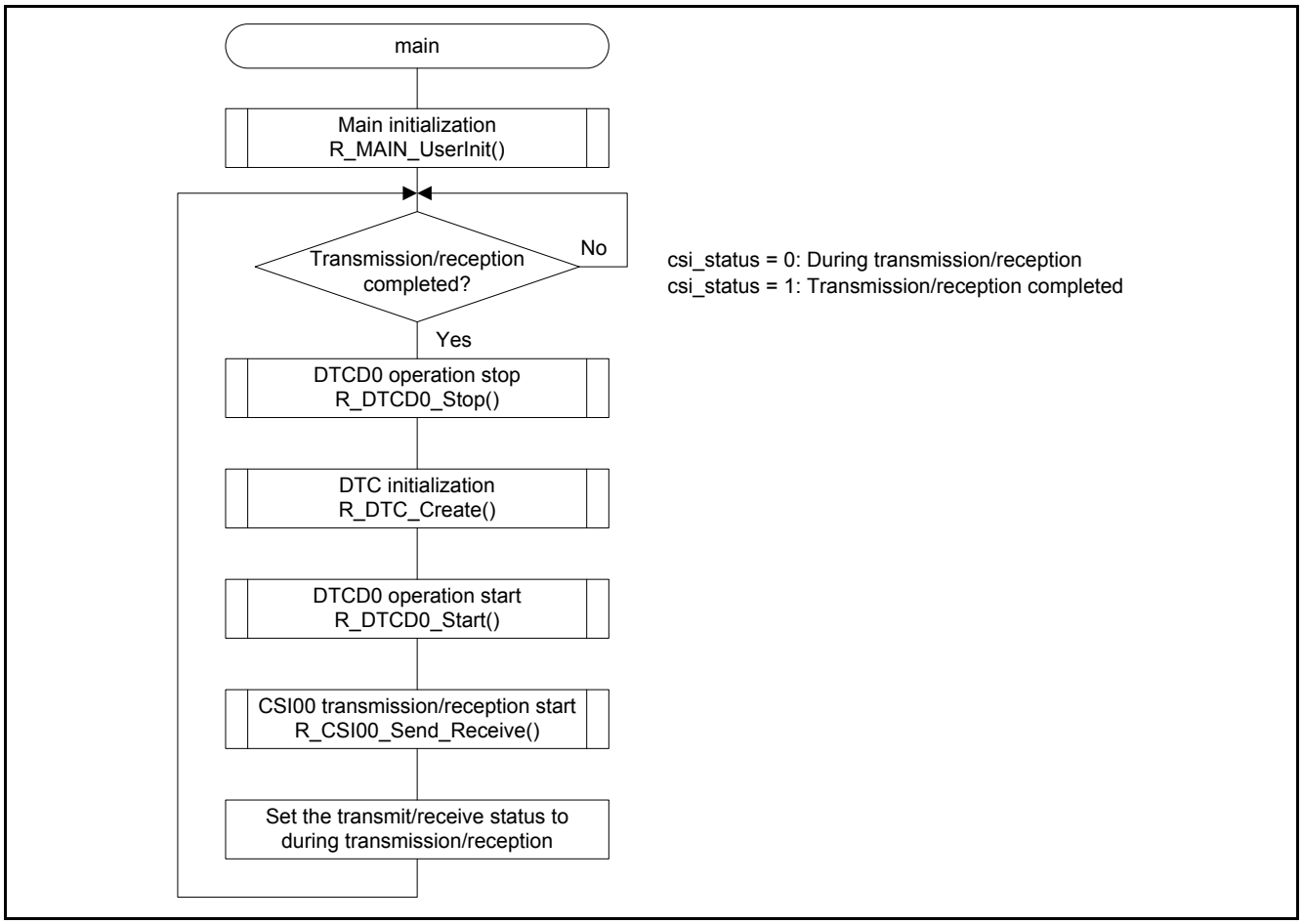


Figure 4.19 Main Processing

4.8.16 Main Initialization

Figure 4.20 shows the main initialization.

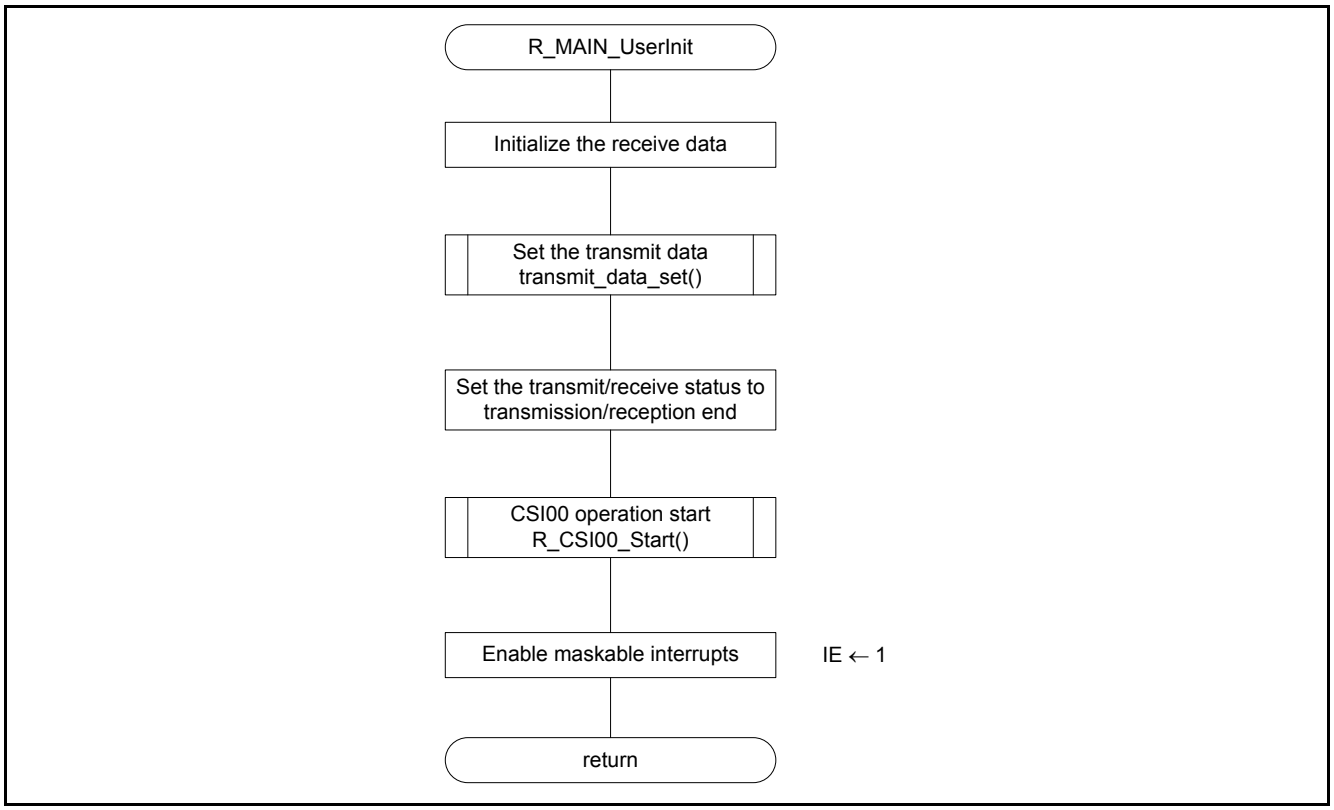


Figure 4.20 Main Initialization

4.8.17 Transmit Data Setting

Figure 4.21 shows the transmit data setting.

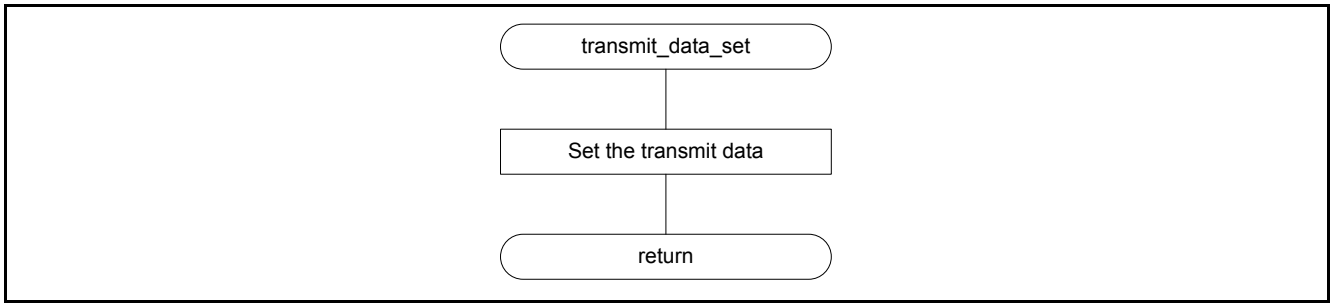


Figure 4.21 Transmit Data Setting

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RL78/G14 User's Manual: Hardware Rev.2.00 (R01UH0186EJ)
RL78 Family User's Manual: Software Rev.1.00 (R01US0015EJ)
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	RL78/G14 Using the DTC to Perform Continuous Clock Synchronous Serial Communication

Rev.	Date	Description	
		Page	Summary
1.00	Feb. 14, 2014	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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