
RL78/G14

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Timer RG Buffer Operation in PWM Mode

Abstract

This document describes a method to output a PWM waveform using buffer operation in PWM mode of RL78/G14 timer RG.

Products

RL78/G14

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

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1. Specifications

A PWM waveform with a 100 μ s period is output. The PWM waveform changes duty each time the predetermined period elapses. This application note defines the active level as low and the inactive level as high.

Table 1.1 lists the Peripheral Functions and Their Applications. Figure 1.1 shows the PWM Output Waveform.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Functions	Applications
Timer RG	PWM waveform output
Timer RJ	Duty change period generation

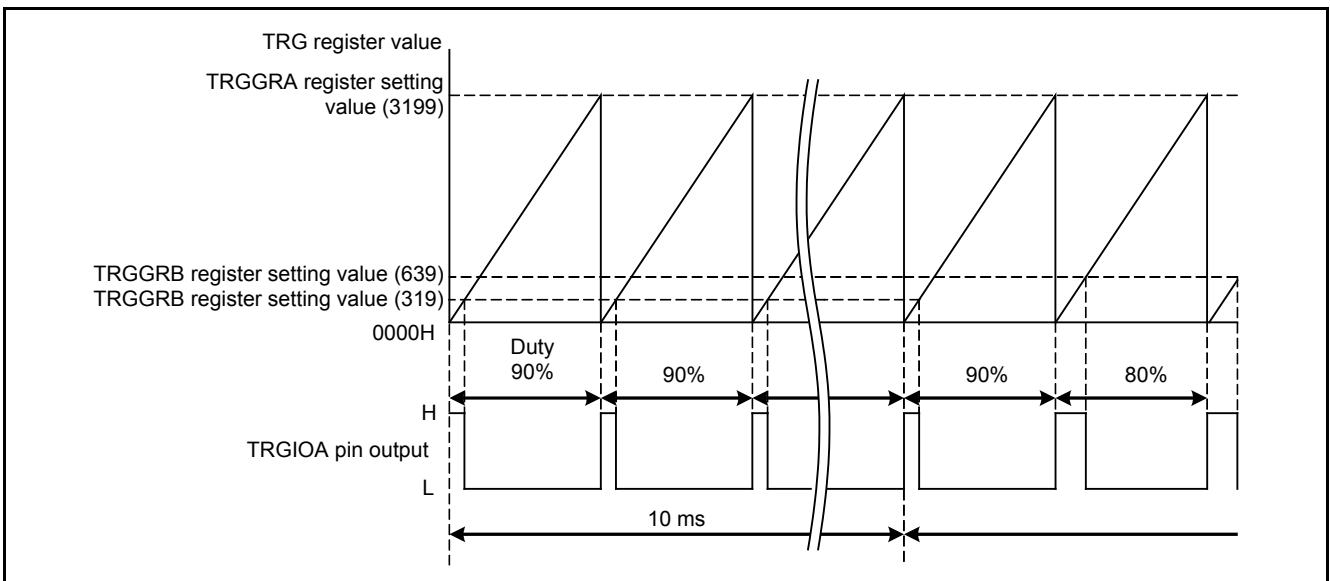


Figure 1.1 PWM Output Waveform

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	RL78/G14 (R5F104LEA)
Operating frequencies	<ul style="list-style-type: none"> • High-speed on-chip oscillator clock (fHOCO): 64 MHz (typical) • CPU/peripheral hardware clock (fCLK): 32 MHz
Operating voltage	5.0 V (2.9 to 5.5 V) LVD operation (VLVI): 2.81 V at the rising edge or 2.75 V at the falling edge in reset mode
Integrated development environment	Renesas Electronics Corporation CubeSuite+ V1.01.00
C compiler	Renesas Electronics Corporation CA78K0R V1.30
RL78/G14 code library	Renesas Electronics Corporation CodeGenerator for RL78/G14 V1.01.01

3. Hardware

3.1 Hardware Configuration

Figure 3.1 shows the Hardware Configuration used in this document.

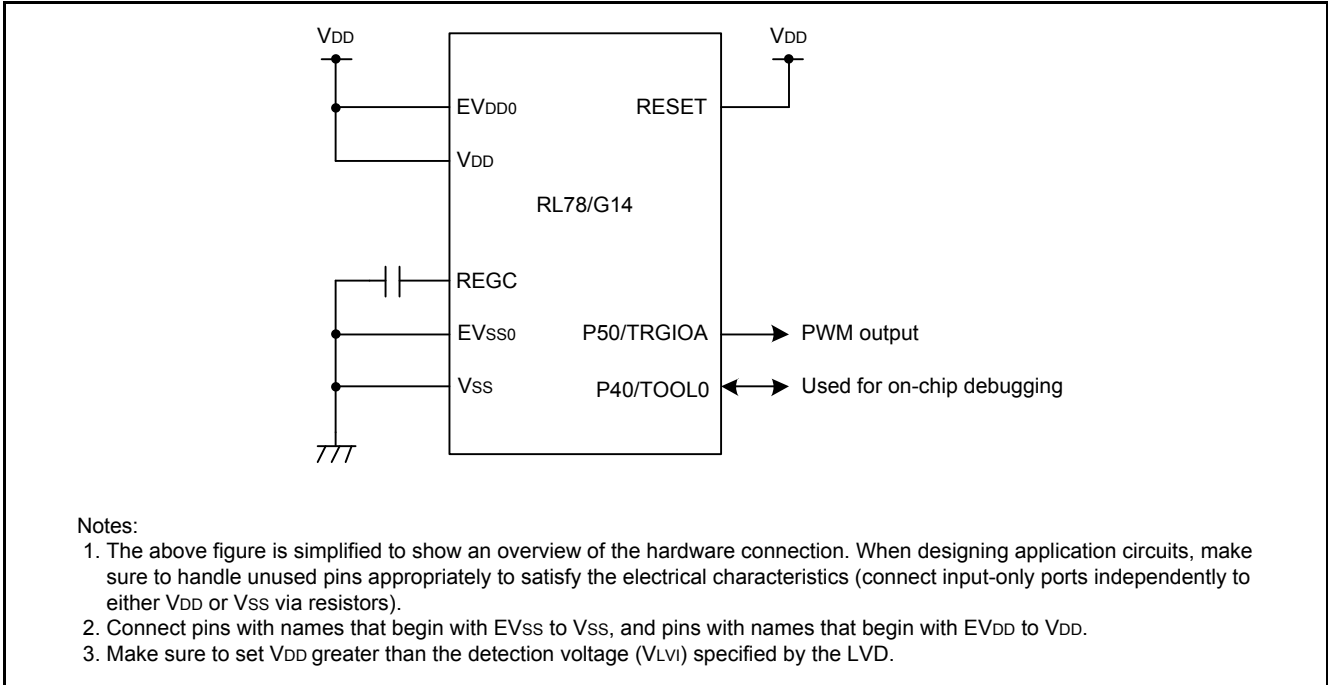


Figure 3.1 Hardware Configuration

3.2 Pin Used

Table 3.1 lists the Pin Used and Its Function.

Table 3.1 Pin Used and Its Function

Pin Name	I/O	Function
P50/TRGIOA	Output	PWM output

4. Software

4.1 Operation Overview

A PWM waveform with a 100 μ s period is output from the TRGIOA pin using PWM mode.

A PWM waveform duty changes in the following manner every 10 ms: 90% \rightarrow 80% \rightarrow ... \rightarrow 10% \rightarrow 0% \rightarrow 10% \rightarrow ... \rightarrow 90%. Timer RJ in timer mode is used to generate the period for changing the duty.

Settings are shown below.

Settings:

- Use fCLK (32 MHz) as the count source of timer RG.
- Clear the TRG register at the compare match with the TRGGRA register.
- Use the TRGGRD register as the buffer register.
- Do not use the TRGGRC register as the buffer register.
- Do not use the INTTRG interrupt.
- Use the fCLK (32 MHz) divided by 8 the count source of timer RJ.
- Disable TRJO output.
- Do not use the INTTRJ0 interrupt.

Figure 4.1 shows the Timing Diagram of the Buffer Operation.

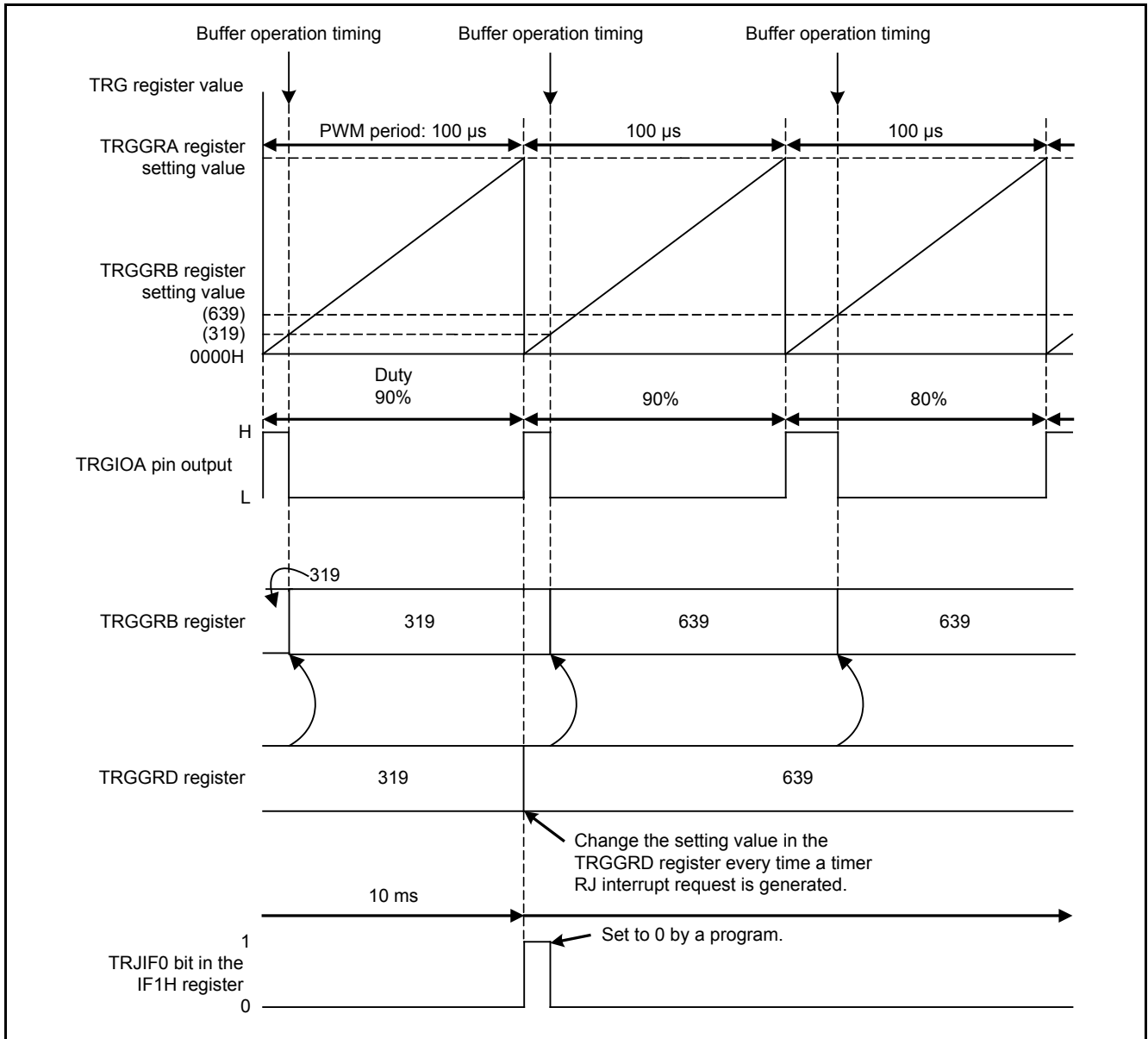


Figure 4.1 Timing Diagram of the Buffer Operation

4.1.1 Duty of the PWM Waveform

The PWM period and duty of a PWM waveform output from the TRGIOA pin can be calculated as follows:

(1) PWM period

$$\begin{aligned} \text{PWM period: } 100 \mu\text{s} &= 1/32 \text{ MHz} \times (\text{TRGGRA} + 1) \\ &= 31.25 \text{ ns} \times (3199 + 1) \end{aligned}$$

- (2) When initial output changes to 90% duty
 - Low active level: $90 \mu\text{s} = 1/32 \text{ MHz} \times (\text{TRGGRA} - \text{TRGGRB})$
 $= 31.25 \text{ ns} \times 2880$
 - High inactive level: $10 \mu\text{s} = 1/32 \text{ MHz} \times (\text{TRGGRB} + 1)$
 $= 31.25 \text{ ns} \times (319 + 1)$

Figure 4.2 shows the Output Timing When the Initial Output Changes to 90% Duty.

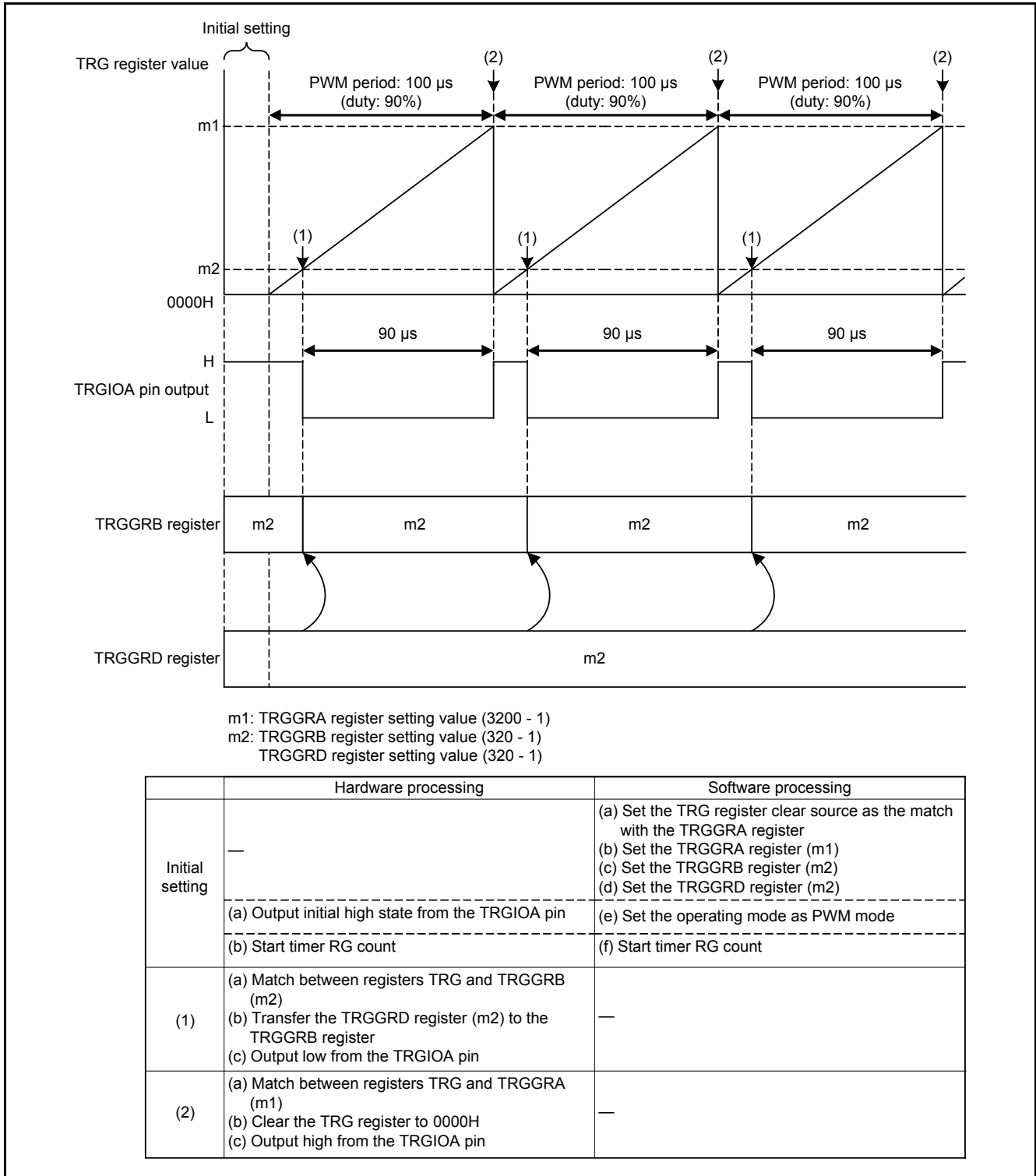


Figure 4.2 Output Timing When the Initial Output Changes to 90% Duty

- (3) When duty changes from 90% to 10%, 10% at a time
 Low active level: $(100 - N) \mu\text{s} = 1/32 \text{ MHz} \times (\text{TRGGRA} - M)$
 High inactive level: $N \mu\text{s} = 1/32 \text{ MHz} \times (\text{TRGGRB} + 1)$
 $= 31.25 \text{ ns} \times (M + 1)$

Table 4.1 lists the Duty and TRGGRB Register Setting Values.

Table 4.1 Duty and TRGGRB Register Setting Values

Duty (%)	90	80	70	60	50	40	30	20	10
High inactive level (N μs)	10	20	30	40	50	60	70	80	90
TRGGRB register setting value M	319	639	959	1279	1599	1919	2239	2559	2879

Figure 4.3 shows the Output Timing When XX% Duty Changes to YY% Duty (Assuming a 10% Decrease Starting at 90%).

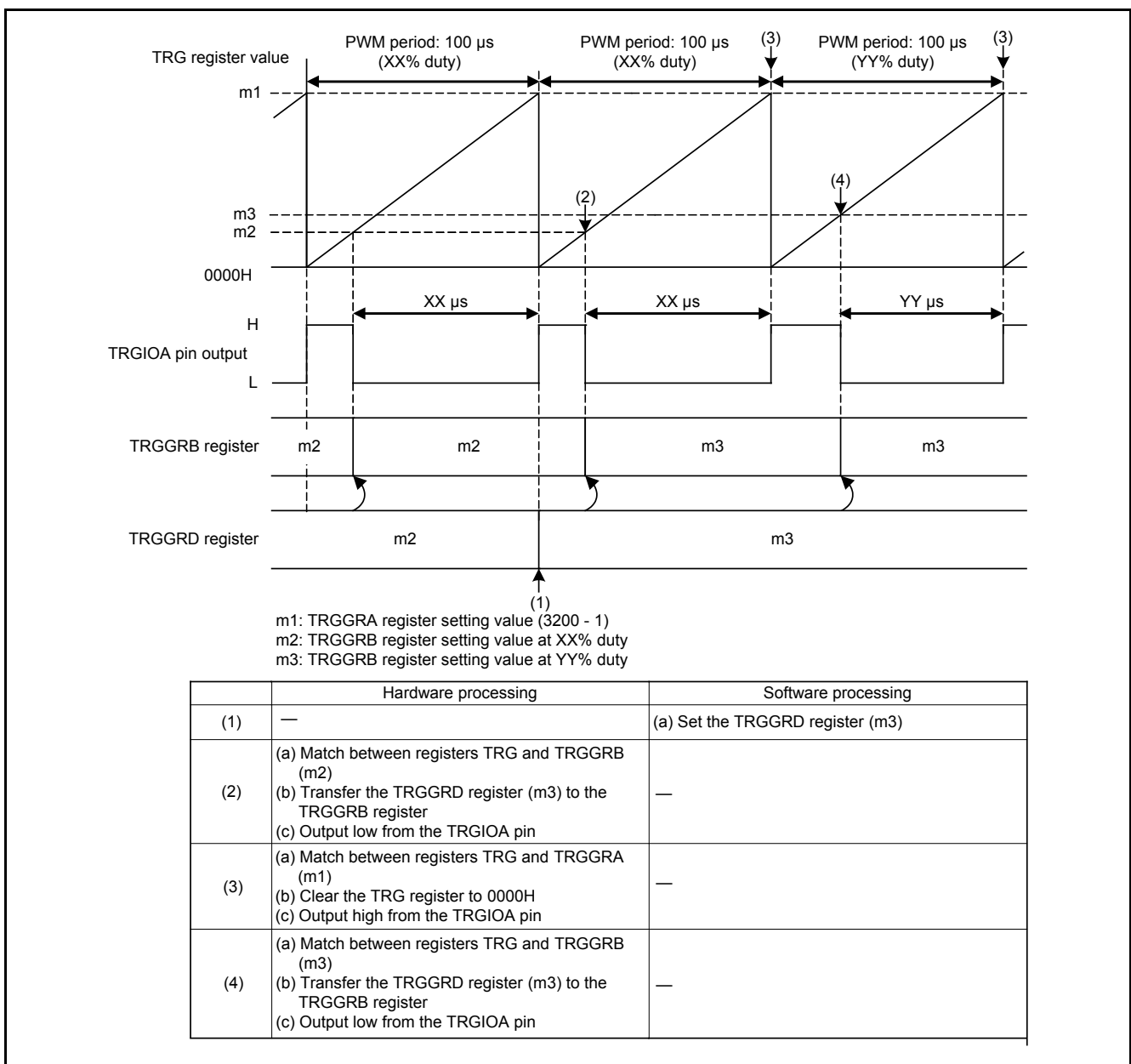


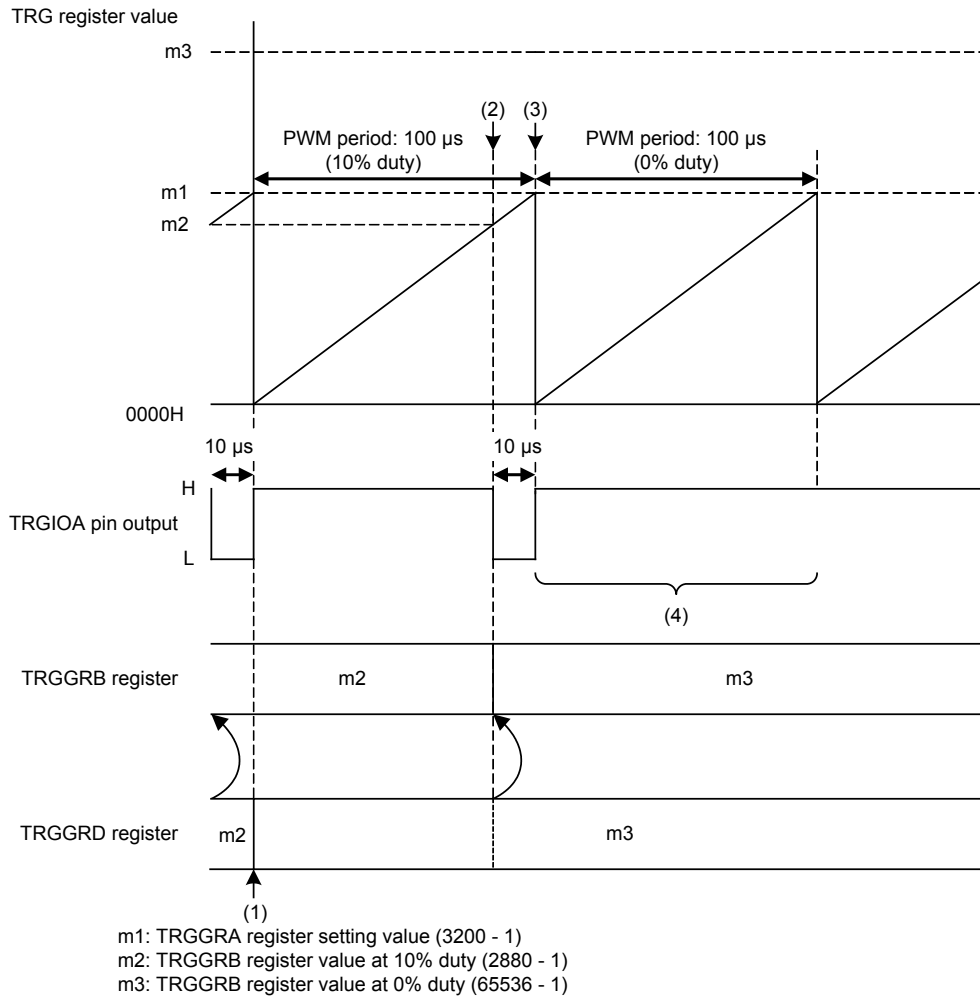
Figure 4.3 Output Timing When XX% Duty Changes to YY% Duty (Assuming a 10% Decrease Starting at 90%)

(4) When 10% duty changes to 0% duty

$$\begin{aligned}\text{Low active level: } 10 \mu\text{s} &= 1/32 \text{ MHz} \times (\text{TRGGRA} - \text{TRGGRB}) \\ &= 31.25 \text{ ns} \times 320\end{aligned}$$

$$\begin{aligned}\text{High inactive level: } 90 \mu\text{s} &= 1/32 \text{ MHz} \times (\text{TRGGRB} + 1) \\ &= 31.25 \text{ ns} \times (2879 + 1)\end{aligned}$$

Figure 4.4 shows the Output Timing When 10% Duty Changes to 0% Duty.



	Hardware processing	Software processing
(1)	—	(a) Set the TRGGRD register (m3)
(2)	(a) Match between registers TRG and TRGGRB (m2) (b) Transfer the TRGGRD register (m3) to the TRGGRB register (c) Output low from the TRGIOA pin	—
(3)	(a) Match between registers TRG and TRGGRA (m1) (b) Clear the TRG register to 0000H (c) Output high from the TRGIOA pin	—
(4)	(a) No match between registers TRG and TRGGRB (m3) (b) No change for the TRGIOA pin ⁽¹⁾	—

Note:

- When setting a value to the TRGGRB register that exceeds the value in the TRGGRA register, 0% duty is output since registers TRG and TRGGRB do not match.

Figure 4.4 Output Timing When 10% Duty Changes to 0% Duty

(5) When 0% duty changes to 10% duty

$$\begin{aligned} \text{Low active level: } 10 \mu\text{s} &= 1/32 \text{ MHz} \times (\text{TRGGRA} - \text{TRGGRB}) \\ &= 31.25 \text{ ns} \times 320 \end{aligned}$$

$$\begin{aligned} \text{High inactive level: } 90 \mu\text{s} &= 1/32 \text{ MHz} \times (\text{TRGGRB} + 1) \\ &= 31.25 \text{ ns} \times (2879 + 1) \end{aligned}$$

Figure 4.5 shows the Output Timing When 0% Duty Changes to 10% Duty.

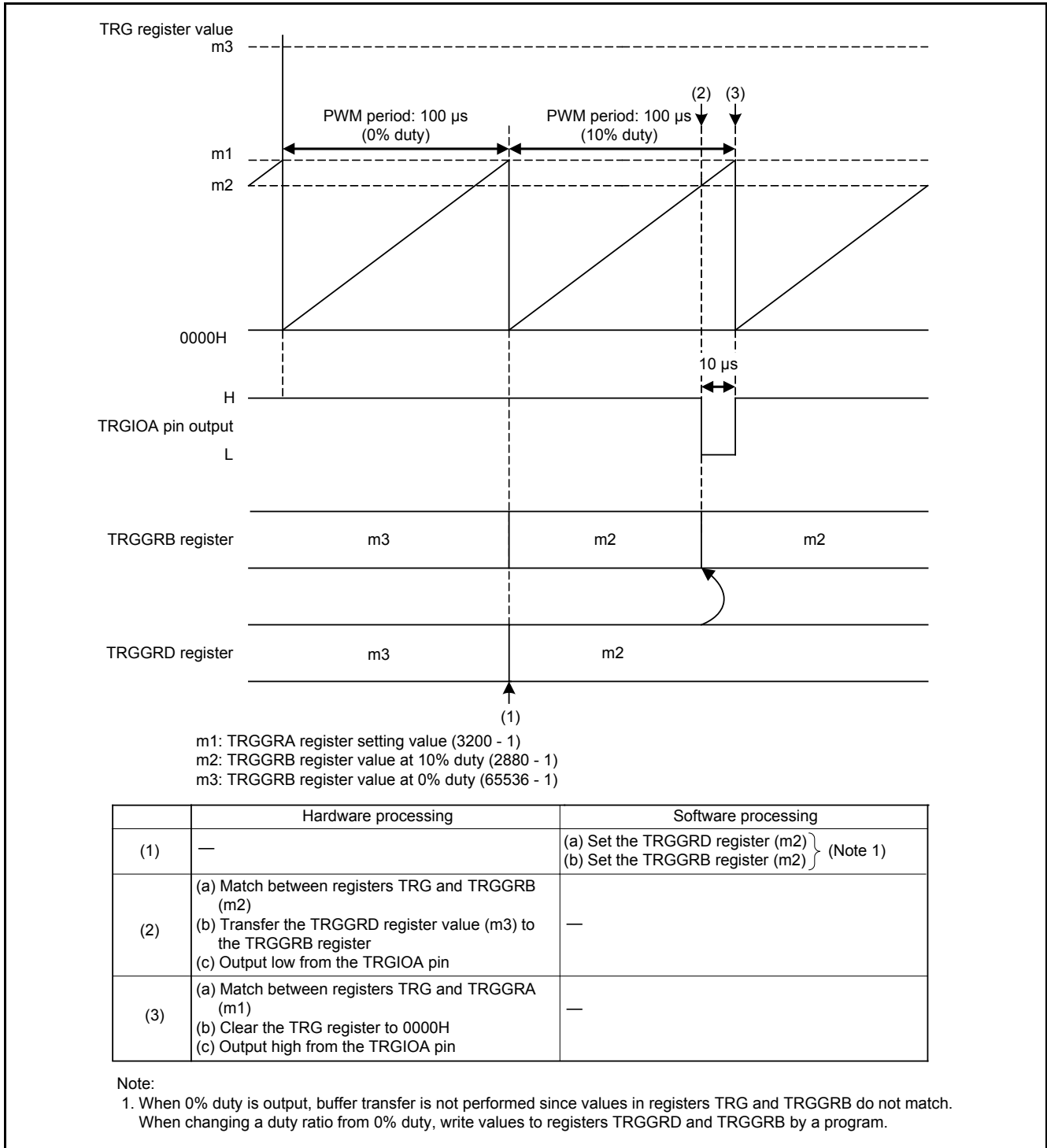


Figure 4.5 Output Timing When 0% Duty Changes to 10% Duty

4.2 Option-Setting Memory

Table 4.2 lists the Option-Setting Memory Configured in the Sample Code. When necessary, set a value suited to the user system.

Table 4.2 Option-Setting Memory Configured in the Sample Code

Address	Setting Value	Contents
000C0H/010C0H	11101111B	Watchdog timer operation is stopped (count is stopped after reset)
000C1H/010C1H	01111111B	LVD reset mode Detection voltage: Rising edge 2.81 V/falling edge 2.75 V
000C2H/010C2H	11111000B	Internal high-speed oscillation HS mode: 64 MHz
000C3H/010C3H	10000100B	On-chip debugging enabled

4.3 Constants

Table 4.3 lists the Constants Used in the Sample Code.

Table 4.3 Constants Used in the Sample Code

Constant Name	Setting Value	Contents
Duty_dec	0	Duty decreasing mode (decreases 10% at a time)
Duty_inc	10	Duty increasing mode (increases 10% at a time)
Duty_inc_end	18	Duty increasing mode completed

4.4 Variables

Table 4.4 lists the Global Variable and Table 4.5 lists the const Variable.

Table 4.4 Global Variable

Type	Variable Name	Contents	Function Used
unsigned char	duty_mode	Duty mode setting	pwm_duty_chg

Table 4.5 const Variable

Type	Variable Name	Contents	Function Used
const unsigned short	TRGGRD_TBL[]	Duty change table data	pwm_duty_chg

4.5 Functions

Table 4.6 lists the Functions.

Table 4.6 Functions

Function Name	Outline
hdwinit	Initial setting
R_Systeminit	Initial setting of peripheral functions
R_CGC_Create	Initial setting of the CPU
R_TMR_RJ0_Create	Initial setting of timer RJ
R_TMR_RG0_Create	Initial setting of timer RG
main	Main processing
R_TMR_RJ0_Start	Timer RJ count start setting
timer_rg_start	Timer RG count start setting
pwm_duty_chg	PWM duty change processing

4.6 Function Specifications

The following tables list the sample code function specifications.

hdwinit	
Outline	Initial setting
Header	None
Declaration	void hdwinit(void)
Description	Perform the initial setting of peripheral functions.
Argument	None
Return Value	None
R_Systeminit	
Outline	Initial setting of peripheral functions
Header	None
Declaration	void R_Systeminit(void)
Description	Perform the initial setting of peripheral functions used in this document.
Argument	None
Return Value	None
R_CGC_Create	
Outline	Initial setting of the CPU
Header	None
Declaration	void R_CGC_Create(void)
Description	Perform the initial setting of the CPU.
Argument	None
Return Value	None

R_TMR_RJ0_Create	
Outline	Initial setting of timer RJ
Header	None
Declaration	void R_TMR_RJ0_Create(void)
Description	Perform the initial setting to change the duty every 10 ms in timer mode of timer RJ.
Argument	None
Return Value	None

R_TMR_RG0_Create	
Outline	Initial setting of timer RG
Header	None
Declaration	void R_TMR_RG0_Create(void)
Description	Perform the initial setting to use buffer operation in PWM mode of timer RG.
Argument	None
Return Value	None

main	
Outline	Main processing
Header	None
Declaration	void main(void)
Description	Perform main processing.
Argument	None
Return Value	None

R_TMR_RJ0_Start	
Outline	Timer RJ count start setting
Header	None
Declaration	void R_TMR_RJ0_Start(void)
Description	Perform timer RJ count start setting.
Argument	None
Return Value	None

timer_rg_start	
Outline	Timer RG count start setting
Header	None
Declaration	void timer_rg_start(void)
Description	Perform timer RG count start setting.
Argument	None
Return Value	None

pwm_duty_chg

Outline	PWM duty change processing
Header	None
Declaration	void pwm_duty_chg(void)
Description	Change the duty.
Argument	None
Return Value	None

4.7 Flowcharts

4.7.1 Overall Flowchart

Figure 4.6 shows the Overall Flowchart.

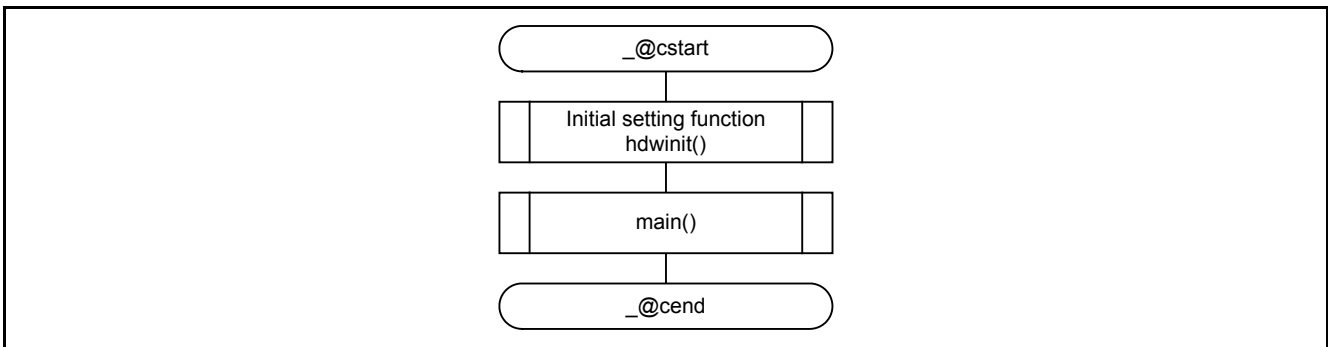


Figure 4.6 Overall Flowchart

4.7.2 Initial Setting

Figure 4.7 shows the Initial Setting.

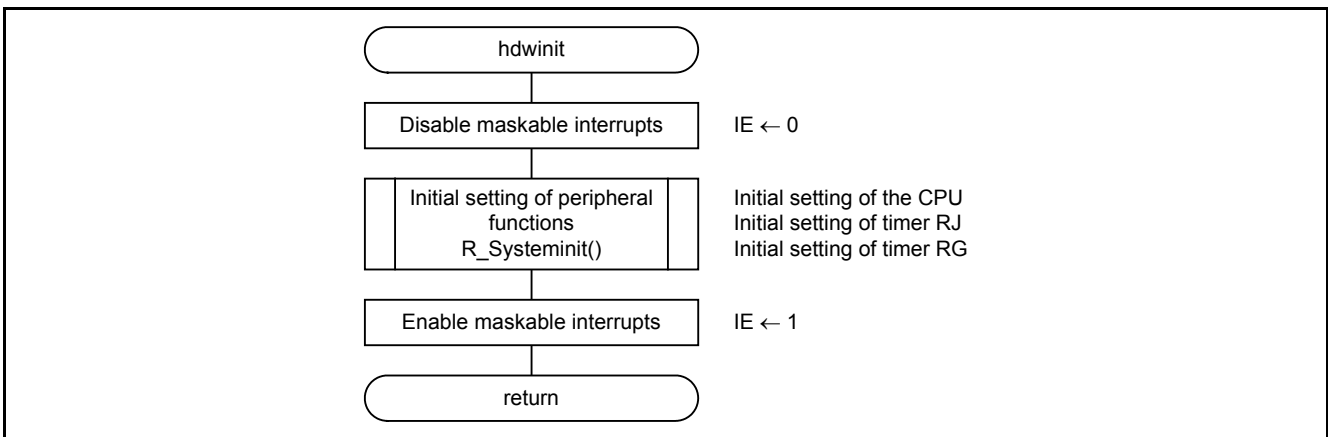


Figure 4.7 Initial Setting

4.7.3 Initial Setting of Peripheral Functions

Figure 4.8 shows the Initial Setting of Peripheral Functions.

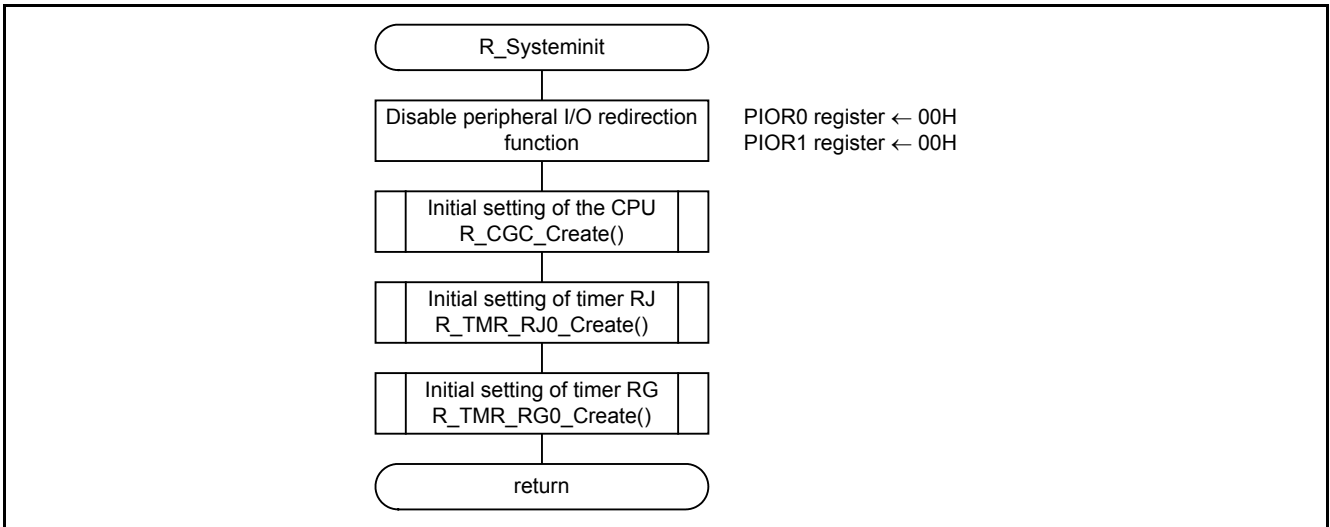


Figure 4.8 Initial Setting of Peripheral Functions

4.7.4 Initial Setting of the CPU

Figure 4.9 shows the Initial Setting of the CPU.

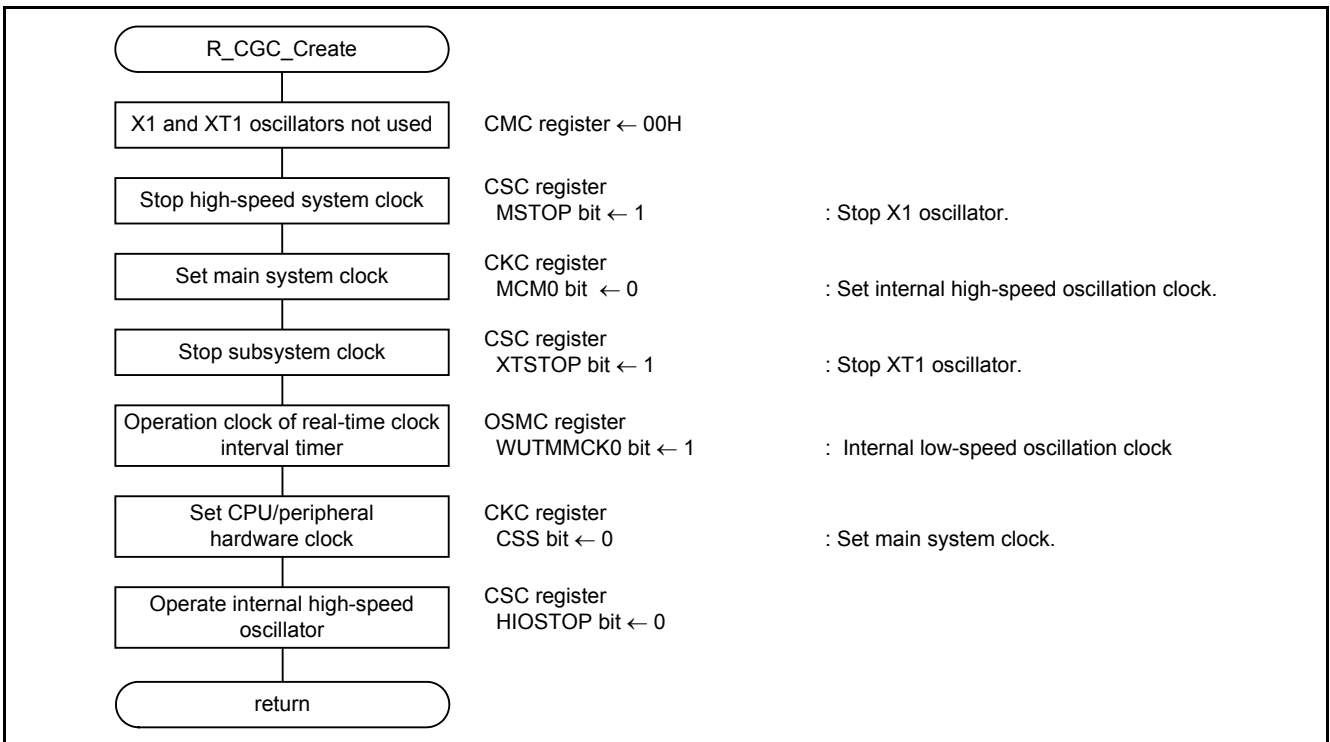


Figure 4.9 Initial Setting of the CPU

4.7.5 Initial Setting of Timer RJ

Figure 4.10 shows the Initial Setting of Timer RJ.

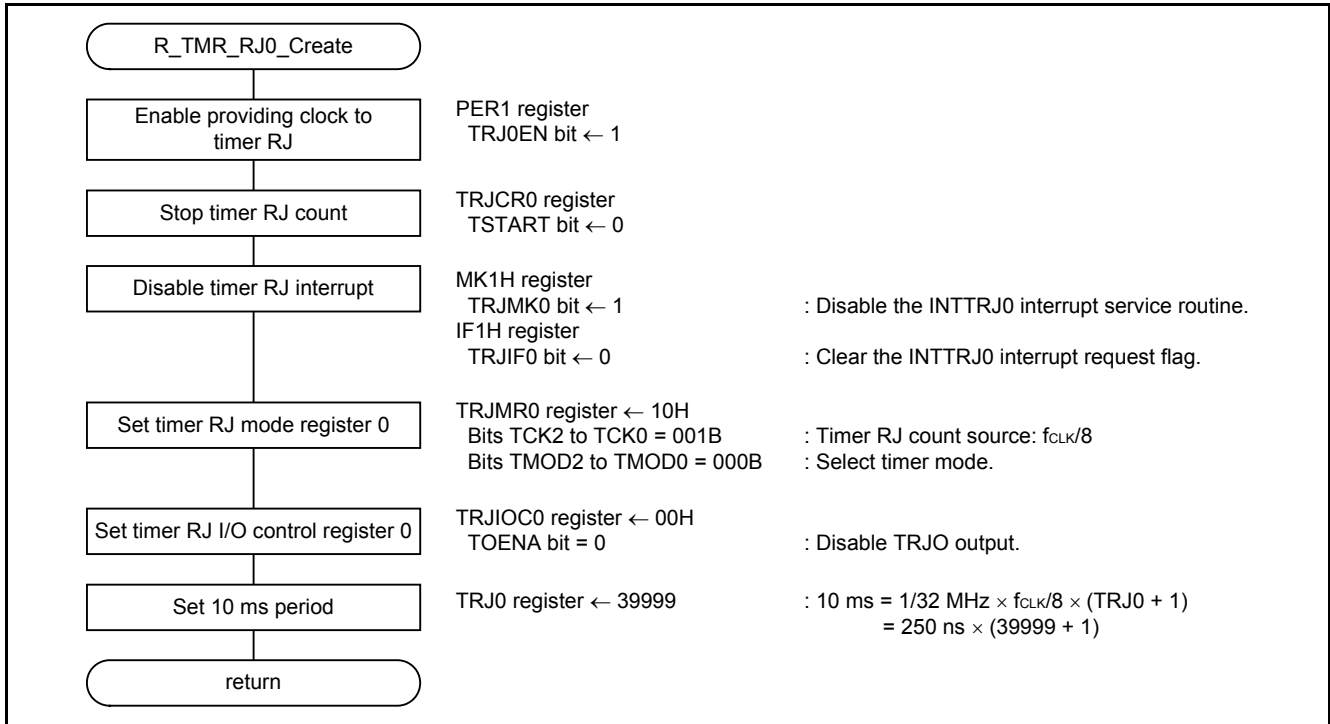


Figure 4.10 Initial Setting of Timer RJ

Enable providing a clock to timer RJ.

- Peripheral Enable Register 1 (PER1)
Enable providing a clock to timer RJ.

Symbol	7	6	5	4	3	2	1	0
PER1	DACEN	TRGEN	COMPEN	TRD0EN	DTCEN	0	0	TRJ0EN
Setting Value	x		x	x	x	—	—	1

Bit 0

TRJ0EN	Control of timer RJ0 input clock supply
0	Stops input clock supply. <ul style="list-style-type: none"> SFR used by timer RD cannot be written. Timer RJ0 is in the reset status.
1	Enables input clock supply. <ul style="list-style-type: none"> SFR used by timer RJ0 can be read and written.

Stop the timer RJ count.

- Timer RJ Control Register 0 (TRJCR0)
Stop the timer RJ count.

Symbol	7	6	5	4	3	2	1	0
TRJCR0	—	—	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
Setting Value	—	—	x	x	—	x	x	0

Bit 0

TSTART	Timer RJ count start
0	Count stops
1	Count starts

Count operation is started by writing 1 to the TSTART bit and stopped by writing 0. When the TSTART bit is set to 1 (count starts), the TCSTF bit is set to 1 (count in progress) in synchronization with the count source. Also, after 0 is written to the TSTART bit, the TCSTF bit is set to 0 (count stops) in synchronization with the count source.

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Disable the timer RJ interrupt.

- Interrupt Mask Flag Register (MK1H)
Disable the INTTRJ interrupt.

Symbol	7	6	5	4	3	2	1	0
MK1H	TMMK10	TRJMK0	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
Setting Value	x	1	x	x	x	x	x	x

Bit 6

TRJMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

- Interrupt Request Flag Register (IF1H)
Clear the INTTRD0 interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF1H	TMIF10	TRJIF0	SRIF3 CSIF31 IICIF31	STIF3 CSIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
Setting Value	x	0	x	x	x	x	x	x

Bit 6

TRJIF0	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Refer to the RL78/G14 user’s manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set timer RJ mode register 0.

- Timer RJ Mode Register 0 (TRJMR0)

Set $f_{CLK}/8$ to the count source and select timer mode for the operating mode.

Symbol	7	6	5	4	3	2	1	0
TRJMR0	—	TCK2	TCK1	TCK0	TEDGPL	TMOD2	TMOD1	TMOD0
Setting Value	—	0	0	1	x	0	0	0

Bits 6 to 4

TCK2	TCK1	TCK0	Timer RJ count source select
0	0	0	f_{CLK}
0	0	1	$f_{CLK}/8$
0	1	0	Do not set.
0	1	1	$f_{CLK}/2$
1	0	0	f_{IL}
1	0	1	Event input from event link controller (ELC)
1	1	0	f_{SUB}
1	1	1	Do not set.

Bits 2 to 0

TMOD2	TMOD1	TMOD0	Timer RJ operating mode select
0	0	0	Timer mode
0	0	1	Pulse output mode
0	1	0	Event counter mode
0	1	1	Pulse width measurement mode
1	0	0	Pulse period measurement mode
1	0	1	Do not set.
1	1	0	Do not set.
1	1	1	Do not set.

Set timer RJ I/O control register 0.

- Timer RJ I/O Control Register 0 (TRJIOC0)

Disable TRJO output.

Symbol	7	6	5	4	3	2	1	0
TRJIOC0	TIOGT1	TIOGT0	TIPF1	TIPF0	—	TOENA	—	TEDGSEL
Setting Value	x	x	x	x	—	0	—	x

Bit 2

TOENA	TRJO output enable
0	TRJO output disabled (port)
1	TRJO output enabled

Refer to the RL78/G14 user’s manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set 10 ms period.

- Timer RJ Count Register 0 (TRJ0), Timer RJ Reload Register
Set 9C3FH to timer RJ count register 0.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRJ0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Setting Value	1	0	0	1	1	1	0	0	0	0	1	1	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	16-bit counter and reload register	0001H to FFFFH

Refer to the RL78/G14 user’s manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

4.7.6 Initial Setting of Timer RG

Figure 4.11 shows the Initial Setting of Timer RG.

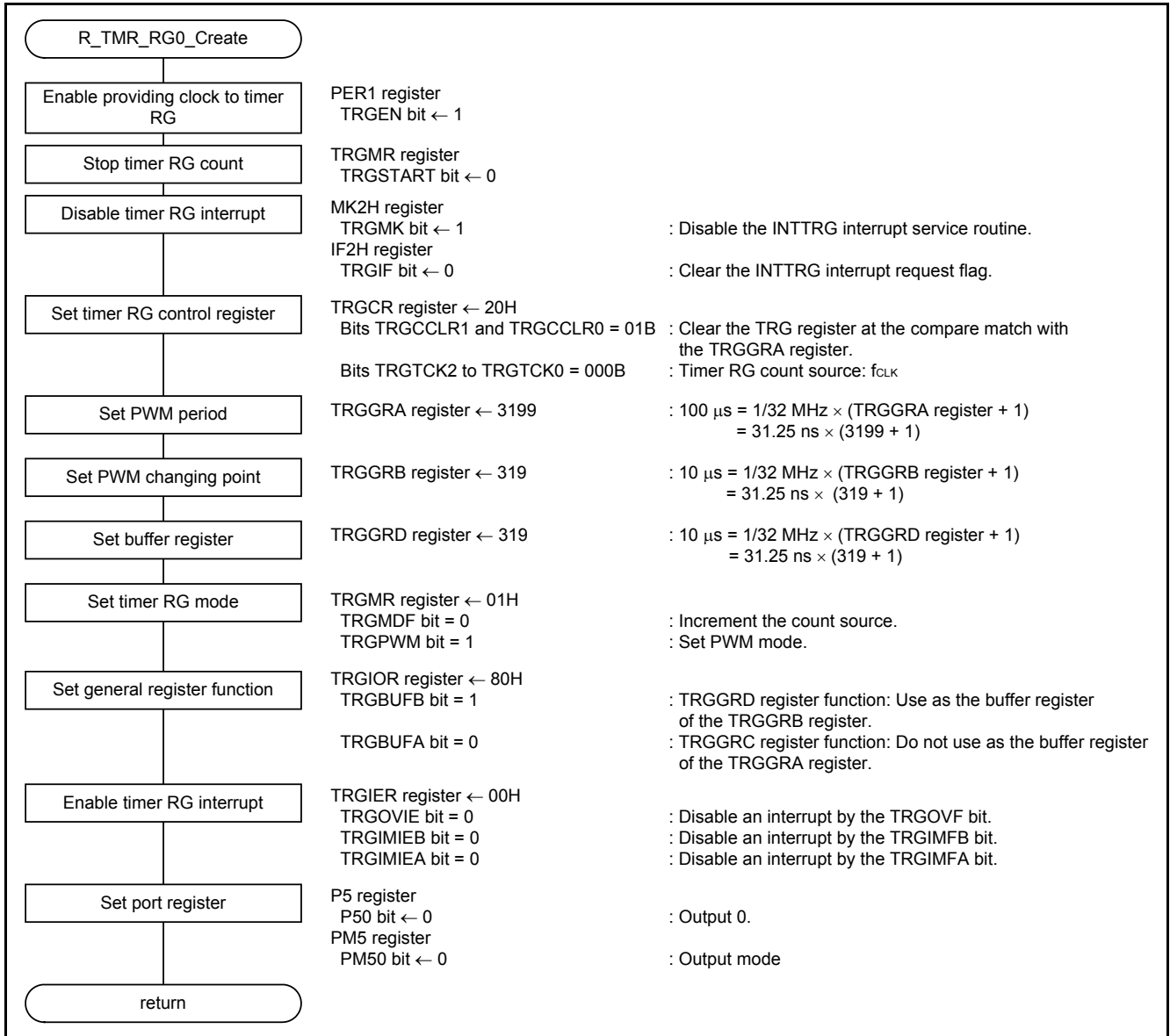


Figure 4.11 Initial Setting of Timer RG

Enable providing a clock to timer RG.

- Peripheral Enable Register 1 (PER1)
Enable providing a clock to timer RG.

Symbol	7	6	5	4	3	2	1	0
PER1	DACEN	TRGEN	CMPEN	TRD0EN	DTCEN	0	0	TRJ0EN
Setting Value	x	1	x	x	x	—	—	

Bit 6

TRGEN	Control of timer RG input clock supply
0	Stops input clock supply. • SFR used by timer RG cannot be written. • Timer RG is in the reset status.
1	Enables input clock supply. • SFR used by timer RG can be read and written.

Stop the timer RG count.

- Timer RG Mode Register (TRGMR)
Stop the timer RG count.

Symbol	7	6	5	4	3	2	1	0
TRGMR	TRGSTART	TRGELCICE	TRGDFCK1	TRGDFCK0	TRGDFB	TRGDFA	TRGMDF	TRGPWM
Setting Value	0	x	x	x	x	x		

Bit 7

TRGSTART	TRG count start
0	Count stops, and PWM output signal (TRGIOA pin) is initialized (in PWM mode)
1	Count starts

Disable the timer RG interrupt.

- Interrupt Mask Flag Register (MK2H)
Disable the INTTRG interrupt.

Symbol	7	6	5	4	3	2	1	0
MK2H	FLMK	IICAMK1	1	SREMK3 TMMK13H	TRGMK	TRDMK1	TRDMK0	PMK11 CMPMK1
Setting Value	x	x	—	x	1	x	x	x

Bit 3

TRGMK	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

- Interrupt Request Flag Register (IF2H)
Clear the INTTRG interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF2H	FLIF	IICAIF1	0	SREIF3 TMIF13H	TRGIF	TRDIF1	TRDIF0	PIF11 CMPIF1
Setting Value	x	x	—	x	0	x	x	x

Bit 3

TRGIF	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Set timer RG control register.

- Timer RG Control Register (TRGCR)
Clear the TRG register at the compare match with the TRGGRA register. Set fCLK to the count source.

Symbol	7	6	5	4	3	2	1	0
TRGCR	—	TRGCCLR1	TRGCCLR0	TRGCKEG1	TRGCKEG0	TRGTCK2	TRGTCK1	TRGTCK0
Setting Value	—	0	1	x	x	0	0	0

Bits 6 and 5

TRGCCLR1	TRGCCLR0	TRG register clear source select
0	0	Clear disabled
0	1	Clear by input capture or compare match with TRGGRA
1	0	Clear by input capture or compare match with TRGGRB
1	1	Do not set.

Bits 2 to 0

TRGTCK2	TRGTCK1	TRGTCK0	Count source select
0	0	0	fCLK
0	0	1	fCLK/2
0	1	0	fCLK/4
0	1	1	fCLK/8
1	0	0	fCLK/32
1	0	1	TRGCLKA input
1	1	0	Do not set.
1	1	1	TRGCLKB input

Refer to the RL78/G14 user’s manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set PWM period.

- Timer RG General Register A (TRGGRA)
Set 0C7FH to timer RG general register A.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRGGRA	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	1	1	0	0	0	1	1	1	1	1	1	1

—	Function
Bits 15 to 0	Function varies depending on the mode or the function. Table 4.7 lists the TRGGRA Register Function.

Set the PWM changing point.

- Timer RG General Register B (TRGGRB)
Set 013FH to timer RG general register B.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRGGRB	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

—	Function
Bits 15 to 0	Function varies depending on the mode or the function. Table 4.7 lists the TRGGRB Register Function.

Set the buffer register.

- Timer RG General Register D (TRGGRD)
Set 013FH to timer RG general register D.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRGGRD	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

—	Function
Bits 15 to 0	Function varies depending on the mode or the function. Table 4.7 lists the TRGGRD Register Function.

Refer to the RL78/G14 user’s manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Table 4.7 General Register Functions

Mode, Function	Register	Setting	Function
Input capture	TRGGRA	TRGIOR (TRGIOA2 = 1) TRGMR (TRGPWM = 0)	Input capture register (stores value of TRG register)
	TRGGRB	TRGIOR (TRGIOB2 = 1) TRGMR (TRGPWM = 0)	Input capture register (stores value of TRG register)
Output compare	TRGGRA	TRGIOR (TRGIOA2 = 0) TRGMR (TRGPWM = 0)	Output compare register (stores compare value with TRG register and outputs set value to TRGIOA at compare match)
	TRGGRB	TRGIOR (TRGIOB2 = 0) TRGMR (TRGPWM = 0)	Output compare register (stores compare value with TRG register and outputs set value to TRGIOB at compare match)
PWM	TRGGRA	TRGMR (TRGPWM = 1)	Output compare register (outputs high level to TRGIOA at compare match)
	TRGGRB		Output compare register (outputs low level to TRGIOA at compare match)
Common	TRGGRC	TRGIOR (TRGBUFA = 0)	Not used
	TRGGRD	TRGIOR (TRGBUFB = 0)	Not used
	TRGGRC	TRGIOR (TRGBUFA = 1)	Buffer register for TRGGRA (transfers from/to TRGGRA) <ul style="list-style-type: none"> • When TRGIOA2 = 1 Input capture signal: Receive previous input capture value from TRGGRA • When TRGIOA2 = 0 TRG and TRGGRA compare match: Send next expected compare value to TRGGRA
	TRGGRD	TRGIOR (TRGBUFB = 1)	Buffer register for TRGGRB (transfers from/to TRGGRB) <ul style="list-style-type: none"> • When TRGIOB2 = 1 Input capture signal: Receive previous input capture value from TRGGRB • When TRGIOB2 = 0 TRG and TRGGRB compare match: Send next expected compare value to TRGGRB

Set timer RG mode.

- Timer RG Mode Register (TRGMR)
Set the count to increment, and set PWM mode to timer RG.

Symbol	7	6	5	4	3	2	1	0
TRGMR	TRGSTART	TRGELCICE	TRGDFCK1	TRGDFCK0	TRGDFB	TRGDFA	TRGMDF	TRGPWM
Setting Value		x	x	x	x	x	0	1

Bit 1

TRGMDF	Phase counting mode select
0	Increment
1	Phase counting mode

When the TRGMDF bit is set to 0, the counter counts the count source set by bits TRGTCK0 to TRGTCK2 in the TRGCR register.

Bit 0

TRGPWM	PWM mode select
0	Timer Mode
1	PWM mode

Set the general register function.

- Timer RG I/O Control Register (TRGIOR)
Use the TRGGRD register function as the buffer register of the TRGGRB register, and do not use the TRGGRC register function as the buffer register of the TRGGRA register.

Symbol	7	6	5	4	3	2	1	0
TRGIOR	TRGBUFB	TRGIOB2	TRGIOB1	TRGIOB0	TRGBUFA	TRGIOA2	TRGIOA1	TRGIOA0
Setting Value	1	x	x	x	0	x	x	x

Bit 7

TRGBUFB	TRGGRD register function select
0	Not used as buffer register for TRGGRB register
1	Used as buffer register for TRGGRB register

Bit 3

TRGBUFA	TRGGRC register function select
0	Not used as buffer register for TRGGRA register
1	Used as buffer register for TRGGRA register

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Enable the timer RG interrupt.

- Timer RG Interrupt Enable Register (TRGIER)
Disable the timer RG interrupt.

Symbol	7	6	5	4	3	2	1	0
TRGIER	—	—	—	—	TRGOVIE	TRGUDIE	TRGIMIEB	TRGIMIEA
Setting Value	—	—	—	—	0	x	0	0

Bit 3

TRGOVIE	Overflow interrupt enable
0	Interrupt by TRGOVF bit disabled
1	Interrupt by TRGOVF bit enabled

Bit 1

TRGIMIEB	Input-capture/compare-match interrupt enable B
0	Interrupt by TRGIMFB bit disabled
1	Interrupt by TRGIMFB bit enabled

Bit 0

TRGIMIEA	Input-capture/compare-match interrupt enable A
0	Interrupt by TRGIMFA bit disabled
1	Interrupt by TRGIMFA bit enabled

Set a port register.

- Port Register 5 (P5)
Set port register 5.

Symbol	7	6	5	4	3	2	1	0
P5	P57	P56	P55	P54	P53	P52	P51	P50
Setting Value	x	x	x	x	x	x	x	0

Bit 0

P50	Output data control
0	Output 0
1	Output 1

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

- Port Mode Register 5 (PM5)
Set P50 pin to output mode.

Symbol	7	6	5	4	3	2	1	0
PM5	PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50
Setting Value	x	x	x	x	x	x	x	0

Bit 0

PM50	P50 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

4.7.7 Main Processing

Figure 4.12 shows the Main Processing.

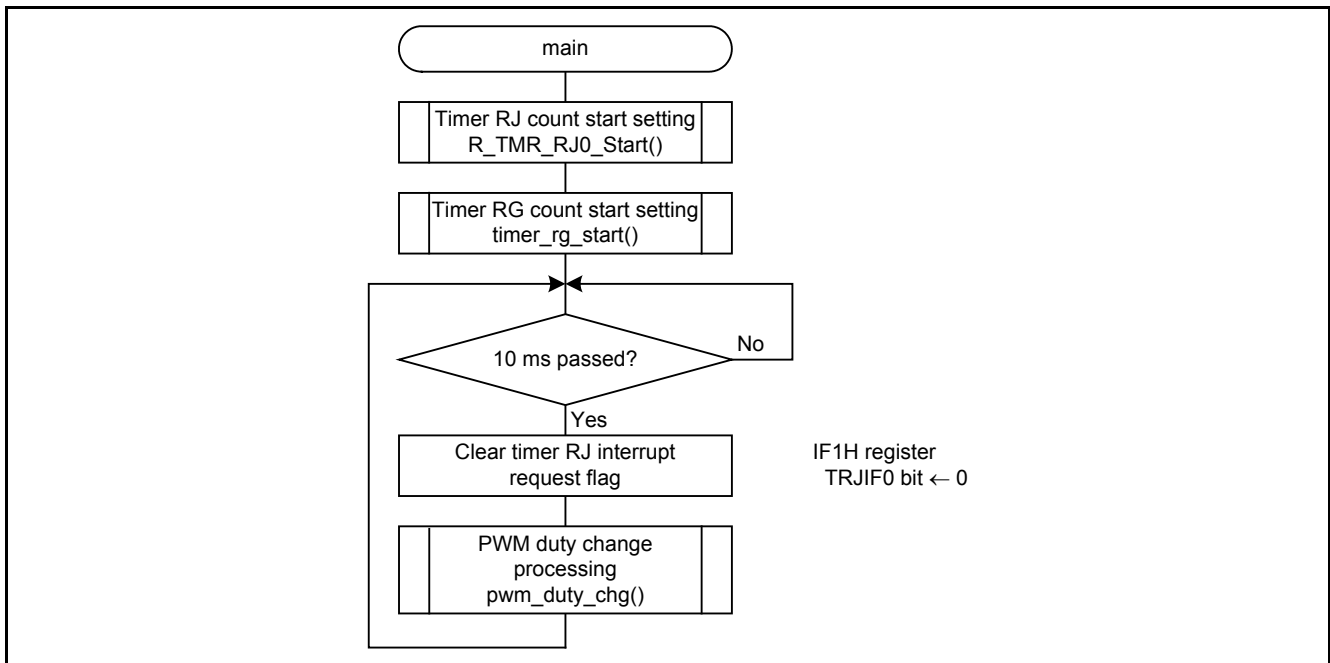


Figure 4.12 Main Processing

Refer to the RL78/G14 user’s manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

4.7.8 Timer RJ Count Start Setting

Figure 4.13 shows the Timer RJ Count Start Setting.

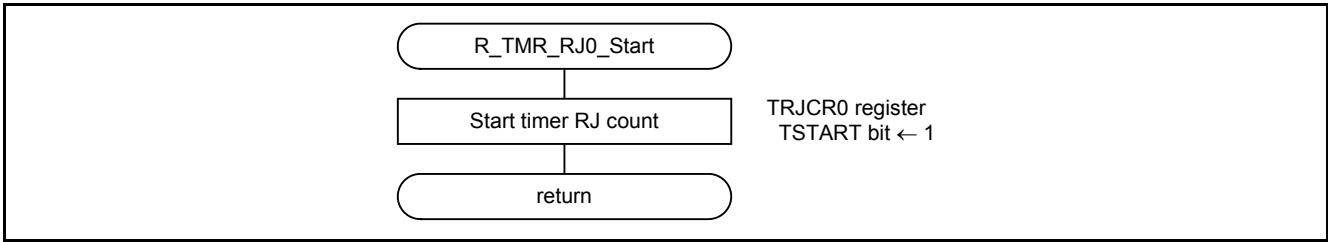


Figure 4.13 Timer RJ Count Start Setting

Start timer RJ count.

- Timer RJ Control Register 0 (TRJCR0)
Start the timer RJ count.

Symbol	7	6	5	4	3	2	1	0
TRJCR0	—	—	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
Setting Value	—	—	x	x	—	x	x	1

Bit 0

TSTART	Timer RJ count start
0	Count stops
1	Count starts

Count operation is started by writing 1 to the TSTART bit and stopped by writing 0. When the TSTART bit is set to 1 (count starts), the TCSTF bit is set to 1 (count in progress) in synchronization with the count source. Also, after 0 is written to the TSTART bit, the TCSTF bit is set to 0 (count stops) in synchronization with the count source.

Refer to the RL78/G14 user’s manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

4.7.9 Timer RG Count Start Setting

Figure 4.14 shows the Timer RG Count Start Setting.

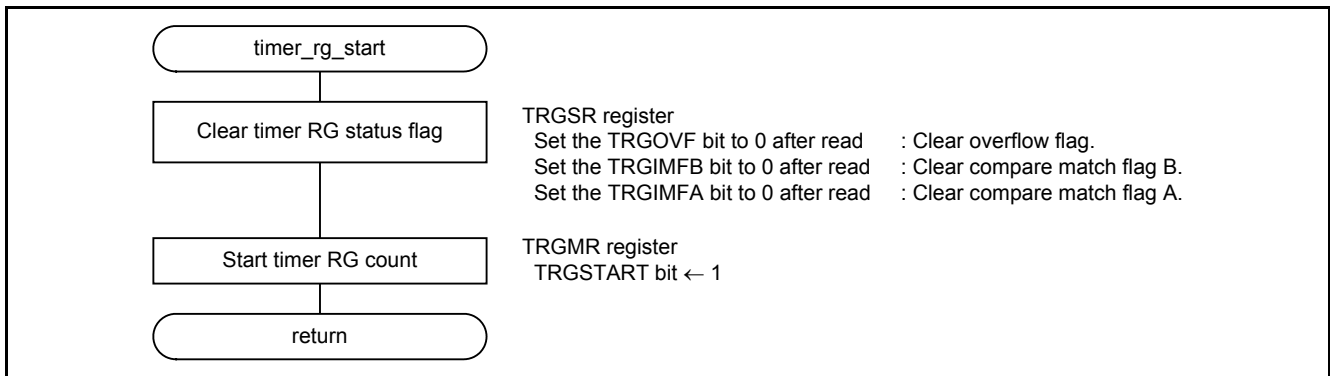


Figure 4.14 Timer RG Count Start Setting

Clear the timer RG status flag.

- Timer RG Status Register (TRGSR)

Clear the overflow flag, compare match flag B, and compare match flag A after read.

Symbol	7	6	5	4	3	2	1	0
TRGSR	—	—	—	TRGDIRF	TRGOVF	TRGUDF	TRGIMFB	TRGIMFA
Setting Value	—	—	—	x	0	x	0	0

Bit 3

TRGOVF	Overflow flag
[Condition for setting to 0] Write 0 after reading [Condition for setting to 1] See Table 4.8 Conditions for Setting Each Flag to 1	

Bit 1

TRGIMFB	Input-capture/compare-match flag B
[Condition for setting to 0] Write 0 after reading [Condition for setting to 1] See Table 4.8 Conditions for Setting Each Flag to 1	

Bit 0

TRGIMFA	Input-capture/compare-match flag A
[Condition for setting to 0] Write 0 after reading [Condition for setting to 1] See Table 4.8 Conditions for Setting Each Flag to 1	

Refer to the RL78/G14 user’s manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Table 4.8 Conditions for Setting Each Flag to 1

Bit Symbol	Timer Mode		PWM Mode
	Input capture function	Output compare function	
TRGOVF	When the TRG register overflows.		
TRGUDF	When the TRG register underflows.		
TRGIMFB	Input edge of TRGIOB pin	When the values of registers TRG and TRGGRB match.	
TRGIMFA	Input edge of TRGIOA pin	When the values of registers TRG and TRGGRA match.	

Start the timer RG count.

- Timer RG Mode Register (TRGMR)
Start the timer RG count.

Symbol	7	6	5	4	3	2	1	0
TRGMR	TRGSTART	TRGELCICE	TRGDFCK1	TRGDFCK0	TRGDFB	TRGDFA	TRGMDF	TRGPWM
Setting Value	1	x	x	x	x	x		

Bit 7

TRGSTART	TRG count start
0	Count stops, and PWM output signal (TRGIOA pin) is initialized (in PWM mode)
1	Count starts

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

4.7.10 PWM Duty Change Processing

Figure 4.15 shows the PWM Duty Change Processing.

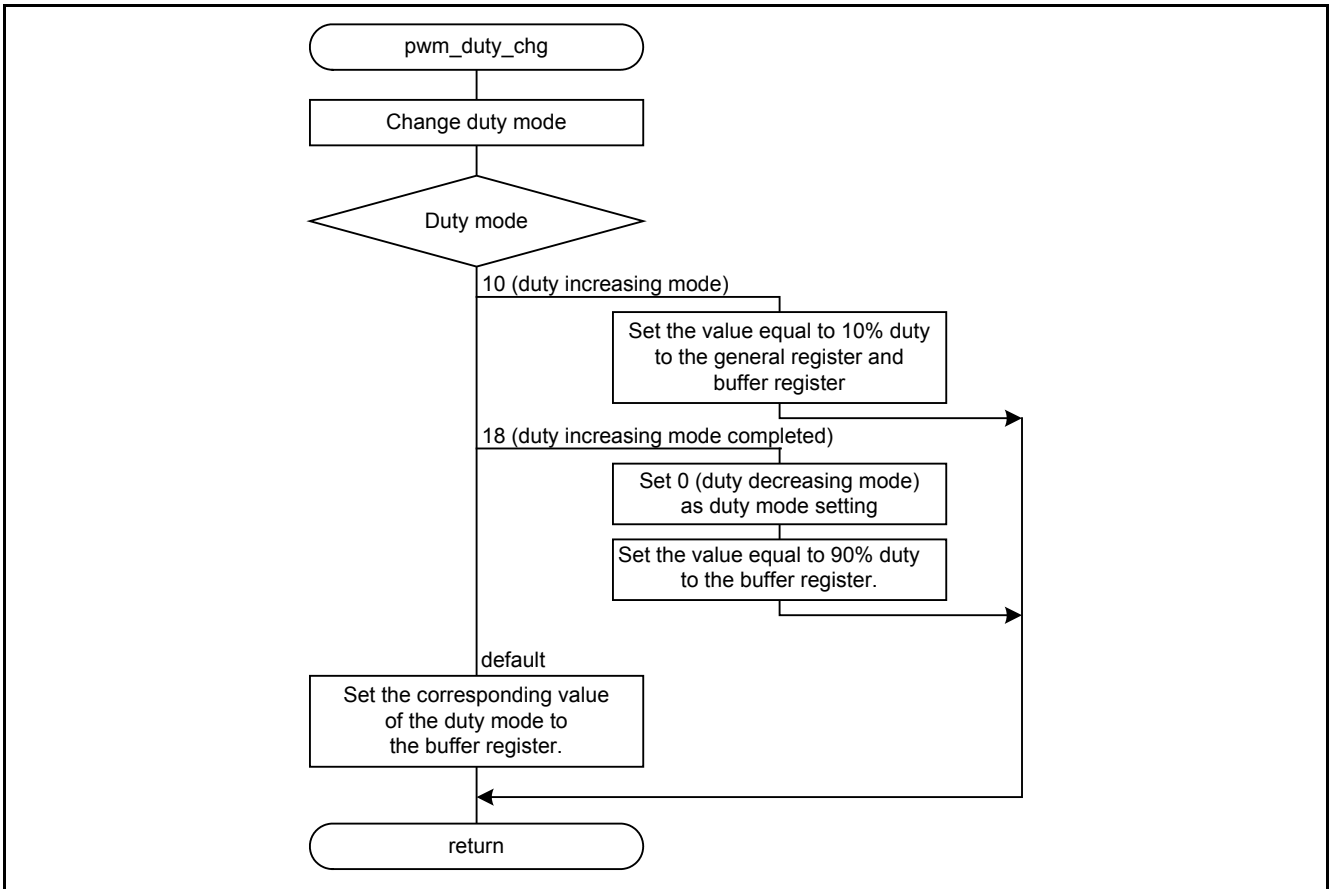


Figure 4.15 PWM Duty Change Processing

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

User's Manual: Hardware

RL78/G14 Group User's Manual: Hardware Rev.0.02

RL78 Family User's Manual: Software Rev.1.00

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

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REVISION HISTORY	RL78/G14 Timer RG Buffer Operation in PWM Mode
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Rev.	Date	Description	
		Page	Summary
1.00	Feb. 29, 2012	—	First edition issued
1.10	June 1, 2013	4	Fixed typo in Table 2.1
		5	Fixed typo in Figure 3.1

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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