# RL78/G14

## Timer RD in PWM3 Mode CC-RL

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### Abstract

This document describes a method to output a PWM waveform using timer RD of the RL78/G14 in PWM3 mode.


### Products

RL78/G14

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

## Contents

# 1. Specifications

Two PWM waveforms with 200 µs periods are output.
Table 1.1 lists the Peripheral Function and Its Application. Figure 1.1 shows the Output Timing Diagram.

**Table 1.1 Peripheral Function and Its Application**

| Peripheral Function | Application |
|---|---|
| Timer RD (timer RD0, timer RD1) | PWM waveform output |

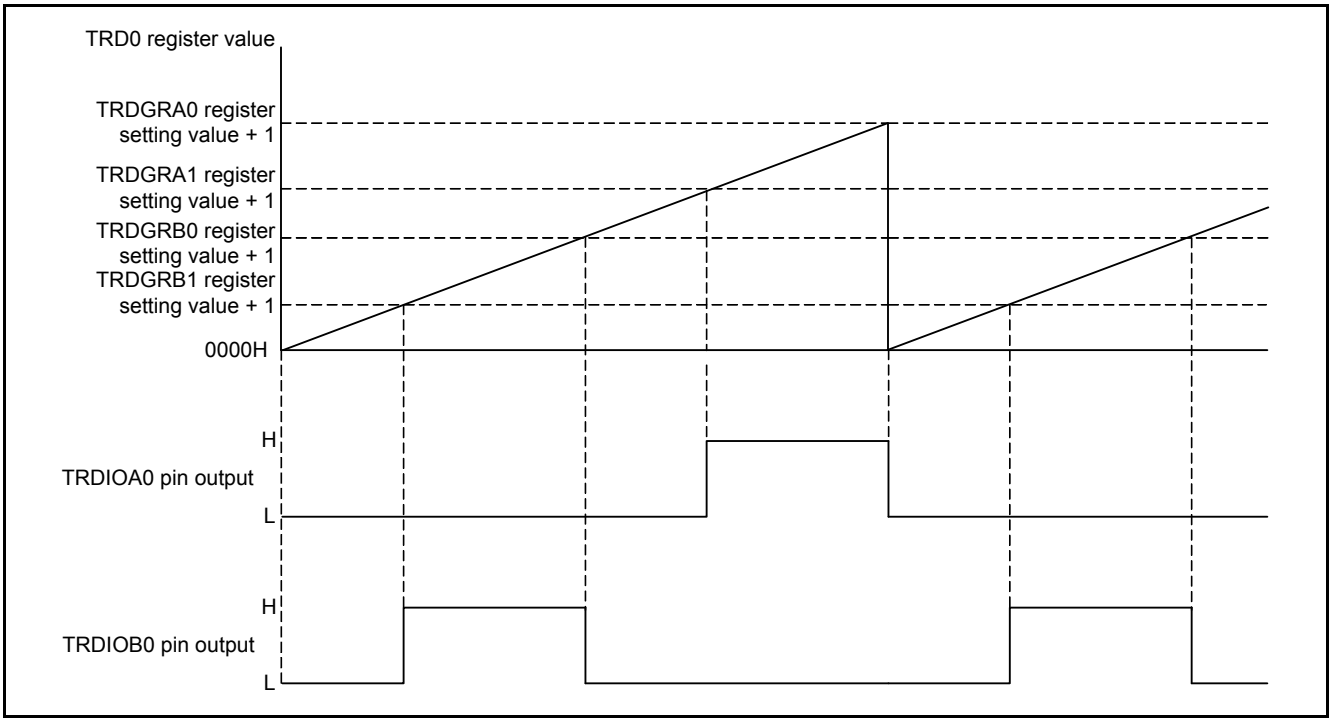



**Figure 1.1 Output Timing Diagram**

## 2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

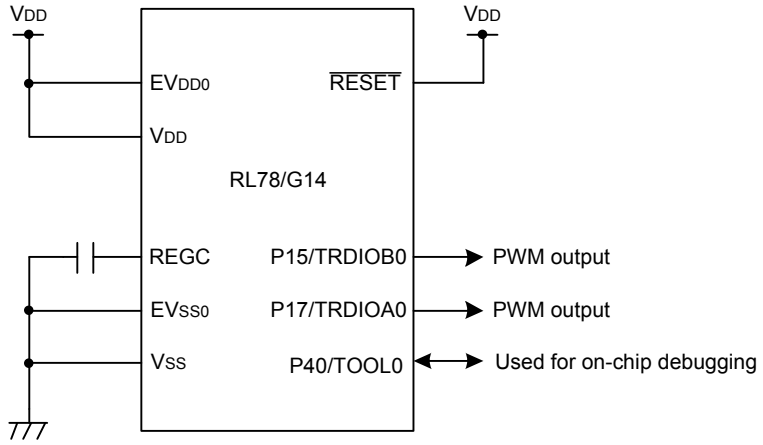
**Table 2.1 Operation Confirmation Conditions**

| Item | Contents |
|---|---|
| MCU used | RL78/G14 (R5F104LEA) |
| Operating frequencies | • High-speed on-chip oscillator clock ($f_{HOCO}$): 16 MHz (typical)<br>• CPU/peripheral hardware clock ($f_{CLK}$): 16 MHz |
| Operating voltage | 5.0 V (2.9 to 5.5 V)<br>LVD operation ($V_{LVD}$): 2.81V at the rising edge or 2.75V at the falling edge in reset mode |
| Integrated development environment (CS+) | Renesas Electronics Corporation<br>CS+ V3.01.00 |
| C compiler (CS+) | Renesas Electronics Corporation<br>CC-RL V1.01.00 |
| Integrated development environment ($e^2$ studio) | Renesas Electronics Corporation<br>$e^2$ studio V4.0.0.26 |
| C compiler ( $e^2$ studio) | Renesas Electronics Corporation<br>CC-RL V1.01.00 |

# 3. Hardware

## 3.1 Hardware Configuration

Figure 3.1 shows the Hardware Configuration used in this document.




Notes:
1. The above figure is simplified to show an overview of the hardware connection. When designing application circuits, make sure to handle unused pins appropriately to satisfy the electrical characteristics (connect input-only ports independently to either $V_{DD}$ or $V_{SS}$ via resistors).
2. Connect pins with names that begin with $EV_{SS}$ to $V_{SS}$, and pins with names that begin with $EV_{DD}$ to $V_{DD}$.
3. Make sure to set $V_{DD}$ greater than the detection voltage ($V_{LVD}$) specified by the LVD.

**Figure 3.1 Hardware Configuration**

## 3.2 Pins Used

Table 3.1 lists the Pins Used and Their Functions.

**Table 3.1 Pins Used and Their Functions**

| Pin Name | I/O | Function |
|---|---|---|
| P15/TRDIOB0 | Output | PWM output |
| P17/TRDIOA0 | Output | PWM output |

# 4. Software

## 4.1 Operation Overview

Two PWM waveforms with 200 µs periods are output using PWM3 mode.

Output signals are as follows:
- TRDIOA0 pin: Low inactive level period (140 µs) → High active level period (60 µs)
- TRDIOB0 pin: Low inactive level period (40 µs) → High active level period (60 µs) → Low inactive level period (100 µs)

The timer RD settings are shown below.

Settings:
- Use fCLK (16 MHz) as the count source.
- Clear the TRD0 register at the compare match with the TRDGRA0 register.
- Continue counting the TRD0 register after the compare match with the TRDGRA0 register.
- Use the TRDGRC1 register as the buffer register of the TRDGRA1 register.
- Use the TRDGRD1 register as the buffer register of the TRDGRB1 register.
- Use the TRDGRC0 register as the buffer register of the TRDGRA0 register.
- Use the TRDGRD0 register as the buffer register of the TRDGRB0 register.
- Enable output for pins TRDIOA0 and TRDIOB0.
- Disable output for pins TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, and TRDIOD1.
- Select TRDIOA0 and TRDIOB0 pin output levels as high active level and the initial output level as low inactive level.
- Do not use the pulse output forced cutoff input function.
- Enable the compare match interrupt for registers TRD0 and TRDGRA0.

### 4.1.1 Output Waveform

Below is a description for calculating the PWM period and PWM waveform output from each pin.

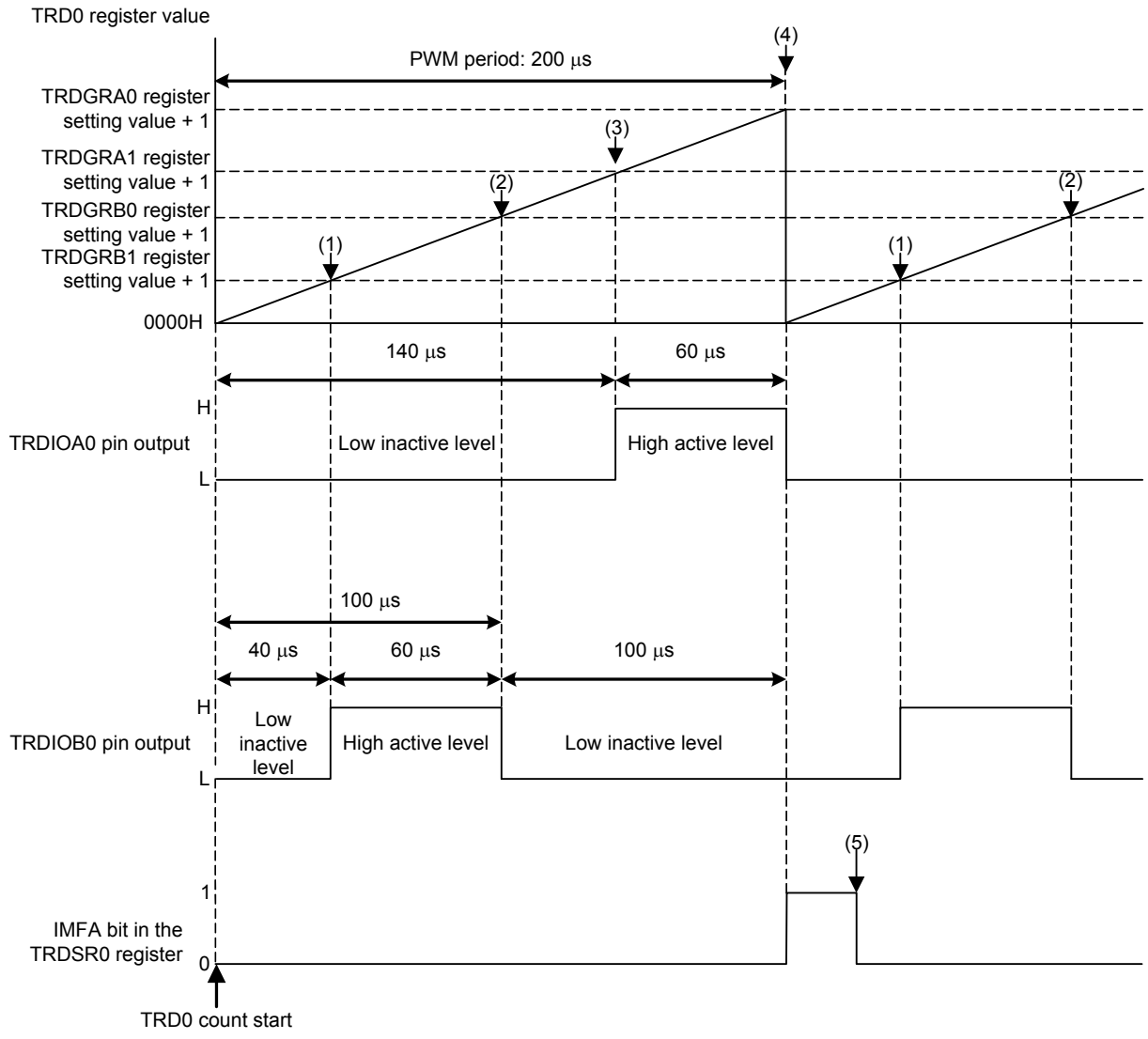
(1) PWM period

Calculate the PWM period as follows:
200 µs = 1/16 MHz × (TRDGRA0 + 1)
= 62.5 ns × 3200

(2) TRDIOA0 pin output
Calculate the high active level period and low inactive level period of the PWM waveform output from the TRDIOA0 pin as follows:
High active level period: 60 µs = 1/16 MHz × (TRDGRA0 + 1) – 1/16 MHz × (TRDGRA1 + 1)
= 62.5 ns × 3200 – 62.5 ns × 2240
Low inactive level period: 140 µs = 1/16 MHz × (TRDGRA1 + 1)
= 62.5 ns × 2240

(3) Calculate the high active level period and low inactive level period of the PWM waveform output from the TRDIOB0 pin as follows:
High active level period: 60 µs = 1/16 MHz × (TRDGRB0 + 1) – 1/16 MHz × (TRDGRB1 + 1)
= 62.5 ns × 1600 – 62.5 ns × 640
Low inactive level period (between TRD0 count start and high active level period start)
: 40 µs = 1/16 MHz × (TRDGRB1 + 1)
= 62.5 ns × 640

Figure 4.1 shows the PWM Output Waveform.




(1) Since the TRD0 register count value and the TRDGRB1 register setting value are compare matched, the TRDIOB0 pin output is changed.
(2) Since the TRD0 register count value and the TRDGRB0 register setting value are compare matched, the TRDIOB0 pin output is changed.
(3) Since the TRD0 register count value and the TRDGRA1 register setting value are compare matched, the TRDIOA0 pin output is changed.
(4) Since the TRD0 register count value and the TRDGRA0 register setting value are compare matched, the TRD0 register is cleared and an INTTRD0 interrupt is generated.
(5) Clear compare match flag A (IMFA bit) in timer RD status register 0 (TRDSR0 register) in the INTTRD0 interrupt service routine by a program.

**Figure 4.1 PWM Output Waveform**

## 4.2 Option-Setting Memory

Table 4.1 lists the Option-Setting Memory Configured in the Sample Code. When necessary, set a value suited to the user system.

**Table 4.1 Option-Setting Memory Configured in the Sample Code**

| Address | Setting Value | Contents |
|---|---|---|
| 000C0H/010C0H | 11101111B | Watchdog timer operation is stopped (count is stopped after reset) |
| 000C1H/010C1H | 01111111B | LVD reset mode<br>Detection voltage: Rising edge 2.81 V/falling edge 2.75 V |
| 000C2H/010C2H | 11101001B | Internal high-speed oscillation HS mode: 16 MHz |
| 000C3H/010C3H | 10000100B | On-chip debugging enabled |

## 4.3 Functions

Table 4.2 lists the Functions.

**Table 4.2 Functions**

| Function Name | Outline |
|---|---|
| hdwinit | Initial setting |
| R_Systeminit | Initial setting of peripheral functions |
| R_CGC_Create | Initial setting of the CPU |
| R_TMR_RD0_Create | Initial setting of timer RD |
| main | Main processing |
| R_TMR_RD0_Start | Timer RD count start setting |
| r_tmr_rd0_interrupt | Timer RD0 interrupt |

## 4.4 Function Specifications

The following tables list the sample code function specifications.

| hdwinit | |
|---|---|
| **Outline** | Initial setting |
| **Header** | None |
| **Declaration** | void hdwinit(void) |
| **Description** | Perform the initial setting of peripheral functions. |
| **Argument** | None |
| **Return Value** | None |

| R_Systeminit | |
|---|---|
| **Outline** | Initial setting of peripheral functions |
| **Header** | None |
| **Declaration** | void R_Systeminit(void) |
| **Description** | Perform the initial setting of peripheral functions used in this document. |
| **Argument** | None |
| **Return Value** | None |

| R_CGC_Create | |
|---|---|
| **Outline** | Initial setting of the CPU |
| **Header** | None |
| **Declaration** | void R_CGC_Create(void) |
| **Description** | Perform the initial setting of the CPU. |
| **Argument** | None |
| **Return Value** | None |

| R_TMR_RD0_Create | |
|---|---|
| **Outline** | Initial setting of timer RD |
| **Header** | None |
| **Declaration** | void R_TMR_RD0_Create(void) |
| **Description** | Perform the initial setting to use PWM3 mode of timer RD. |
| **Argument** | None |
| **Return Value** | None |

| main | |
|---|---|
| **Outline** | Main processing |
| **Header** | None |
| **Declaration** | void main(void) |
| **Description** | Perform main processing. |
| **Argument** | None |
| **Return Value** | None |

| R_TMR_RD0_Start | |
|---|---|
| **Outline** | Timer RD count start setting |
| **Header** | None |
| **Declaration** | void R_TMR_RD0_Start(void) |
| **Description** | Perform timer RD count start setting. |
| **Argument** | None |
| **Return Value** | None |

| r_tmr_rd0_interrupt | |
|---|---|
| **Outline** | Timer RD0 interrupt |
| **Header** | None |
| **Declaration** | void r_tmr_rd0_interrupt(void) |
| **Description** | • Perform timer RD0 interrupt service routine.<br>• Clear compare match flag A. |
| **Argument** | None |
| **Return Value** | None |

## 4.5 Flowcharts

### 4.5.1 Overall Flowchart

Figure 4.2 shows the Overall Flowchart.

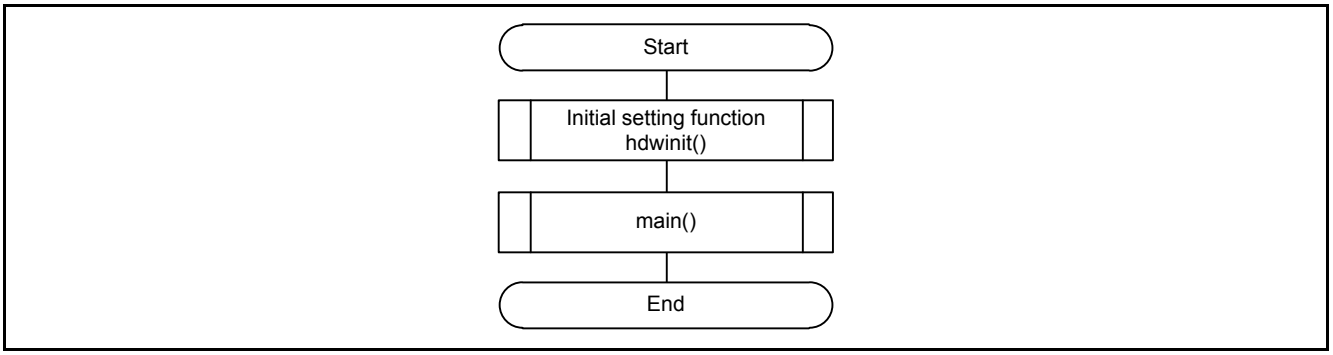



**Figure 4.2 Overall Flowchart**

### 4.5.2 Initial Setting

Figure 4.3 shows the Initial Setting.

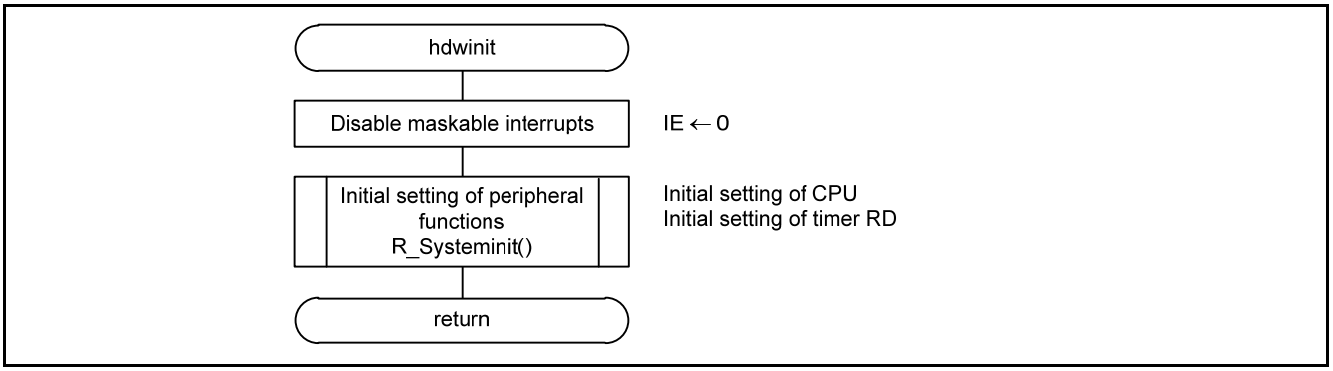



**Figure 4.3 Initial Setting**

### 4.5.3 Initial Setting of Peripheral Functions

Figure 4.4 shows the Initial Setting of Peripheral Functions.

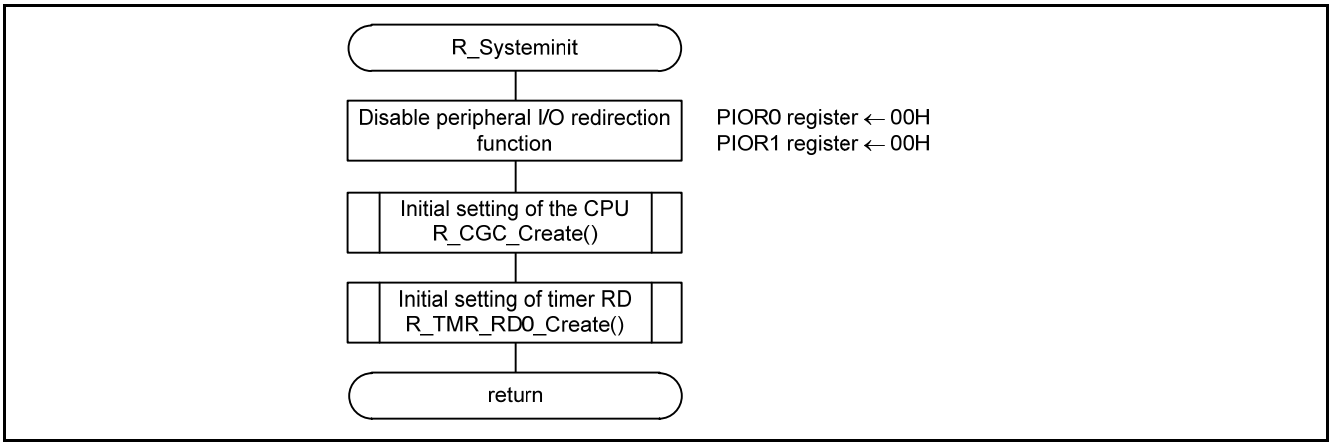



**Figure 4.4 Initial Setting of Peripheral Functions**

### 4.5.4 Initial Setting of the CPU

Figure 4.5 shows the Initial Setting of the CPU.

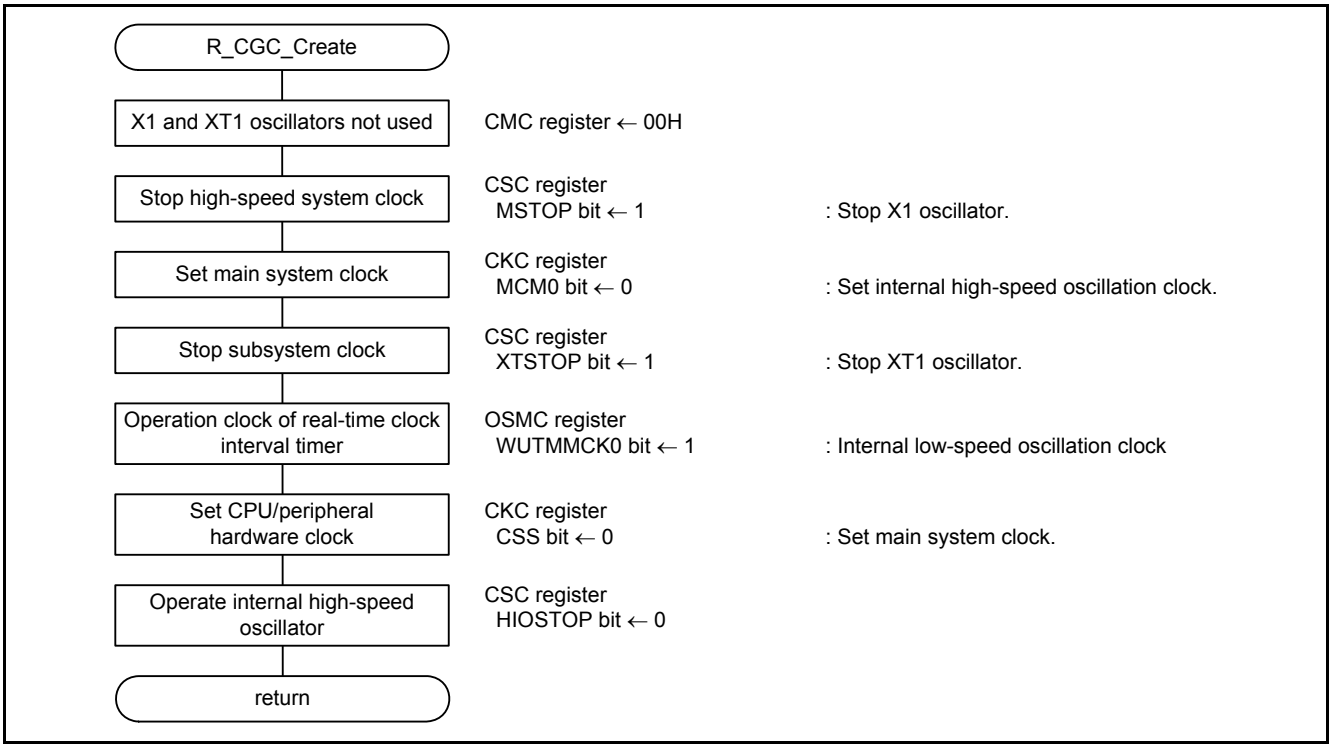



**Figure 4.5 Initial Setting of the CPU**

### 4.5.5 Initial Setting of Timer RD

Figure 4.6 and Figure 4.7 show the Initial Setting of Timer RD.

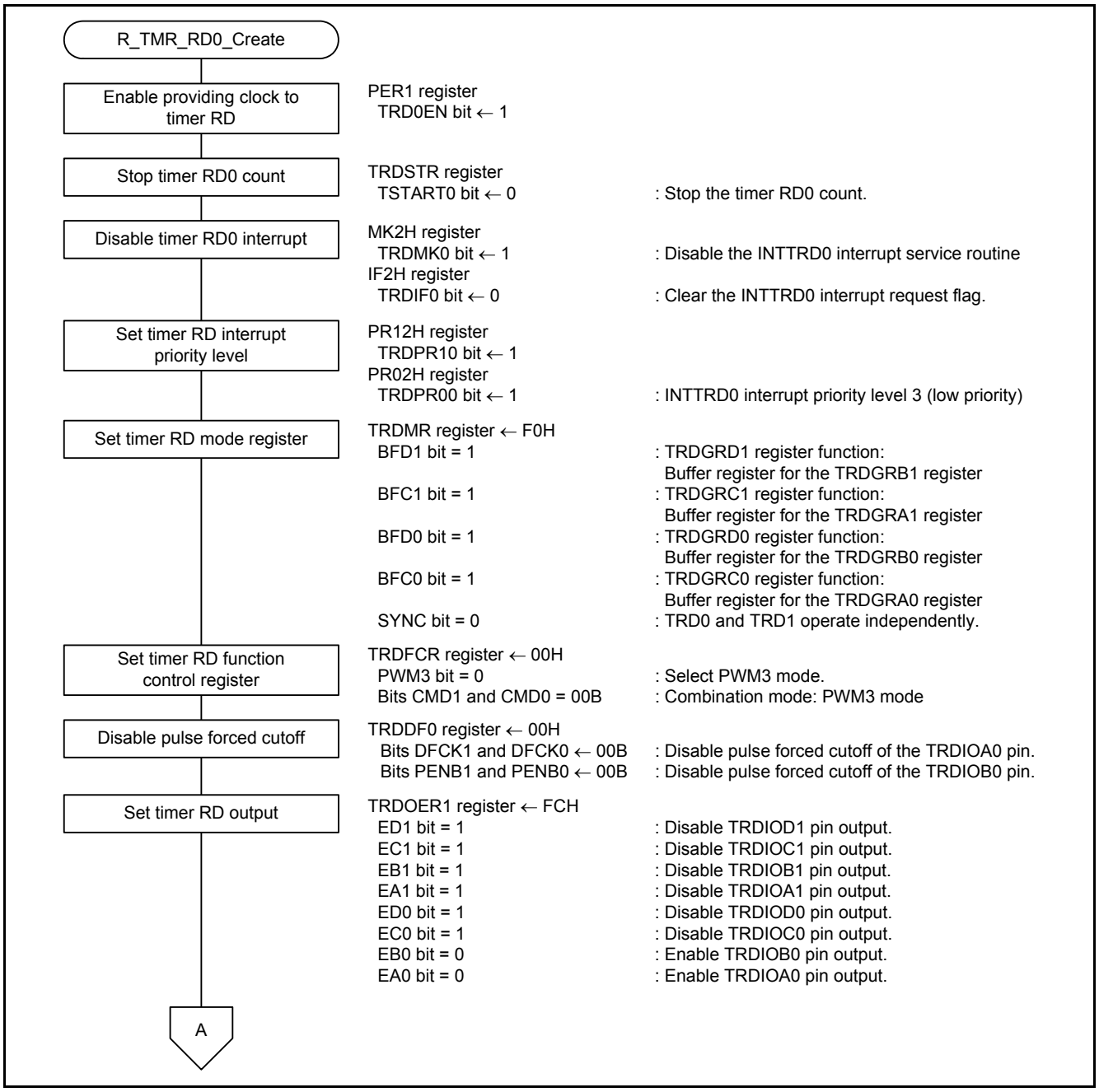



**Figure 4.6 Initial Setting of Timer RD (1/2)**

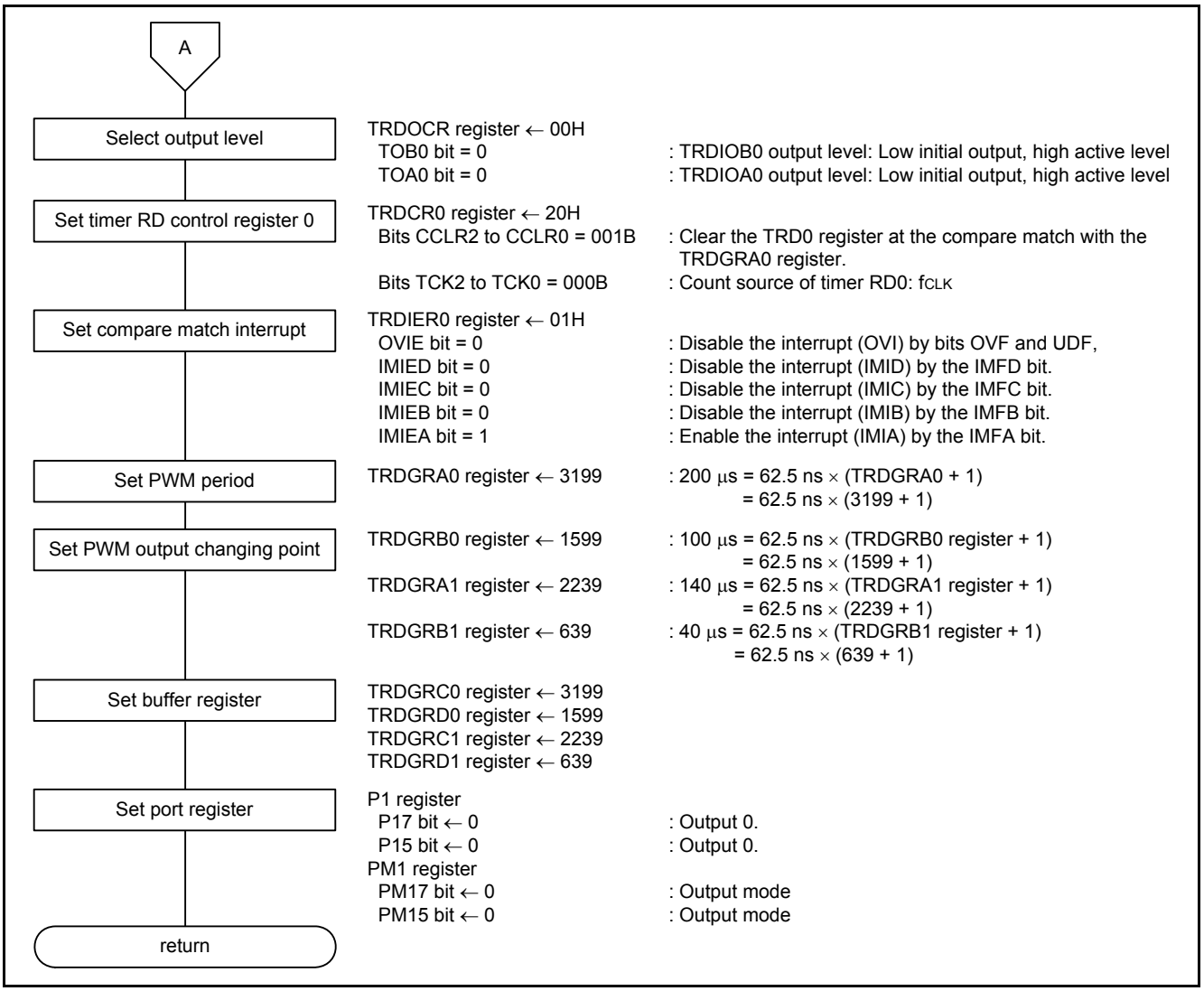



**Figure 4.7 Initial Setting of Timer RD (2/2)**

Enable providing a clock to timer RD.

- Peripheral Enable Register 1 (PER1)
  Enable providing a clock to timer RD.

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PER1 | DACEN | TRGEN | CMPEN | TRD0EN | DTCEN | 0 | 0 | TRJ0EN |
| Setting Value | x | x | x | 1 | x | — | — | x |

Bit 4

| TRD0EN | Control of timer RD input clock supply |
|---|---|
| 0 | Stops input clock supply.<br>• SFR used by timer RD cannot be written.<br>• Timer RD is in the reset status. |
| 1 | Enables input clock supply.<br>• SFR used by timer RD can be read and written. |

Stop the timer RD0 count.

- Timer RD Mode Register (TRDSTR)
  Stop the timer RD0 count.

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TRDSTR | — | — | — | — | CSEL1 | CSEL0 | TSTART1 | TSTART0 |
| Setting Value | — | — | — | — | x | | x | 0 |

Bit 2

| CSEL0 | TRD0 count operation select |
|---|---|
| 0 | Count stops at compare match with TRDGRA0 register |
| 1 | Count continues after compare match with TRDGRA0 register |

Bit 0

| TSTART0 | TRD0 count start flag |
|---|---|
| 0 | Count stops |
| 1 | Count starts |

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Disable the timer RD0 interrupt.

- Interrupt Mask Flag Register (MK2H)
  Disable the INTTRD0 interrupt.

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| MK2H | FLMK | IICAMK1 | 1 | SREMK3<br>TMMK13H | TRGMK | TRDMK1 | TRDMK0 | PMK11<br>CMPMK1 |
| Setting Value | x | x | — | x | x | x | 1 | x |

Bit 1

| TRDMK0 | Interrupt servicing control |
|---|---|
| 0 | Interrupt servicing enabled |
| 1 | Interrupt servicing disabled |

- Interrupt Request Flag Register (IF2H)
  Clear the INTTRD0 interrupt request flag.

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| IF2H | FLIF | IICAIF1 | 0 | SREIF3<br>TMIF13H | TRGIF | TRDIF1 | TRDIF0 | PIF11<br>CMPIF1 |
| Setting Value | x | x | — | x | x | x | 0 | x |

Bit 1

| TRDIF0 | Interrupt request flag |
|---|---|
| 0 | No interrupt request signal is generated |
| 1 | Interrupt request is generated, interrupt request status |

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the timer RD interrupt priority level.

- Priority Specification Flag Registers (PR02H and PR12H)
  Set to level 3 (low priority).

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PR02H | FLPR0 | IICAPR01 | 1 | SREPR03<br>TMPR013H | TRGPR0 | TRDPR01 | TRDPR00 | PPR011<br>CMPPR01 |
| Setting Value | x | x | — | x | x | x | 1 | x |

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PR12H | FLPR1 | IICAPR11 | 1 | SREPR13<br>TMPR113H | TRGPR1 | TRDPR11 | TRDPR10 | PPR111<br>CMPPR11 |
| Setting Value | x | x | — | x | x | x | 1 | x |

| TRDPR10 | TRDPR00 | Priority level selection |
|---|---|---|
| 0 | 0 | Specify level 0 (high priority level). |
| 0 | 1 | Specify level 1 |
| 1 | 0 | Specify level 2 |
| 1 | 1 | Specify level 3 (low priority level) |

Set the timer RD mode register.

- Timer RD Mode Register (TRDMR)
  Use registers TRDGRC0, TRDGRD0, TRDGRC1, and TRDGRD1 as the buffer registers.

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TRDMR | BFD1 | BFC1 | BFD0 | BFC0 | — | — | — | SYNC |
| Setting Value | 1 | 1 | 1 | 1 | — | — | — | 0 |

Bit 7

| BFD1 | TRDGRD1 register function select |
|---|---|
| 0 | General register |
| 1 | Buffer register for TRDGRB1 register |

Bit 6

| BFC1 | TRDGRC1 register function select |
|---|---|
| 0 | General register |
| 1 | Buffer register for TRDGRA1 register |

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Bit 5

| BFD0 | TRDGRD0 register function select |
|---|---|
| 0 | General register |
| 1 | Buffer register for TRDGRB0 register |

Bit 4

| BFC0 | TRDGRC0 register function select |
|---|---|
| 0 | General register |
| 1 | Buffer register for TRDGRA0 register |

Bit 0

| SYNC | Timer RD synchronous |
|---|---|
| 0 | TRD0 and TRD1 operate independently |
| 1 | TRD0 and TRD1 operate synchronously |

Set to 0 in PWM3 mode.

Set the timer RD function control register.

- Timer RD Function Control Register (TRDFCR)

Set PWM3 mode. Set PWM3 mode as a combination mode.

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TRDFCR | PWM3 | STCLK | 0 | 0 | OLS1 | OLS0 | CMD1 | CMD0 |
| Setting Value | 0 | x | — | — | x | x | 0 | 0 |

Bit 7

| PWM3 | PWM3 mode select |
|---|---|
| • In the timer mode, set to 1 (other than PWM3 mode).<br>• In PWM3 mode, set to 0 (PWM3 mode).<br>• Disabled in reset synchronous and complementary PWM modes. | |

Bits 1 and 0

| CMD1 | CMD0 | Combination mode select |
|---|---|---|
| • In timer and PWM3 modes, set to 00B (timer mode or PWM3 mode).<br>• In reset synchronous PWM mode, set to 01B (reset synchronous PWM mode).<br>• In complementary PWM mode,<br>CMD1 CMD0<br>1 0: Complementary PWM mode (transfer from the buffer register to the general register when TRD1 underflows)<br>1 1: Complementary PWM mode (transfer from the buffer register to the general register at compare match between registers TRD0 and TRDGRA0)<br>Other than the above: Do not set. | | |

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Disable pulse forced cut-off.

- Timer RD Digital Filter Function Select Register 0 (TRDDF0)
  Disable pulse forced cut-off of pins TRDIOA0 and TRDIOB0.

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TRDDF0 | DFCK1 | DFCK0 | PENB1 | PENB0 | DFD | DFC | DFB | DFA |
| Setting Value | 0 | 0 | 0 | 0 | x | x | x | x |

Bits 7 and 6

| DFCK1 | DFCK0 | TRDIOA0 pin pulse forced cutoff control |
|---|---|---|
| 0 | 0 | Forced cutoff disabled |
| 0 | 1 | High-impedance output |
| 1 | 0 | Low output |
| 1 | 1 | High output |
| Set these bits to 00B (forced cutoff disabled) if the corresponding pin is not used as a timer RD output port in these modes. Also, set these bits while the count is stopped. | | |

Bits 5 and 4

| PENB1 | PENB0 | TRDIOB0 pin pulse forced cutoff control |
|---|---|---|
| 0 | 0 | Forced cutoff disabled |
| 0 | 1 | High-impedance output |
| 1 | 0 | Low output |
| 1 | 1 | High output |
| Set these bits to 00B (forced cutoff disabled) if the corresponding pin is not used as a timer RD output port in these modes. Also, set these bits while the count is stopped. | | |

Set timer RD output.

- Timer RD Output Master Enable Register 1 (TRDOER1)
  Enable output of pins TRDIOA0 and TRDIOB0, and disable output of pins TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, and TRDIOD1.

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TRDOER1 | ED1 | EC1 | EB1 | EA1 | ED0 | EC0 | EB0 | EA0 |
| Setting Value | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |

Bit 7

| ED1 | TRDIOD1 output disable |
|---|---|
| 0 | Output enabled |
| 1 | Output disabled (TRDIOD1 pin functions as an I/O port.) |

Set to 1 in PWM3 mode.

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Bit 6

| EC1 | TRDIOC1 output disable |
|---|---|
| 0 | Output enabled |
| 1 | Output disabled (TRDIOC1 pin functions as an I/O port.) |

Set to 1 in PWM3 mode.

Bit 5

| EB1 | TRDIOB1 output disable |
|---|---|
| 0 | Output enabled |
| 1 | Output disabled (TRDIOB1 pin functions as an I/O port.) |

Set to 1 in PWM3 mode.

Bit 4

| EA1 | TRDIOA1 output disable |
|---|---|
| 0 | Output enabled |
| 1 | Output disabled (TRDIOA1 pin functions as an I/O port.) |

Set to 1 in PWM3 mode.

Bit 3

| ED0 | TRDIOD0 output disable |
|---|---|
| 0 | Output enabled |
| 1 | Output disabled (TRDIOD0 pin functions as an I/O port.) |

Set to 1 in PWM3 mode.

Bit 2

| EC0 | TRDIOC0 output disable |
|---|---|
| 0 | Output enabled |
| 1 | Output disabled (TRDIOC0 pin functions as an I/O port.) |

Set to 1 in PWM3 mode.

Bit 1

| EB0 | TRDIOB0 output disable |
|---|---|
| 0 | Output enabled |
| 1 | Output disabled (TRDIOB0 pin functions as an I/O port.) |

Bit 0

| EA0 | TRDIOA0 output disable |
|---|---|
| 0 | Output enabled |
| 1 | Output disabled (TRDIOA0 pin functions as an I/O port.) |

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Select output levels.

- Timer RD Output Control Register (TRDOCR)
  Set low for initial output of pins TRDIOA0 and TRDIOB0, and high for the active level.

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TRDOCR | TOD1 | TOC1 | TOB1 | TOA1 | TOD0 | TOC0 | TOB0 | TOA0 |
| Setting Value | x | x | x | x | x | x | 0 | 0 |

Bit 1

| TOB0 | TRDIOB0 initial output level select |
|---|---|
| 0 | Low initial output, high active level, high output at TRDGRB1 compare match, and low output at TRDGRB0 compare match |
| 1 | High initial output, low active level, low output at TRDGRB1 compare match, and high output at TRDGRB0 compare match |

Bit 0

| TOA0 | TRDIOA0 initial output level select |
|---|---|
| 0 | Low initial output, high active level, high output at TRDGRA1 compare match, and low output at TRDGRA0 compare match |
| 1 | High initial output, low active level, low output at TRDGRA1 compare match, and high output at TRDGRA0 compare match |

Set timer RD control register 0.

- Timer RD Control Register 0 (TRDCR0)
  Set the timing to clear the TRD0 register at the compare match with the TRDGRA0 register. Set $f_{CLK}$ to the count source of timer RD0.

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TRDCR0 | CCLR2 | CCLR1 | CCLR0 | CKEG1 | CKEG0 | TCK2 | TCK1 | TCK0 |
| Setting Value | 0 | 0 | 1 | x | x | 0 | 0 | 0 |

Bits 7 to 5

| CCLR2 | CCLR1 | CCLR0 | TRD0 counter clear select |
|---|---|---|---|
| Set to 001B (TRD0 register is cleared at compare match with TRDGRA0 register). | | | |

Bits 2 to 0

| TCK2 | TCK1 | TCK0 | Count source select |
|---|---|---|---|
| 0 | 0 | 0 | $f_{CLK}$, $f_{HOCO}$ |
| 0 | 0 | 1 | $f_{CLK}/2$ |
| 0 | 1 | 0 | $f_{CLK}/4$ |
| 0 | 1 | 1 | $f_{CLK}/8$ |
| 1 | 0 | 0 | $f_{CLK}/32$ |
| 1 | 0 | 1 | Do not set. |
| 1 | 1 | 0 | Do not set. |
| 1 | 1 | 1 | Do not set. |

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the compare match interrupt.

- Timer RD Interrupt Enable Register 0 (TRDIER0)
  Set the IMFA bit to enable the interrupt (IMIA).

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TRDIER0 | — | — | — | OVIE | IMIED | IMIEC | IMIEB | IMIEA |
| Setting Value | — | — | — | 0 | 0 | 0 | 0 | 1 |

Bit 4

| OVIE | Overflow/underflow interrupt enable |
|---|---|
| 0 | Interrupt (OVI) by bits OVF and UDF disabled |
| 1 | Interrupt (OVI) by bits OVF and UDF enabled |

Bit 3

| IMIED | Input capture/compare match interrupt enable D |
|---|---|
| 0 | Interrupt (IMID) by the IMFD bit is disabled |
| 1 | Interrupt (IMID) by the IMFD bit is enabled |

Bit 2

| IMIEC | Input capture/compare match interrupt enable C |
|---|---|
| 0 | Interrupt (IMIC) by the IMFC bit is disabled |
| 1 | Interrupt (IMIC) by the IMFC bit is enabled |

Bit 1

| IMIEB | Input capture/compare match interrupt enable B |
|---|---|
| 0 | Interrupt (IMIB) by the IMFB bit is disabled |
| 1 | Interrupt (IMIB) by the IMFB bit is enabled |

Bit 0

| IMIEA | Input capture/compare match interrupt enable A |
|---|---|
| 0 | Interrupt (IMIA) by the IMFA bit is disabled |
| 1 | Interrupt (IMIA) by the IMFA bit is enabled |

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the PWM period.

- Timer RD General Register A0 (TRDGRA0)
  Set the PWM period to 200 µs.

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRDGRA0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Setting Value | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| — | Function | Setting Range |
|---|---|---|
| Bits 15 to 0 | See Table 4.3 TRDGRA0 register function in PWM3 mode. | 0000H to FFFFH |

Set the PWM output changing point.

- Timer RD General Register B0 (TRDGRB0)
  Set this register after 100 µs from the count start to change the output of the TRDIOB0 pin.

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRDGRB0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Setting Value | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

| — | Function | Setting Range |
|---|---|---|
| Bits 15 to 0 | See Table 4.3 TRDGRB0 register function in PWM3 mode. | 0000H to FFFFH |

- Timer RD General Register A1 (TRDGRA1)
  Set this register after 140 µs from the count start to change the output of the TRDIOA0 pin.

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRDGRA1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Setting Value | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

| — | Function | Setting Range |
|---|---|---|
| Bits 15 to 0 | See Table 4.3 TRDGRA1 register function in PWM3 mode. | 0000H to FFFFH |

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

- Timer RD General Register B1 (TRDGRB1)
  Set this register after 40 μs from the count start to change the output of the TRDIOB0 pin.

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRDGRB1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Setting Value | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| — | Function | Setting Range |
|---|---|---|
| Bits 15 to 0 | See Table 4.3 TRDGRB1 register function in PWM3 mode. | 0000H to FFFFH |

## Set the buffer register

- Timer RD General Register C0 (TRDGRC0)
  Set C7FH to the buffer register (TRDGRC0) of the TRDGRA0 register.

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRDGRC0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Setting Value | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| — | Function | Setting Range |
|---|---|---|
| Bits 15 to 0 | See Table 4.3 TRDGRC0 register function in PWM3 mode. | 0000H to FFFFH |

- Timer RD General Register D0 (TRDGRD0)
  Set 63FH to the buffer register (TRDGRD0) of the TRDGRB0 register.

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRDGRD0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Setting Value | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

| — | Function | Setting Range |
|---|---|---|
| Bits 15 to 0 | See Table 4.3 TRDGRD0 register function in PWM3 mode. | 0000H to FFFFH |

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

• Timer RD General Register C1 (TRDGRC1)
Set 8BFH to the buffer register (TRDGRC1) of the TRDGRA1 register.

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRDGRC1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Setting Value | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

| — | Function | Setting Range |
|---|---|---|
| Bits 15 to 0 | See Table 4.3 TRDGRC1 register function in PWM3 mode. | 0000H to FFFFH |

• Timer RD General Register D1 (TRDGRD1)
Set 27FH to the buffer register (TRDGRD1) of the TRDGRB1 register.

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRDGRD1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Setting Value | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| — | Function | Setting Range |
|---|---|---|
| Bits 15 to 0 | See Table 4.3 TRDGRD1 register function in PWM3 mode. | 0000H to FFFFH |

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

**Table 4.3 General Register Functions in PWM3 Mode**

| Register | Setting | Register Function | PWM Output Pin |
|---|---|---|---|
| TRDGRA0 | — | General register. Set the PWM period.<br>Setting range: ≥ Value set in TRDGRA1 register | TRDIOA0 |
| TRDGRA1 | | General register. Set the changing point (active level timing) of PWM output<br>Setting range: ≤ Value set in TRDGRA0 register | |
| TRDGRB0 | | General register. Set the changing point (the timing for returning to initial output level) of PWM output.<br>Setting range: ≥ Value set in TRDGRB1 register and ≤ Value set in TRDGRA0 register | TRDIOB0 |
| TRDGRB1 | | General register. Set the changing point (active level timing) of PWM output<br>Setting range: ≤ Value set in TRDGRB0 register | |
| TRDGRC0 | BFC0 = 0 | (Not used in PWM3 mode.) | — |
| TRDGRC1 | BFC1 = 0 | | |
| TRDGRD0 | BFD0 = 0 | | |
| TRDGRD1 | BFD1 = 0 | | |
| TRDGRC0 | BFC0 = 1 | Buffer register. Set the next PWM period<br>Setting range: ≥ Value set in TRDGRC1 register | TRDIOA0 |
| TRDGRC1 | BFC1 = 1 | Buffer register. Set the changing point of next PWM output<br>Setting range: ≤ Value set in TRDGRC0 register | |
| TRDGRD0 | BFD0 = 1 | Buffer register. Set the changing point of next PWM output<br>Setting range: ≥ Value set in TRDGRD1 register and ≤ Value set in TRDGRC0 register | TRDIOB0 |
| TRDGRD1 | BFD1 = 1 | Buffer register. Set the changing point of next PWM output<br>Setting range: ≤ Value set in TRDGRD0 register | |

Set the port registers.

- Port Register 1 (P1)
  Set port register 1.

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| P1 | P17 | P16 | P15 | P14 | P13 | P12 | P11 | P10 |
| Setting Value | 0 | x | 0 | x | x | x | x | x |

Bit 7

| P17 | Output data control |
|---|---|
| 0 | Output 0 |
| 1 | Output 1 |

Bit 5

| P15 | Output data control |
|---|---|
| 0 | Output 0 |
| 1 | Output 1 |

- Port Mode Register 1 (PM1)
  Set pins P17 and P15 to output mode.

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PM1 | PM17 | PM16 | PM15 | PM14 | PM13 | PM12 | PM11 | PM10 |
| Setting Value | 0 | x | 0 | x | x | x | x | x |

Bit 7

| PM17 | P17 pin I/O mode selection |
|---|---|
| 0 | Output mode (output buffer on) |
| 1 | Input mode (output buffer off) |

Bit 5

| PM15 | P15 pin I/O mode selection |
|---|---|
| 0 | Output mode (output buffer on) |
| 1 | Input mode (output buffer off) |

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

### 4.5.6 Main Processing

Figure 4.8 shows the Main Processing.

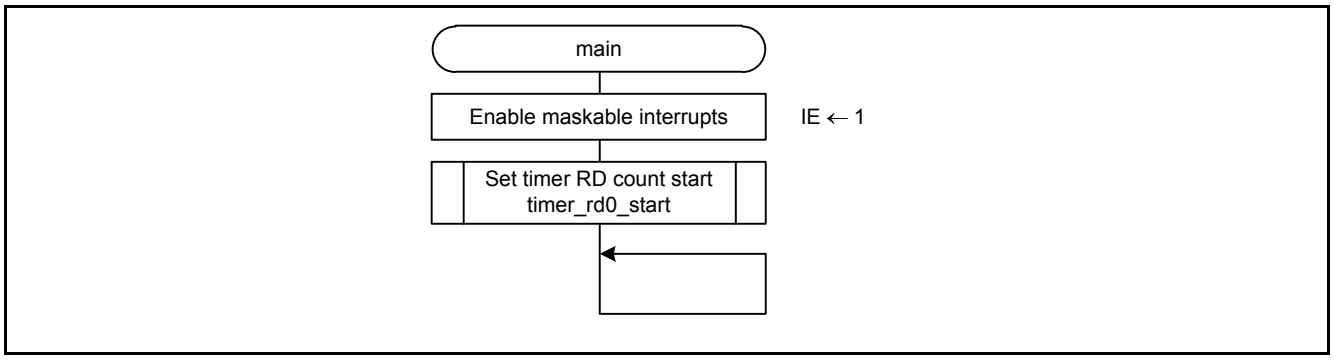



**Figure 4.8 Main Processing**

### 4.5.7 Timer RD Count Start Setting

Figure 4.9 shows the Timer RD Count Start Setting.

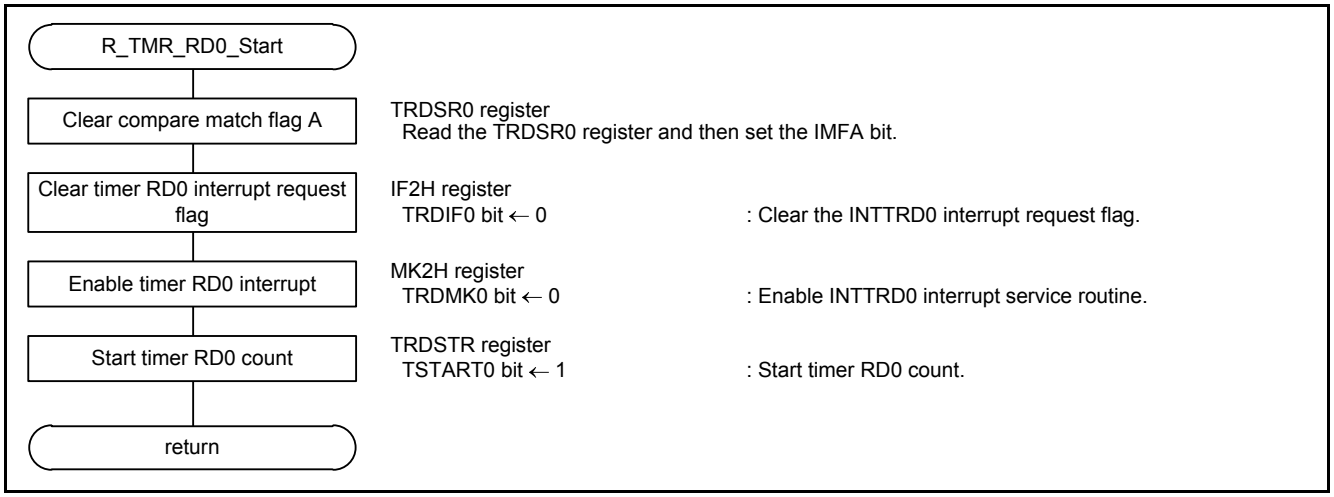



**Figure 4.9 Timer RD Count Start Setting**

Clear compare match flag A.

- Timer RD Status Register 0 (TRDSR0)
  Clear compare match flag A after reading timer RD status register 0.

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TRDSR0 | — | — | — | OVF | IMFD | IMFC | IMFB | IMFA |
| Setting Value | — | — | — | x | x | x | x | 0 |

Bit 0

| IMFA | Input capture/compare match flag A |
|---|---|
| [Source for setting to 0]<br>Write 0 after reading.<br>[Source for setting to 1]<br>When the values of TRD0 and TRDGRA0 match. | |

Clear the timer RD0 interrupt request flag.

- Interrupt Request Flag Register (IF2H)
  Clear the INTTRD0 interrupt request flag.

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| IF2H | FLIF | IICAIF1 | 0 | SREIF3<br>TMIF13H | TRGIF | TRDIF1 | TRDIF0 | PIF11<br>CMPIF1 |
| Setting Value | x | x | — | x | x | x | 0 | x |

Bit 1

| TRDIF0 | Interrupt request flag |
|---|---|
| 0 | No interrupt request signal is generated |
| 1 | Interrupt request is generated, interrupt request status |

Enable the timer RD0 interrupt.

- Interrupt Mask Flag Register (MK2H)
  Enable the INTTRD0 interrupt.

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| MK2H | FLMK | IICAMK1 | 1 | SREMK3<br>TMMK13H | TRGMK | TRDMK1 | TRDMK0 | PMK11<br>CMPMK1 |
| Setting Value | x | x | — | x | x | x | 0 | x |

Bit 1

| TRDMK0 | Interrupt servicing control |
|---|---|
| 0 | Interrupt servicing enabled |
| 1 | Interrupt servicing disabled |

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Start the timer RD0 count.

- Timer RD Mode Register (TRDSTR)
  Start the timer RD0 count.

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TRDSTR | — | — | — | — | CSEL1 | CSEL0 | TSTART1 | TSTART0 |
| Setting Value | — | — | — | — | x | | x | 1 |

Bit 0

| TSTART0 | TRD0 count start flag |
|---|---|
| 0 | Count stops |
| 1 | Count starts |

### 4.5.8 Timer RD0 Interrupt

Figure 4.10 shows the Timer RD0 Interrupt.

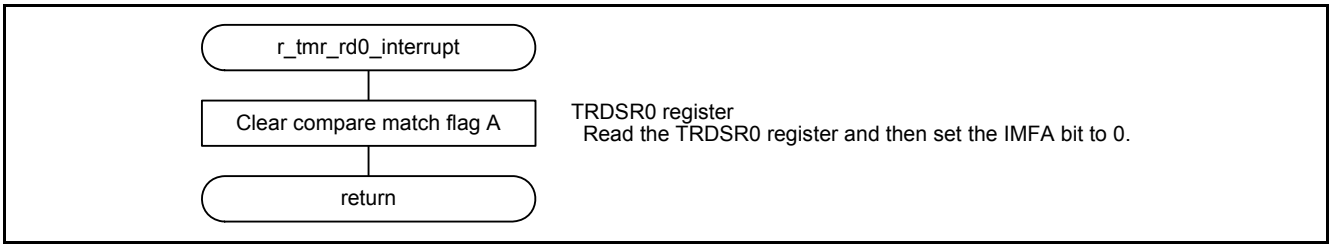



**Figure 4.10 Timer RD0 Interrupt**

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

## 5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

## 6. Reference Documents

User's Manual: Hardware
RL78/G14 Group User's Manual: Hardware Rev.0.02
RL78 Family User's Manual: Software Rev.1.00
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
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| REVISION HISTORY | RL78/G14 Timer RD in PWM3 Mode |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Apr. 16, 2015 | — | First edition issued |

## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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