RL78/G14

Setting the Window Comparator

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Abstract

This document describes a method to operate the window comparator using the RL78/G14 comparator.

Products

RL78/G14

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

Operate the window comparator using the comparator. When the following conditions for the analog input voltage are met, high level is output from the VCOUT0 pin. When the conditions are not met, low level is output from the VCOUT0 pin.
Reference on low-voltage side < analog input voltage < reference on high-voltage side

Table 1.1 lists the Peripheral Function and Its Application. Figure 1.1 shows the Operation Outline.

Table 1.1 Peripheral Function and Its Application

Peripheral Function	Application
Comparator	Compare the analog input voltage and reference voltage

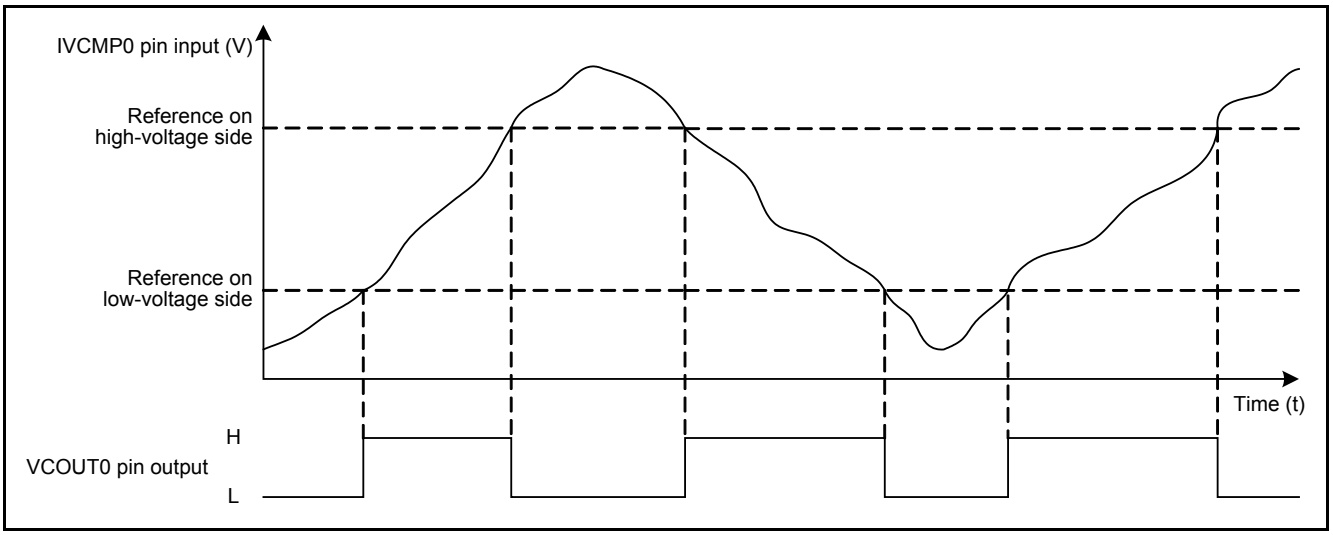


Figure 1.1 Operation Outline

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

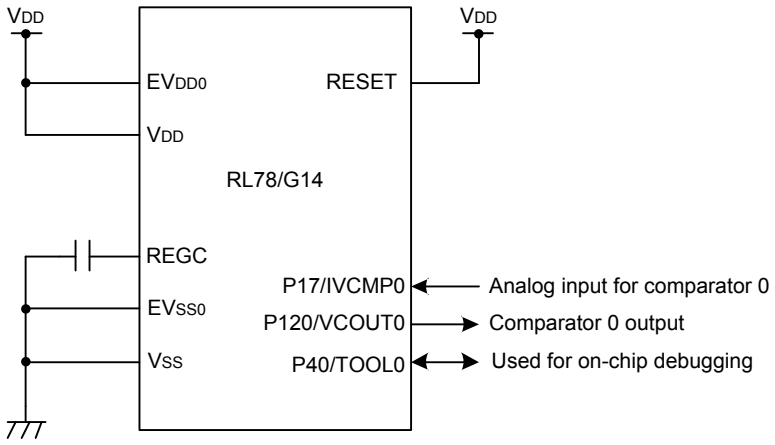
Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	RL78/G14 (R5F104PJA)
Operating frequencies	• High-speed on-chip oscillator clock (f_{HOCO}): 16 MHz (typical) • CPU/peripheral hardware clock (f_{CLK}): 16 MHz
Operating voltage	5.0 V (2.9 to 5.5 V) LVD operation (V_{LVI}): 2.81 V at the rising edge or 2.75 V at the falling edge in reset mode
Integrated development environment	Renesas Electronics Corporation CubeSuite+ V1.02.00
C compiler	Renesas Electronics Corporation CA78K0R V1.40
RL78/G14 code library	Renesas Electronics Corporation CodeGenerator for RL78/G14 V1.01.01

3. Hardware

3.1 Hardware Configuration

Figure 3.1 shows the Hardware Configuration used in this document.



Notes:
1. The above figure is simplified to show an overview of the hardware connection. When designing application circuits, make sure to handle unused pins appropriately to satisfy the electrical characteristics (connect input-only ports independently to either V_{DD} or V_{SS} via resistors).
2. Connect pins with names that begin with EV_{SS} to V_{SS}, and pins with names that begin with EV_{DD} to V_{DD}.
3. Make sure to set V_{DD} greater than the detection voltage (V_{LVI}) specified by the LVD.

Figure 3.1 Hardware Configuration

3.2 Pins Used

Table 3.1 lists the Pins Used and Their Functions.

Table 3.1 Pins Used and Their Functions

Pin Name	I/O	Functions
P17/IVCMP0	Input	Analog input for comparator 0
P120/VCOUT0	Output	Output for comparator 0

4. Software

4.1 Operation Overview

Use comparator 0 in window mode to operate the window comparator. Use a digital filter (sampling clock: f_{CLK}/32) and output the compared result for the filtered comparator from the VCOUT0 pin.

Comparator 0 settings are shown below.

Settings:
- Use high-speed mode for the comparator response speed.
- Use window mode for the operation mode.
- Use a digital filter. f_{CLK}/32 is selected for the sampling clock.
- Enable the VCOUT0 pin output of comparator 0.
- Output the comparator 0 output to the VCOUT0 pin.
- Do not use the comparator 0 interrupt.
- Use the IVCMP0 pin for the analog input.
- Use the VCOUT0 pin for the comparator 0 output.

4.2 Option-Setting Memory

Table 4.1 lists the Option-Setting Memory Configured in the Sample Code. When necessary, set a value suited to the user system.

Table 4.1 Option-Setting Memory Configured in the Sample Code

Address	Setting Value	Contents
000C0H/010C0H	11101111B	Watchdog timer operation is stopped (count is stopped after reset)
000C1H/010C1H	01111111B	LVD reset mode Detection voltage: Rising edge 2.81 V/falling edge 2.75 V
000C2H/010C2H	11101001B	Internal high-speed oscillation HS mode: 16 MHz
000C3H/010C3H	10000100B	On-chip debugging enabled

4.3 Functions

Table 4.2 lists the Functions.

Table 4.2 Functions

Function Name	Outline
hdwinit	Initial setting
R_Systeminit	Initial setting of peripheral functions
R_CGC_Create	Initial setting of the CPU clock
R_COMP_Create	Initial setting of the comparator
R_COMP_ Create_UserInit	Initial setting of the comparator (user function)
main	Main processing
R_COMP_Start	Comparator 0 operation start setting

4.4 Function Specifications

The following tables list the sample code function specifications.

hdwinit	
Outline	Initial setting
Header	None
Declaration	void hdwinit(void)
Description	Perform the initial setting of peripheral functions.
Argument	None
Return Value	None

R_Systeminit	
Outline	Initial setting of peripheral functions
Header	None
Declaration	void R_Systeminit(void)
Description	Perform the initial setting of peripheral functions used in this document.
Argument	None
Return Value	None

R_CGC_Create	
Outline	Initial setting of the CPU clock
Header	r_cg_cgc.h
Declaration	void R_CGC_Create(void)
Description	Perform the initial setting of the CPU clock.
Argument	None
Return Value	None

R_COMP_Create	
Outline	Initial setting of the comparator
Header	r_cg_comp.h
Declaration	void R_COMP_Create(void)
Description	Perform the initial setting to use the comparator in window mode.
Argument	None
Return Value	None

R_COMP_Create_UserInit	
Outline	Initial setting of the comparator (user function)
Header	r_cg_comp.h
Declaration	void R_COMP_Create_UserInit(void)
Description	Perform the initial setting added by the user after initializing the comparator.
Argument	None
Return Value	None

main	
Outline	Main processing
Header	None
Declaration	void main(void)
Description	Perform main processing.
Argument	None
Return Value	None

R_COMP0_Start	
Outline	Comparator 0 operation start setting
Header	r_cg_comp.h
Declaration	void R_COMP0_Start(void)
Description	Start window comparator operation
Argument	None
Return Value	None

4.5 Flowcharts

4.5.1 Overall Flowchart

Figure 4.1 shows the Overall Flowchart.

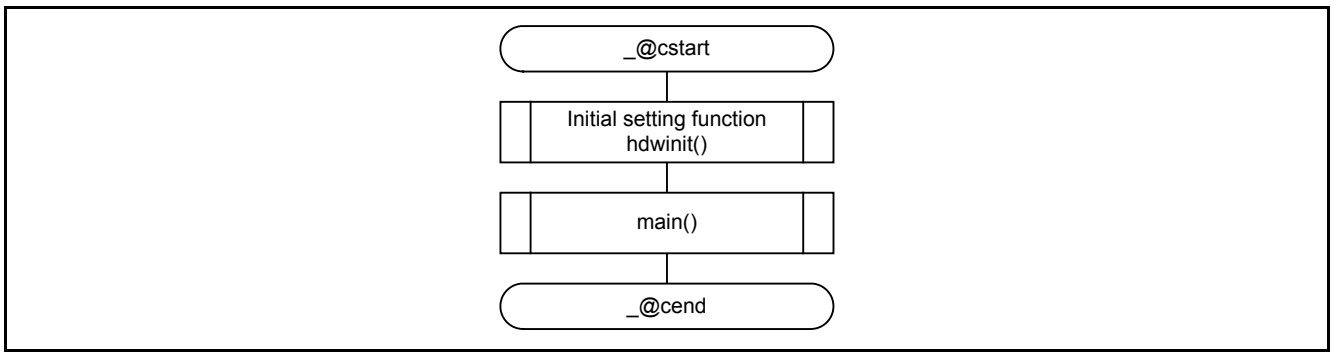


Figure 4.1 Overall Flowchart

4.5.2 Initial Setting

Figure 4.2 shows the Initial Setting.

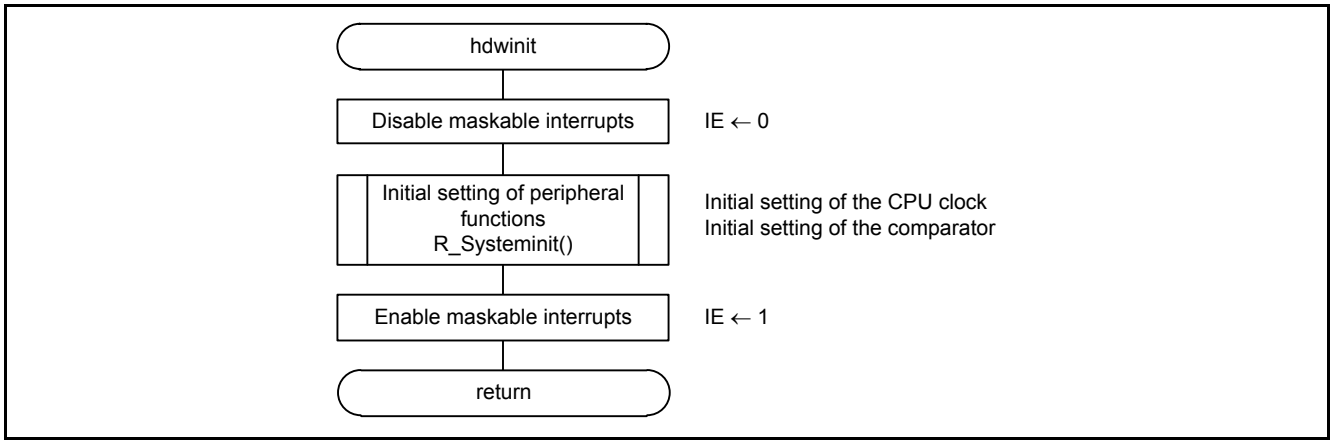


Figure 4.2 Initial Setting

4.5.3 Initial Setting of Peripheral Functions

Figure 4.3 shows the Initial Setting of Peripheral Functions.

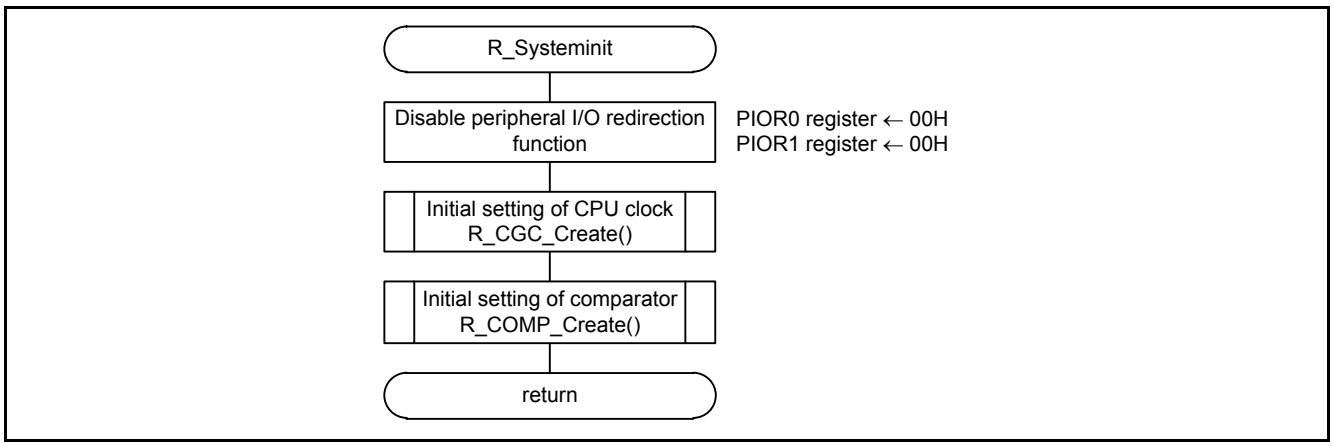


Figure 4.3 Initial Setting of Peripheral Functions

4.5.4 Initial Setting of the CPU Clock

Figure 4.4 shows the Initial Setting of the CPU Clock.

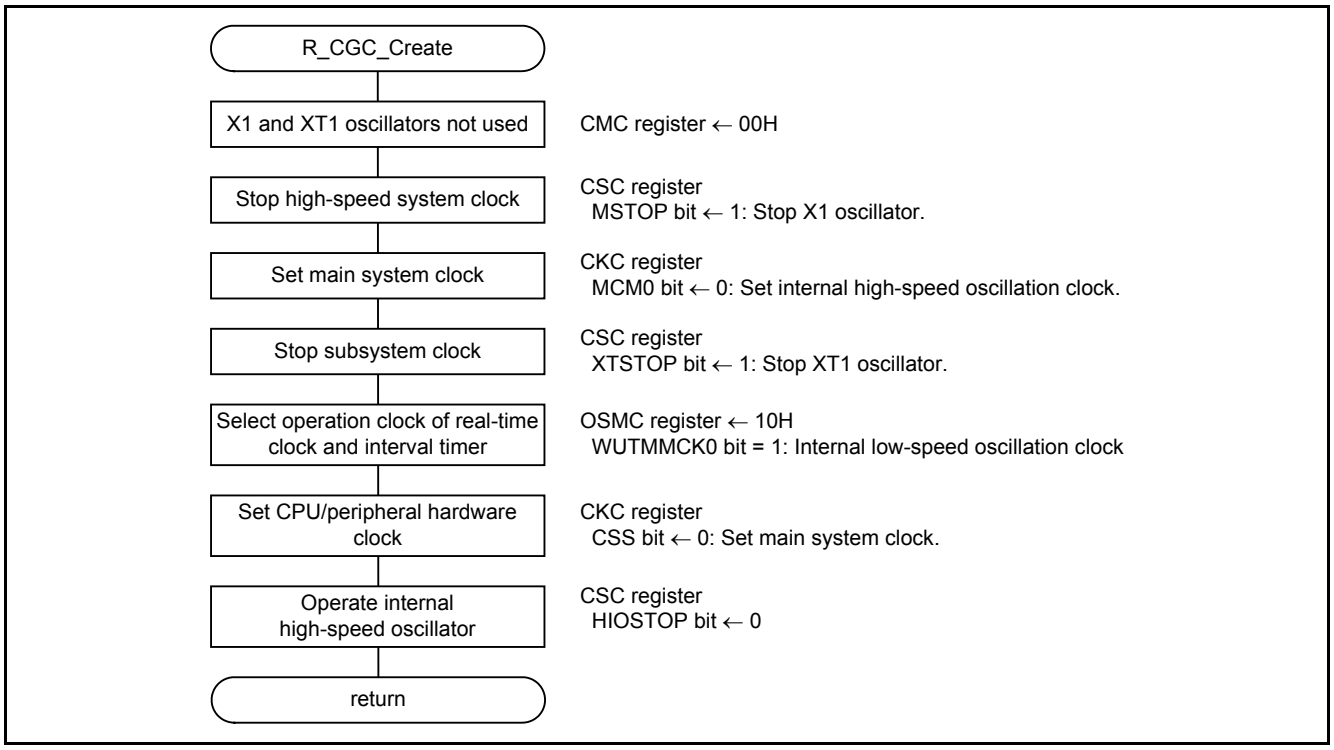


Figure 4.4 Initial Setting of the CPU Clock

4.5.5 Initial Setting of the Comparator

Figure 4.5 shows the Initial Setting of the Comparator.

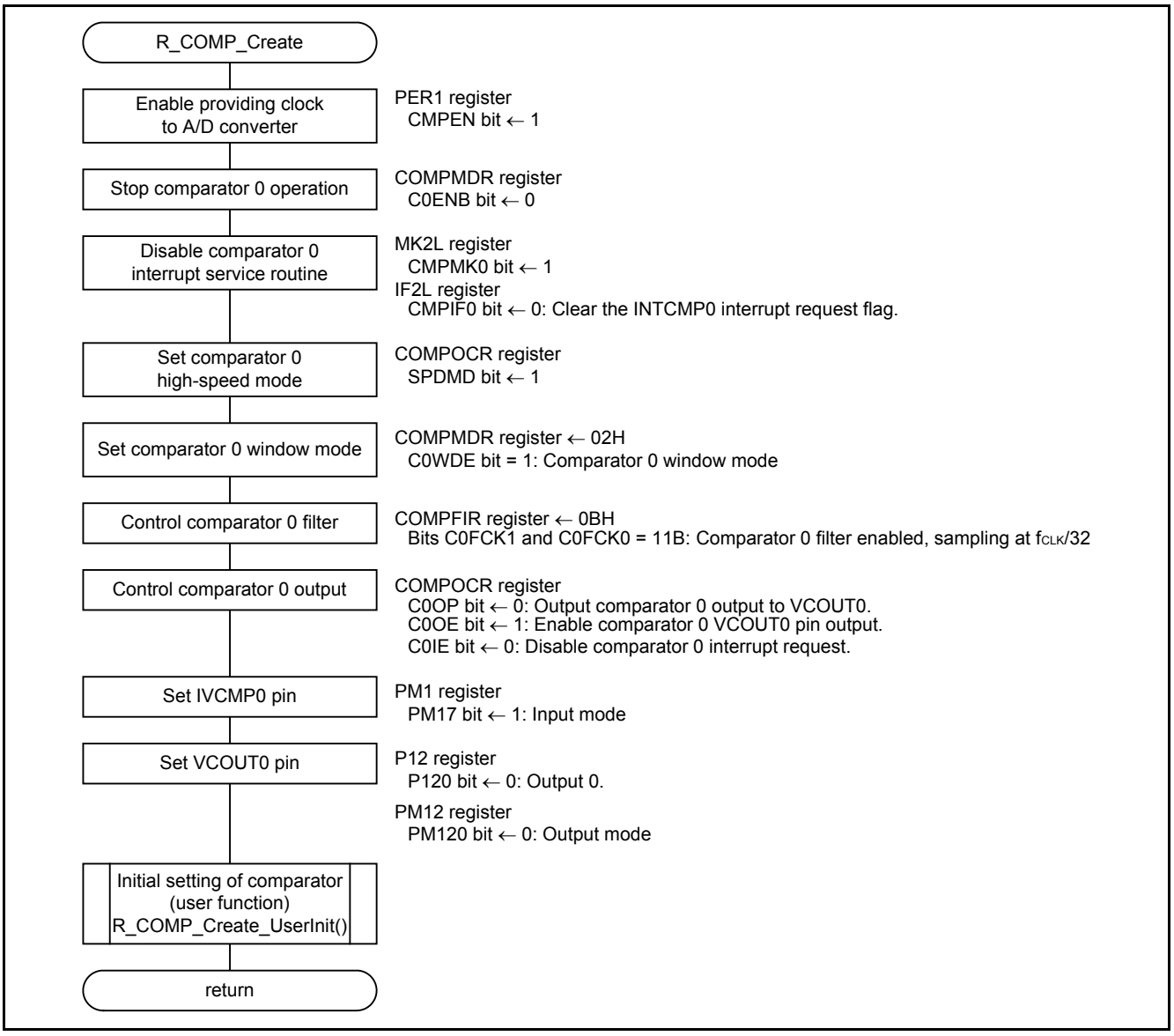


Figure 4.5 Initial Setting of the Comparator

Enable providing a clock to the comparator.

• Peripheral Enable Register 1 (PER1)

Symbol	7	6	5	4	3	2	1	0
PER1	DACEN	TRGEN	**CMPEN**	TRD0EN	DTCEN	0	0	TRJ0EN
Setting Value	x	x	**1**	x	x	—	—	x

Bit 5

CMPEN	Control of comparator input clock supply
0	Stops input clock supply. • SFR used by comparator cannot be written. • Comparator is in the reset status.
1	**Enables input clock supply.** **• SFR used by comparator can be read and written.**

Stop comparator 0 operation.

• Comparator Mode Setting Register (COMPMDR)

Symbol	7	6	5	4	3	2	1	0
COMPMDR	C1MON	C1VRF	C1WDE	C1ENB	C0MON	C0VRF	C0WDE	**C0ENB**
Setting Value	x	x	x	x		x		**0**

Bit 0

C0ENB	Comparator 0 operation enable
0	**Comparator 0 operation disabled**
1	Comparator 0 operation enabled

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Disable the comparator 0 interrupt service routine.

• Interrupt Mask Flag Register (MK2L)

Symbol	7	6	5	4	3	2	1	0
MK2L	PMK10 **CMPMK0**	PMK9	PMK8	PMK7	PMK6	TMMK13	TMMK12	TMMK11
Setting Value	**1**	x	x	x	x	x	x	x

Bit 7

CMPMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

• Interrupt Request Flag Register (IF2L)

Symbol	7	6	5	4	3	2	1	0
IF2L	PIF10 **CMPIF0**	PIF9	PIF8	PIF7	PIF6	TMIF13	TMIF12	TMIF11
Setting Value	**0**	x	x	x	x	x	x	x

Bit 7

CMPIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Set comparator 0 high-speed mode.

• Comparator Output Control Register (COMPOCR)

Symbol	7	6	5	4	3	2	1	0
COMPOCR	**SPDMD**	C1OP	C1OE	C1IE	0	C0OP	C0OE	C0IE
Setting Value	**1**	x	x	x	—			

Bit 7

SPDMD	Comparator speed selection
0	Comparator low-speed mode
1	**Comparator high-speed mode**

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set comparator 0 window mode.

• Comparator Mode Setting Register (COMPMDR)

Symbol	7	6	5	4	3	2	1	0
COMPMDR	C1MON	C1VRF	C1WDE	C1ENB	C0MON	C0VRF	**C0WDE**	C0ENB
Setting Value	x	x	x	x		x	**1**	

Bit 1

C0WDE	Comparator 0 window mode selection
0	Comparator 0 standard mode
1	**Comparator 0 window mode**

Control the comparator 0 filter.

• Comparator Filter Control Register (COMPFIR)

Symbol	7	6	5	4	3	2	1	0
COMPFIR	C1EDG	C1EPO	C1FCK1	C1FCK0	C0EDG	C0EPO	**C0FCK1**	**C0FCK0**
Setting Value	x	x	x	x	x	x	**1**	**1**

Bits 1 and 0

C0FCK1	C0FCK0	Comparator 0 filter selection
0	0	No comparator 0 filter
0	1	Comparator 0 filter enabled, sampling at f_{CLK}
1	0	Comparator 0 filter enabled, sampling at $f_{CLK}8$
1	**1**	**Comparator 0 filter enabled, sampling at $f_{CLK}/32$**

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Control comparator 0 output.

• Comparator Output Control Register (COMPOCR)

Symbol	7	6	5	4	3	2	1	0
COMPOCR	SPDMD	C1OP	C1OE	C1IE	0	**C0OP**	**C0OE**	**C0IE**
Setting Value		x	x	x	—	**0**	**1**	**0**

Bit 2

C0OP	VCOUT0 output polarity selection
0	**Comparator 0 output is output to VCOUT0**
1	Inverted comparator 0 output is output to VCOUT0

Bit 1

C0OE	VCOUT0 pin output enable
0	Comparator 0 VCOUT0 pin output disabled
1	**Comparator 0 VCOUT0 pin output enabled**

Bit 0

C0IE	Comparator 0 interrupt request enable
0	**Comparator 0 interrupt request disabled**
1	Comparator 0 interrupt request enabled

Set the IVCMP0 pin.

• Port Mode Register 1 (PM1)

Symbol	7	6	5	4	3	2	1	0
PM1	**PM17**	PM16	PM15	PM14	PM13	PM12	PM11	PM10
Setting Value	**1**	x	x	x	x	x	x	x

Bit 7

PM17	P17 pin I/O mode selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the VCOUT0 pin.

• Port Register 12 (P12)

Symbol	7	6	5	4	3	2	1	0
P12	0	0	0	P124	P123	P122	P121	**P120**
Setting Value	—	—	—	x	x	x	x	**0**

Bit 0

P120	Output data control
0	**Output 0**
1	Output 1

• Port Mode Register 1 (PM12)

Symbol	7	6	5	4	3	2	1	0
P12	1	1	1	1	1	1	1	**PM120**
Setting Value	—	—	—	—	—	—	—	**0**

Bit 0

PM120	P120 pin I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

4.5.6 Initial Setting of the Comparator (User Function)

Figure 4.6 shows the Initial Setting of the Comparator (User Function).

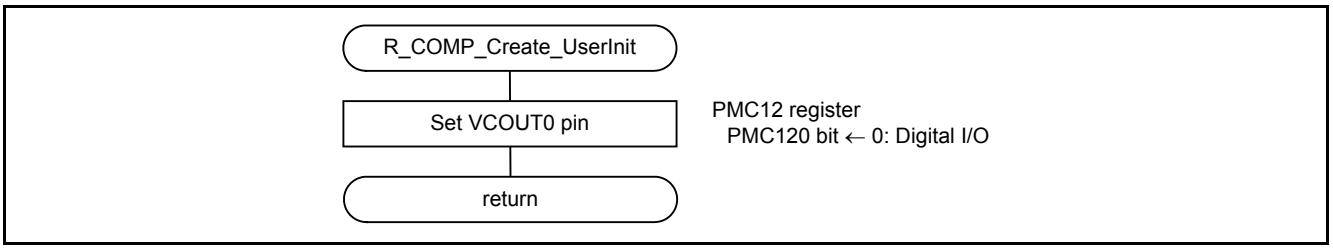


Figure 4.6 Initial Setting of the Comparator (User Function)

Set the VCOUT0 pin.

- Port Mode Control Register (PMC12)

Symbol	7	6	5	4	3	2	1	0
PMC12	1	1	1	1	1	1	1	**PMC120**
Setting Value	—	—	—	—	—	—	—	**0**

Bit 0

PMC120	P120 pin digital I/O and analog input selection
0	**Digital I/O (multiplexed function other than analog input)**
1	Analog input

4.5.7 Main Processing

Figure 4.7 shows the Main Processing.

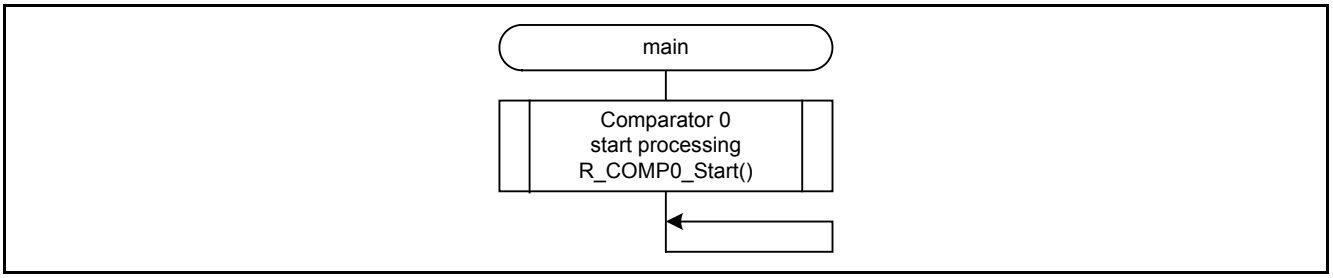


Figure 4.7 Main Processing

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

4.5.8 Comparator 0 Operation Start Setting

Figure 4.8 shows the Comparator 0 Operation Start Setting.

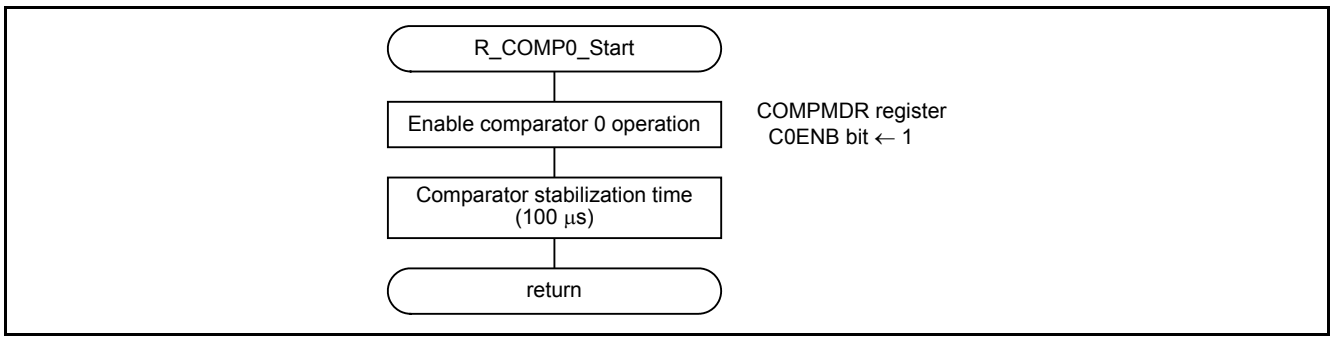


Figure 4.8 Comparator 0 Operation Start Setting

Enable comparator 0 operation.

• Comparator Mode Setting Register (COMPMDR)

Symbol	7	6	5	4	3	2	1	0
COMPMDR	C1MON	C1VRF	C1WDE	C1ENB	C0MON	C0VRF	C0WDE	**C0ENB**
Setting Value	x	x	x	x		x		**1**

Bit 0

C0ENB	Comparator 0 operation enable
0	Comparator 0 operation disabled
1	**Comparator 0 operation enabled**

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

User's Manual: Hardware
RL78/G14 Group User's Manual: Hardware Rev.0.02
RL78 Family User's Manual: Software Rev.1.00
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
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REVISION HISTORY	RL78/G14 Setting the Window Comparator

Rev.	Date	Description	
		Page	Summary
1.00	Aug. 31, 2012	—	First edition issued
1.10	June 1, 2013	4	Fixed typo in Table 2.1
		5	Fixed typo in Figure 3.1

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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