RL78/G14, R8C/36M Group

Migration Guide from R8C to RL78: Timer RA to Timer Array Unit

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Abstract

This document describes how to migrate from timer RA in the R8C/36M Group to the timer array unit (TAU) in RL78/G14 (80- and 100-pin packages).

This document contains register and bit symbols with variables. In this document, m = 0, 1 (unit number); n = 0 to 3 (channel number); and k = 0, 1, unless otherwise noted.

Products

RL78/G14, R8C/36M Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Differences between the R8C/36M Group and RL78/G14

1.1 Differences in Function Overview

Table 1.1 lists the differences between timer RA in the R8C/36M Group and the TAU in RL78/G14.

Table 1.1 Differences

Item	R8C/36M Group Timer RA	RL78/G14 TAU
Configuration	8-bit timer with 8-bit prescaler	16-bit timer (Note 1)
Count sources	f1, f2, f8, fOCO, fC32, fC	f_{CLK}
Counters	• TRAPRE register • TRA register	TCRmn register
Count value setting	• TRAPRE register • TRA register	TDRmn register
Modes	• Timer mode • Pulse output mode • Event counter mode • Pulse width measurement mode • Pulse period measurement mode	• Interval timer • Square wave output • External event counter • Divider (channel 0 in unit 0 only) • Input pulse interval measurement • Measurement of high-/low-level width of input signal • Delay counter • One-shot pulse output (Note 2) • PWM output (Note 2) • Multiple PWM output (Note 2)
Count operations	Decrement	• Count up (Note 3) • Count down (Note 3)
Timer input	Input from the TRAIO pin	• Channel 0 — Input from the TI00 pin — Event input signal from the ELC • Channel 1 — Input from the TI01 pin — Event input signal from the ELC — Low-speed on-chip oscillator clock (f_{IL}) — Subsystem clock (f_{SUB})
I/O pin selection	Yes	No
Simultaneous channel operation function	No	Yes (Note 2)
LIN communication	Available when timer RA links with UART0	Available when TAU links with UART (channel 3 in unit 0 only)
Coordination with event link controller (ELC)	No	Yes

Notes: 1. Channels 1 and 3 can operate as 8-bit timers.
2. These modes are available by using a master channel to link with slave channels.
3. Count operations depend on modes specified.

1.2 Differences in Timer Mode

The interval timer in RL78/G14 corresponds to timer mode in the R8C/36M Group.

Table 1.2 lists the differences between timer mode in the R8C/36M Group and interval timer in RL78/G14.

Table 1.2 Differences Between Timer Mode and Interval Timer

Item	R8C/36M Group (Timer Mode)	RL78/G14 (Interval Timer)
Count sources	f1, f2, f8, fOCO, fC32, fC	f_{CLK}
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count continues	No operation is carried out from start trigger detection (TSmn = 1) until count clock generation. The first count clock loads the value of the TDRmn register to the TCRmn register and the subsequent count clock performs count down operation.
Count start condition	1 is written to the TSTART bit in the TRACR register	1 is written to the TSmn, TSHm1, or TSHm3 bit in the TSm register
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register	1 is written to the TTmn, TTHm1, or TTHm3 bit in the TTm register
Read from timer	Read registers TRAPRE and TRA	Read the TCRmn register
Write to timer	Write to registers TRAPRE and TRA	Write to the TDRmn register

1.3 Differences in Pulse Output Mode

Square wave output in RL78/G14 corresponds to pulse output mode in the R8C/36M Group.

Table 1.3 lists the differences between pulse output mode in the R8C/36M Group and square wave output in RL78/G14.

Table 1.3 Differences Between Pulse Output and Square Wave Output

Item	R8C/36M Group (Pulse Output Mode)	RL78/G14 (Interval Timer)
Count sources	f1, f2, f8, fOCO, fC32, fC	f_{CLK}
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued	No operation is carried out from start trigger detection (TSmn = 1) until count clock generation. The first count clock loads the value of the TDRmn register to the TCRmn register and the subsequent count clock performs count down operation.
Count start condition	1 is written to the TSTART bit in the TRACR register	1 is written to the TSmn, TSHm1, or TSHm3 bit in the TSm register
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register	1 is written to the TTmn, TTHm1, or TTHm3 bit in the TTm register
Read from timer	Read registers TRAPRE and TRA	Read the TCRmn register
Write to timer	Write to registers TRAPRE and TRA	Write to the TDRmn register
Selectable functions	• TRAIO signal polarity switch function • TRAO output function • Pulse output stop function • TRAIO pin select function • TRAO pin select function	• Whether the timer interrupt is generated when counting is started • Output pin level when pulse output is started

1.4 Differences in Event Counter Mode

External event counter in RL78/G14 corresponds to event counter mode in the R8C/36M Group.

Table 1.4 lists the differences between event counter mode in the R8C/36M Group and external event counter in RL78/G14.

Table 1.4 Differences Between Event Counter Mode and External Event Counter

Item	R8C/36M Group (Event Counter Mode)	RL78/G14 (External Event Counter)
Count sources	External signal input to the TRAIO pin	External signal input to the TImn pin
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued	The TCRmn register loads the value of TDRmn register by setting the TSmn bit to 1. When the input edge of the TImn pin is detected, the subsequent count clock performs count down operation.
Count start condition	1 is written to the TSTART bit in the TRACR register	1 is written to the TSmn, TSHm1, or TSHm3 bit in the TSm register
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register	1 is written to the TTmn, TTHm1, or TTHm3 bit in the TTm register
I/O pins	• TRAIO pin: count source input • TRAO pin: programmable I/O port or pulse output	TImn pin: count source input
Read from timer	Read registers TRAPRE and TRA	Read the TCRmn register
Write to timer	Write to registers TRAPRE and TRA	Write to the TDRmn register
Selectable functions	• TRAIO signal polarity switch function • Count source input pin select function • Pulse output function • TRAO pin select function • Digital filter function • Event input control function	• Select the input edge of the TImn pin • Whether the timer interrupt is generated when counting is started • Enable or disable the noise filter

1.5 Differences in Pulse Width Measurement Mode

Measurement of high-/low-level width of input signal in RL78/G14 correspond to pulse width measurement mode in the R8C/36M Group.

Table 1.5 lists the differences between pulse width measurement mode in the R8C/36M Group and measurement of high-/low-level width of input signal in RL78/G14.

Table 1.5 Differences Between Pulse Width Measurement Mode and Measurement of High-/Low-level Width of Input Signal

Item	R8C/36M Group (Pulse Width Measurement Mode)	RL78/G14 (Measurement of High-/Low-level Width of Input Signal)
Count sources	f1, f2, f8, fOCO, fC32, fC	f_{CLK}
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count continues	• Count up • When the counter overflows, the OVF bit in the TRSmn register is set to 1 (count is continued) RL78/G14 enters start trigger wait status by setting the TSmn bit to 1 when the timer operation is stopped (TEmn = 0). No operation is carried out from start trigger detection (TSmn = 1) until count clock generation. The first count clock loads 0000H to the TCRmn register and the subsequent count clock performs count up operation.
Count start condition	1 is written to the TSTART bit in the TRACR register	1 is written to the TSmn bit in the TSm register
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register	1 is written to the TTmn bits in the TTm register
Interrupt request generation timing	• When timer RA underflows • Rising or falling of the TRAIO input	When the valid capture edge is detected
I/O Pins	• TRAIO pin: Measurement pulse input • TRAO pin: Programmable I/O port	TImn pin: Measurement pulse input
Read from timer	Read registers TRAPRE and TRA	Read the TCRmn register
Write to timer	Write to registers TRAPRE and TRA	N/A
Selectable functions	• Measurement level setting • Measured pulse input pin select function • Digital filter function	• Whether the timer interrupt is generated when counting is started • Output pin level when pulse output is started

1.6 Pulse Period Measurement Mode

Input pulse interval measurement in RL78/G14 corresponds to pulse period measurement mode in the R8C/36M Group.

Table 1.6 lists the differences between pulse period measurement in the R8C/36M Group and input pulse interval measurement in RL78/G14.

Table 1.6 Differences Between Pulse Period Measurement Mode and Input Pulse Interval Measurement

Item	R8C/36M Group (Pulse Period Measurement Mode)	RL78/G14 (Input Pulse Interval Measurement)
Count sources	f1, f2, f8, fOCO, fC32, fC	f_{CLK}
Count operations	• Decrement • After the active edge of the measurement pulse is input, the contents of the read-out buffer are retained at the first underflow of timer RA prescaler. Then timer RA reloads the contents in the reload register at the second underflow of timer RA prescaler and continues counting.	• Count up • No operation is carried out from start trigger detection until count clock generation. The first count clock loads 0000H to the TCRmn register and the subsequent count clock performs count up operation.
Count start condition	1 is written to the TSTART bit in the TRACR register	1 is written to the TSmn bit in the TSm register
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register	1 is written to the TTmn bit in the TTm register
Interrupt request generation timing	• When timer RA underflows or reloads • Rising or falling of the TRAIO input	When the valid capture edge is detected
I/O Pins	• TRAIO pin: Measured pulse input • TRAO pin: Programmable I/O port	TImn pin: Measurement pulse input
Read from timer	Read registers TRAPRE and TRA	Read registers TCRmn and TDRmn
Write to timer	Write to registers TRAPRE and TRA	N/A
Selectable functions	• Measurement period selection • Measured pulse input pin select function • Digital filter function	• Measurement period selection • Enable or disable the noise filter

1.7 Assigned I/O Pins

Table 1.7 lists the I/O pins assigned for use in the R8C/36M Group.

Table 1.7 R8C/36M Group I/O Pins

Pin Name	Assigned Pins	I/O
TRAIO	P1_5, P1_7, or P3_2	Input/output
TRAO	P3_0, P3_7, or P5_6	Output

Table 1.8 lists the I/O pins assigned for use in RL78/G14.

Table 1.8 RL78/G14 I/O Pins

Unit Number	Target Channel	Pin Name	Assigned Pins	I/O
Unit 0	Channel 0	TI00	P00	Input
		TO00	P01	Output
	Channel 1	TI01	P16	Input
		TO01	P16	Output
	Channel 2	TI02	P17	Input
		TO02	P17	Output
	Channel 3	TI03	P31	Input
		TO03	P31	Output
Unit 1	Channel 0	TI10	P64	Input
		TO10	P64	Output
	Channel 1	TI11	P65	Input
		TO11	P65	Output
	Channel 2	TI12	P66	Input
		TO12	P66	Output
	Channel 3	TI13	P67	Input
		TO13	P67	Output

2. Register Compatibility

Register compatibility between timer RA in the R8C/36M Group and TAU in RL78/G14 is listed in Table 2.1 and Table 2.2.

Table 2.1 Register Compatibility (1/2)

Item	R8C/36M Group	RL78/G14
Count start	• TRACR register TSTART bit	• TSm register Bits TSmn, TSHm1, TSHm3 (Note 1)
Count status flag	• TRACR register TCSTF bit	• TEm register Bits TEmn, TEHm1, TEHm3 (Note 2)
Count stop	• TRACR register TSTART bit	• TTm register Bits TTmn, TTHm1, TTHm3 (Note 3)
Count forcible stop	• TRACR register TSTOP bit	N/A
Active edge judgment flag	• TRACR register TEDGF bit	N/A
Underflow flag	• TRACR register TUNDF bit	N/A
TRAIO polarity switch	• TRAIOC register TEDGSEL bit	• TOm register TOmn bit • TMRmn register Bits CISmn0 and CISmn1
TRAIO output control	• TRAIOC register TOPCR bit	• TOEm register TOEmn bit
TRAO output enable	• TRAIOC register TOENA bit	N/A
Hardware LIN function select	• TRAIOC register TIOSEL bit	• ISC register ISC1 bit
TRAIO input filter select	• TRAIOC register Bits TIPF0 and TIPF1	• Registers NFEN1, NFEN2
TRAIO event input control	• TRAIOC register Bits TIOGT0 and TIOGT1	N/A
Operating mode select	• TRAMR register Bits TMOD0 to TMOD2	• TMRmn register Bits MDmn1 to MDmn3
Count source select	• TRAMR register Bits TCK0 to TCK2	• TPSm register • TMRmn register Bits CKSmn0, CKSmn1, CCSmn
Count source cutoff	• TRAMR register TCKCUT bit	N/A
Prescaler	• TRAPRE register	N/A
Timer	• TRA register	• Registers TCRmn, TDRmn

Notes: 1. When channels 1 and 3 are in 8-bit timer mode, bits TSHm1 and TSHm3 are triggers to enable operation of (start) the higher 8-bit timer.
2. When channels 1 and 3 are in 8-bit timer mode, bits TEHm1 and TEHm3 indicate whether the higher 8-bit timer is enabled or stopped.
3. When channels 1 and 3 are in 8-bit timer mode, bits TTHm1 and TTHm3 are triggers to stop the higher 8-bit timer.

Table 2.2 Register Compatibility (2/2)

Item	R8C/36M Group	RL78/G14
TRAIO pin select	• TRASR register Bits TRAIOSEL0 and TRAIOSEL1	N/A
TRAO pin select	• TRASR register Bits TRAOSEL0 and TRAOSEL1	N/A
Independent channel operation/simultaneous channel operation (slave/master) select	N/A	• TMRmn register Bits MASTERmn, SPLITmn (Notes 1, 2)
8-bit timer/16-bit timer select on channels 1 and 3	N/A	• TMRmn register SPLITmn bit (Note 2)
Start trigger and capture trigger setting on channel n	N/A	• TMRmn register Bits STSmn0 to STSmn2
Count start and interrupt setting	N/A	• TMRmn register MDmn0 bit
Counter overflow status	N/A	• TSRmn register OVF bit
Timer input select on channels 1 and 3	N/A	• TIS0 register Bits TIS00 to TIS02, TIS04
Timer output buffer	N/A	• TOm register TOmn bit
Timer output level control	N/A	• TOLm register TOLmn bit
Timer output mode control	N/A	• TOMm register TOMmn bit

Notes: 1. MASTERmn bit: n = 2
2. SPLITmn bit: n = 1, 3

3. Comparison of Timer RA and TAU Settings

3.1 Count Start

3.1.1 R8C/36M Group

Set the TSTART bit in the TRACR register to start the timer RA count. Table 3.1 lists the functions of the TSTART bit.

Table 3.1 TSTART Bit Functions

TSTART Bit	Timer RA Count Start Bit
0	Count stops
1	Count starts

3.1.2 RL78/G14

Set the TSmn, TSHm1, or TSHm3 bit in the TSm register to start count operation in each channel. The TSHm1 or TSHm3 bit enables the operation (start) of the higher 8-bit timer when channel 1 or 3 is in 8-bit timer mode.

Table 3.2 lists the functions of the TSmn bit. Table 3.3 lists the functions of the TSHm1 bit. Table 3.4 lists the functions of the TSHm3 bit.

Table 3.2 TSmn Bit Functions

TSmn Bit	Operation Enable (Start) Trigger of Channel n
0	No trigger operation
1	The TEmn bit is set to 1 and the count operation becomes enabled (Note 1)

Note: 1. The TCRmn register count operation start in the count operation enabled state depends on the operating mode.

Table 3.3 TSHm1 Bit Functions

TSHm1 Bit	Trigger to Enable Operation (Start Operation) of the Higher 8-bit Timer When Channel 1 is in the 8-bit Timer Mode
0	No trigger operation
1	The TEHm1 bit is set to 1 and the count operation becomes enabled (Note 1)

Note: 1. The TCRm1 register count operation start is in interval timer mode when the TAU is in the count operation enabled state.

Table 3.4 TSHm3 Bit Functions

TSHm3 Bit	Trigger to Enable Operation (Start Operation) of the Higher 8-bit Timer When Channel 3 is in the 8-bit Timer Mode
0	No trigger operation
1	The TEHm3 bit is set to 1 and the count operation becomes enabled (Note 1)

Note: 1. The TCRm3 register count operation start is in interval timer mode when the TAU is in the count operation enabled state.

3.2 Count Status Flag

3.2.1 R8C/36M Group

Read the TCSTF bit in the TRACR register to ascertain the status of the timer RA count. Table 3.5 lists the functions of the TCSTF bit.

Table 3.5 TCSTF Bit Functions

TCSTF Bit	Timer RA Count Status Flag
0	Count stops
1	During count

3.2.2 RL78/G14

Read the TEmn, TEHm1, or TEHm3 bit in the TEm register to ascertain the status of the timer operation in each channel. Table 3.6 lists the functions of the TEmn bit. Table 3.7 lists the functions of the TEHm1 bit. Table 3.8 lists the functions of the TEHm3 bit.

Table 3.6 TEmn Bit Functions

TEmn Bit	Indication of Operation Enable/Stop Status of Channel n
0	Operation is stopped
1	Operation is enabled

Table 3.7 TEHm1 Bit Functions

TEHm1 Bit	Indication of Whether Operation of the Higher 8-bit Timer is Enabled or Stopped When Channel 1 is in the 8-bit Timer Mode
0	Operation is stopped
1	Operation is enabled

Table 3.8 TEHm3 Bit Functions

TEHm3 Bit	Indication of Whether Operation of the Higher 8-bit Timer is Enabled or Stopped When Channel 3 is in the 8-bit Timer Mode
0	Operation is stopped
1	Operation is enabled

3.3 Count Stop

3.3.1 R8C/36M Group

Set the TSTART bit in the TRACR register to stop timer RA to count. Table 3.9 lists the functions of the TSTART bit.

Table 3.9 TSTART Bit Functions

TSTART Bit	Timer RA Count Start Bit
0	Count stops
1	Count starts

3.3.2 RL78/G14

Set the TTmn, TTHm1, or TTHm3 bit in the TSm register to stop count operation in each channel. The TTHm1 or TTHm3 bit stops the operation of the higher 8-bit timer when channel 1 or 3 is in 8-bit timer mode.

Table 3.10 lists the functions of the TTmn bit. Table 3.11 lists the functions of the TTHm1 bit. Table 3.12 lists the functions of the TTHm3 bit.

Table 3.10 TTmn Bit Functions

TTmn Bit	Operation Stop Trigger of Channel n
0	TEmn bit is cleared to 0 and the count operation is stopped
1	Operation is stopped (stop trigger is generated). This bit is the trigger to stop operation of the lower 8-bit timer for TTm1 and TTm3 when channel 1 or 3 is in the 8-bit timer mode.

Table 3.11 TTHm1 Bit Functions

TTHm1 Bit	Trigger to Stop Operation of the Higher 8-bit Timer When Channel 1 is in the 8-bit Timer Mode
0	No trigger operation
1	TEHm1 bit is cleared to 0 and the count operation is stopped

Table 3.12 TTHm3 Bit Functions

TTHm3 Bit	Trigger to Stop Operation of the Higher 8-bit Timer When Channel 3 is in the 8-bit Timer Mode
0	No trigger operation
1	TEHm3 bit is cleared to 0 and the count operation is stopped

3.4 TRAIO Polarity Switch

3.4.1 R8C/36M Group (Pulse Output Mode)

Set the TEDGSEL bit in the TRAIOC register to select the level of the TRAIO pin while in pulse output mode or when the pulse output is started. Table 3.13 lists the functions of the TEDGSEL bit.

Table 3.13 TEDGSEL Bit Functions (Pulse Output Mode)

TEDGSEL Bit	TRAIO Polarity Switch Bit
0	TRAIO output starts at “H”
1	TRAIO output starts at “L”

3.4.2 RL78/G14 (Square Wave Output)

Set the TOmn bit in the TOm register to select the level of the output pin (TOmn pin) when square wave output is started. Table 3.14 lists the functions of the TOmn bit.

Table 3.14 TOmn Bit Functions

TOmn Bit	Timer Output of Channel n
0	Timer output value is “0”
1	Timer output value is “1”

3.4.3 R8C/36M Group (Event Counter Mode)

Set the TEDGSEL bit in the TRAIOC register to select the valid edge of the event count source. Table 3.15 lists the functions of the TEDGSEL bit.

Table 3.15 TEDGSEL Bit Functions (Event Counter Mode)

TEDGSEL Bit	TRAIO Polarity Switch Bit
0	Starts counting at rising edge of the TRAIO input and TRAO starts output at “L”
1	Starts counting at falling edge of the TRAIO input and TRAO starts output at “H”

3.4.4 RL78/G14 (External Event Counter)

Set bits CISmn0 and CISmn1 in the TMRmn register to select the valid edge of the input pin (TImn pin). Table 3.16 lists the functions of bits CISmn0 and CISmn1.

Table 3.16 CISmn0, CISmn1 Bit Functions (External Event Counter)

CISmn1 Bit	CISmn0 Bit	Selection of TImn Pin Input Valid Edge
0	0	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge

3.4.5 R8C/36M Group (Pulse Width Measurement)

Set the TEDGSEL bit in the TRAIOC register to select “L” width or “H” width of the TRAIO input to measure in pulse width measurement mode. Table 3.17 lists the functions of the TEDGSEL bit.

Table 3.17 TEDGSEL Bit Functions (Pulse Width Measurement)

TEDGSEL Bit	TRAIO Polarity Switch Bit
0	TRAIO input starts at “L”
1	TRAIO input starts at “H”

3.4.6 RL78/G14 (Measurement of High-/Low-level Width of Input Signal)

Set bits CISmn0 and CISmn1 in the TMRmn register to select the valid edge of the input pin (TImn pin). Table 3.18 lists the functions of bits CISmn0 and CISmn1.

Table 3.18 CISmn0, CISmn1 Bit Functions (Measurement of High-/Low-level Width of Input Signal)

CISmn1 Bit	CISmn0 Bit	Selection of TImn Pin Input Valid Edge
0	0	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge

3.4.7 R8C/36M Group (Pulse Period Measurement)

Set the TEDGSEL bit in the TRAIOC register to select the measurement period of the input pulse. Table 3.19 lists the functions of the TEDGSEL bit.

Table 3.19 TEDGSEL Bit Functions (Pulse Period Measurement)

TEDGSEL Bit	TRAIO Polarity Switch Bit
0	Measures measurement pulse from one rising edge to next rising edge
1	Measures measurement pulse from one falling edge to next falling edge

3.4.8 RL78/G14 (Input Pulse Interval Measurement)

Set bits CISmn0 and CISmn1 in the TMRmn register to select the measurement interval of the input pulse. Table 3.20 lists the functions of bits CISmn0 and CISmn1.

Table 3.20 CISmn0, CISmn1 Bit Functions (Input Pulse Interval Measurement)

CISmn1 Bit	CISmn0 Bit	Selection of TImn Pin Input Valid Edge
0	0	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge

3.5 TRAIO Output Control

3.5.1 R8C/36M Group (Pulse Output Mode)

Set the TOPCR bit in the TRAIOC register to enable or disable the pulse output. Table 3.21 lists the functions of the TOPCR bit.

Table 3.21 TOPCR Bit Functions

TOPCR Bit	TRAIO Output Control Bit
0	TRAIO output
1	TRAIO output disabled

3.5.2 RL78/G14

Set the TOEmn bit in the TOEm register to enable or disable the output from the TOmn pin. Table 3.22 lists the functions of the TOEmn bit.

Table 3.22 TOEmn Bit Functions

TOEmn Bit	Timer Output Enable/Disable of Channel n
0	Timer output is disabled. Timer operation is not applied to the TOmn bit and the output is fixed. Writing to the TOmn bit is enabled and the level set in the TOmn bit is output from the TOmn pin.
1	Timer output is enabled. Timer operation is applied to the TOmn bit and an output waveform is generated. Writing to the TOmn bit is ignored.

3.6 Hardware LIN Function Select

3.6.1 R8C/36M Group

Set the TIOSEL bit in the TRAIOC register to select the hardware LIN function. Table 3.23 lists the functions of the TIOSEL bit. Hardware LIN function is available in timer mode or pulse width measurement mode.

Table 3.23 TIOSEL Bit Functions

TIOSEL Bit	Hardware LIN Function Select Bit
0	Set to 0. However, set to 1 when the hardware LIN function is used.
1	

3.6.2 RL78/G14

Channel 3 in TAU establishes LIN-bus communication to link with SAU. Set the ISC1 bit in the ISC register to enable this link. Table 3.24 lists the functions of the ISC1 bit.

Table 3.24 ISC1 Bit Functions

ISC1 Bit	Switching Channel 3 Input of Timer Array Unit 0
0	Uses the input signal of the TI03 pin as a timer input (normal operation)
1	Input signal of the RxD0 pin is used as timer input (detects the wakeup signal and measures the low width of the break field and the pulse width of the sync field)

3.7 TRAIO Input Filter Select

3.7.1 R8C/36M Group

The input filter is available in event counter mode, pulse width measurement mode, or pulse period measurement mode. Set bits TIPF0 and TIPF1 in the TRAIOC register to select the input filter. Table 3.25 lists the functions of bits TIPF0 and TIPF1.

Table 3.25 TIPF0, TIPF1 Bit Functions

TIPF0 Bit	TIPF1 Bit	TRAIO Input Filter Select Bit
0	0	No filter
0	1	Filter with f1 sampling
1	0	Filter with f8 sampling
1	1	Filter with f32 sampling

3.7.2 RL78/G14

In RL78/G14, each channel can be set to either use or not use a noise filter on the input signal from the input pin (TImn). Set the TNFEN00, TNFEN01, TNFEN02, or TNFEN03 bit in the NFEN1 register and the TNFEN10, TNFEN11, TNFEN12, or TNFEN13 bit in the NFEN2 register to use or not use the noise filter. Table 3.26 to Table 3.33 list functions of bits TNFEN00, TNFEN01, TNFEN02, TNFEN03, TNFEN10, TNFEN11, TNFEN12, and TNFEN13.

Table 3.26 TNFEN00 Bit Functions

TNFEN00 Bit	Enable/Disable Using Noise Filter of TI00 Pin Input Signal
0	Noise filter OFF
1	Noise filter ON

Table 3.27 TNFEN01 Bit Functions

TNFEN01 Bit	Enable/Disable Using Noise Filter of TI01 Pin Input Signal
0	Noise filter OFF
1	Noise filter ON

Table 3.28 TNFEN02 Bit Functions

TNFEN02 Bit	Enable/Disable Using Noise Filter of TI02 Pin Input Signal
0	Noise filter OFF
1	Noise filter ON

Table 3.29 TNFEN03 Bit Functions

TNFEN03 Bit	Enable/Disable Using Noise Filter of TI03 Pin or RxD0 Pin Input Signal
0	Noise filter OFF
1	Noise filter ON

Table 3.30 TNFEN10 Bit Functions

TNFEN10 Bit	Enable/Disable Using Noise Filter of TI10 Pin Input Signal
0	Noise filter OFF
1	Noise filter ON

Table 3.31 TNFEN11 Bit Functions

TNFEN11 Bit	Enable/Disable Using Noise Filter of TI11 Pin Input Signal
0	Noise filter OFF
1	Noise filter ON

Table 3.32 TNFEN12 Bit Functions

TNFEN12 Bit	Enable/Disable Using Noise Filter of TI12 Pin Input Signal
0	Noise filter OFF
1	Noise filter ON

Table 3.33 TNFEN13 Bit Functions

TNFEN13 Bit	Enable/Disable Using Noise Filter of TI13 Pin Input Signal
0	Noise filter OFF
1	Noise filter ON

3.8 Operating Mode Select

3.8.1 R8C/36M Group

Set bits TMOD0 to TMOD2 in the TRAMR register to select operating mode. Table 3.34 lists the functions of bits TMOD0 to TMOD2.

Table 3.34 TMOD0 to TMOD2 Bit Functions

TMOD0 Bit	TMOD1 Bit	TMOD2 Bit	Timer RA Operating Mode Select Bit
0	0	0	Timer mode
0	0	1	Pulse output mode
0	1	0	Event counter mode
0	1	1	Pulse width measurement mode
1	0	0	Pulse period measurement mode
1	0	1	Do not set.
1	1	0	Do not set.
1	1	1	Do not set.

3.8.2 RL78/G14

Set bits MDmn1 to MDmn3 in the TMRmn register to select operating mode. Table 3.35 lists the functions of bits MDmn1 to MDmn3.

Table 3.35 MDmn1 to MDmn3 Bit Functions

MDmn3 Bit	MDmn2 Bit	MDmn1 Bit	Operating Mode of Channel n	Corresponding Function	Count operation of TCR
0	0	0	Interval timer mode	Interval timer/square wave output/divider function/PWM output (master)	Counting down
0	1	0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	Event counter mode	External event counter	Counting down
1	0	0	One-count mode	Delay counter/one-shot pulse output/PWM output (slave)	Counting down
1	1	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above			Setting prohibited		

Set the MDmn0 bit in the TMRmn register whether to generate a timer interrupt when counting started, and enable or disable the start trigger during count operation. Table 3.36 lists the functions of the MDmn0 bit.

Table 3.36 MDmn0 Bit Functions

Operating Mode	MDmn0 Bit	Setting of Starting Counting and Interrupt
• Interval timer • Capture mode	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	Start trigger is valid during counting operation. At that time, interrupt is not generated.
• Capture & one-count mode	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated.
Other than above		Setting prohibited

3.9 Operating Clock Setting

3.9.1 R8C/36M Group

Set the TCK0 to TCK2 bits in the TRAMR register to select the count source of the operating clock. Table 3.37 lists the functions of bits TCK0 to TCK2.

Table 3.37 TCK0 to TCK2 Bit Functions

TCK2 Bit	TCK1 Bit	TCK0 Bit	Timer RA Count Source Select Bit
0	0	0	f1
0	0	1	f8
0	1	0	fOCO
0	1	1	f2
1	0	0	fC32
1	0	1	Do not set.
1	1	0	fC
1	1	1	Do not set.

Set the TCKCUT bit in the TRAMR register to provide or cut off the count source. Table 3.38 lists the functions of the TCKCUT bit.

Table 3.38 TCKCUT Bit Functions

TCKCUT Bit	Timer RA Count Source Cutoff Bit
0	Provides count source
1	Cuts off count source

3.9.2 RL78/G14

Set the TPSm register to specify the operating clock (CKm0, CKm1, CKm2, or CKm3) of each channel. Set bits PRSm00 to PRSm03 in the TPSm register to specify CKm0. To specify CKm1, set bits PRSm10 to PRSm13 in the TPSm register.

CKm2 and CKm3 are available on channels 1 and 3. Interval time can be achieved by using CKm2 and CKm3 with the interval timer function. Specify CKm2 by bits PRSm20 and PRSm21, and specify CKm3 by bits PRSm30 and PRSm31.

Table 3.39 lists the functions of bits PRSmk0 to PRSmk3. Table 3.40 lists the functions of bits PRSm20 and PRSm21. Table 3.41 lists the functions of bits PRSm30 and PRSm31.

Table 3.39 PRSmk0 to PRSmk3 Bit Functions

PRSmk3 Bit	PRSmk2 Bit	PRSmk1 Bit	PRSmk0 Bit	Selection of Operating Clock (CKmk)
0	0	0	0	f_{CLK}
0	0	0	1	$f_{CLK}/2$
0	0	1	0	$f_{CLK}/2^2$
0	0	1	1	$f_{CLK}/2^3$
0	1	0	0	$f_{CLK}/2^4$
0	1	0	1	$f_{CLK}/2^5$
0	1	1	0	$f_{CLK}/2^6$
0	1	1	1	$f_{CLK}/2^7$
1	0	0	0	$f_{CLK}/2^8$
1	0	0	1	$f_{CLK}/2^9$
1	0	1	0	$f_{CLK}/2^{10}$
1	0	1	1	$f_{CLK}/2^{11}$
1	1	0	0	$f_{CLK}/2^{12}$
1	1	0	1	$f_{CLK}/2^{13}$
1	1	1	0	$f_{CLK}/2^{14}$
1	1	1	1	$f_{CLK}/2^{15}$

Table 3.40 PRSm20 and PRSm21 Bit Functions

PRSm21 Bit	PRSm20 Bit	Selection of Operating Clock (CKm2)
0	0	f_{CLK}
0	1	$f_{CLK}/2$
1	0	$f_{CLK}/2^4$
1	1	$f_{CLK}/2^6$

Table 3.41 PRSm30 and PRSm31 Bit Functions

PRSm31 Bit	PRSm30 Bit	Selection of Operating Clock (CKm3)
0	0	$f_{CLK}/2^8$
0	1	$f_{CLK}/2^{10}$
1	0	$f_{CLK}/2^{12}$
1	1	$f_{CLK}/2^{14}$

Set bits CKSmn0 and CKSmn1 in the TMRmn register to specify the operating clock (f_{MCK}) of channel n. Table 3.42 lists the functions of bits CKSmn0 and CKSmn1.

Table 3.42 CKSm0 and CKSm1 Bit Functions

CKSmn1 Bit	CKSmn0 Bit	Selection of Operating Clock (f_{MCK}) of Channel n
0	0	Operating clock CKm0 set by timer clock select register m (TPSm)
0	1	Operating clock CKm1 set by timer clock select register m (TPSm)
1	0	Operating clock CKm2 set by timer clock select register m (TPSm)
1	1	Operating clock CKm3 set by timer clock select register m (TPSm)

Set the CCSmn bit in the TMRmn register to specify the count clock (f_{TCLK}) of channel n. Table 3.43 lists the functions of the CCSmn bit.

Table 3.43 CCSmn Bit Functions

CCSmn Bit	Selection of Count Clock (f_{TCLK}) of Channel n
0	Operating clock (f_{MCK}) specified by the CKSmn0 and CKSmn1 bits
1	Valid edge of input signal input from the TImn pin

3.10 Prescaler and Timer

3.10.1 R8C/36M Group

An internal or external count source is counted by the TRAPRE register. TRA register counts the underflows of the TRAPRE register.

3.10.2 RL78/G14

A count clock is counted by the TCRmn register. Set the count value in the TDRmn register.

3.11 Simultaneous Channel Operation Function

3.11.1 R8C/36M Group

There is no equivalent function in the R8C/36M Group.

3.11.2 RL78/G14

The simultaneous channel operation function is available by using a master channel (a reference timer that mainly counts cycles) to link with slave channels (timers operate according to the master channel).

Only channel 2 can be specified as the master channel. Channel 0 is fixed as the master channel regardless of the setting.

Set the MASTERm2 bit in the TMRm2 register to specify channel 2 in independent channel function operation function or in simultaneous channel operation function (slave or master). Table 3.44 lists the functions of the MASTERm2 bit.

Table 3.44 MASTERm2 Bit Functions

MASTERm2 Bit	Selection Between Using Channel n Independently or Simultaneously with Another Channel (as a Slave or Master)
0	Operates in independent channel operation function or as slave channel in simultaneous channel operation function
1	Operates as master channel in simultaneous channel operation function

Set the SPLITmn bit in the TMRmn register to 1 to use channel 1 or 3 as an independent channel. Also, set the SPLITmn bit to specify 8-bit timer operation or 16-bit timer operation.

Table 3.45 lists the function of the SPLITmn bit.

Table 3.45 SPLITmn Bit Functions

SPLITmn Bit	Selection of 8 or 16-bit Timer Operation for Channels 1 and 3
0	Operates as 16-bit timer (Operates in independent channel operation function or as slave channel in simultaneous channel operation function).
1	Operates as 8-bit timer

3.12 Start Trigger and Capture Trigger Setting

3.12.1 R8C/36M Group

There is no equivalent function in the R8C/36M Group.

3.12.2 RL78/G14

Set bits STSmn0 to STSmn2 in the TMRmn register to specify the start trigger or capture trigger on channel n. Table 3.46 lists the functions of bits STSmn0 to STSmn2.

Table 3.46 STSmn0 to STSmn2 Bit Functions

STSmn2 Bit	STSmn1 Bit	STSmn0 Bit	Setting of Start Trigger or Capture Trigger of Channel n
0	0	0	Only software trigger start is valid (other trigger sources are unselected)
0	0	1	Valid edge of the TImn pin input is used as both the start trigger and capture trigger
0	1	0	Both the edges of the TImn pin input are used as a start trigger and a capture trigger
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function)
Other than above			Setting prohibited

3.13 Timer Input

3.13.1 R8C/36M Group

There is no equivalent function in the R8C/36M Group.

3.13.2 RL78/G14

Set the TIS0 register to specify timer input on channel 0 or 1. Set the TIS04 bit to specify the timer input to use on channel 0. Set bits TIS00 to TIS02 to specify the timer input to use on channel 1. Table 3.47 lists the functions of bits TIS00 to TIS02. Table 3.48 lists the functions of the TIS04 bit.

Table 3.47 TIS00 to TIS02 Bit Functions

TIS02 Bit	TIS01 Bit	TIS00 Bit	Selection of Timer Input Used with Channel 1
0	0	0	Input signal of timer input pin (TI01)
0	0	1	Event input signal from ELC
0	1	0	Input signal of timer input pin (TI01)
0	1	1	
1	0	0	Low-speed on-chip oscillator clock (f_{IL})
1	0	1	Subsystem clock (f_{SUB})
Other than above			Setting prohibited

Table 3.48 TIS04 Bit Functions

TIS04 Bit	Selection of Timer Input Used with Channel 0
0	Input signal of timer input pin (TI00)
1	Event input signal from ELC

3.14 Timer Output

3.14.1 R8C/36M Group

There is no equivalent function in the R8C/36M Group.

3.14.2 RL78/G14

Set the TOmn bit in the TOm register to output signals from the timer output pin on each channel when timer output is disabled on channel n. Table 3.49 lists the functions of the TOmn bit.

Table 3.49 TOmn Bit Functions

TOmn Bit	Timer Output of Channel n
0	Timer output value is “0”
1	Timer output value is “1”

Set the TOMmn bit in the TOMm register to specify master channel output mode or slave channel output mode. Table 3.50 lists the functions of the TOMmn bit.

Table 3.50 TOMmn Bit Functions

TOMmn Bit	Control of Timer Output Mode of Channel n
0	Master channel output mode (to produce toggle output by timer interrupt request signal (INTTMmn))
1	Slave channel output mode (output is set by the timer interrupt request signal (INTTMmn) of the master channel, and reset by the timer interrupt request signal (INTTMmp) of the slave channel)

Set the TOLmn bit in the TOLm register to control the timer output level on each channel.

The setting of the inverted output of channel by the TOLm register is reflected when the timer output signal is set or reset while the timer output is enabled (TOEmn = 1) in slave channel output mode (TOMmn = 1). Setting in this register is invalid in master channel output mode (TOMmn = 0).

Table 3.51 lists the functions of the TOLmn bit.

Table 3.51 TOLmn Bit Functions

TOLmn Bit	Control of Timer Output Level of Channel n
0	Positive logic output (active-high)
1	Negative logic output (active-low)

4. Note When Using the TAU

4.1 Note When Using Timer Output

An MCU pin which is assigned to the timer output function may also be assigned to other functions. To use the timer output on such a pin, set the output of the other functions to initial status.

5. Reference Documents

User's Manual: Hardware

RL78/G14 User's Manual: Hardware Rev.2.00 (R01UH0186EJ)

R8C/36M Group User's Manual: Hardware Rev.1.00 (R01UH0259EJ)

The latest versions can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	RL78/G14, R8C/36M Group Migration Guide from R8C to RL78: Timer RA to Timer Array Unit

Rev.	Date	Description	
		Page	Summary
1.00	Nov. 18, 2013	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 2.2