RL78/G13

Timer Array Unit (PWM Output) CC-RL

R01AN2589EJ0200
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Introduction

This application note describes the PWM output function of the timer array unit (TAU). This unit changes the PWM output duty ratio and inverts the LED indication at 500 ms intervals.

Target Device

RL78/G13

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

This application note describes the PWM output function which is realized using channel 0 as the master and channel 1 as the slave in simultaneous channel operation mode. The brightness of the LEDs is controlled by connecting the PWM output to LED1 (for PWM output). Timing signals with fixed cycle time (500 ms) are created by counting the number of timer interrupts (INTTM00) generated by channel 0. Using these timing signals, the duty ratio of the PWM output is changed and the output of LED2 (for updating) is inverted.

Table 1.1 shows the Required Peripheral Function and Its Use. Figure 1.1 presents an Overview of PWM Output Operation. Table 1.2 shows the Relation between PWM Output Duty Ratios and LED Brightnesses. Figure 1.2 is a Simplified Timing Chart for PWM Output Operation.

Table 1.1 Required Peripheral Function and Its Use

Peripheral function	Use
Timer array unit 0	This unit is used to realize the PWM function by operating channel 0 and channel 1 together and deliver a PWM output from the TO01 pin.

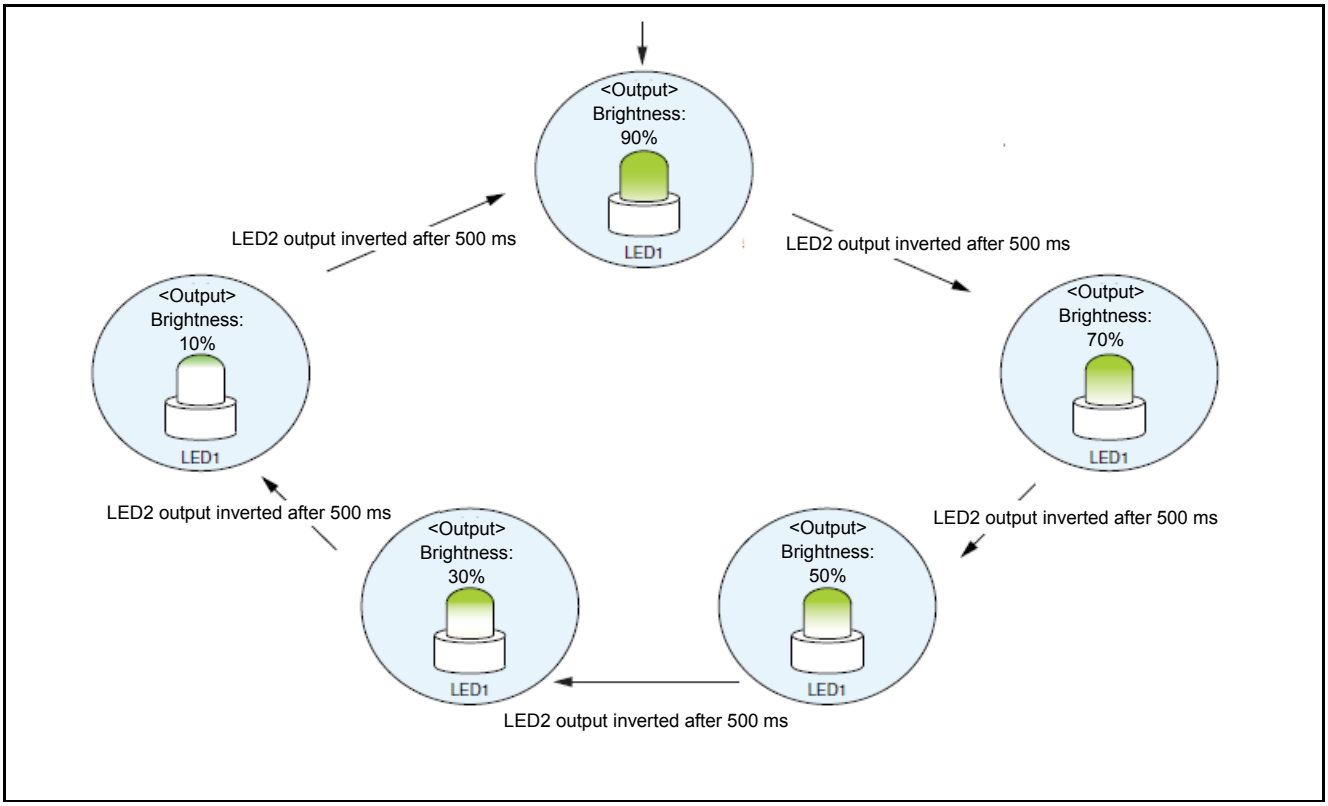

Figure 1.1 Overview of PWM Output Operation

Table 1.2 Relation between PWM Output Duty Ratios and LED Brightnesses

Duty ratio	LED1 brightness
10%	90%
30%	70%
50%	50%
70%	30%
90%	10%

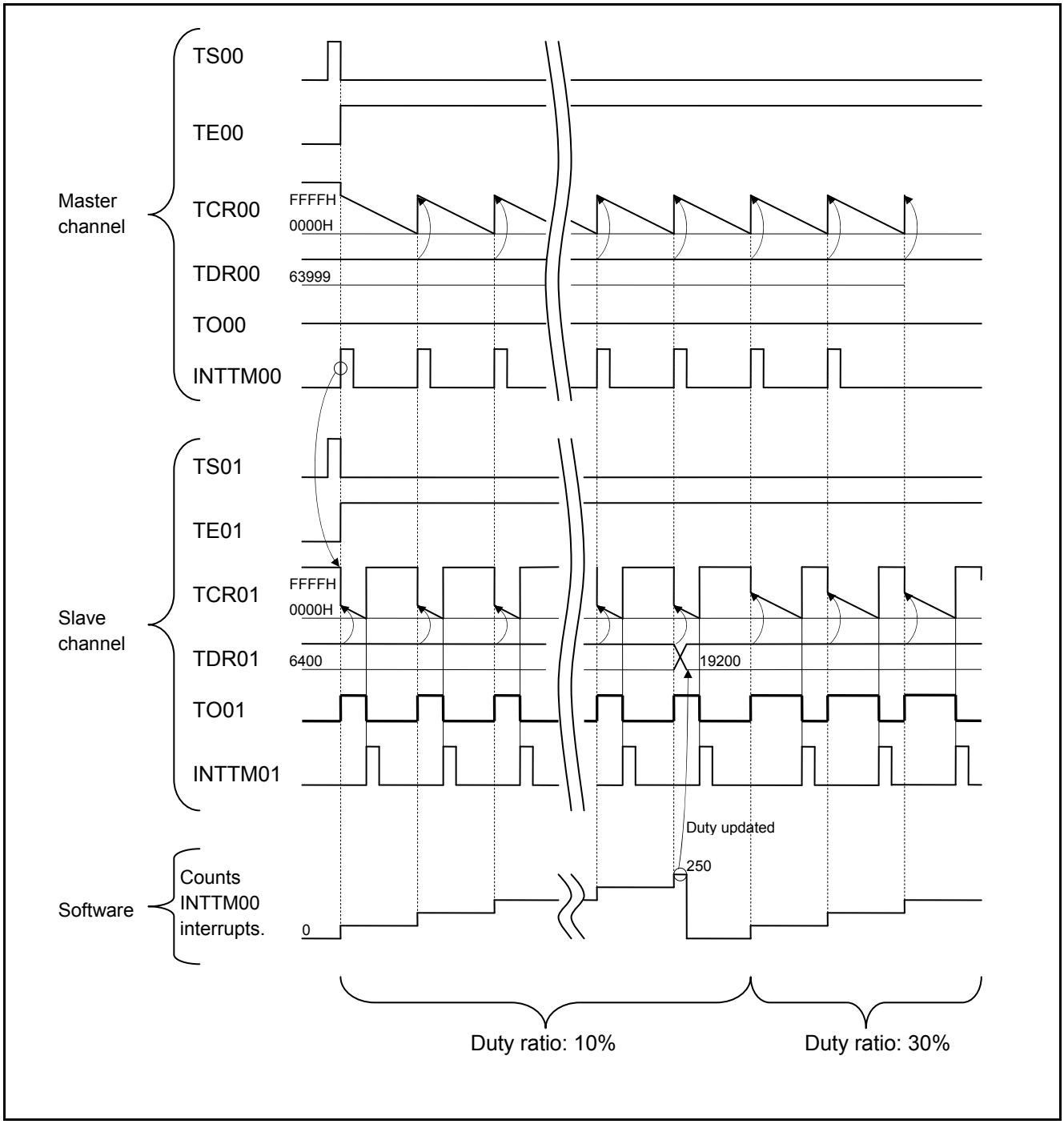

Figure 1.2 Simplified Timing Chart for PWM Output Operation

2. Operation Check Conditions

The sample code described in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G13 (R5F100LEA)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 32 MHz • CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0 V (Operation is possible over a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode which uses 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ for CC V3.01.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V4.0.0.26 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.01.00 from Renesas Electronics Corp.

3. Related Application Note

The application note that is related to this application note is listed below for reference.

- RL78/G13 Initialization (R01AN2575E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the Hardware Configuration used for this application note.

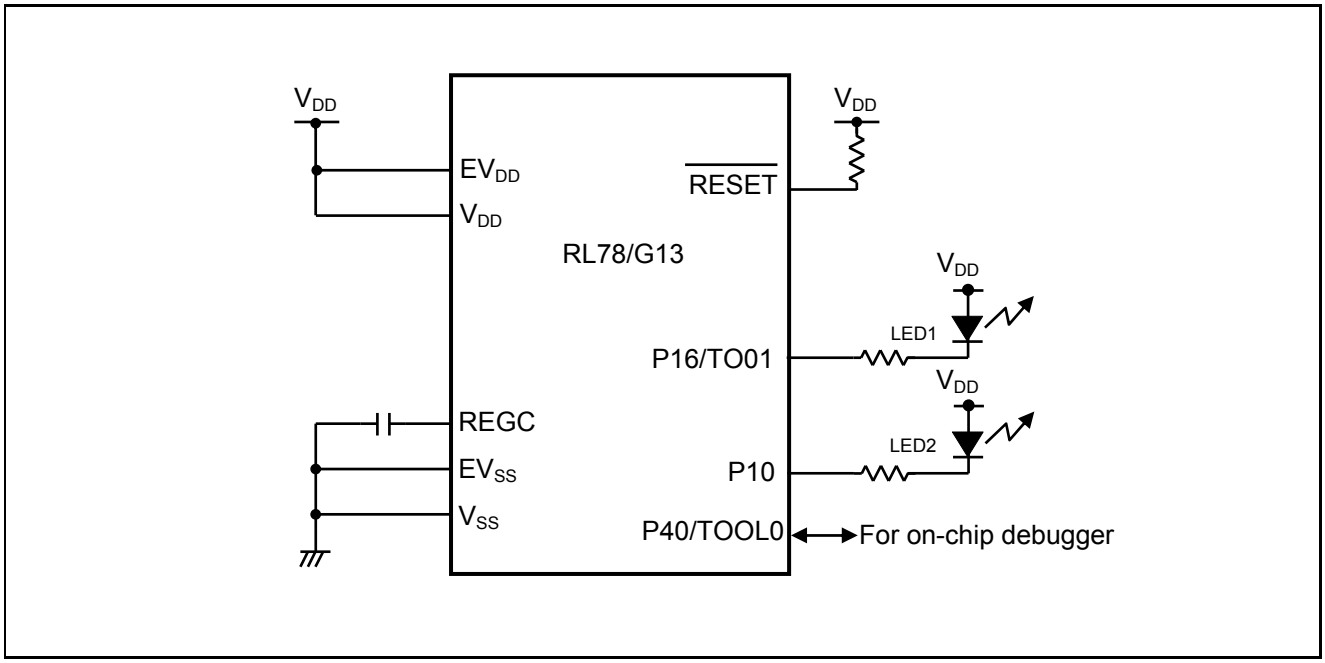

Figure 4.1 Hardware Configuration

Caution: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).
2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

4.2 List of Pins to be Used

Table 4.1 lists the Pins to be Used and Their Functions.

Table 4.1 Pins to be Used and Their Functions

Pin Name	I/O	Description
P16/TO01	Output	PWM output port
P10	Output	Output port for LED indications

5. Description of the Software

5.1 Operation Outline

The sample program covered in this application note implements PWM by operating channel 0 and channel 1 together, and delivers a PWM output from P16/TO01.

Also, this program detects 250 timer interrupts (INTTM00) with 2 ms cycle time which are generated by channel 0. Then, it changes the PWM output duty ratio and inverts the LED indication at 500 ms intervals.

(1) Initialize the TAU.
<Conditions for setting>

- Set the P16/TO01 pin to a PWM output.
- Set TAU0 channel 0 to 2-ms cycle interval timer mode.
- Set TAU0 channel 1 to one-count mode.
- Initialize the duty ratio of the PWM output to 10 %.
- Use timer interrupts (INTTM00) from timer channel 0.

(2) Operation starts when both the operation enable trigger bits for TAU0's channel 0 and channel 1 are set to 1 simultaneously. The sample program executes a HALT instruction to wait for a timer interrupt (INTTM00) from channel 0.

(3) After the start of timer operation, channel 0 generates a timer interrupt (INTTM00) at 2 ms intervals.

(4) When the HALT mode is canceled by a timer interrupt (INTTM00) from channel 0, the sample program starts counting the number of INTTM00 interrupts generated. After channel 0 has generated 250 timer interrupts (i.e., after 500 ms), the sample program updates the channel 1 count value and changes the duty ratio. This duty ratio is increased from 10% to 90% (10% → 30% → 50% → 70% → 90%). It is incremented by 20% each time the number of channel 0 timer interrupts (INTTM00) generated reaches 250. (Thus, it is incremented at 500 ms intervals). It is reset to 10% after it becomes 90%.

(5) After processing timer interrupts (INTTM00) from channel 0, the sample program executes another HALT instruction and waits for the next timer interrupt (INTTM00) from channel 0.

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD reset mode which uses 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

5.3 List of Constant

Table 5.2 lists the constant that is used in this sample program.

Table 5.2 Constant for the Sample Program

Constant	Setting	Description
_1900_TAU_TDR01_VALUE	0x1900U	TDR01 setting for a 10% duty ratio

5.4 List of Functions

Table 5.3 lists the Functions that are used in this sample program.

Table 5.3 Functions

Function	Outline
R_TAU0_Channel0_Start	TAU0 channel 0 start processing
r_tau0_channel0_interrupt	TAU0 channel 0 timer interrupt processing

5.5 Function Specifications

Shown below are the functions that are used in this sample program.

[Function Name] R_TAU0_Channel0_Start	
Synopsis	TAU0 channel 0 start processing
Header	#include "r_cg_macrodriver.h" #include "r_cg_timer.h" #include "r_cg_userdefine.h"
Declaration	void R_TAU0_Channel0_Start(void)
Explanation	This function unmasks TAU0 channel 0 interrupts and starts count operation.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_tau0_channel0_interrupt	
Synopsis	Channel 0 timer interrupt processing
Header	r_cg_timer.h
Declaration	static void __near r_tau0_channel0_interrupt(void)
Explanation	This function counts the number of INTTM00 interrupts generated. Each time the count reaches 250, it updates the duty ratio of a PWM output. (Thus, it updates the duty ratio at 500 ms intervals.)
Arguments	None
Return value	None
Remarks	None

5.6 Flowcharts

Figure 5.1 shows the Overall Flow of the sample program described in this application note.

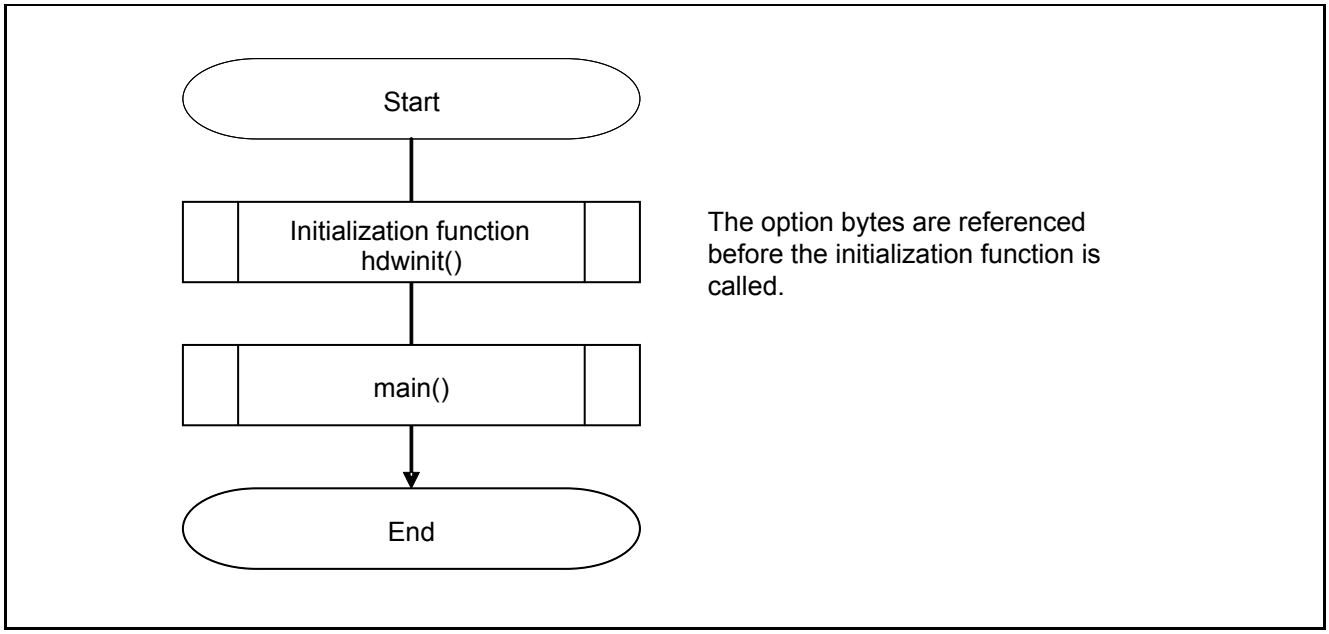

Figure 5.1 Overall Flow

Note: Startup routine is executed before and after the initialization function.

5.6.1 Initialization Function

Figure 5.2 shows the flowchart for the Initialization Function.

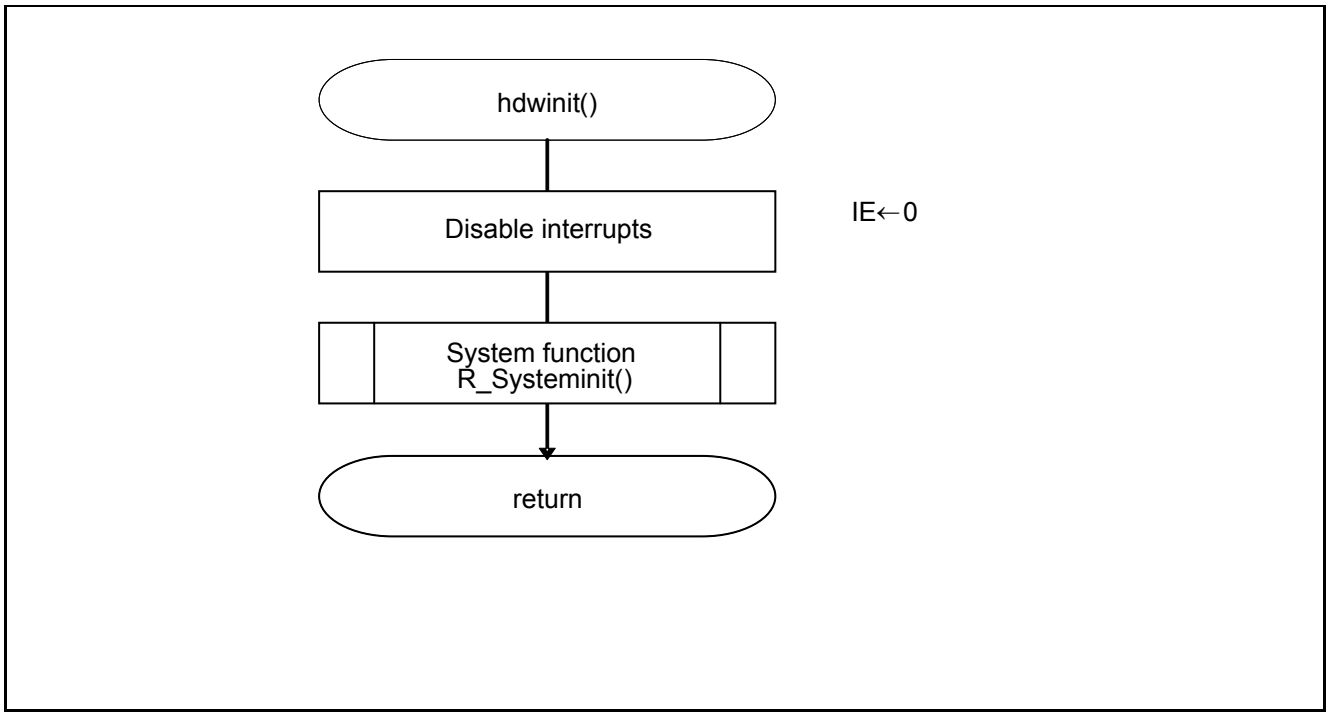

Figure 5.2 Initialization Function

5.6.2 System Function

Figure 5.3 shows the flowchart for the System Function.

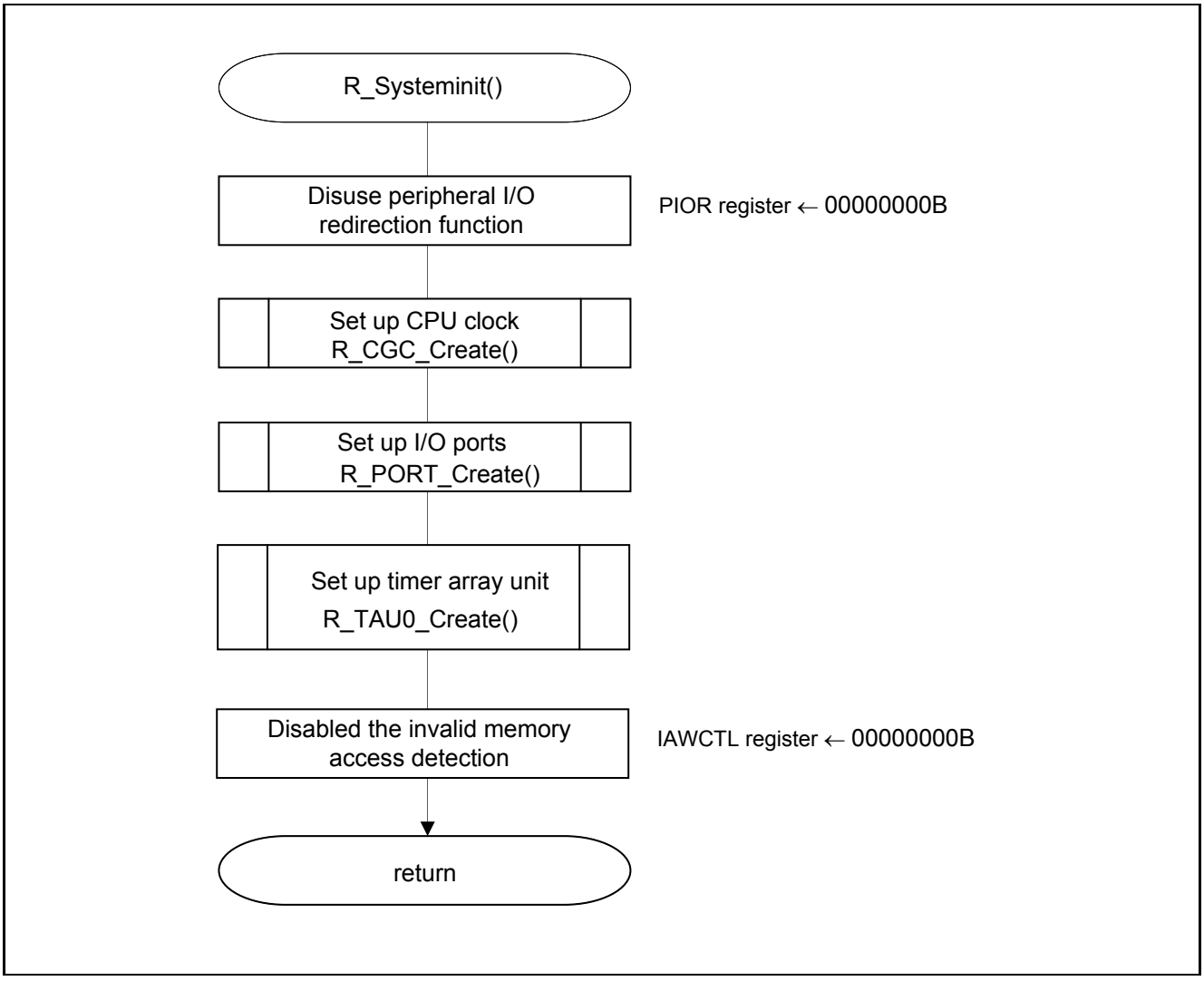

Figure 5.3 System Function

5.6.3 I/O Port Setup

Figure 5.4 shows the flowchart for setting up the I/O ports.

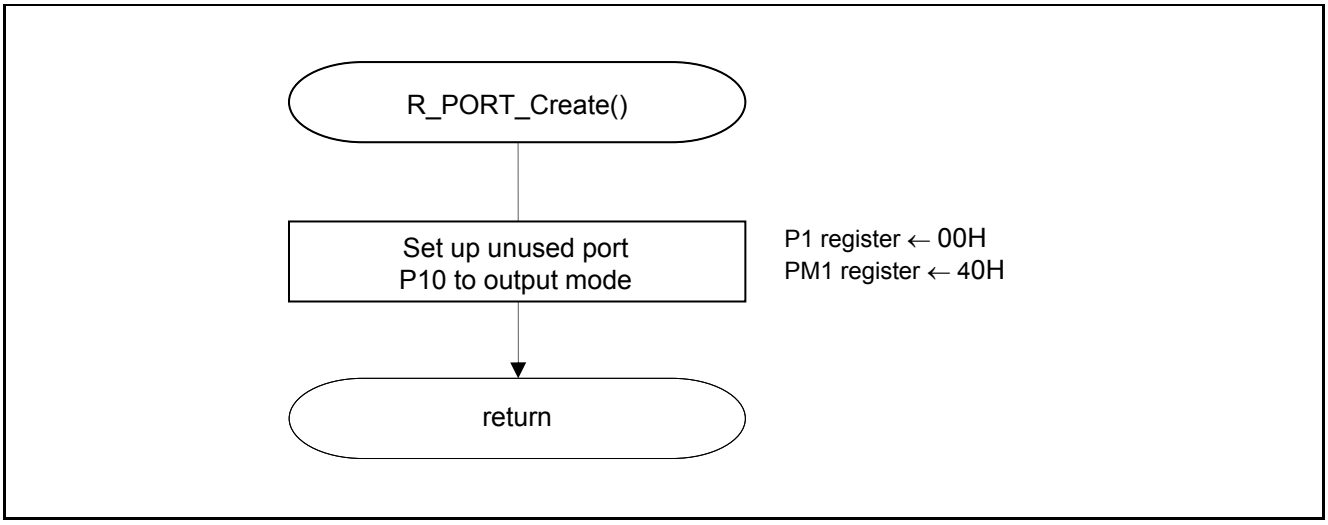

Figure 5.4 I/O Port Setup

Note: Refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E) for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

Setting up the LED pin to indicate updating of the duty ratio

- Port mode register (PM1)

  Select I/O mode for PM10.

  Symbol: PM1

7	6	5	4	3	2	1	0
PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10
x	x	x	x	x	x	x	**0**

  Bit 0

PM10	PM10 I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

  Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.6.4 CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock.

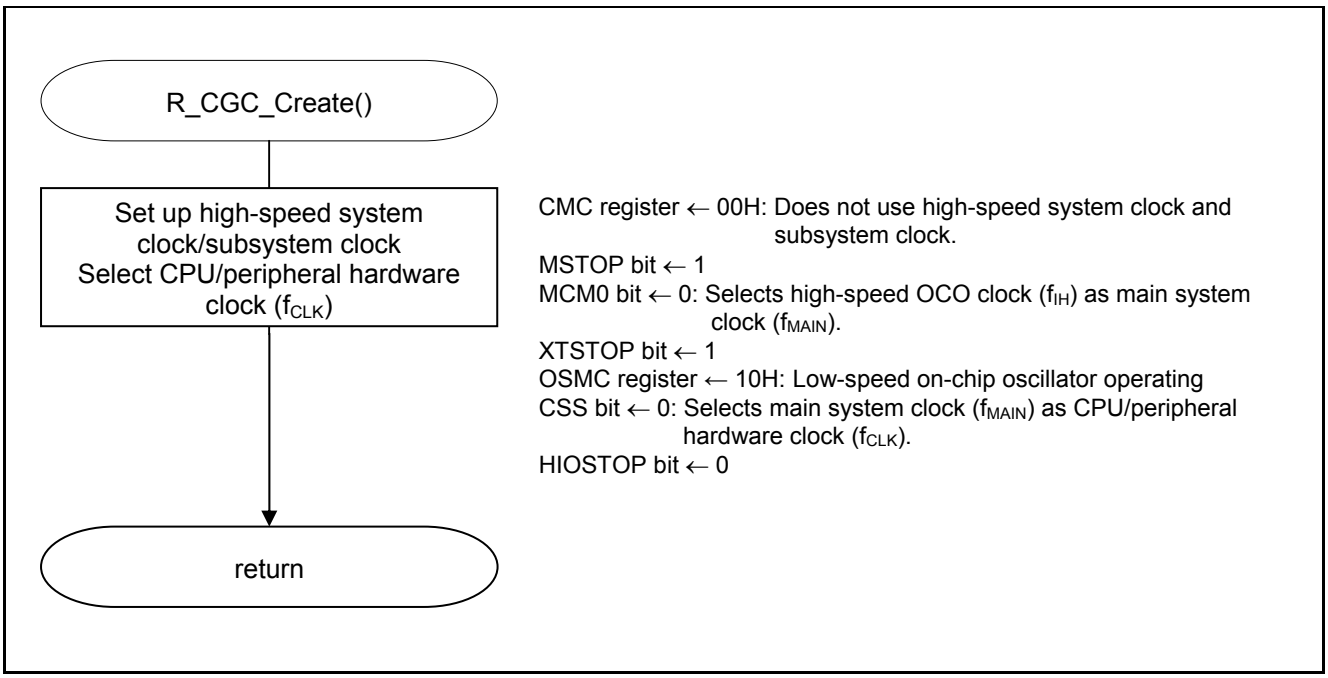

Figure 5.5 CPU Clock Setup

Caution: For details on the procedure for setting up the CPU clock (R_CGC_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E).

5.6.5 Timer Array Unit Setup

Figure 5.6 and 5.7 show the flowchart for setting up the timer array unit.

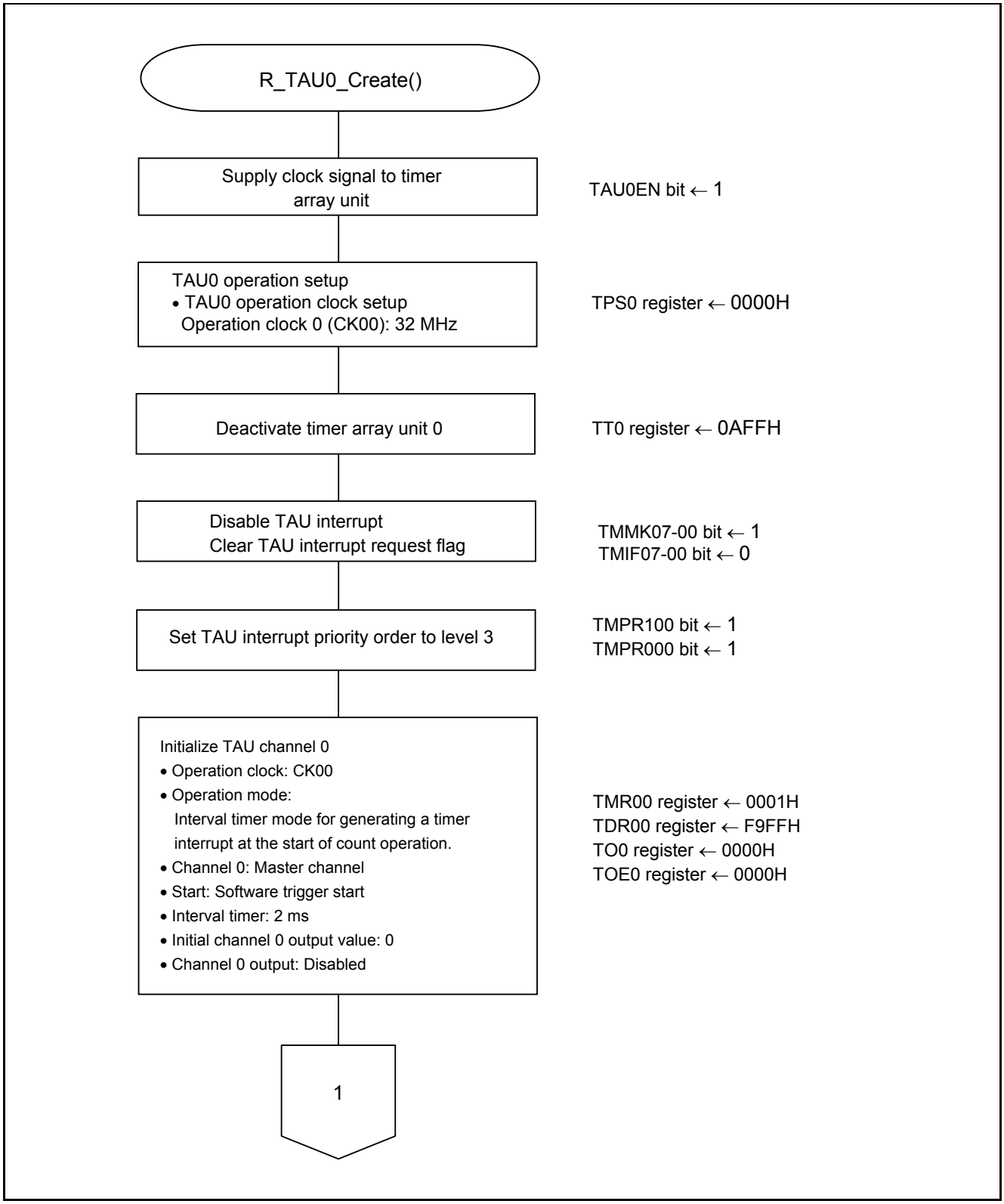

Figure 5.6 Timer Array Unit Setup (1/2)

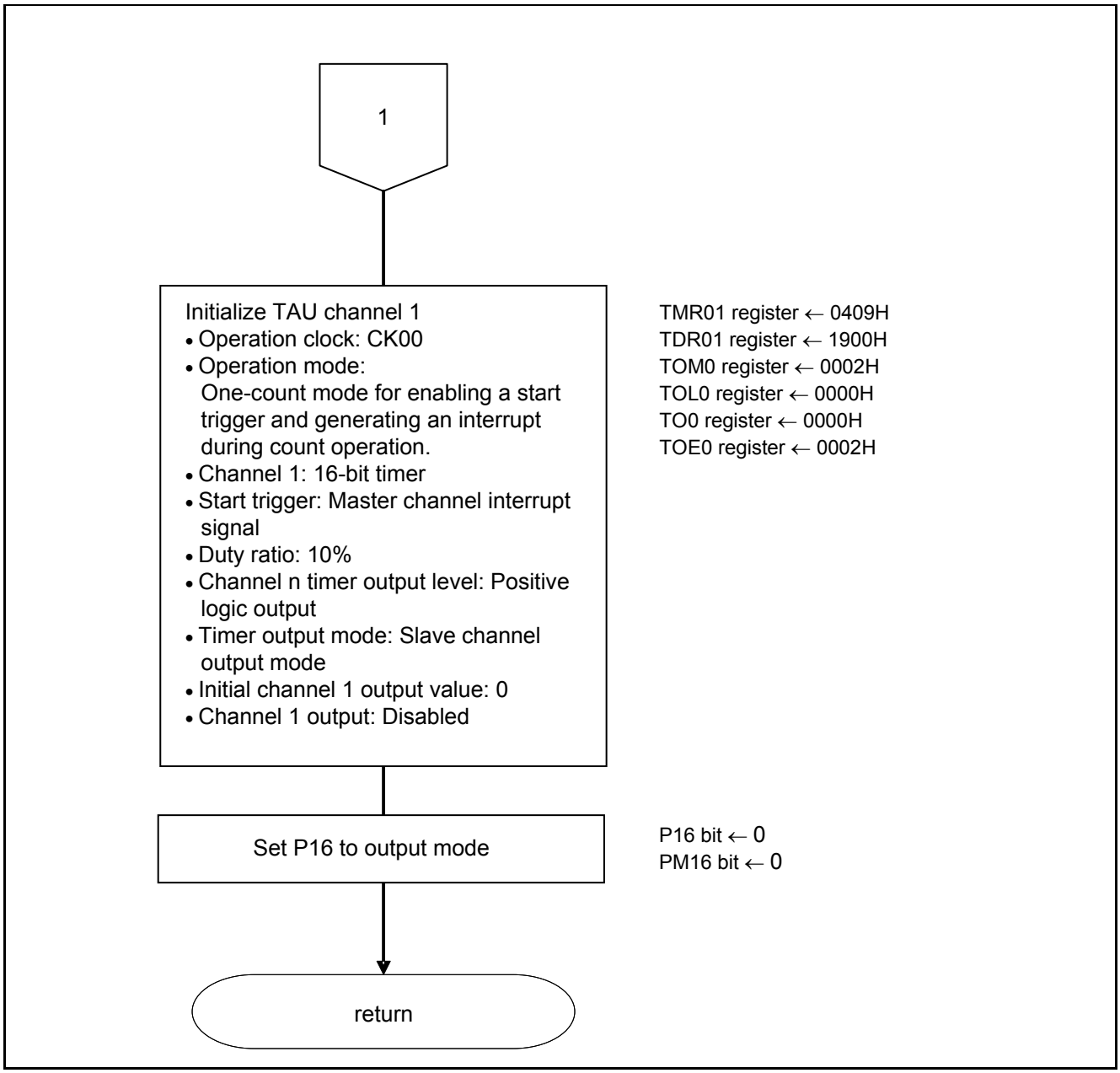

Figure 5.7 Timer Array Unit Setup (2/2)

Starting clock signal supply to the timer array unit 0

- Peripheral enable register 0 (PER0)
  Start clock signal supply to the timer array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
x	x	x	x	x	x	x	**1**

Bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Configuring the timer clock frequency

- Timer clock select register 0 (TPS0)
  Select an operation clock for timer array unit 0.

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS 031	PRS 030	0	0	PRS 021	PRS 020	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
x	x	x	x	x	x	x	x	x	x	x	x	**0**	**0**	**0**	**0**

Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000		Operation clock (CK00) selection				
					f_{CLK}= 2 MHz	f_{CLK}= 5 MHz	f_{CLK}= 10 MHz	f_{CLK}= 20 MHz	f_{CLK}= 32 MHz
0	**0**	**0**	**0**	**f_{CLK}**	2 MHz	5 MHz	10 MHz	20 MHz	**32 MHz**
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	16 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	8 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	4 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz	2 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156.2 kHz	312.5 kHz	625 kHz	1 MHz
0	1	1	0	$f_{CLK}/2^6$	31.25 kHz	78.1 kHz	156.2 kHz	312.5 kHz	500 kHz
0	1	1	1	$f_{CLK}/2^7$	15.62 kHz	39.1 kHz	78.1 kHz	156.2 kHz	250 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	125 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.76 kHz	19.5 kHz	39.1 kHz	62.5 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.76 kHz	19.5 kHz	31.25 kHz
1	0	1	1	$f_{CLK}/2^{11}$	976 Hz	2.44 kHz	4.88 kHz	9.76 kHz	15.63 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	7.81 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	3.91 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.95 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	976 Hz

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the channel 0 operation mode

- Timer mode register 00 (TMR00)
  Select an operation clock (f_{MCK}).
  Select a count clock.
  Select a start trigger and capture trigger.
  Select a valid edge for timer input.
  Set up the operation mode.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS001	CKS000	0	CCS00	0	STS002	STS001	STS000	CIS001	CIS000	0	0	MD003	MD002	MD001	MD000
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**1**

Bits 15 and 14

CKS001	CKS000	Selection of operation clock (f_{MCK}) of channel 0
0	**0**	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
0	1	**Operation clock CK02 set by timer clock select register 0 (TPS0)**
1	0	**Operation clock CK01 set by timer clock select register 0 (TPS0)**
1	1	**Operation clock CK03 set by timer clock select register 0 (TPS0)**

Bit 12

CCS00	Selection of count clock (f_{TCLK}) of channel 0
0	**Operation clock (f_{MCK}) specified by the CKSmn0 and CKSmn1 bits**
1	Valid edge of input signal input from the TImn pin

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS001	CKS000	0	CCS00	0	STS002	STS001	STS000	CIS001	CIS000	0	0	MD003	MD002	MD001	MD000
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**1**

Bits 10 to 8

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 0
0	**0**	**0**	**Only software trigger start is valid (other trigger sources are unselected).**
0	0	1	**Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.**
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Bits 7 and 6

CIS001	CIS000	Selection of TI00 pin input valid edge
0	**0**	**Falling edge**
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS001	CKS000	0	CCS00	0	STS002	STS001	STS000	CIS001	CIS000	0	0	MD003	MD002	MD001	MD000
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**1**

Bits 3 to 0

MD003	MD002	MD001	MD000	Operation mode of channel 0	Related function	TCR counting operation
0	**0**	**0**	**1**/0	**Interval timer mode**	**Interval timer / Square wave output / Divider function / PWM output (master)**	**Counting down**
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The MD000 bit operation varies depending on the operation mode (see the table below)

Operation mode (Value set by the MD003 to MD001 bits) (see table above)	MD000	TCR counting operation
• **Interval timer mode (0, 0, 0)** • **Capture mode (0, 1, 0)**	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	**Timer interrupt is generated when counting is started (timer output also changes).**
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated, either.
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the channel 1 operation mode

- Timer mode register 01 (TMR01)
  Select an operation clock (f_{MCK}).
  Select a count clock.
  Select the 16/8-bit timer.
  Select a start trigger and capture trigger.
  Select a valid edge for timer input.
  Set up the operation mode.

Symbol: TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS011	CKS010	0	CCS01	SPLIT01	STS012	STS011	STS010	CIS011	CIS010	0	0	MD013	MD012	MD011	MD010
0	**0**	0	**0**	**0**	**1**	**0**	**0**	**0**	**0**	0	0	**1**	**0**	**0**	**1**

Bits 15 and 14

CKS011	CKS010	Channel 1 operation clock (f_{MCK}) selection
0	**0**	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
0	1	**Operation clock CK02 set by timer clock select register 0 (TPS0)**
1	0	**Operation clock CK01 set by timer clock select register 0 (TPS0)**
1	1	**Operation clock CK03 set by timer clock select register 0 (TPS0)**

Bit 12

CCS01	Selection of count clock (f_{TCLK}) of channel 1
0	**Operation clock (f_{MCK}) specified with the CKS010 and CKS011 bits**
1	Valid edge of the input signal from the TI01 pin

Bit 11

SPLIT01	Selection of 8 or 16-bit timer operation for channel 1
0	**Operates as 16-bit timer** **(Operates in independent channel operation function or as slave channel in simultaneous channel operation function.)**
1	Operates as 8-bit timer.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS011	CKS010	0	CCS01	SPLIT01	STS012	STS011	STS010	CIS011	CIS010	0	0	MD013	MD012	MD011	MD010
0	**0**	0	**0**	**0**	**1**	**0**	**0**	**0**	**0**	0	0	**1**	**0**	**0**	**1**

Bits 10 to 8

STS012	STS011	STS010	Setting of start trigger or capture trigger of channel 1
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	**Valid edge of the TI01 pin input is used as both the start trigger and capture trigger.**
0	1	0	Both the edges of the TI01 pin input are used as a start trigger and a capture trigger.
1	**0**	**0**	**Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).**
Others than above			Setting prohibited

Bits 7 and 6

CIS011	CIS010	Selection of TI01 pin input valid edge
0	**0**	**Falling edge**
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS011	CKS010	0	CCS01	SPLIT01	STS012	STS011	STS010	CIS011	CIS010	0	0	MD013	MD012	MD011	MD010
0	**0**	0	**0**	**0**	**1**	**0**	**0**	**0**	**0**	0	0	**1**	**0**	**0**	**1**

Bits 3 to 0

MD013	MD012	MD011	MD010	Operation mode of channel 1	Related function	TCR counting operation
0	**0**	**0**	1/**0**	Interval timer mode	**Interval timer / Square wave output / Divider function / PWM output (master)**	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	**0**	**0**	**1**/0	**One-count mode**	**Delay counter / One-shot pulse output / PWM output (slave)**	**Counting down**
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The MD010 bit operation varies depending on the operation mode (see the table below)

Operation mode (Value set by the MD013 to MD011 bits) (see table above)	MD010	TCR counting operation
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	**Start trigger is valid during counting operation.** **At that time, interrupt is also generated.**
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated, either.
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Configuring the PWM output pulse cycle time

- Timer data register 00 (TDR00)
  Configure the PWM output pulse cycle time.

Symbol: TDR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Pulse cycle time = (TDR00 setting + 1) x Count clock cycle time
2 [ms] = (1/32[MHz]) x (TDR00 setting + 1)

⇒ **TDR00 setting = 63999**

Configuring the PWM output duty ratio

- Timer data register 01 (TDR01)
  Configure the PWM output duty ratio.

Symbol: TDR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Duty ratio = (TDR01 setting)/(TDR00 setting + 1) x 100
10 [%] = (TDR01 setting)/(63999 + 1) x 100

⇒ **TDR01 setting = 6400**

Setting up the timer output mode

- Timer output mode register 0 (TOM0)
  Set up the timer output mode for each channel.

Symbol: TOM0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TOM07	TOM06	TOM05	TOM04	TOM03	TOM02	TOM01	0
0	0	0	0	0	0	0	0	x	x	x	x	x	x	**1**	0

Bit 1

TOM01	Channel 1 timer output mode control
0	Master channel output mode. (Output is toggled with the timer interrupt request signal (INTTM01).)
1	**Slave channel output mode. (Output is set with the master channel's timer interrupt request signal (INTTM01) and reset with the slave channel's timer interrupt request signal (INTTM0p).)**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Configuring the output level for the timer output pin

- Timer output level register 0 (TOL0)
  Configure the output level for the timer output pin for each channel.

Symbol: TOL0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TOL07	TOL06	TOL05	TOL04	TOL03	TOL02	TOL01	0
0	0	0	0	0	0	0	0	x	x	x	x	x	x	**0**	0

Bit 1

TOL01	Channel 1 timer output level control
0	**Positive logic output (active-high)**
1	Negative logic output (active-low)

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Configuring the output value for the timer output pin

- Timer output register 0 (TO0)
  Configure the output value for the timer output pin for each channel.

Symbol: TO0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TO07	TO06	TO05	TO04	TO03	TO02	TO01	TO00
0	0	0	0	0	0	0	0	x	x	x	x	x	x	**0**	x

Bit 1

TO01	Channel 1 timer output
0	**Timer output value is 0**
1	Timer output value is 1

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Enabling the timer output

- Timer output enable register 0 (TOE0)
  Enable/disable the timer output for each channel.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TOE07	TOE06	TOE05	TOE04	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	0	0	x	x	x	x	x	x	**1**	**0**

Bit 1

TOE01	Timer output enable/disable of channel 1
0	The TO01 operation stopped by count operation (timer channel output bit). Writing to the TO01 bit is enabled. The TO01 pin functions as data output, and it outputs the level set to the TO01 bit. The output level of the TO01 pin can be manipulated be software.
1	**The TO01 operation enabled by count operation (timer channel output bit).** **Writing to the TO01 bit is disabled (writing is ignored).** **The TO01 pin functions as timer output, and the TOE01 bit is set or reset depending on the timer operation.** **The TO01 pin outputs the square-wave or PWM depending on the timer operation.**

Bit 0

TOE00	Timer output enable/disable of channel 0
0	**The TO00 operation stopped by count operation (timer channel output bit).** **Writing to the TO00 bit is enabled.** **The TO00 pin functions as data output, and it outputs the level set to the TO00 bit.** **The output level of the TO00 pin can be manipulated be software.**
1	The TO00 operation enabled by count operation (timer channel output bit). **Writing to the TO00 bit is disabled (writing is ignored).** **The TO00 pin functions as timer output, and the TOE00 bit is set or reset depending on the timer operation.** **The TO00 pin outputs the square-wave or PWM depending on the timer operation.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the PWM output pin

- Port mode register (PM1)
  Select the PM16 I/O mode.

Symbol: PM1

7	6	5	4	3	2	1	0
PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10
x	**0**	x	x	x	x	x	x

Bit 6

PM16	PM16 I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.6.6 Main Processing

Figure 5.8 shows the flowchart for Main Processing.

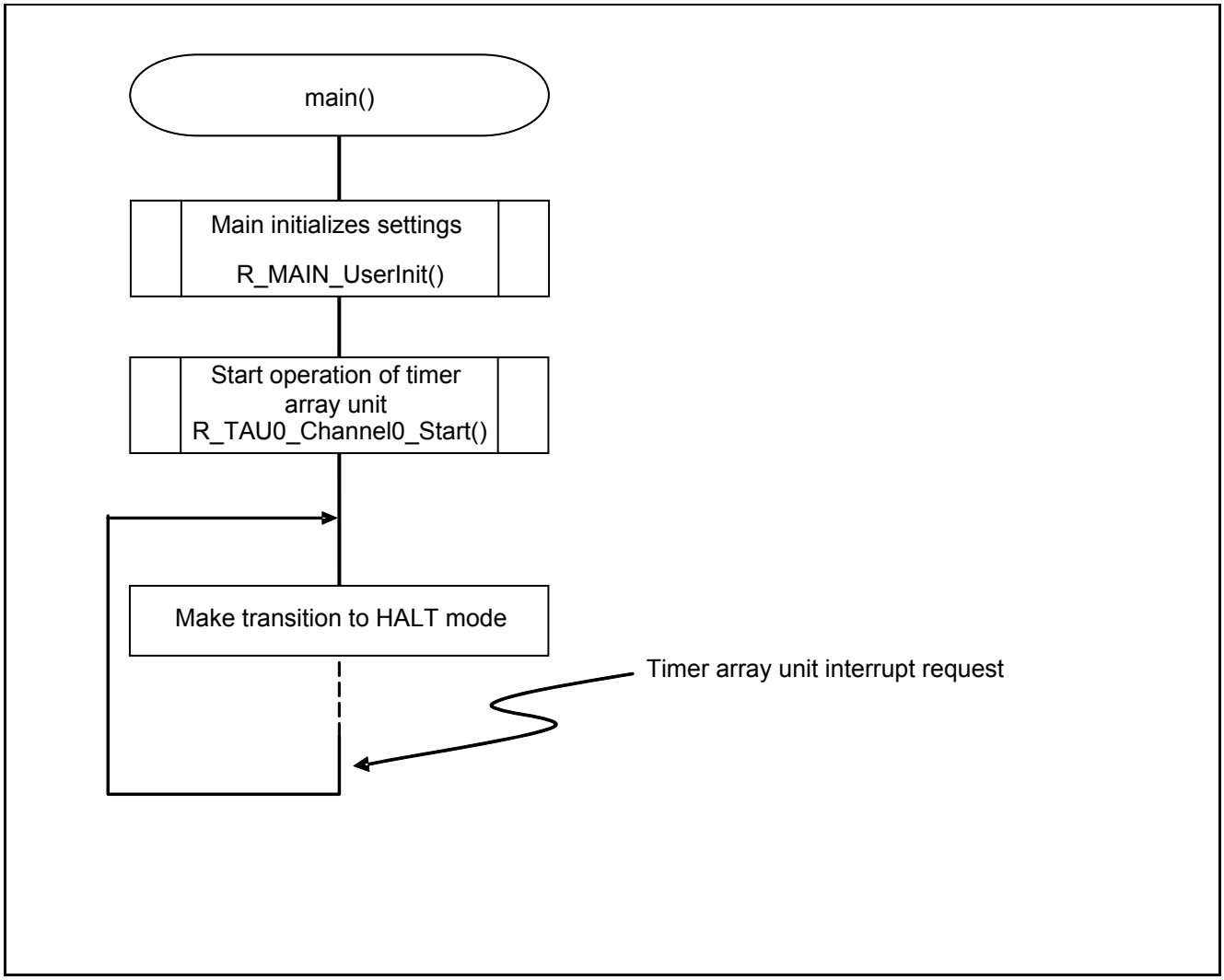

Figure 5.8 Main Processing

5.6.7 Main initializes settings

Figure 5.9 shows the flowchart for the main initializes settings.

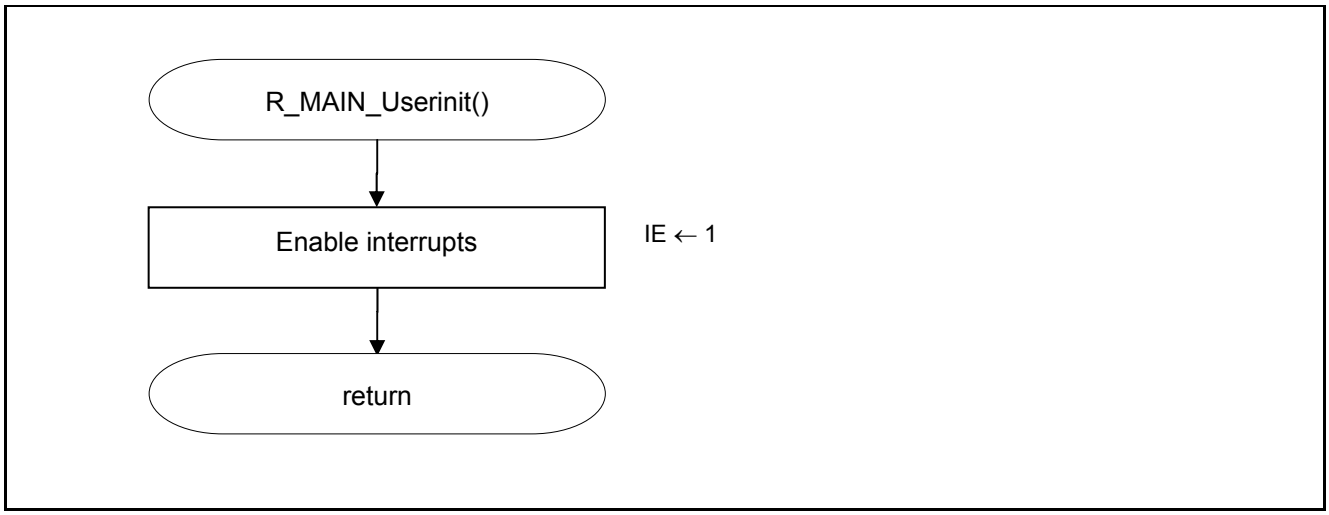

Figure 5.9 Main initializes settings

5.6.8 Timer Array Unit Startup

Figure 5.10 shows the flowchart for starting the operation of the timer array unit.

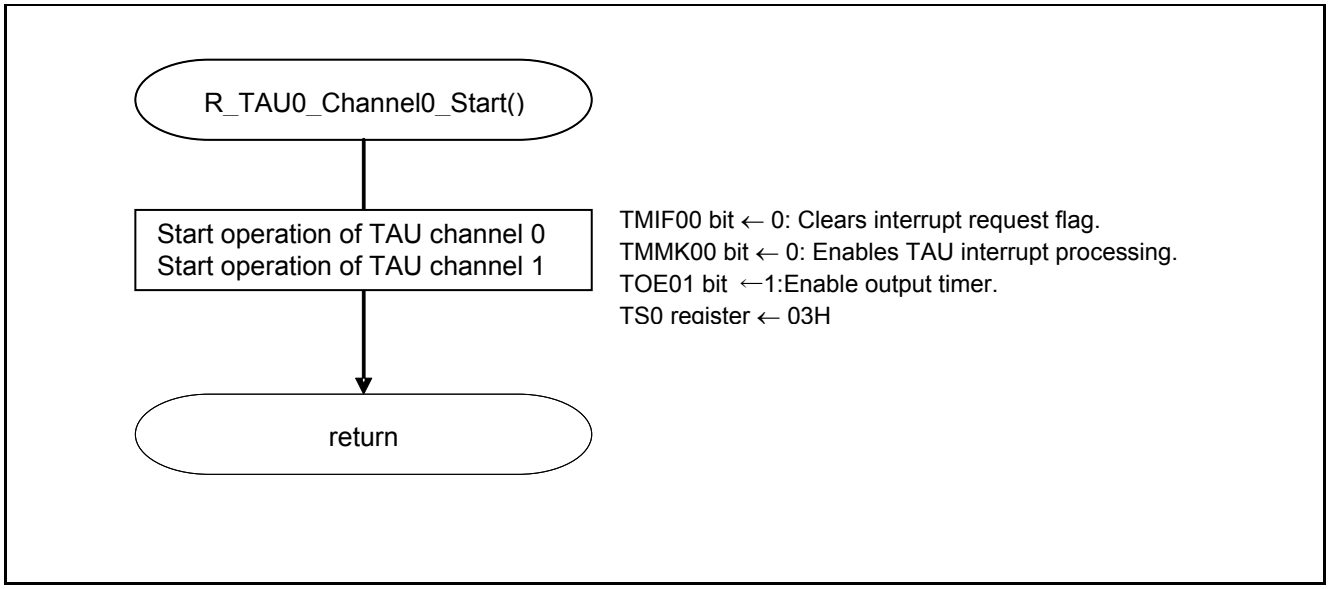

Figure 5.10 Timer Array Unit Startup

Configuring the timer count end interrupts

- Interrupt request flag register (IF1L)
  Clear the interrupt request flag.
- Interrupt mask flag register (MK1L)
  Mask interrupts.

Symbol: IF1L

7	6	5	4	3	2	1	0
TMIF03	TMIF02	TMIF01	TMIF00	IICAIF0	SREIF1 TMIF03H	SRIF1 CSIIF11 IICIF11	STIF1 CSIIF10 IICIF10
x	x	x	**0**	x	x	x	x

Bit 4

TMIF00	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK1L

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TMMK03	TMMK02	TMMK01	TMMK00	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
x	x	x	**0**	x	x	x	x

Bit 4

TMMK00	Interrupt processing control
0	**Enables interrupt processing.**
1	Disables interrupt processing.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Configuring the timer startup

- Timer channel start register 0 (TS0)
  Enable count operation of channel 0 and channel 1.

Symbol: TS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TSH03	0	TSH01	0	TS08	TS06	TS05	TS04	TS03	TS02	TS01	TS00
0	0	0	0	x	0	x	0	x	x	x	x	x	x	**1**	**1**

Bit 1

TS01	Operation enable (start) trigger of channel 1
0	No trigger operation
1	**The TE01 bit is set to 1 and the count operation becomes enabled.** **The TCR01 register count operation start in the count operation enabled state varies depending on each operation mode.**

Bit 0

TS00	Operation enable (start) trigger of channel 0
0	No trigger operation
1	**The TE00 bit is set to 1 and the count operation becomes enabled.** **The TCR00 register count operation start in the count operation enabled state varies depending on each operation mode.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.6.9 INTTM0 Interrupt Processing

Figure 5.11 shows the flowchart for INTTM0 interrupt processing.

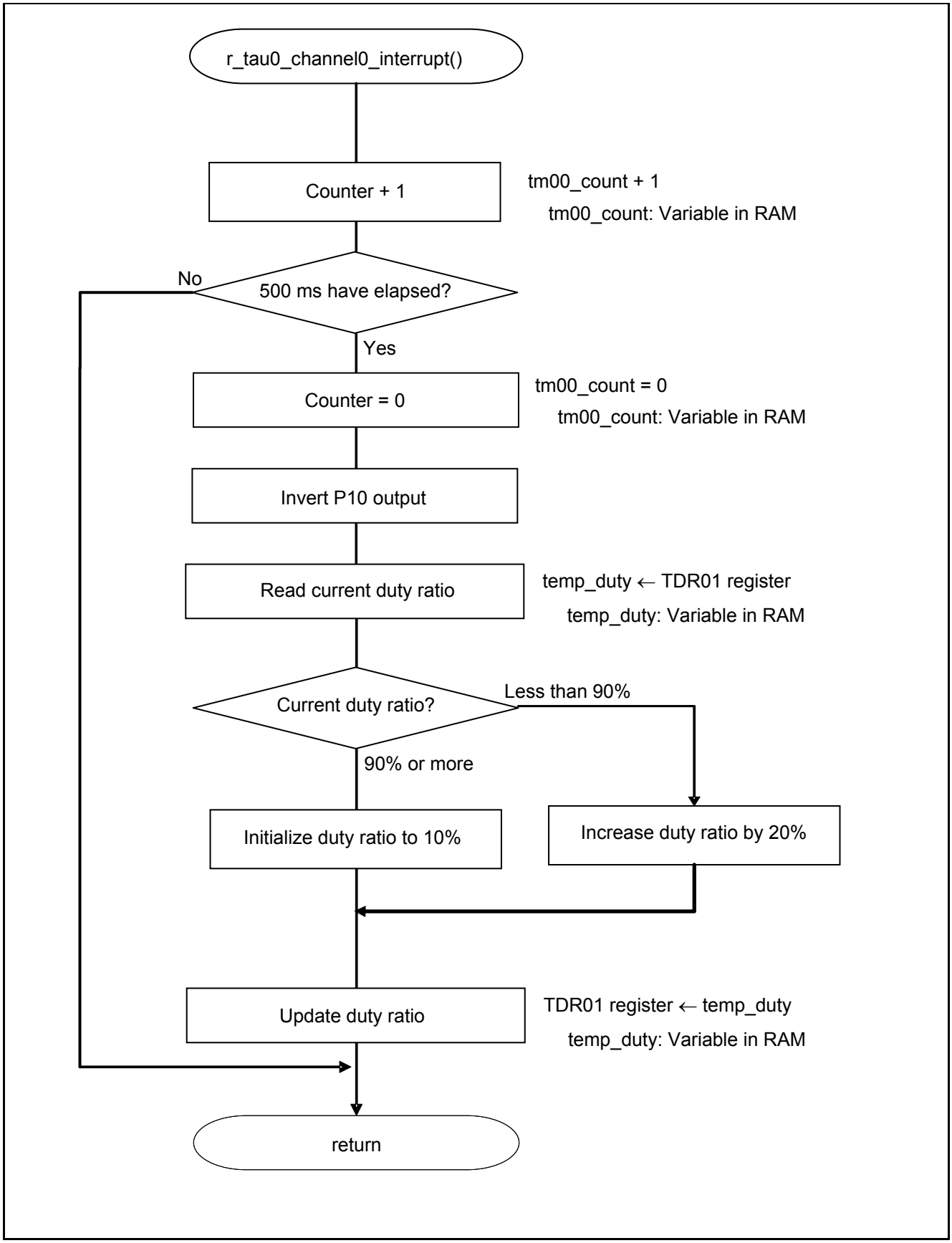

Figure 5.11 INTTM0 Interrupt Service Routine

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

User's Manual:

RL78/G13 User's Manual: Hardware (R01UH0146E)

RL78 Family User's Manual: Software (R01US0015E)

The latest version can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	RL78/G13 Timer Array Unit (PWM Output) CC-RL

Rev.	Date	Description	
		Page	Summary
1.00	Jun. 01, 2015	—	First edition issued
2.00	July 01, 2015	5	Table2.1: Added e^2 studio

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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