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# RL78/G13

R01AN1358EJ0110

Rev. 1.10

## Self-Programming (Received Data via IIC)

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June 01, 2016

### Introduction

This application note gives the outline of flash memory reprogramming using a self-programming technique. In this application note, flash memory is reprogrammed using the flash memory self-programming library Type01. The reprogramming data is received via IIC.

The sample program described in this application note limits the target of reprogramming to the boot area. For details on the procedures for performing self-programming and for reprogramming the entire area of code flash memory, refer to RL78/G13 Microcontroller Flash Memory Self-Programming Execution (R01AN0718E) Application Note.

### Target Device

RL78/G13

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

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## 1. Specifications

This application note explains a sample program that performs flash memory reprogramming using a self-programming library.

The sample program displays the information about the current version of the library on the LCD. Subsequently, the program receives data (reprogramming data) from the sending side and, after turning on the LED indicating that it is accessing flash memory, carries out self-programming to rewrite the code flash memory with the reprogramming data. When the rewrite is completed, the sample program turns off the LED and displays the information about the new version on the LCD.

Table 1.1 lists the peripheral functions to be used and their uses.

**Table 1.1 Peripheral Functions to be Used and their Uses**

Peripheral Function	Use
Serial interface IICA	Receives data via IIC.
Port I/O	Displays text on the LCD. Turns on and off the LED.

### 1.1 Outline of the Flash Memory Self-Programming Library

The flash memory self-programming library is a software product that is used to reprogram the data in the code flash memory using the firmware installed on the RL78 microcontroller.

The contents of the code flash memory can be reprogrammed by calling the flash memory self-programming library from a user program.

To do flash memory self-programming, it is necessary for the user program to perform initialization for flash memory self-programming and to execute the C or assembler functions that correspond to the library functions to be used.

### 1.2 Code Flash Memory

The configuration of the RL78/G13 (R5F100LE) code flash memory is shown below.

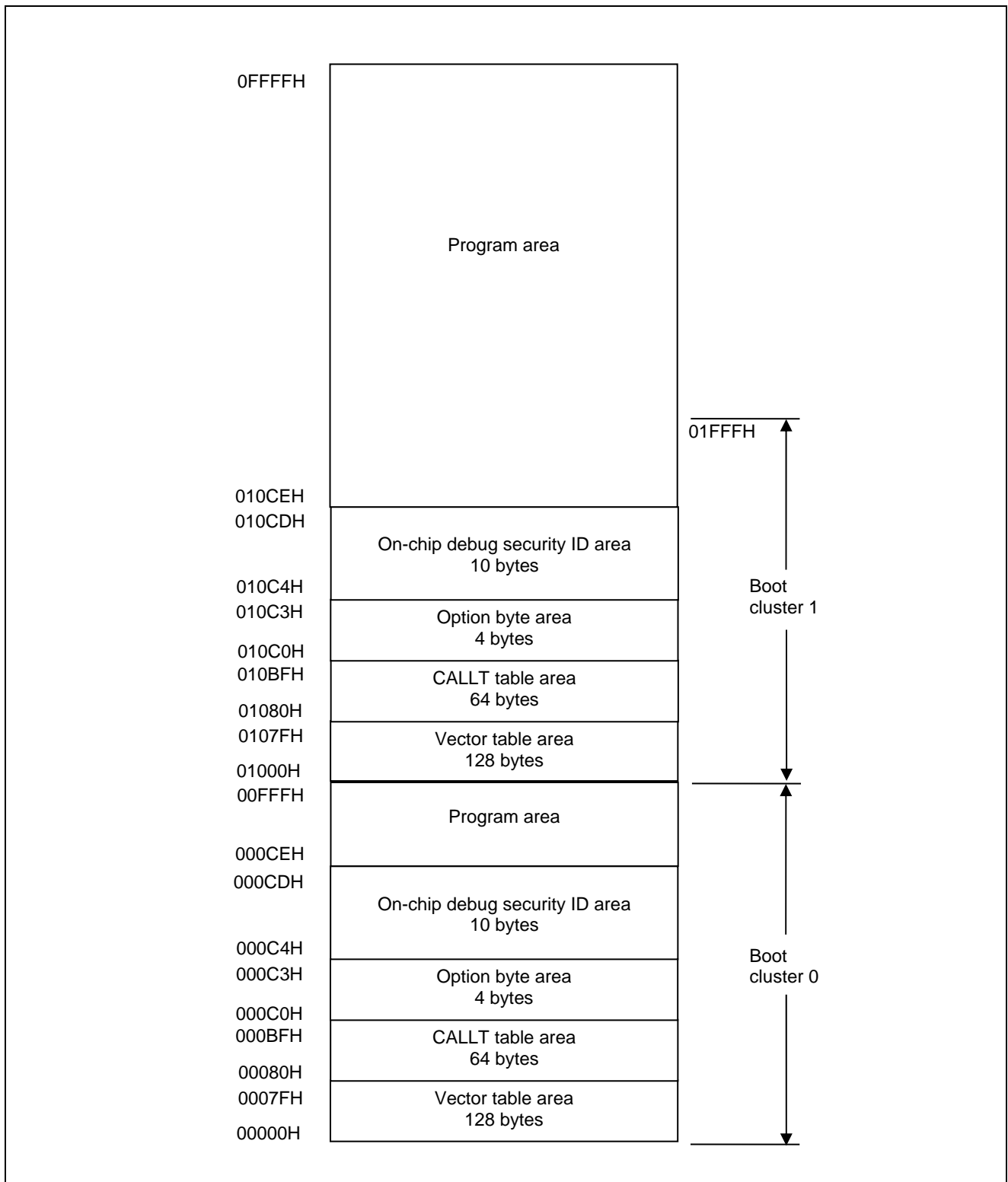


Figure 1.1 Code Flash Memory Configuration

Caution: When the boot swap function is used, the option byte area (000C0H to 000C3H) in boot cluster 0 is swapped with the option byte area (010C0H to 010C3H) in boot cluster 1. Accordingly, place the same values in the area (010C0H to 010C3H) as those in the area (000C0H to 000C3H) when using the boot swap function.

The features of the RL78/G13 code flash memory are summarized below.

**Table 1.2 Features of the Code Flash Memory**

Item	Description
Minimum unit of erasure and verification	1 block (1024 bytes)
Minimum unit of programming	1 word (4 bytes)
Security functions	Block erasure, programming, and boot area reprogramming protection are supported. (They are enabled at shipment)
	It is possible to disable reprogramming and erasure outside the specified window only at flash memory self-programming time using the flash shield window.
	Security settings programmable using the flash memory self-programming library

Caution: The boot area reprogramming protection setting and the security settings for outside the flash shield window are disabled during flash memory self-programming.

### 1.3 Flash Memory Self-Programming

The RL78/G13 is provided with a library for flash memory self-programming. Flash memory self-programming is accomplished by calling functions of the flash memory self-programming library from the reprogramming program.

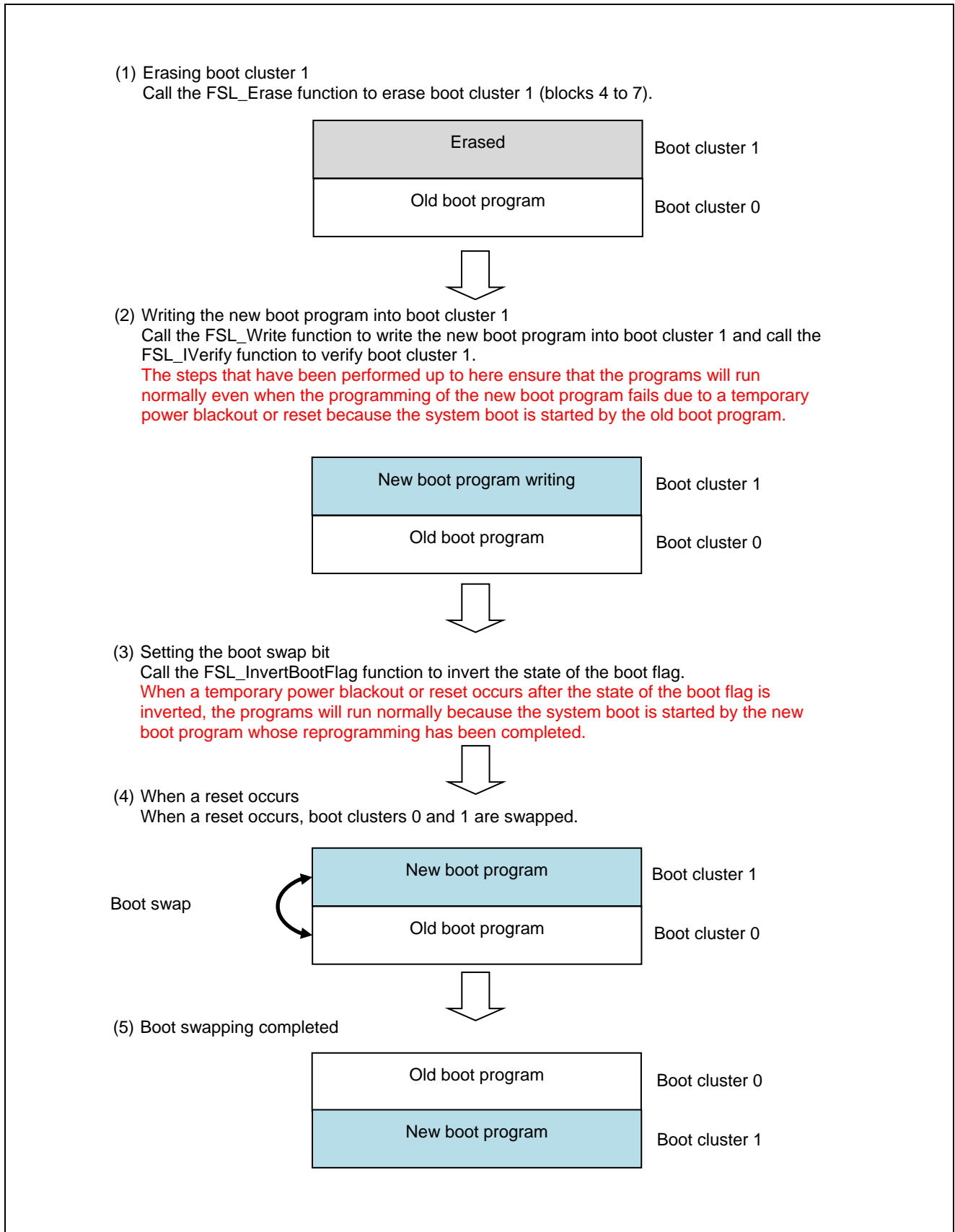
The flash memory self-programming library for the RL78/G13 controls flash memory reprogramming using a sequencer (a dedicated circuit for controlling flash memory). The code flash memory cannot be referenced while control by the sequencer is in progress. When the user program needs to be run while the sequencer control is in progress, therefore, it is necessary to relocate part of the segments for the flash memory self-programming library and the reprogramming program in RAM when erasing or reprogramming the code flash memory or making settings for the security flags. If there is no need to run the user program while the sequencer control is in progress, it is possible to keep the flash memory self-programming library and reprogramming program on ROM (code flash memory) for execution.

#### 1.3.1 Boot Swap Function

When reprogramming of the area where vector table data, the basic functions of the program, and flash memory self-programming library are allocated fails due to a temporary power blackout or a reset caused by an external factor, the data that is being reprogrammed will be corrupted, as the result of which the restarting of the user program or reprogramming cannot be accomplished when a reset is subsequently performed. This problem is avoided by the introduction of the boot swap function.

The boot swap function swaps between boot cluster 0 which is the boot program area and boot cluster 1 which is the target of boot swapping. A new program is written into boot cluster 1 before reprogramming is attempted. This boot cluster 1 is swapped with boot cluster 0 and boot cluster 1 is designated as the boot program area. In this configuration, even when a temporary power blackout occurs while the boot program area is being reprogrammed, the system boot will start at boot cluster 1 on the next reset start, thus ensuring the normal execution of the programs.

The outline image of boot swapping is shown in the figure below.



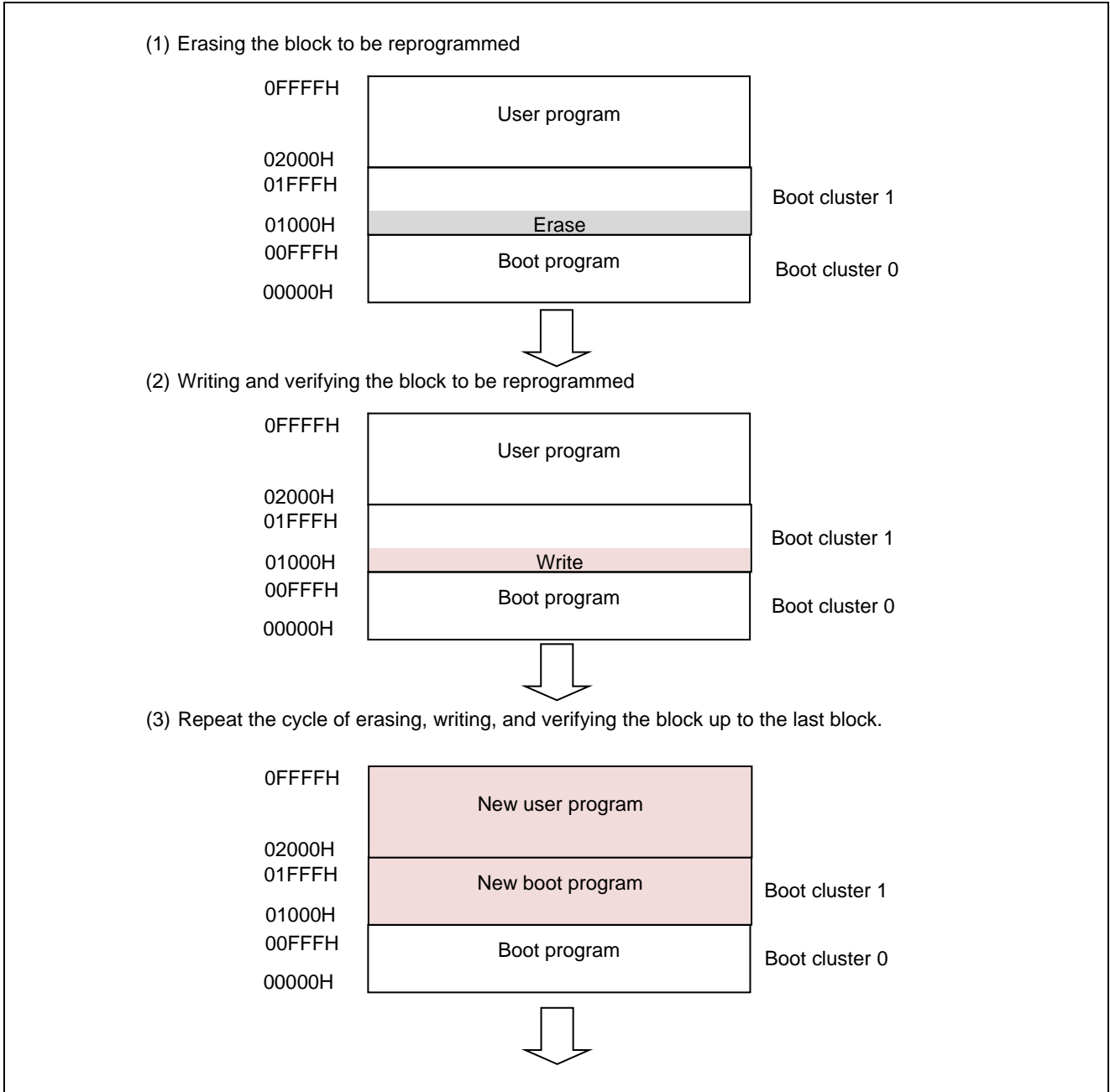
**Figure 1.2 Outline of Boot Swapping**



### 1.3.2 Flash Memory Reprogramming

This subsection describes the outline image of reprogramming using the flash memory self-programming technique. The program that performs flash memory self-programming is placed in boot cluster 0.

The sample program covered in this application note limits the target of reprogramming to the boot area. For details on the procedures for perform self-programming and for reprogramming the entire area of code flash memory, refer to RL78/G13 Microcontroller Flash Memory Self-Programming Execution (R01AN0718E) Application Note.



**Figure 1.3 Outline of Flash Memory Reprogramming (1/2)**

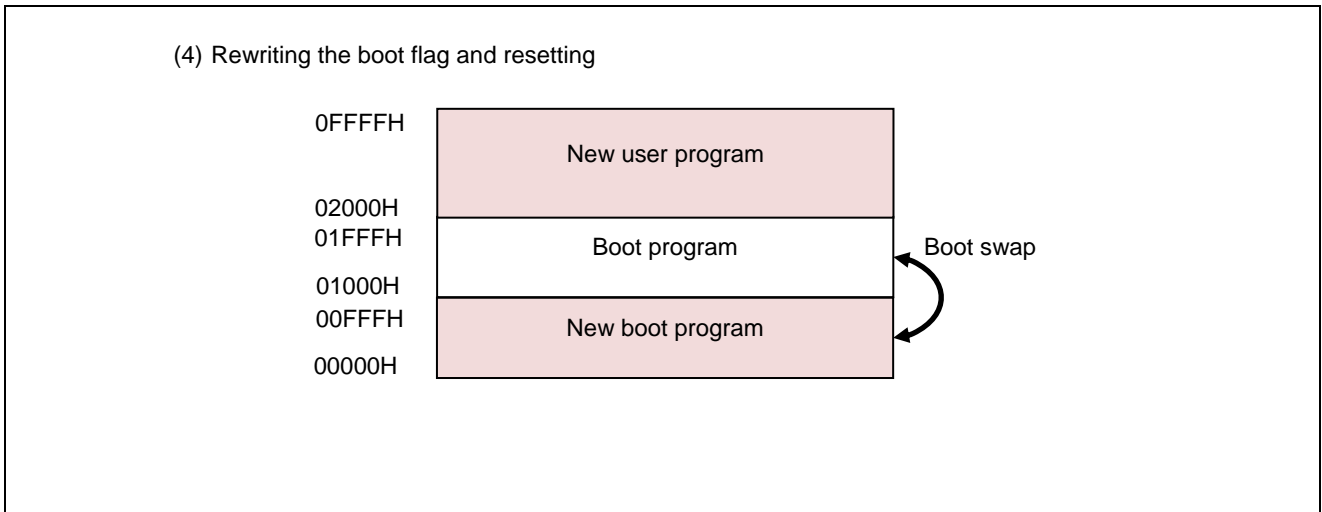


Figure 1.4 Outline of Flash Memory Reprogramming (2/2)

### 1.3.3 Flash Shield Window

The flash shield window is one of security mechanisms used for flash memory self-programming. It disables the write and erase operations on the areas outside the designated window only during flash memory self-programming.

The figure below shows the outline image of the flash shield window on the area of which the start block is 08H and the end block is 1FH.

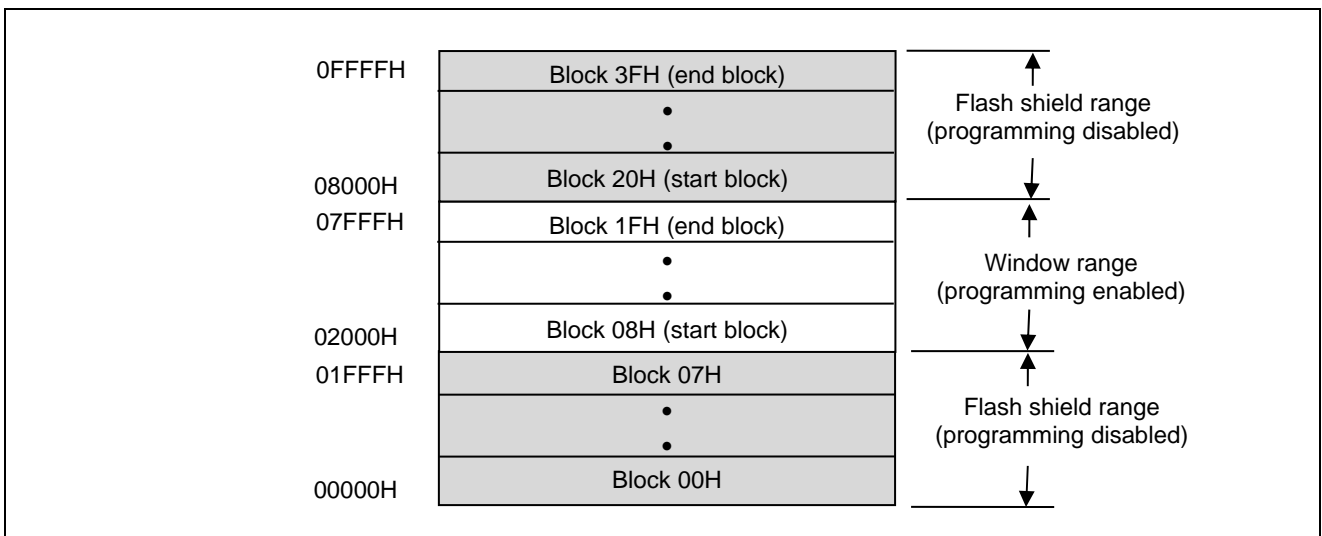


Figure 1.5 Outline of the Flash Shield Window

## 1.4 How to Get the Flash Memory Self-Programming Library

Before compiling the sample program, please download the latest flash self-programming library and copy the library files to the following folder below “Workspace”.

incl78 folder : fsl.h, fsl.inc, fsl\_types.h

lib78 folder : fsl.lib

The flash memory self-programming library is available on the Renesas Electronics Website.

Please contact your local Renesas Electronics sales office or distributor for more information.

## 2. Operation Check Conditions

The sample code described in this application note has been checked under the conditions listed in the table below.

**Table 2.1 Operation Check Conditions**

Item	Description
Microcontroller used	RL78/G13 (R5F100LEA)
Operating frequency	<ul style="list-style-type: none"> <li>High-speed on-chip oscillator (HOCO) clock: 32 MHz</li> <li>CPU/peripheral hardware clock: 32 MHz</li> </ul>
Operating voltage	5.0 V (Operation is possible over a voltage range of 2.9 V to 5.5 V.) LVD operation ( $V_{LVD}$ ): Reset mode which uses 2.81 V (2.76 V to 2.87 V)
Integrated development environment	CS+ V3.02.00 from Renesas Electronics Corp.
C compiler	CA78K0R V1.72 from Renesas Electronics Corp.
Board to be used	Renesas Starter Kit for RL78/G13 (R0K50100LS000BE)
Flash memory self-programming library (Type, Ver)	FSLRL78 Type01, Ver 2.20 <sup>Note</sup>

Note: Use and evaluate the latest version.

## 3. Related Application Notes

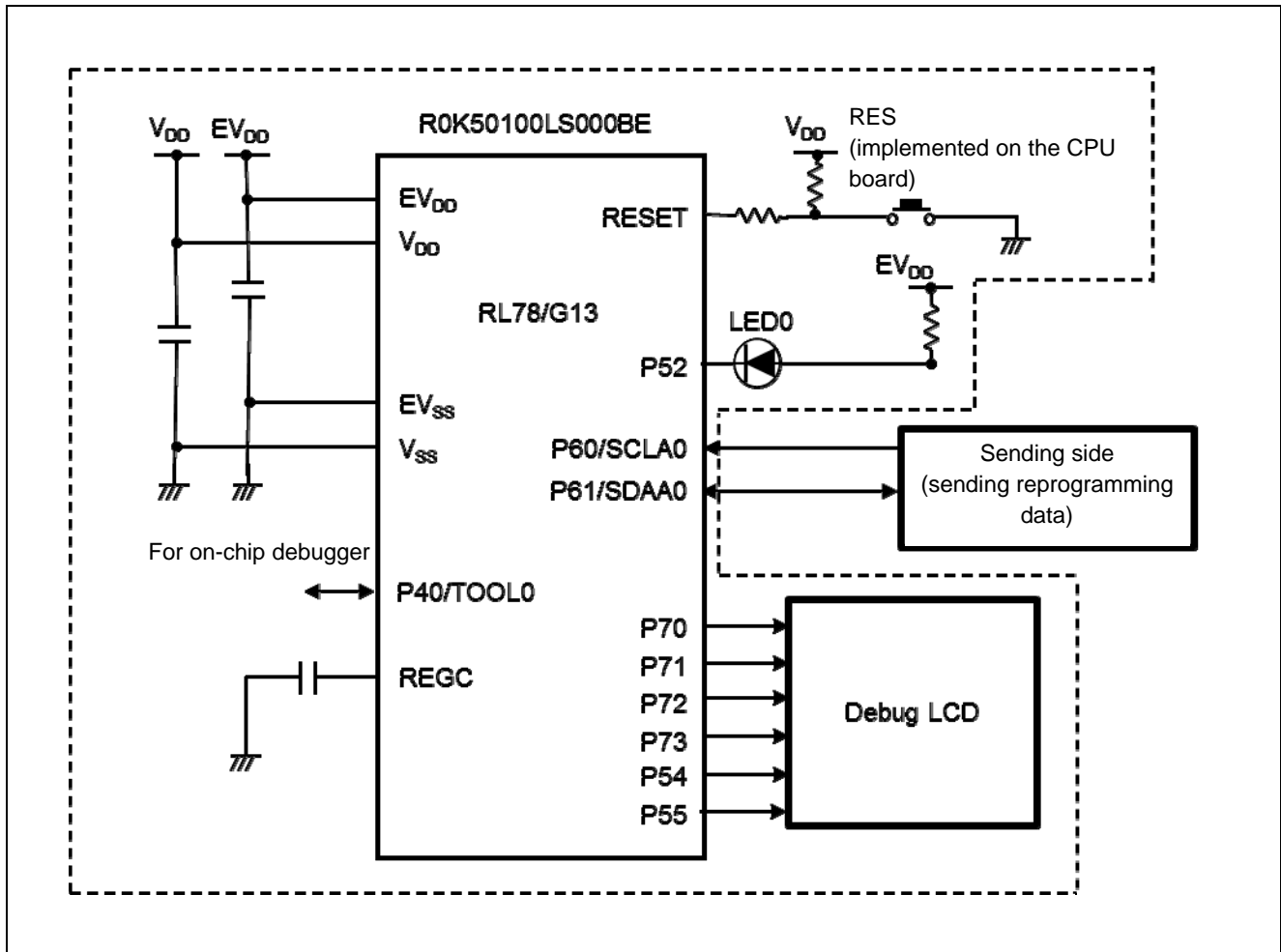
The application notes that are related to this application note are listed below for reference.

- RL78/G13 Initialization (R01AN0451E) Application Note
- RL78/G13 Serial Interface IICA (for Master Transmission/Reception) (R01AN0462E) Application Note
- RL78/G13 Serial Interface IICA (for Slave Transmission/Reception) (R01AN0463E) Application Note
- RL78 Microcontroller Flash Memory Self-Programming Library Type01 (R01AN0350E) Application Note

## 4. Description of the Hardware

### 4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration used for this application note.



**Figure 4.1 Hardware Configuration**

- Cautions:
1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V<sub>DD</sub> or V<sub>SS</sub> via a resistor).
  2. V<sub>DD</sub> must be held at not lower than the reset release voltage (V<sub>LVD</sub>) that is specified as LVD.

## 4.2 List of Pins to be Used

Table 4.1 lists pins to be used and their functions.

**Table 4.1 Pins to be Used and their Functions**

Pin Name	I/O	Description
P60/SCLA0	Input	IIC serial clock output pin
P61/SDAA0	Input/Output	IIC serial data I/O pin
P52	Output	LED0 (indicating flash memory access status) on/off control
P54	Output	Debug LCD control
P55	Output	Debug LCD control
P70/KR0/SCK21/SCL21	Output	Debug LCD control
P71/KR1/SI21/SDA21	Output	Debug LCD control
P72/KR2/SO21	Output	Debug LCD control
P73/KR3/SO01	Output	Debug LCD control

## 5. Description of the Software

### 5.1 Communication Specifications

The sample program covered in this application note receives reprogramming data via the IIC bus for flash memory self-programming. The sending side sends three commands, i.e., the START, WRITE, and END commands. When the sample program completes the reception of a command, it places the IIC bus in the wait state, takes actions according to the command it received, and, if the command terminates normally, releases the IIC bus from the wait state and receives the next command. If the command terminates abnormally, the program keeps the IIC bus in the wait state, displays "ERROR!" on the LCD, and suppresses the execution of the subsequent operations. This section describes the necessary IIC communication settings and the specifications for the commands.

**Table 5.1 IIC Communication Settings**

Local address	0xA0
Operation mode	Standard (100 KHz)

#### 5.1.1 START Command

When the sample program receives the START command, it places the IIC bus in the wait state and performs initialization processing for flash memory self-programming. When the command terminates normally, the program releases the IIC bus from the wait state. In the case of an abnormal termination, the sample program displays "ERROR!" on the LCD and suppresses the execution of the subsequent operations.

START code (0x01)	Data length (0x0002)	Command (0x02)	Data (None)	Checksum (1 byte)
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#### 5.1.2 WRITE Command

When the sample program receives the WRITE command, it places the IIC bus in the wait state, writes the data it received into flash memory, and performs verify processing each time it completes the write of one block. The sample program releases the IIC bus from the wait state on normal termination of the command. In the case of an abnormal termination, the sample program displays "ERROR!" on the LCD and suppresses the execution of the subsequent operations.

START code (0x01)	Data length (0x0102)	Command (0x03)	Data (256 bytes)	Checksum (1 byte)
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#### 5.1.3 END Command

When the sample program receives the END command, it places the IIC bus in the wait state and performs verify processing on the block that is currently being written. If the verification terminates normally, the program inverts the state of the boot flag, then generates a reset for boot swapping. In the case of an abnormal termination, the sample program displays "ERROR!" on the LCD and suppresses the execution of the subsequent operations.

START code (0x01)	Data length (0x0002)	Command (0x04)	Data (None)	Checksum (1 byte)
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\* The checksum is the sum of the command and data fields in units of bytes.

### 5.1.4 Communication Sequence

This sample program takes actions according to the sequence described below upon receipt of a command from the sending side.

(1) Sending side:

Sends the START command.

(2) Sample program:

Places the IIC bus in the wait state and turns on LED1 which indicates that flash memory is being accessed. The program then performs initialization for flash memory self-programming and releases the IIC bus from the wait state upon normal termination.

(3) Sending side:

Sends the WRITE command and reprogramming data (256 bytes).

(4) Sample program:

Places the IIC bus in the wait state and writes the data it received into the code flash memory. The write address starts at 0x1000 (start of boot cluster 1). Subsequently, it is incremented by the receive data size (size of reprogramming data: 256 bytes) each time the sample program receives the WRITE command and reprogramming data.

The program performs verify processing when the rewrite of 1 block (1024 bytes) is completed.

When all of these steps terminate normally, the sample program releases the IIC bus from the wait state.

(5) Steps (3) and (4) are repeated until the reprogramming of all data is completed.

(6) Sending side:

Sends the END command.

(7) Sample program:

Places the IIC bus in the wait state and performs verify processing on the block that is currently subjected to reprogramming. The program then inverts the state of the boot flag, and generates a reset after turning off LED0 which indicates that flash memory is being accessed.



## 5.2 Operation Outline

This application note explains a sample program that performs flash memory reprogramming using a self-programming library.

The sample program displays the information about the current version of the library on the LCD. Subsequently, the program receives data (reprogramming data) from the sending side and, after turning on the LED indicating that it is accessing flash memory, carries out self-programming to rewrite the code flash memory with the reprogramming data. When reprogramming is completed, the sample program turns off the LED and displays the information about the new version on the LCD.

### (1) Initializes the IICA serial interface.

<Setting conditions>

- Sets the operation mode to standard.
- Sets the transfer clock to 100 KHz.
- Sets the local address to 0xA0.
- Sets up interrupts so that an interrupt occurs on every ninth clock.
- Disables interrupt requests to be generated on detection of the stop condition.

### (2) Sets up the I/O port.

<Setting conditions>

- LED on/off control port (LED0): Sets P52 for output.

### (3) Disables interrupts.

### (4) Initializes the LCD and displays on the LCD the string that is set to the constant LCD\_STRING.

### (5) Enters the HALT mode and waits for data from the sending side.

### (6) Switches into the normal operation mode from the HALT mode upon an IICA0 transfer end interrupt request.

### (7) Upon receipt of an address and transfer direction information from the sending side, places the IIC bus in the wait state and checks the transfer direction.

- When the master sends data to the slave, it clears the receive end interrupt request flag and releases the IIC bus from the wait state.
- When the master receives data from the slave, it displays "ERROR!" on the LCD and suppresses the execution of the subsequent operations.

- (8) Upon receipt of a START command (0x02) from the sending side, places the IIC bus in the wait state and performs initialization for self-programming.**
- Sets P52 to the low level and turns on LED0 indicating that flash memory is being accessed.
  - Calls the FSL\_Init function to initialize the flash memory self-programming environment and makes the following settings:
    - Voltage mode : Full-speed mode
    - CPU operating frequency : 32 [MHz]
    - Status check mode : Status check internal mode
  - Calls the FSL\_Open function to start flash memory self-programming (starting the flash memory environment).
  - Calls the FSL\_PrepareFunctions function to make available the flash memory functions (standard reprogramming functions) that are necessary for the RAM executive.
  - Calls the FSL\_PrepareExtFunctions function to make available the flash memory functions (extended functions) that are necessary for the RAM executive.
  - Calls the FSL\_GetFlashShieldWindow function to get the start and end blocks of the flash shield window.
  - If the start block of the flash shield window is a block other than block 0 or if the end block is a block other than block 63, calls the FSL\_SetFlashShieldWindow function to set the start block of the flash shield window to block 0 and the end block to block 63.
- (9) Sets the write destination address to 0x1000 (start of boot cluster 1).**
- (10) Releases the IIC bus from the wait state and notifies the sending side of the transmission-enabled state.**
- (11) Receives the WRITE command (0x03) and reprogramming data (256 bytes).**
- (12) Places the IIC bus in the wait state and computes the reprogramming target block from the write destination address.**
- (13) Calls the FSL\_BlankCheck function to check whether the reprogramming target block has already been reprogrammed.**
- (14) If the reprogramming target block is reprogrammed, calls the FSL\_Erase function to erase the reprogramming target block.**
- (15) Calls the FSL\_Write function to write the received data at the write destination address.**
- (16) Adds the write size to the write destination address.**
- (17) Releases the IIC bus from the wait state and notifies the sending side of the transmission-enabled state.**
- (18) Receives the WRITE command and reprogramming data (256 bytes) or the END command (0x04).**
- (19) Repeats steps (15) to (18) until 1 block (1024 bytes) of programming is completed or an END command (0x04) is received from the sending side. Proceeds with the next step when 1 block (1024 bytes) of programming is completed or an END command (0x04) is received from the sending side.**
- (20) Calls the FSL\_IVerify function to verify the reprogramming target block.**
- (21) Repeats steps (12) to (20) unless an END command (0x04) is received from the sending side. Proceeds with the next step when an END command is received.**
- (22) Calls the FSL\_InvertBootFlag function to invert the state of the boot flag. Boots clusters 0 and 1 will then be swapped at reset time.**
- (23) Turns off LED0 indicating that flash memory is being accessed, then calls the FSL\_ForceReset function to generate an internal reset.**

Caution: When flash memory self-programming could not be terminated normally (error occurring during processing), the sample program displays "ERROR!" on the LCD and suppresses the execution of the subsequent operations.

### 5.3 File Configuration

Table 5.2 lists the additional functions for files that are automatically generated in the integrated development environment and other additional files.

**Table 5.2 List of Additional Functions and Files**

File Name	Outline	Remarks
r_main.c	Main module	Additional functions: R_MAIN_PacketAnalyze R_MAIN_SelfInitialize R_MAIN_SelfExecute R_MAIN_WriteExecute
r_cg_serial_user.c	SAU module	Additional functions: R_IICA0_CheckTransferDirection R_IICA0_ReceiveStart
lcd.c	DebugLCD module	Controls DebugLCD included in Renesas Starter Kit for RL78/G13.

## 5.4 List of Option Byte Settings

Table 5.3 summarizes the settings of the option bytes.

**Table 5.3 Option Byte Settings**

Address	Setting	Description
000C0H/010C0H	11101111B	Disables the watchdog timer. (Stops counting after the release from the reset status.)
000C1H/010C1H	01111111B	LVD reset mode 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger Erases the data in the flash memory when on-chip debug security ID authentication fails.

The option bytes of the RL78/G13 comprise the user option bytes (000C0H to 000C2H) and on-chip debug option byte (000C3H).

The option bytes are automatically referenced and the specified settings are configured at power-on time or the reset is released. When using the boot swap function for self-programming, it is necessary to set the same values that are set in 000C0H to 000C3H also in 010C0H to 010C3H because the bytes in 000C0H to 000C3H are swapped with the bytes in 010C0H to 010C3H.

## 5.5 On-chip Debug Security ID

The RL78/G13 has the on-chip debug security ID area allocated to addresses 000C4H to 000CDH of flash memory to preclude the memory contents from being sneaked by the unauthorized third party.

When using the boot swap function for self-programming, it is necessary to set the same values that are set in 000C4H to 000CDH also in 010C4H to 010CDH because bytes in 000C4H to 000CDH are swapped with the bytes in 010C4H to 010CDH.

### 5.6 Link Directive File

The reprogramming program that performs flash memory self-programming and the flash memory self-programming library are allocated to blocks 0 to 3 (boot cluster 0) by the link directive file. It is also used to make configuration so that the RAM area to be used by the flash memory self-programming library will not be used.

The outline of the link directive file that this sample program uses is shown below.

<pre> ***** ; ; Redefined ROM area ***** ; ; ; Define new memory entry for boot cluster 0 ; MEMORY ROM      : ( 000000H, 001000H ) ; ; Define new memory entry for write-data area ; MEMORY OCDROM   : ( 00FE00H, 000200H ) ; ***** ; ; Library(fsl.lib) segment ***** ; ; Merge FSL_FCD segment ; MERGE FSL_FCD   := ROM ; ; Merge FSL_FECD segment ; MERGE FSL_FECD := ROM ; ; Merge FSL_RCD segment ; MERGE FSL_RCD   := ROM ; ; Merge FSL_BCD segment ; MERGE FSL_BCD   := ROM ; ; Merge FSL_BECD segment ; MERGE FSL_BECD := ROM ; ***** ; ; Redefined RAM area ***** ; ; Define new memory entry for self-RAM ; MEMORY SELFRAM  : ( 0FEF00H, 00040AH ) ; ; Redefined default data segment RAM ; MEMORY RAM      : ( 0FF30AH, 000B16H ) ; ; Define new memory entry for saddr area ; MEMORY RAM_SADDR : ( 0FFE20H, 0001E0H ) ; ***** ; ; run-time library segment ( 0000H - FFFFH ) ***** ; ; Merge @@LCODE, @@LCODEL(run-time library) segment ; MERGE @@LCODE   := ROM MERGE @@LCODEL := ROM ; ; const segment ; ***** MERGE CNST_SEG := ROM </pre>	<div style="border: 1px solid red; padding: 5px; margin-bottom: 10px;"> <p>Code area definition The code is allocated to the boot area.</p> </div> <div style="border: 1px solid red; padding: 5px; margin-bottom: 10px;"> <p>OCD monitor area definition</p> </div> <div style="border: 1px solid red; padding: 5px; margin-bottom: 10px;"> <p>Allocates the flash memory self-programming library to the boot area.</p> </div> <div style="border: 1px solid red; padding: 5px; margin-bottom: 10px;"> <p>Defines so that the area to be used by the flash memory self-programming library will not be used as the standard RAM area.</p> </div> <div style="border: 1px solid red; padding: 5px; margin-bottom: 10px;"> <p>Standard RAM area definition</p> </div> <div style="border: 1px solid red; padding: 5px; margin-bottom: 10px;"> <p>Defines so that the area to be used by the flash memory self-programming library will not be used as the standard RAM area.</p> </div> <div style="border: 1px solid red; padding: 5px; margin-bottom: 10px;"> <p>Allocates the run-time library to the boot area.</p> </div> <div style="border: 1px solid red; padding: 5px;"> <p>Allocates the const variable to the boot area.</p> </div>
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## 5.7 List of Constants

Table 5.4 lists the constants for the sample program.

**Table 5.4 Constants for the Sample Program**

Constant	Setting	Description
LCD_DISPLAY	"Ver 1.0 "	String to be displayed on the LCD (version information)
ERR_DISPLAY	"ERROR! "	String to be displayed on the LCD at occurrence of error
NORMAL_END	0x00	Normal termination
ERROR	0xFF	Abnormal termination
NO_RECIEVE	0x00	Command reception state: Not received
START_CODE	0x01	Command reception state: START code received
PACKET_SIZE	0x02	Command reception state: Data length received
START	0x02	START command
WRITE	0x03	WRITE command
END	0x04	END command
FULL_SPEED_MODE	0x00	Argument to flash memory self-programming library initialization function: Set operation mode to full-speed mode.
FREQUENCY_32M	0x20	Argument to flash memory self-programming library initialization function: RL78/G13's operating frequency = 32 MHz
INTERNAL_MODE	0x01	Argument to flash memory self-programming library initialization function: Turn on status check internal mode.
START_BLOCK_NUM	0x00	Start block number of flash shield window
END_BLOCK_NUM	0x3F	End block number of flash shield window
BLOCK_SIZE	0x400	One block size of code flash memory (1024 bytes)
RXSIZE	0x102	Size of receive buffer

## 5.8 List of Variables

Table 5.5 lists the global variables that are used in this sample program.

**Table 5.5 Global Variables for the Sample Program**

Type	Variable Name	Contents	Function Used
__far const int8_t	display[]	String for display (Version information)	main() DisplayString()
__far const int8_t	Err[]	String for display (Error information)	main() DisplayString()

## 5.9 List of Functions

Table 5.6 lists the functions that are used in this sample program.

**Table 5.6 List of Functions**

Function Name	Outline
R_IICA0_CheckTransferDirection	Checks direction of data transfer via IICA0.
R_IICA0_ReceiveStart	Receives data via IICA0.
R_MAIN_PacketAnalyze	Analyzes receive data.
R_MAIN_SelfExecute	Executes flash memory self-programming.
R_MAIN_SelfInitialize	Executes initialization for flash memory self-programming.
R_MAIN_WriteExecute	Executes self-programming.

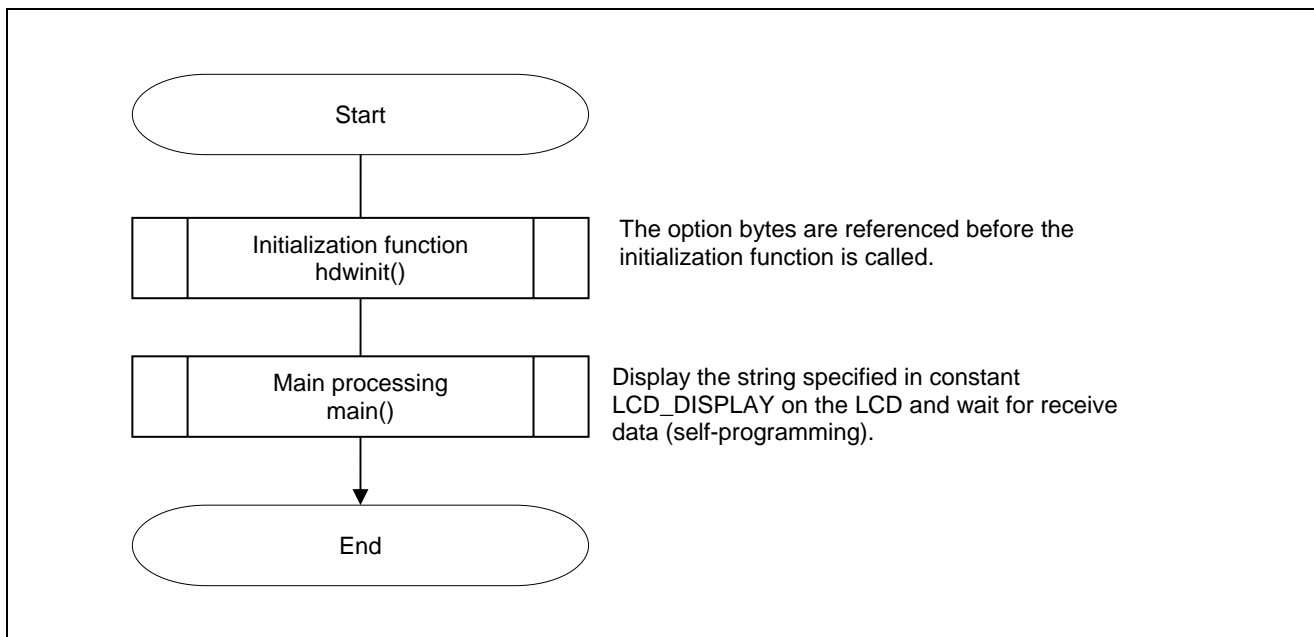






### 5.11 Flowcharts

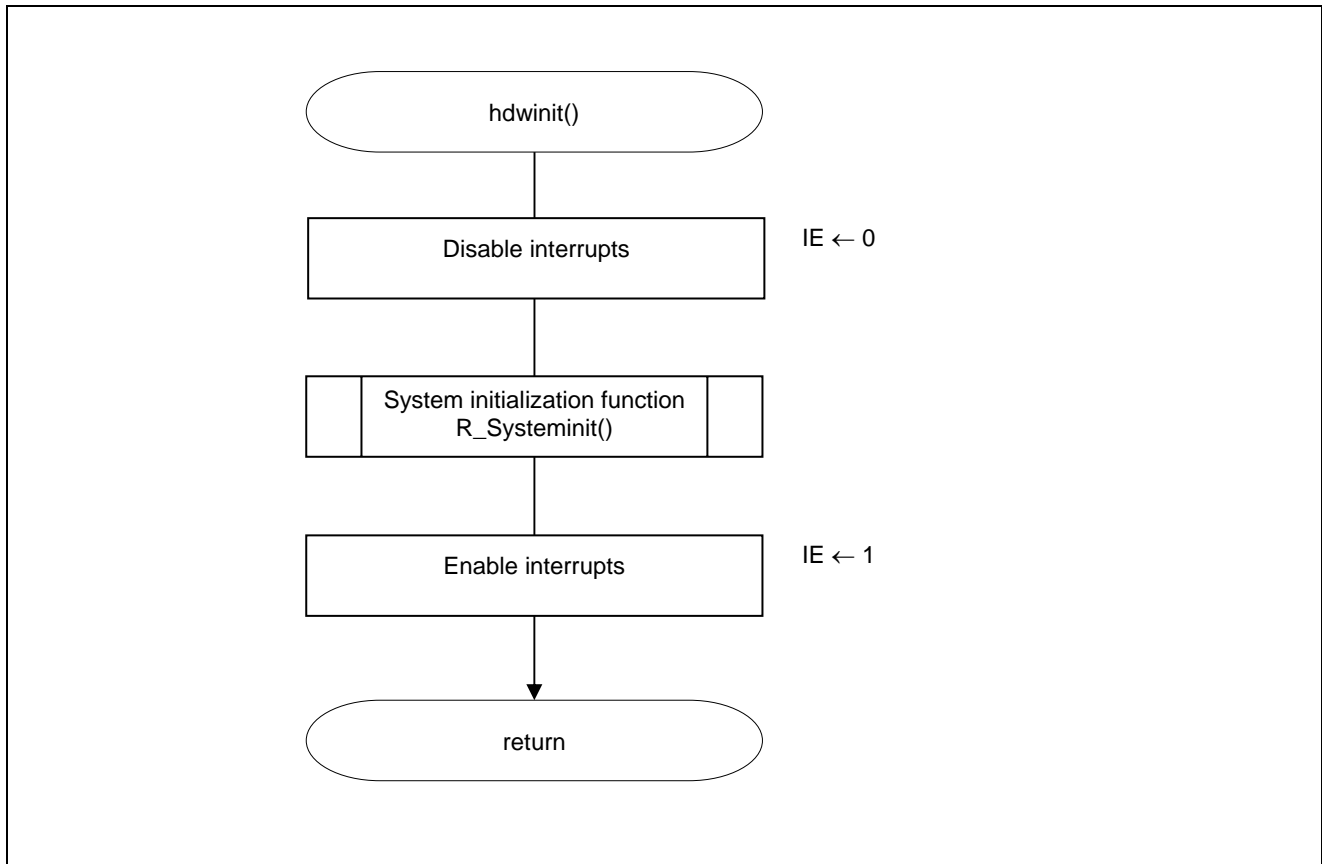
Figure 5.1 shows the overall flow of the sample program described in this application note.



**Figure 5.1 Overall Flow**

### 5.11.1 Initialization Function

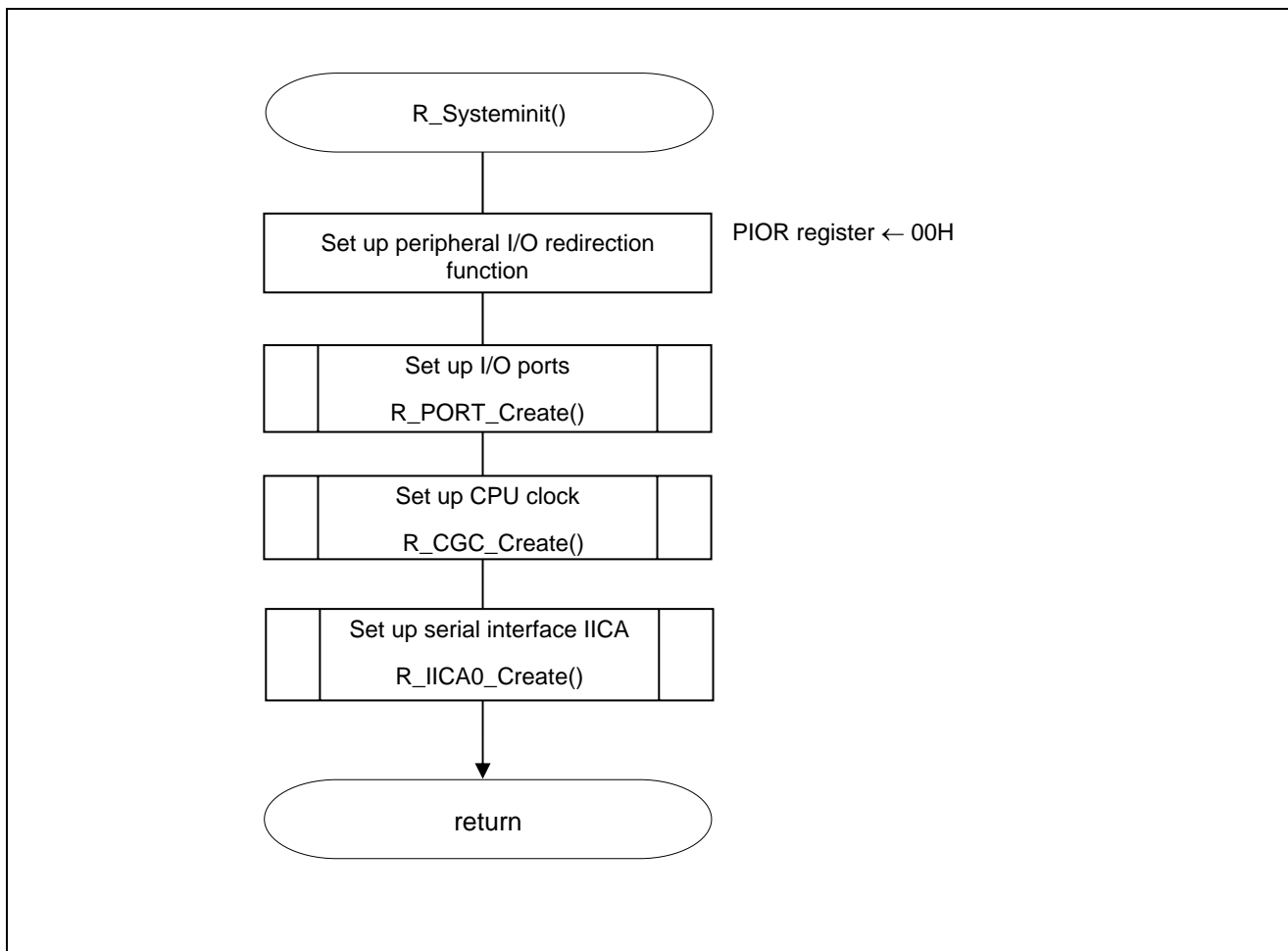
Figure 5.2 shows the flowchart for the initialization function.



**Figure 5.2 Initialization Function**

### 5.11.2 System Initialization Function

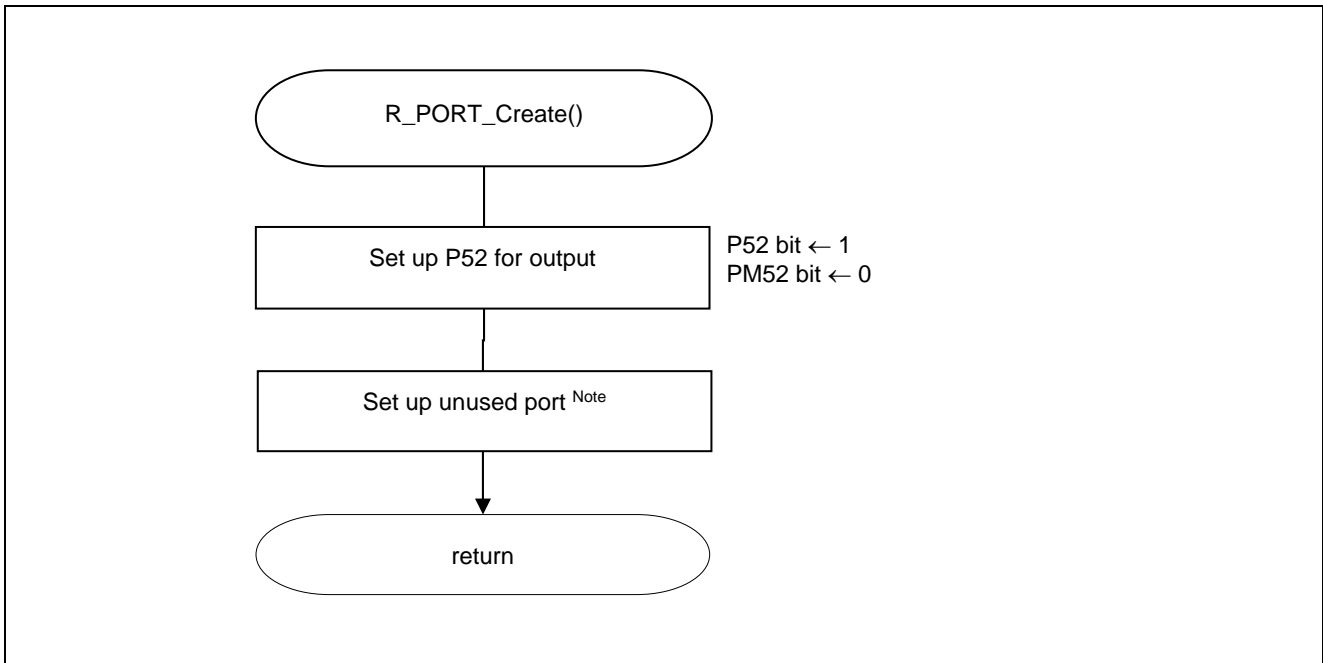
Figure 5.3 shows the flowchart for the system initialization function.



**Figure 5.3 System Initialization Function**

### 5.11.3 I/O Port Setup

Figure 5.4 shows the flowchart for I/O port setup.



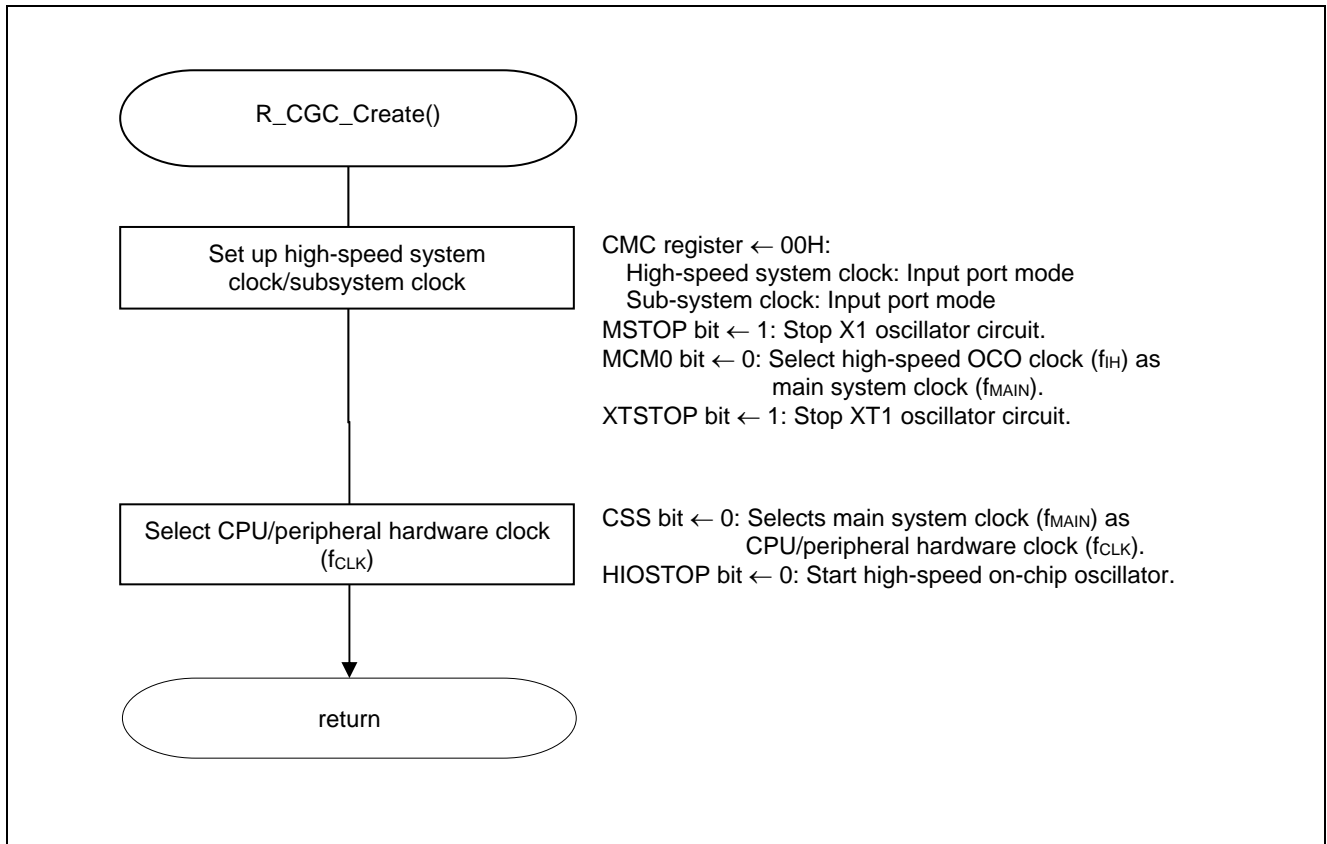
**Figure 5.4 I/O Port Setup**

**Note:** Refer to the section entitled "Flowcharts" in RL78/G13 Initialization (R01AN0451E) Application Note for the configuration of the unused ports.

**Caution:** Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to  $V_{DD}$  or  $V_{SS}$  via a separate resistor.

### 5.11.4 CPU Clock Setup

Figure 5.5 shows the flowchart for CPU clock setup.



**Figure 5.5 CPU Clock Setup**

**Caution:** For details on the procedure for setting up the CPU clock (R\_CGC\_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Initialization (R01AN0451E) Application Note.

### 5.11.5 Serial Interface (IICA) Setup

Figure 5.6 shows the flowchart for serial interface (IICA) setup (1/2). Figure 5.7 shows the flowchart for serial interface (IICA) setup (2/2).

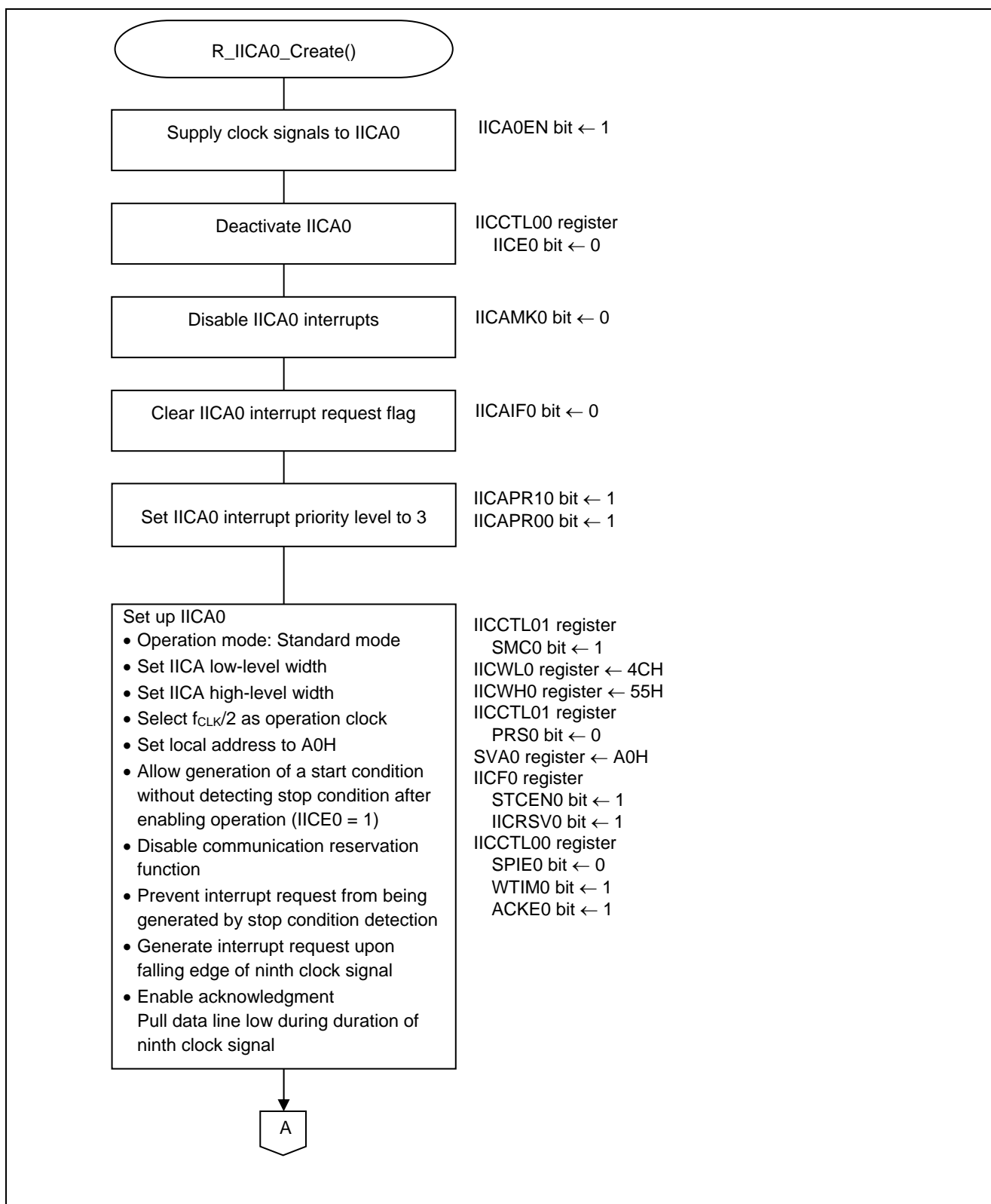
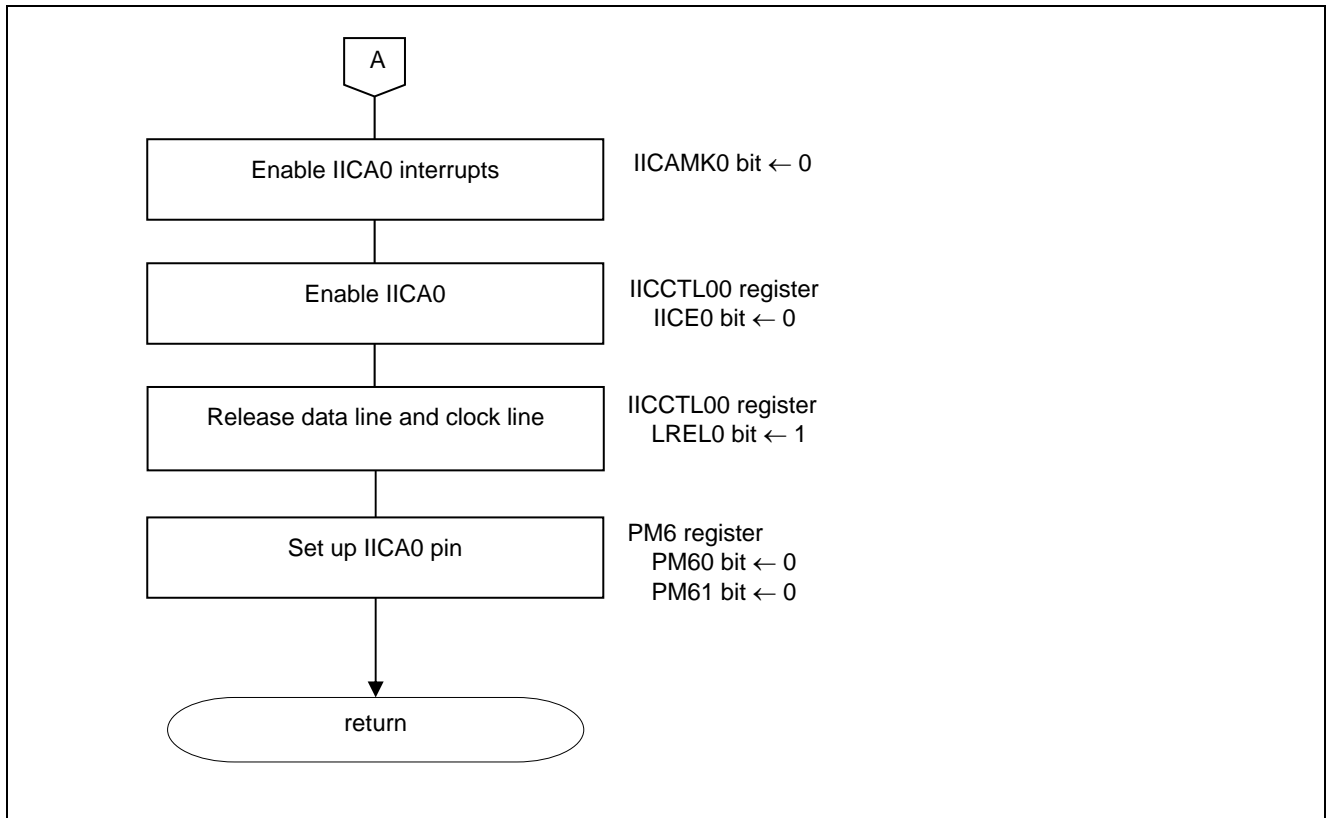


Figure 5.6 Serial Interface (IICA) Setup (1/2)



**Figure 5.7 Serial Interface (IICA) Setup (2/2)**

5.11.6 Main Processing

Figure 5.8 shows the flowchart for main processing (1/2). Figure 5.9 shows the flowchart for main processing (2/2).

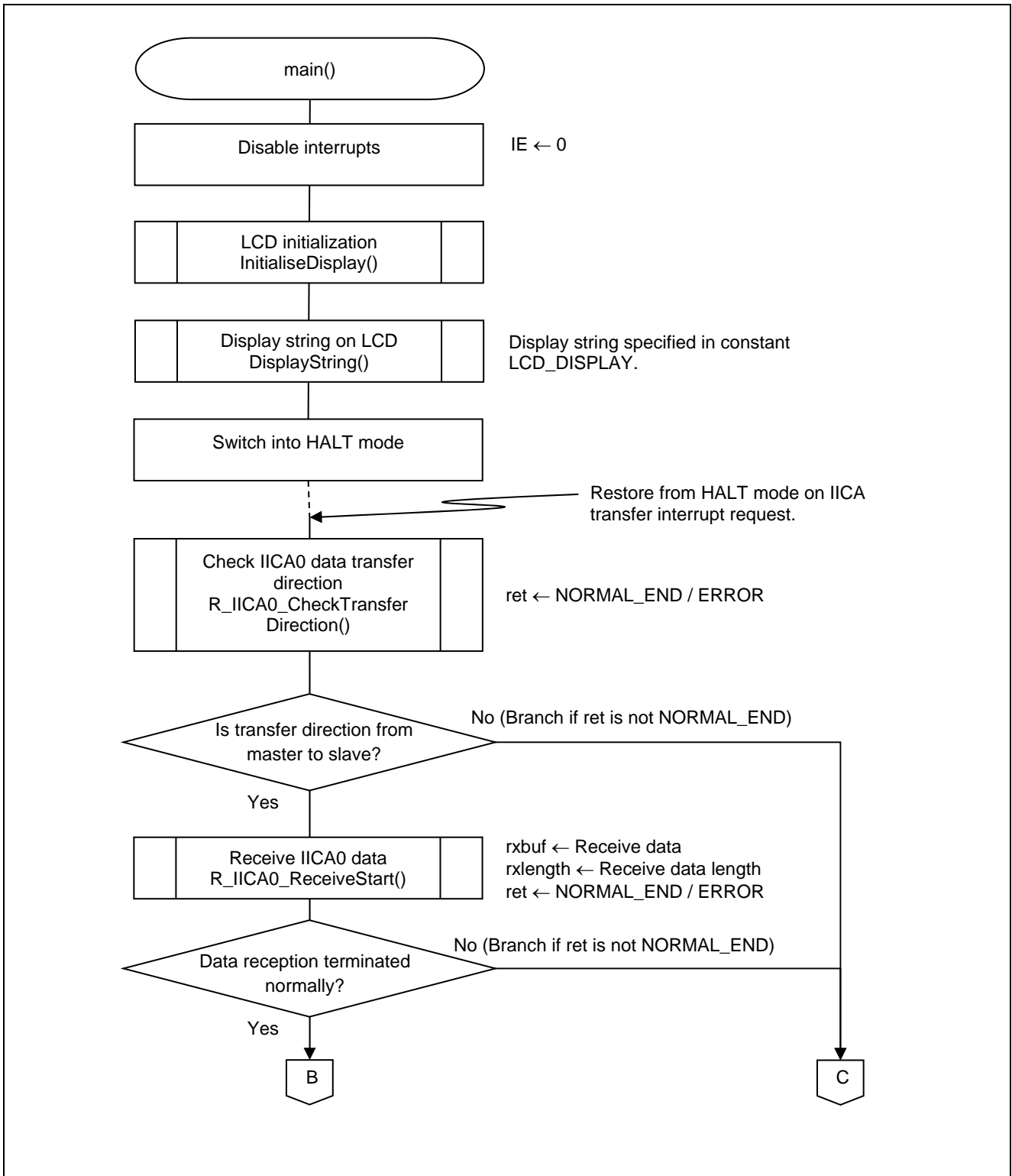


Figure 5.8 Main Processing (1/2)



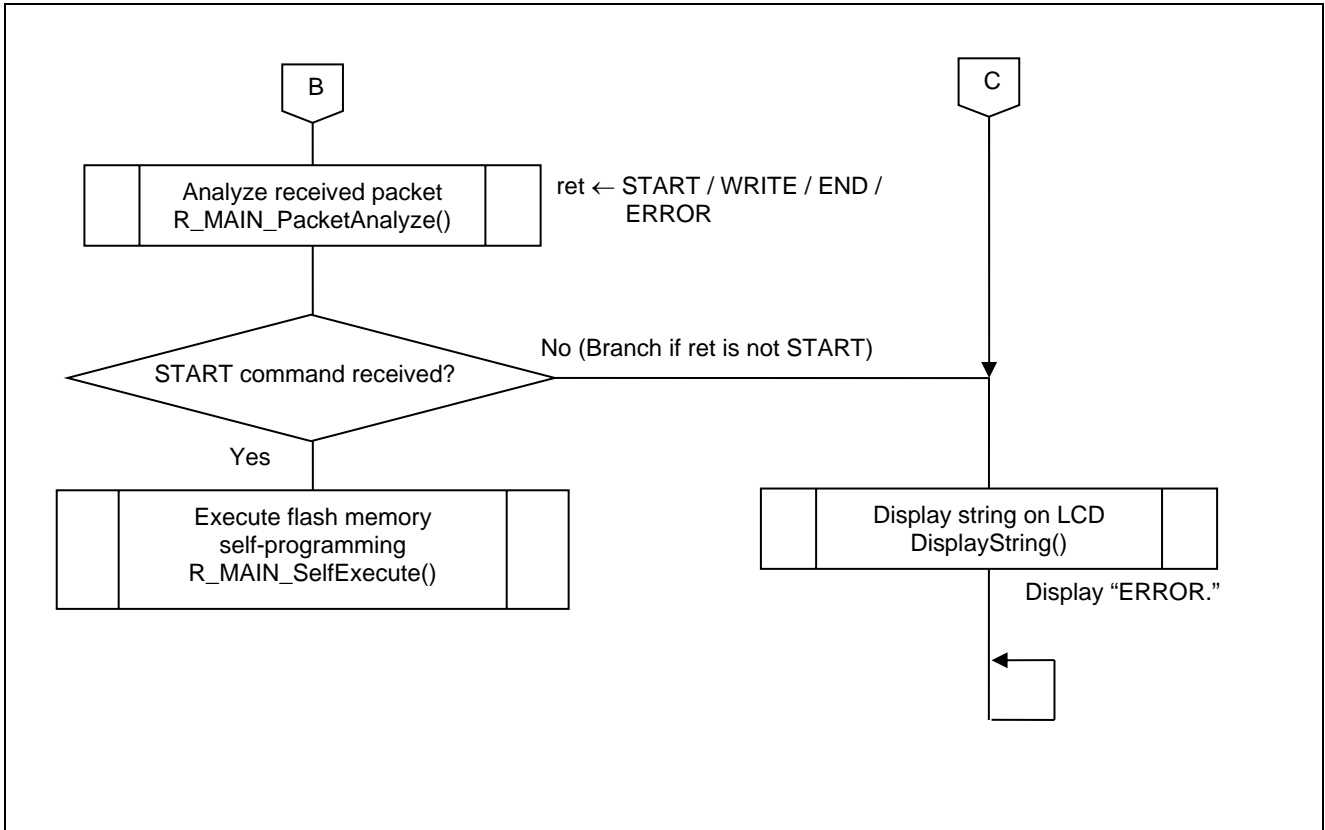


Figure 5.9 Main Processing (2/2)

5.11.7 Checking the Direction of Data Transfer via IICA0

Figure 5.10 shows the flowchart for checking the direction of data transfer via IICA0.

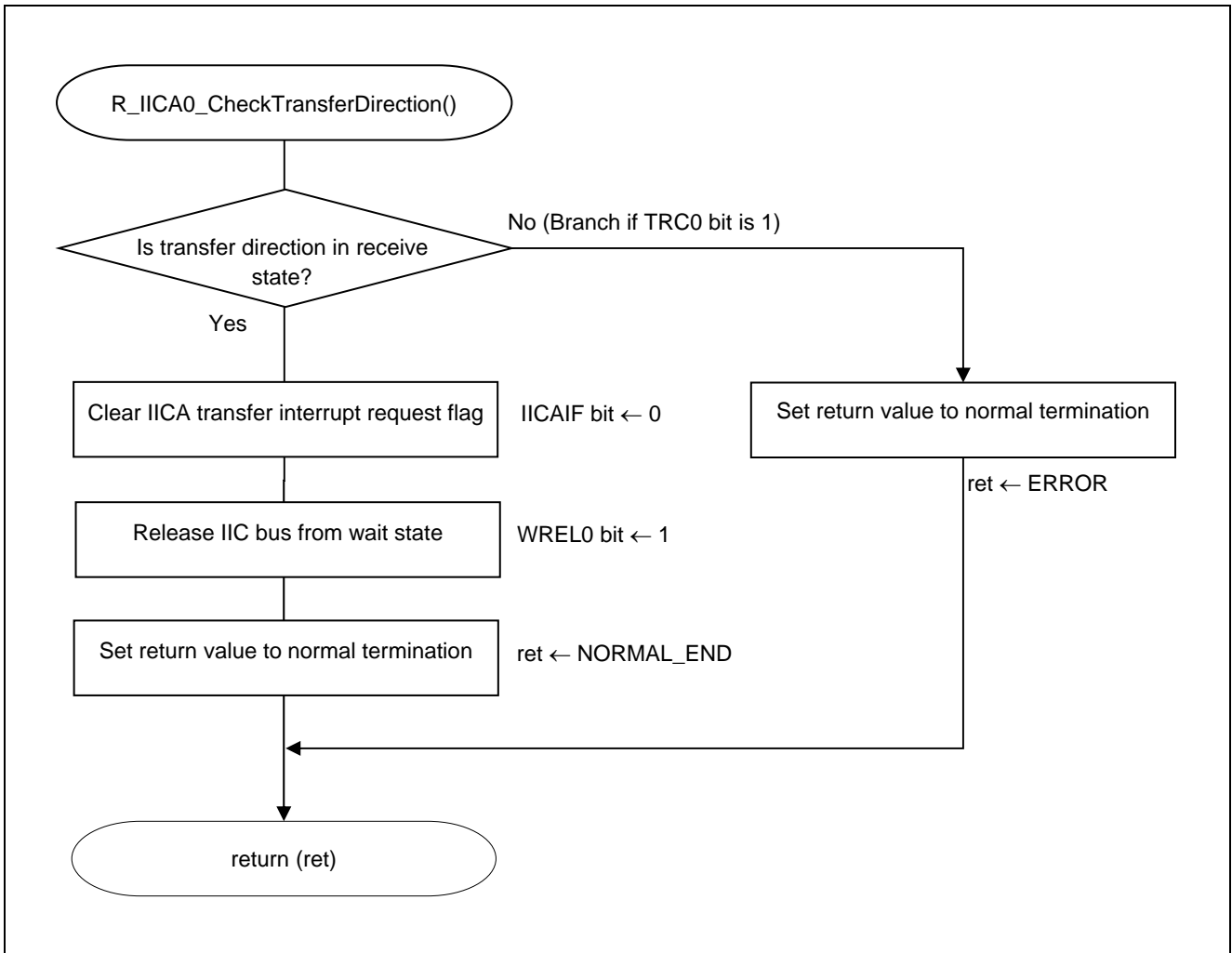


Figure 5.10 Checking the Direction of Data Transfer via IICA0

5.11.8 Data Reception via IICA0

Figure 5.11 shows the flowchart for data reception via the IICA0 (1/3). Figure 5.12 shows the flowchart for data reception via the IICA0 (2/3). Figure 5.13 shows the flowchart for data reception via the IICA0 (3/3).

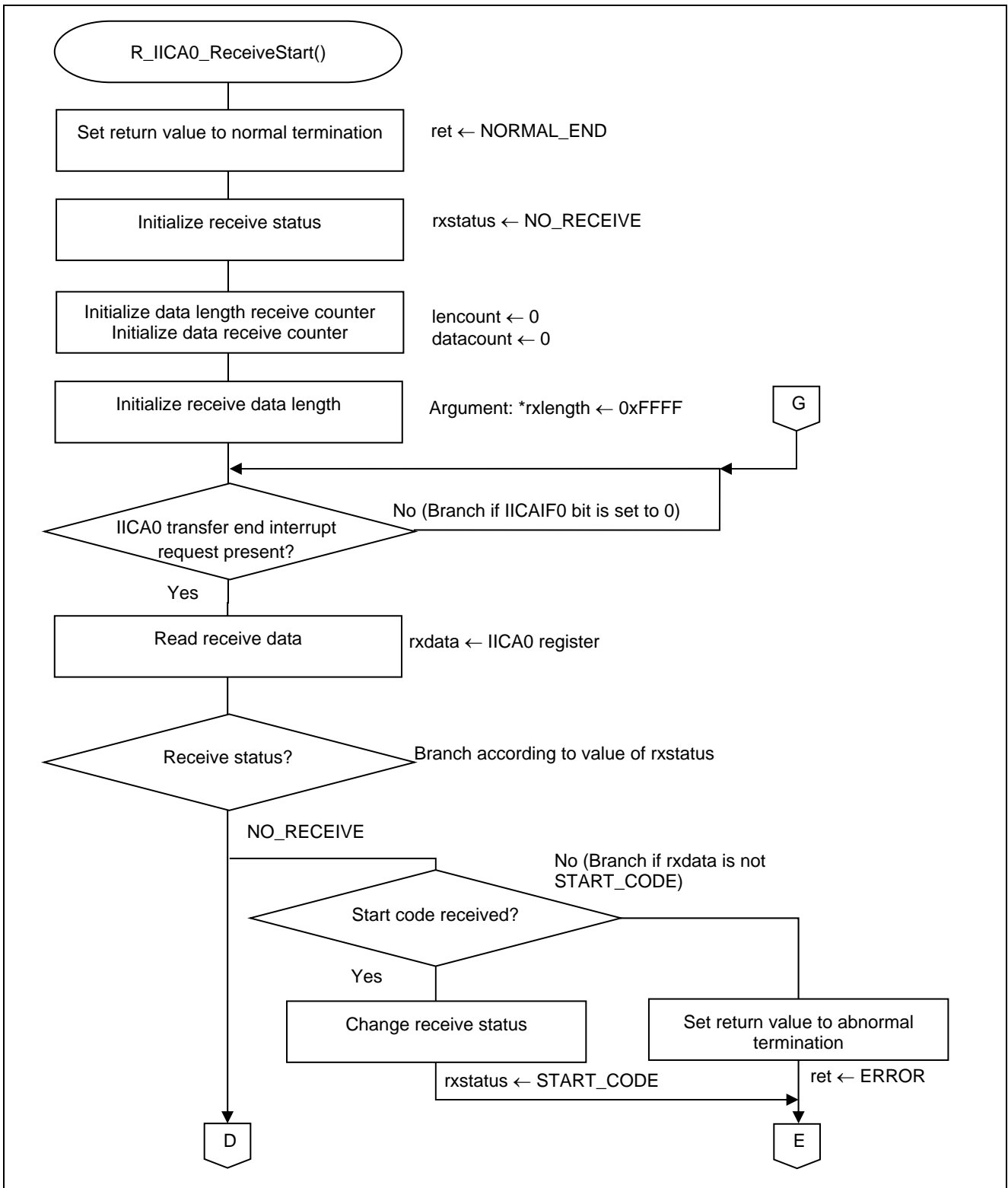


Figure 5.11 Data Reception via IICA0 (1/3)

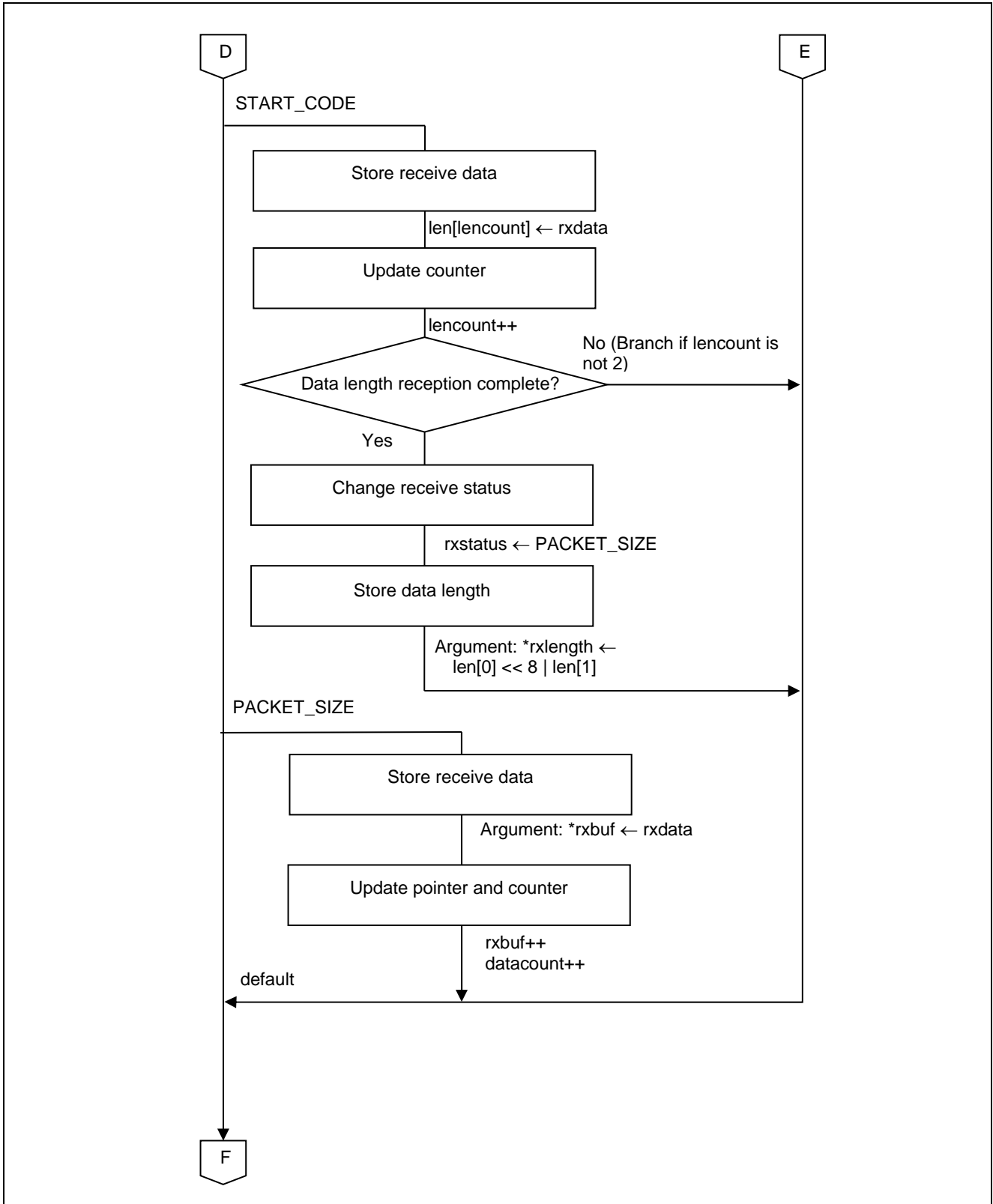


Figure 5.12 Data Reception via IICA0 (2/3)

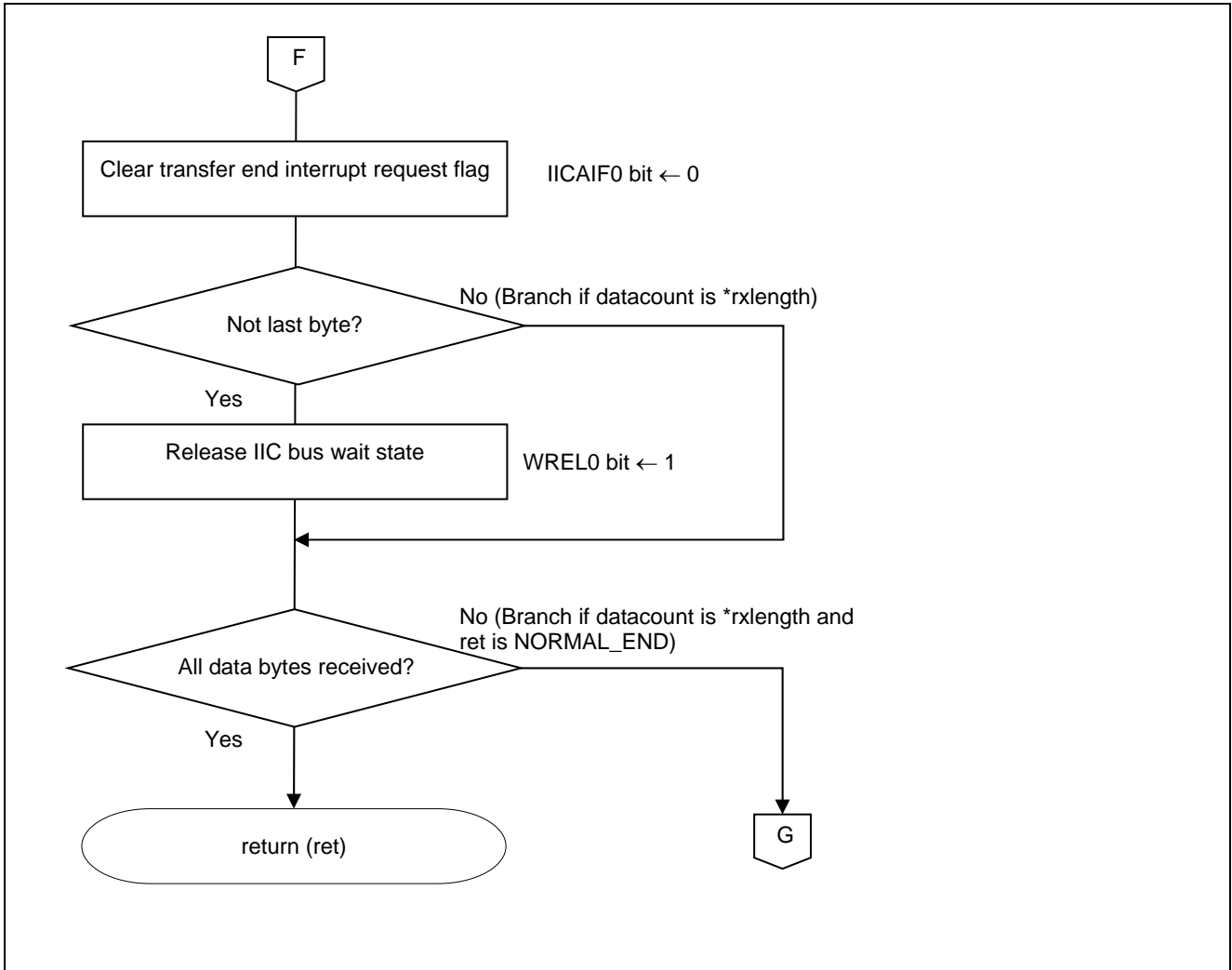


Figure 5.13 Data Reception via IICA0 (3/3)

5.11.9 Receive Packet Analysis

Figure 5.14 shows the flowchart for receive packet analysis.

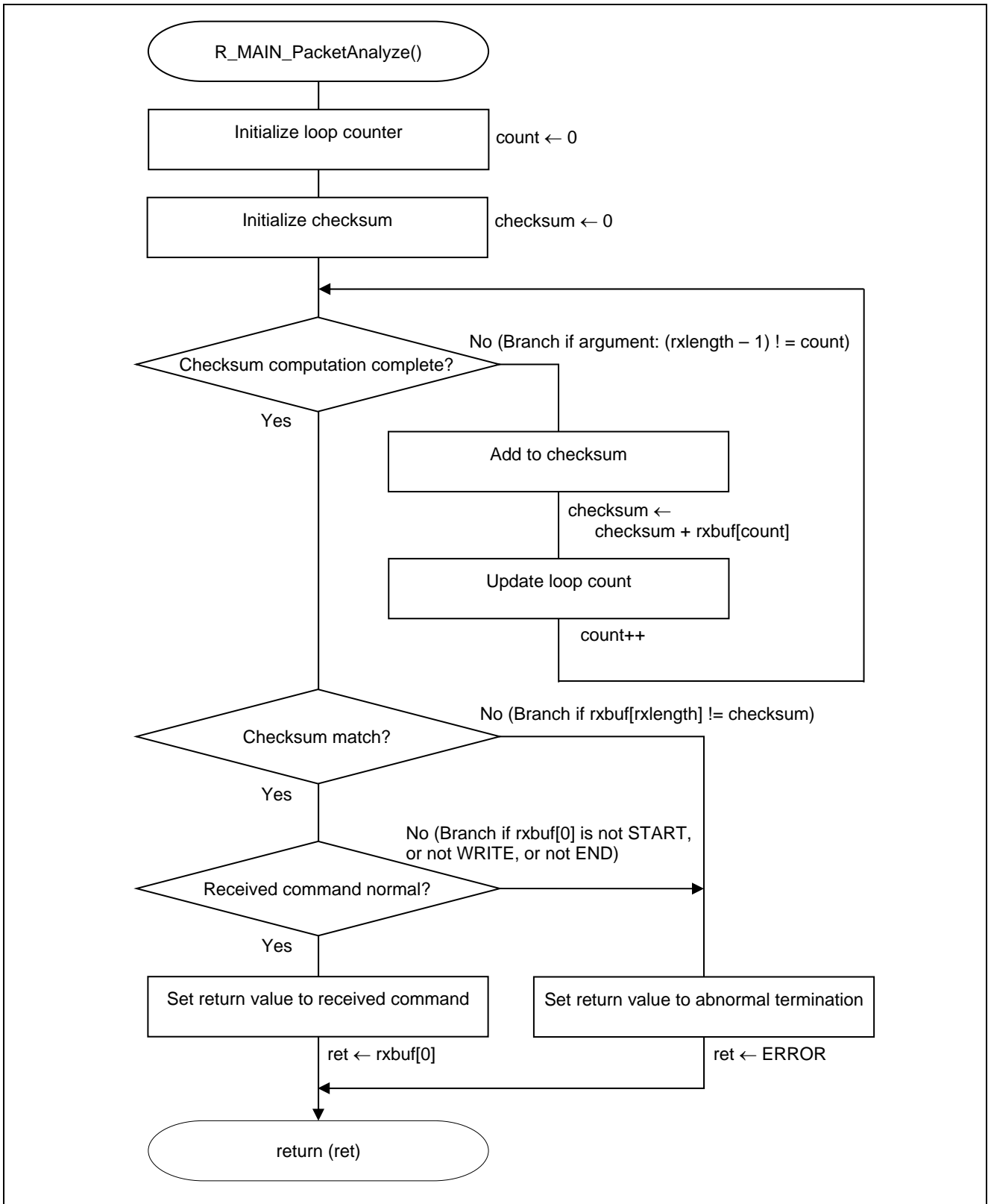


Figure 5.14 Receive Packet Analysis

5.11.10 Flash Memory Self-Programming Execution

Figure 5.15 shows the flowchart for flash memory self-programming execution.

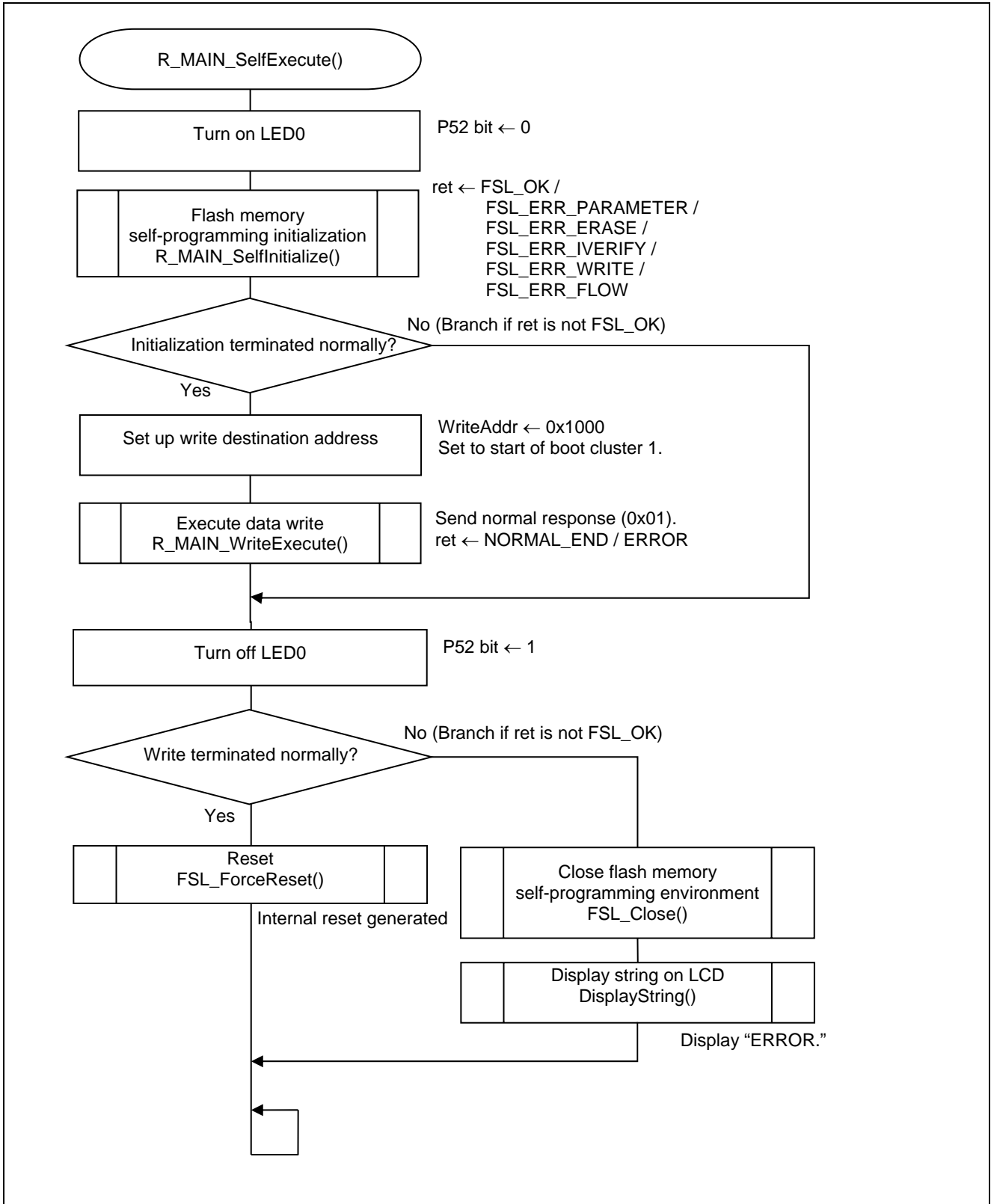


Figure 5.15 Flash Memory Self-Programming Execution

5.11.11 Flash Memory Self-Programming Initialization

Figure 5.16 shows the flowchart for flash memory self-programming initialization (1/2). Figure 5.17 shows the flowchart for flash memory self-programming initialization (2/2).

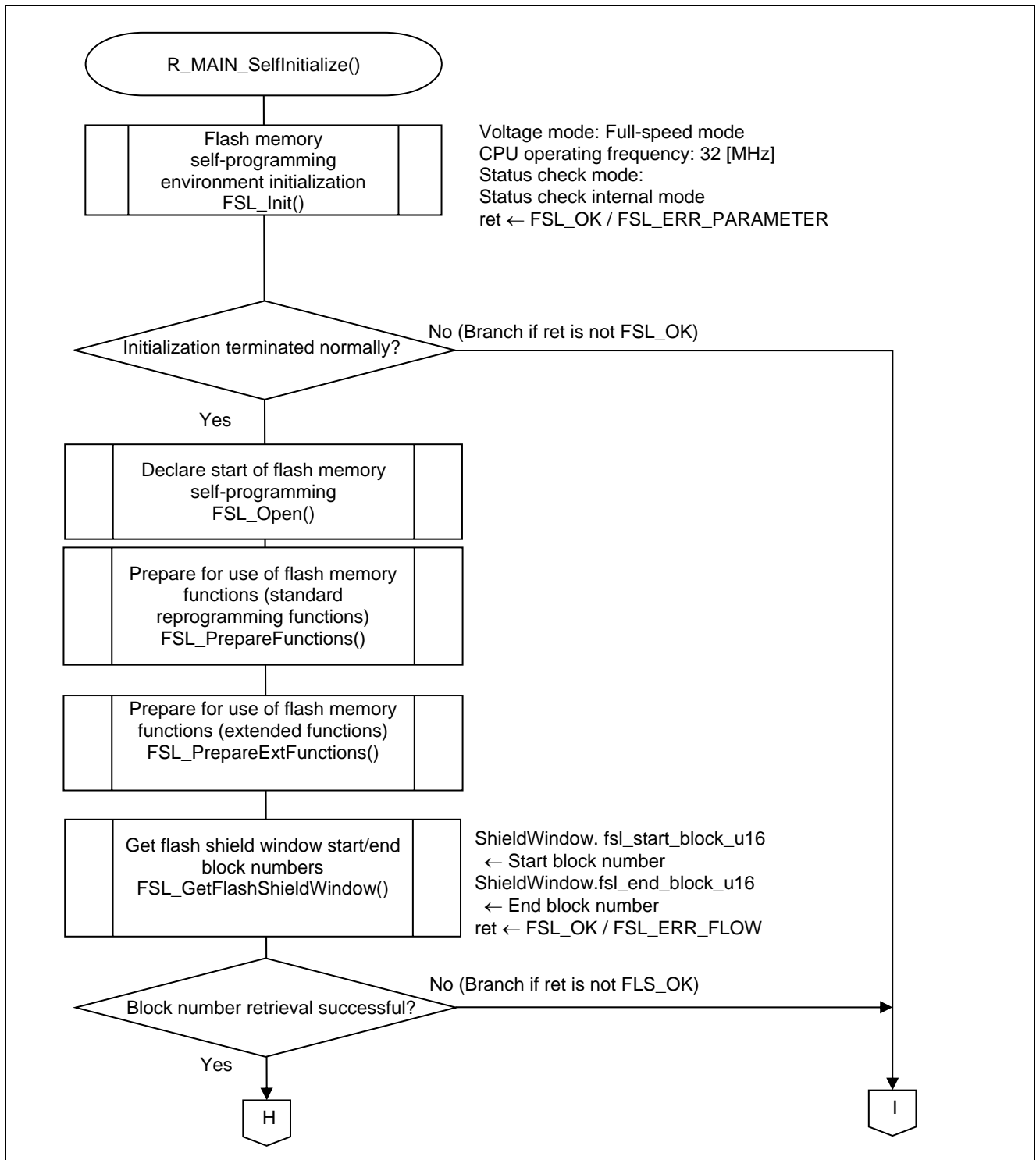


Figure 5.16 Flash Memory Self-Programming Initialization (1/2)



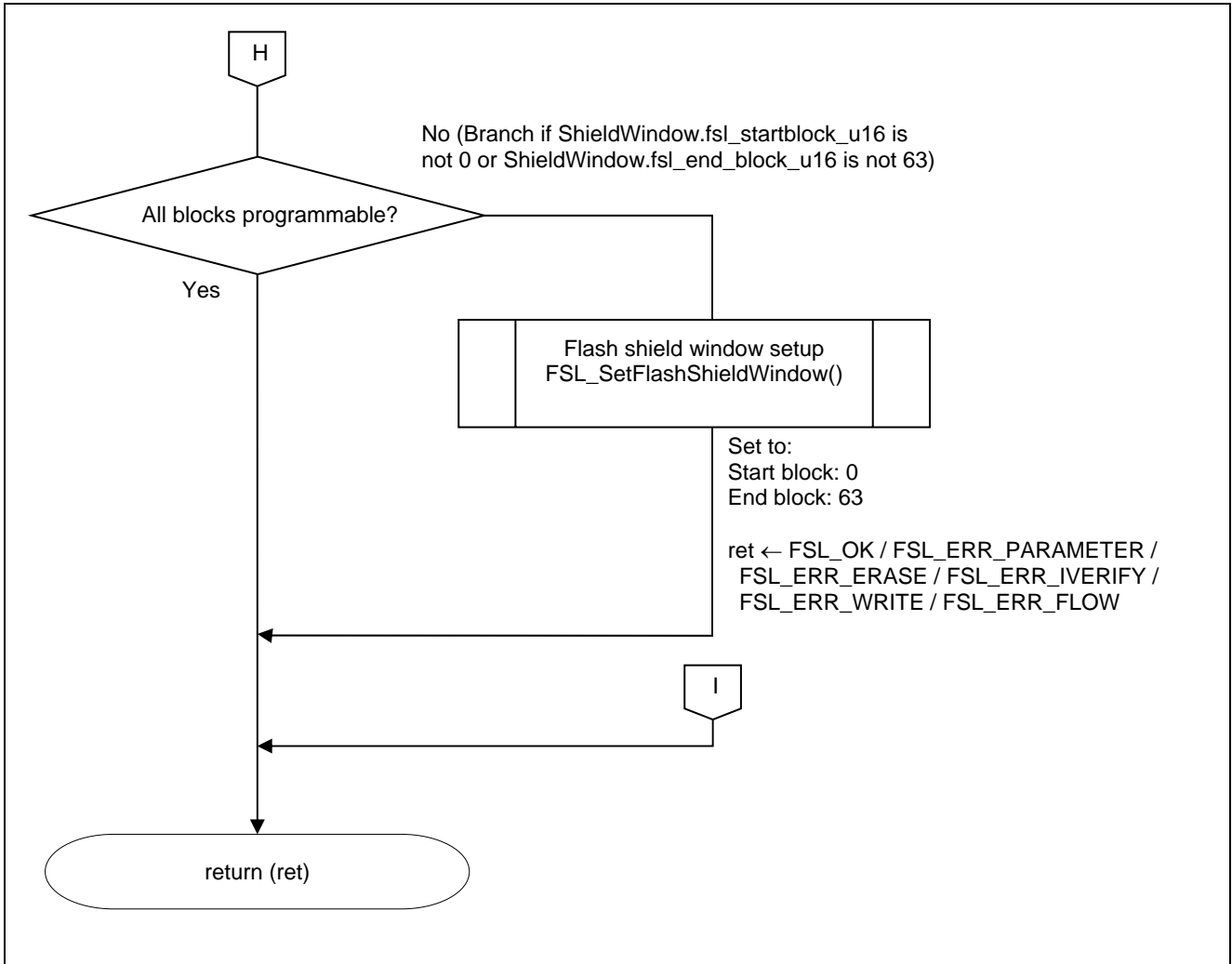


Figure 5.17 Flash Memory Self-Programming Initialization (2/2)

5.11.12 Flash Memory Reprogramming Execution

Figure 5.18 shows the flowchart for flash memory reprogramming execution (1/3). Figure 5.19 shows the flowchart for flash memory reprogramming execution (2/3). Figure 5.20 shows the flowchart for flash memory reprogramming execution (3/3).

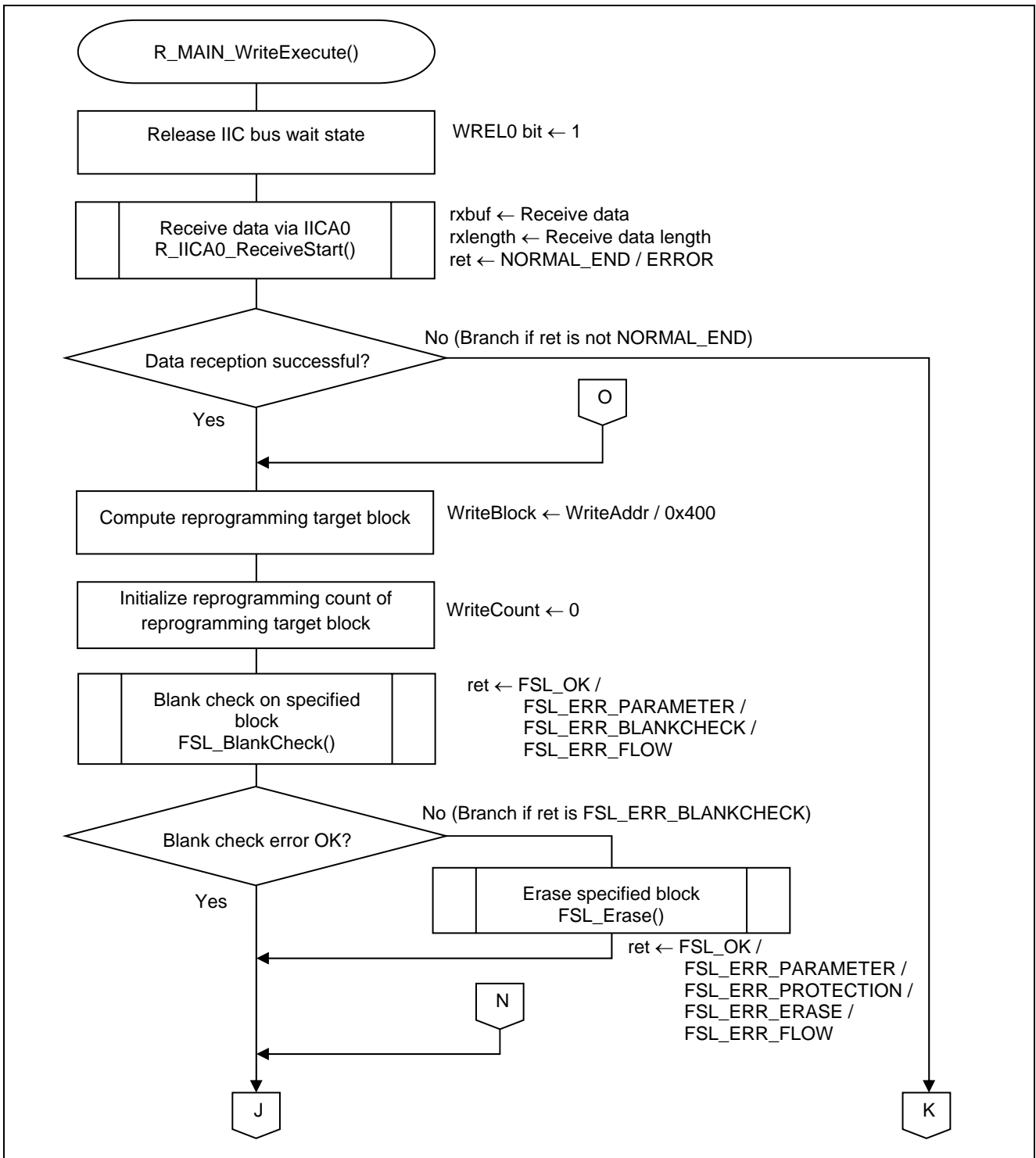


Figure 5.18 Flash Memory Reprogramming Execution (1/3)

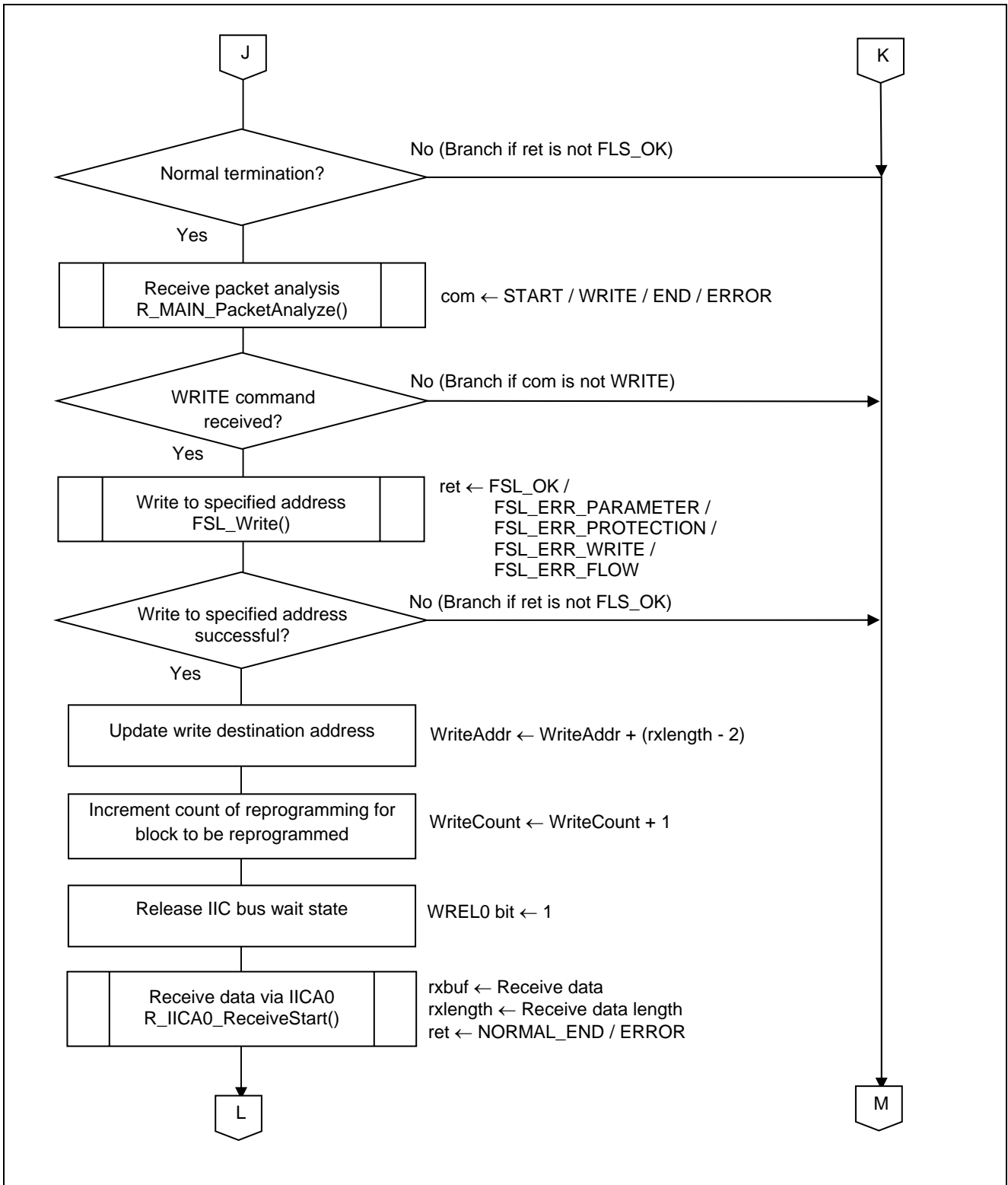


Figure 5.19 Flash Memory Reprogramming Execution (2/3)

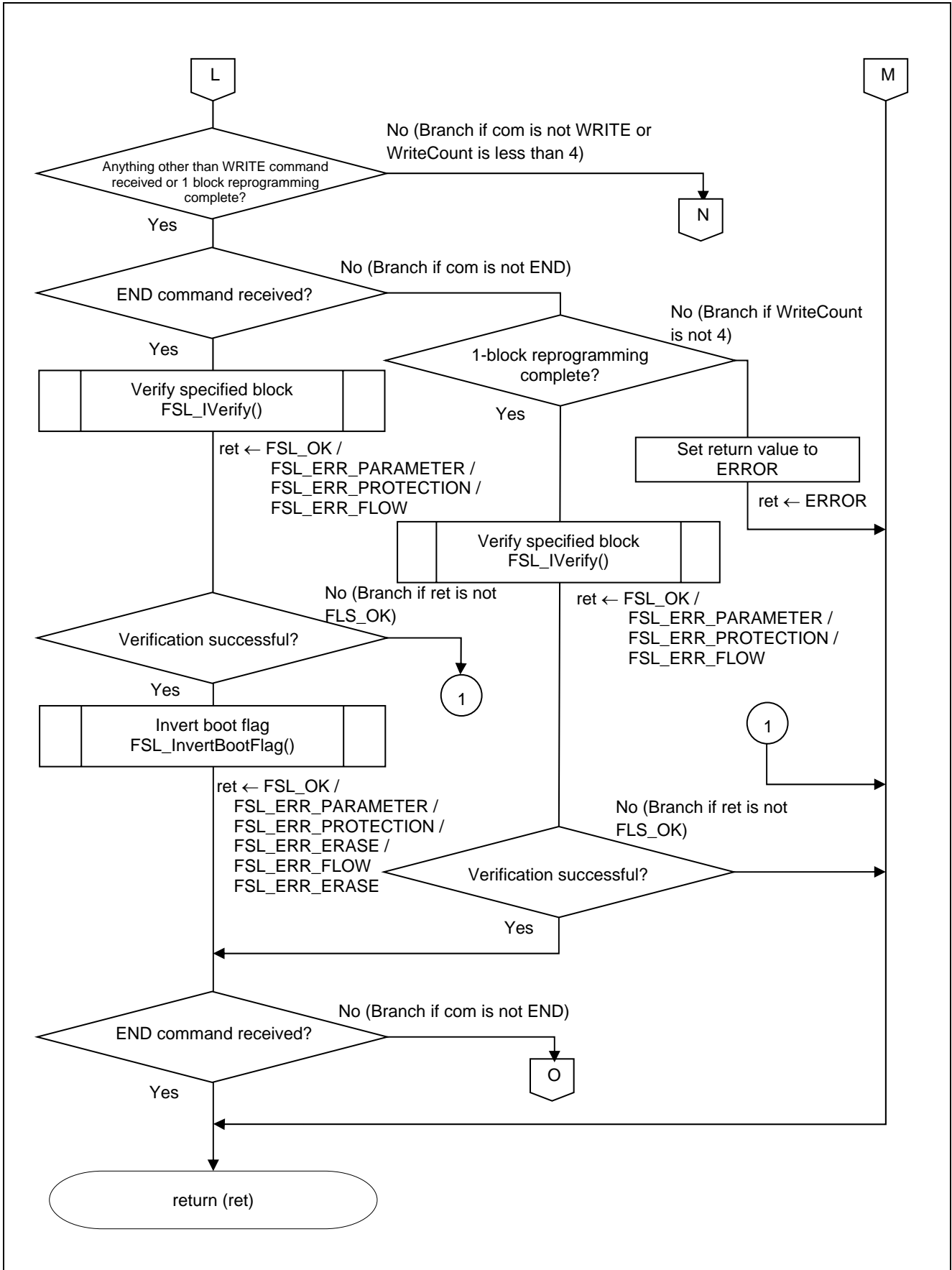


Figure 5.20 Flash Memory Reprogramming Execution (3/3)

## 5.12 Operation Check Procedure

Change the string defined in the constant `LCD_DISPLAY` that is defined in `r_cg_userdefine.h` for the sample program and rebuild the project. Flash memory self-programming is carried out by sending the HEX file that is generated as the reprogramming data from the sending side. Refer to Section 5.1, Communication Specifications, for the specifications for the communication between the sending side and this sample program.

For example, the operation of the sample program will look like as shown below when the value of the constant `LCD_DISPLAY` is changed to "Ver 2.0."

- (1) "Ver 1.0" is displayed on the LCD.

The constant `LCD_DISPLAY` is defined as "Ver 1.0" by this sample program.

- (2) Send a START command from the sending side to initiate communication.

After the START command is sent, communication between the sending side and this sample program proceeds as specified in Section 5.1, Communication Specifications.

- (3) When the sample program receives a WRITE command and reprogramming data and starts flash memory self-programming, LED0 on the RSK board turns on.

- (4) LED0 turns off when the sample program receives an END command.

- (5) A reset occurs and "Ver 2.0" is displayed on the LCD.

### 5.12.1 Making Checks with a Debugger

When flash memory self-programming is executed with a debugger (E1 emulator) connected, it becomes unable to check the execution of the program correctly with the debugger after the reprogramming. To check the program execution with the debugger after reprogramming, it is necessary to change the HEX file that is to be used as reprogramming data from the state established immediately when it is generated by CS+.

More specifically, it is necessary to rewrite the reset vector (address 0x00000) to the address where the monitor program is placed and to add changes to a part of the monitor program (addresses 0x000CE to 0x000D3) as shown below.

Address	CS+ Output State	Change To
0x00000 (Reset vector)	0xD8	0xD0
0x000CE	0xFF	0xD8
0x000CF	0xFF	0x00
0x000D0	0xFF	0xEC
0x000D1	0xFF	0xFD
0x000D2	0xFF	0xFF
0x000D3	0xFF	0x00

**[Data for normal operation check (CS+ output state)]**

```

/* 0000 */ 0xD8, 0x00, 0xFF, 0xFF, 0x56, 0x65, 0x72, 0x20, 0x32, 0x2E, 0x30, 0x20, 0x00, 0x20, 0x45, 0x52,
/* 0010 */ 0x52, 0x4F, 0x52, 0x21, 0x20, 0x00, 0xFE, 0x0F, 0x00, 0xDF, 0x0A, 0xC7, 0x52, 0x12, 0x56, 0x04,
/* 0020 */ 0xFE, 0x11, 0x00, 0xC6, 0xD7, 0x52, 0x1F, 0xD7, 0xC1, 0x51, 0xF3, 0x50, 0x03, 0x5F, 0x90, 0x08,
/* 0030 */ 0x61, 0x48, 0xC0, 0xD7, 0xC7, 0xC5, 0xC1, 0x66, 0x75, 0x30, 0x80, 0x08, 0x16, 0xBF, 0x04, 0x08,
/* 0040 */ 0xFC, 0xF8, 0xFF, 0x0E, 0xD2, 0xDF, 0x10, 0xC3, 0x65, 0x73, 0xF2, 0xA8, 0x02, 0x14, 0x61, 0xE9,
/* 0050 */ 0x99, 0xA5, 0x82, 0x93, 0xDF, 0xF8, 0xC2, 0xC0, 0xC4, 0xC6, 0xD7, 0xFF, 0xFF, 0x00, 0xFF, 0xFF,
/* 0060 */ 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF,
/* 0070 */ 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF,
/* 0080 */ 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF,
/* 0090 */ 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF,
/* 00A0 */ 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF,
/* 00B0 */ 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF,
/* 00C0 */ 0xEF, 0x7F, 0xE8, 0x84, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0xFF, 0xFF,
/* 00D0 */ 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x61, 0xCF, 0x51, 0x00, 0x71, 0x8C, 0x71, 0x09,
    
```

•  
•  
•

Change address 00000H from D8H to D0H.

Change addresses 000CEH to 000D3H from FFH, FFH, FFH, FFH, FFH, FFH to D8H, 00H, ECH, FDH, FFH, 00H.

**[Data for debugger operation check]**

```

/* 0000 */ 0xD0, 0x00, 0xFF, 0xFF, 0x56, 0x65, 0x72, 0x20, 0x32, 0x2E, 0x30, 0x20, 0x00, 0x20, 0x45, 0x52,
/* 0010 */ 0x52, 0x4F, 0x52, 0x21, 0x20, 0x00, 0xFE, 0x0F, 0x00, 0xDF, 0x0A, 0xC7, 0x52, 0x12, 0x56, 0x04,
/* 0020 */ 0xFE, 0x11, 0x00, 0xC6, 0xD7, 0x52, 0x1F, 0xD7, 0xC1, 0x51, 0xF3, 0x50, 0x03, 0x5F, 0x90, 0x08,
/* 0030 */ 0x61, 0x48, 0xC0, 0xD7, 0xC7, 0xC5, 0xC1, 0x66, 0x75, 0x30, 0x80, 0x08, 0x16, 0xBF, 0x04, 0x08,
/* 0040 */ 0xFC, 0xF8, 0xFF, 0x0E, 0xD2, 0xDF, 0x10, 0xC3, 0x65, 0x73, 0xF2, 0xA8, 0x02, 0x14, 0x61, 0xE9,
/* 0050 */ 0x99, 0xA5, 0x82, 0x93, 0xDF, 0xF8, 0xC2, 0xC0, 0xC4, 0xC6, 0xD7, 0xFF, 0xFF, 0x00, 0xFF, 0xFF,
/* 0060 */ 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF,
/* 0070 */ 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF,
/* 0080 */ 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF,
/* 0090 */ 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF,
/* 00A0 */ 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF,
/* 00B0 */ 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF,
/* 00C0 */ 0xEF, 0x7F, 0xE8, 0x84, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0xD8, 0x00,
/* 00D0 */ 0xEC, 0xFD, 0xFF, 0x00, 0xFF, 0xFF, 0xFF, 0xFF, 0x61, 0xCF, 0x51, 0x00, 0x71, 0x8C, 0x71, 0x09,
    
```

•  
•  
•

This sample program generates a reset by inverting the state of the boot flag and carries out boot swapping after rewriting boot cluster 1. The FSL\_ForceReset function of the flash memory self-programming library is used to generate the reset. When this function is executed with a debugger (E1 emulator) connected, a break will occur and processing stop. After the break occurs, it is necessary to manually effect a reset and execute the program again.

## 6. Sample Code

The sample code is available on the Renesas Electronics Website.

## 7. Documents for Reference

RL78/G13 User's Manual: Hardware (R01UH0146E)

RL78 Family User's Manual: Software (R01US0015E)

RL78 family's Flash Self Programming Library Type01 User's Manual (R01US0050E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

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Revision Record	RL78/G13 Self-Programming (IIC)
-----------------	---------------------------------

Rev.	Date	Description	
		Page	Summary
1.00	Mar.01, 2013	—	First edition issued
1.10	June 01, 2016	11	Modification of 1.4 How to Get the Flash Memory Self-Programming Library.
		47	Addition of Documents for Reference.

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Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.  
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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