RL78/G13

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Safety Function (Flash Memory CRC Operation Function) CC-RL

Introduction

This application note explains how to use the flash memory CRC operation function, which is one of the safety functions incorporated in the RL78/G13.

The high-speed CRC performs operation on and compares the data in the code flash memory (addresses 00000H to 0FFFBH) with the results of the operation performed by the object converter.

The general-purpose CRC performs operation on the data in a part of the on-chip RAM and compares their results with the results of the operation preformed again in the same area. The data to be operated on can be changed using by switch input.

Both of the high-speed CRC and general-purpose CRC turn on an LED when the results of the operation match.

Target Device

RL78/G13

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

This application note explains how to use the flash memory CRC operation function, which is one of the safety functions incorporated in the RL78/G13.

The high-speed CRC performs operation on and compares the data in the code flash memory (addresses 00000H to 0FFFBH) with the results of the operation performed by the object converter.

The general-purpose CRC performs operation on the data in a part of the on-chip RAM and compares their results with the results of the operation preformed again in the same area. The data to be operated on can be changed using switch input.

Both of the high-speed CRC and general-purpose CRC turn on an LED when the results of the operation match.

Table 1.1 lists the peripheral function to be used and its use. Figure 1.1 shows the outline of operation of the high-speed CRC. Figure 1.2 shows the outline of operation of the general-purpose CRC.

Table 1.1 Peripheral Functions to be Used and its Use

Peripheral Function	Use
Safety function: Flash memory CRC operation function	Performs high-speed CRC and general-purpose CRC operation in a specified memory area and compares their results with the separately prepared values to verify the validity of the data.

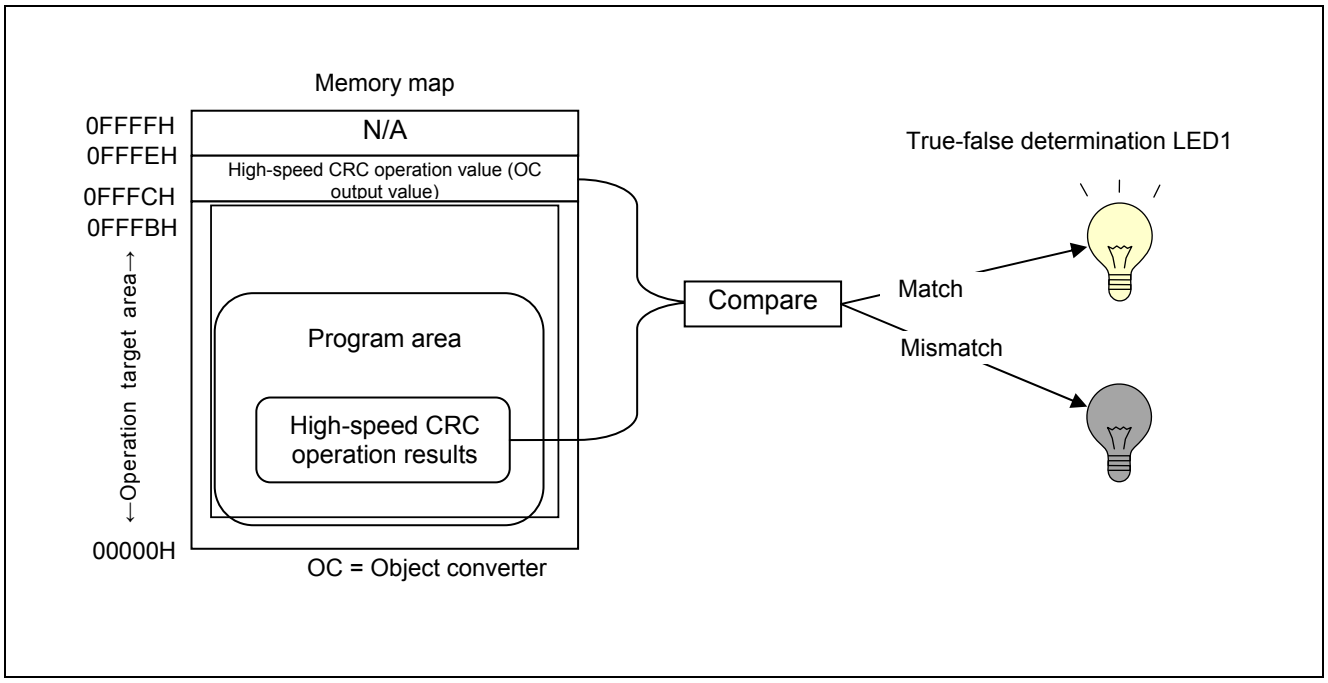


Figure 1.1 Outline of High-speed CRC Operation

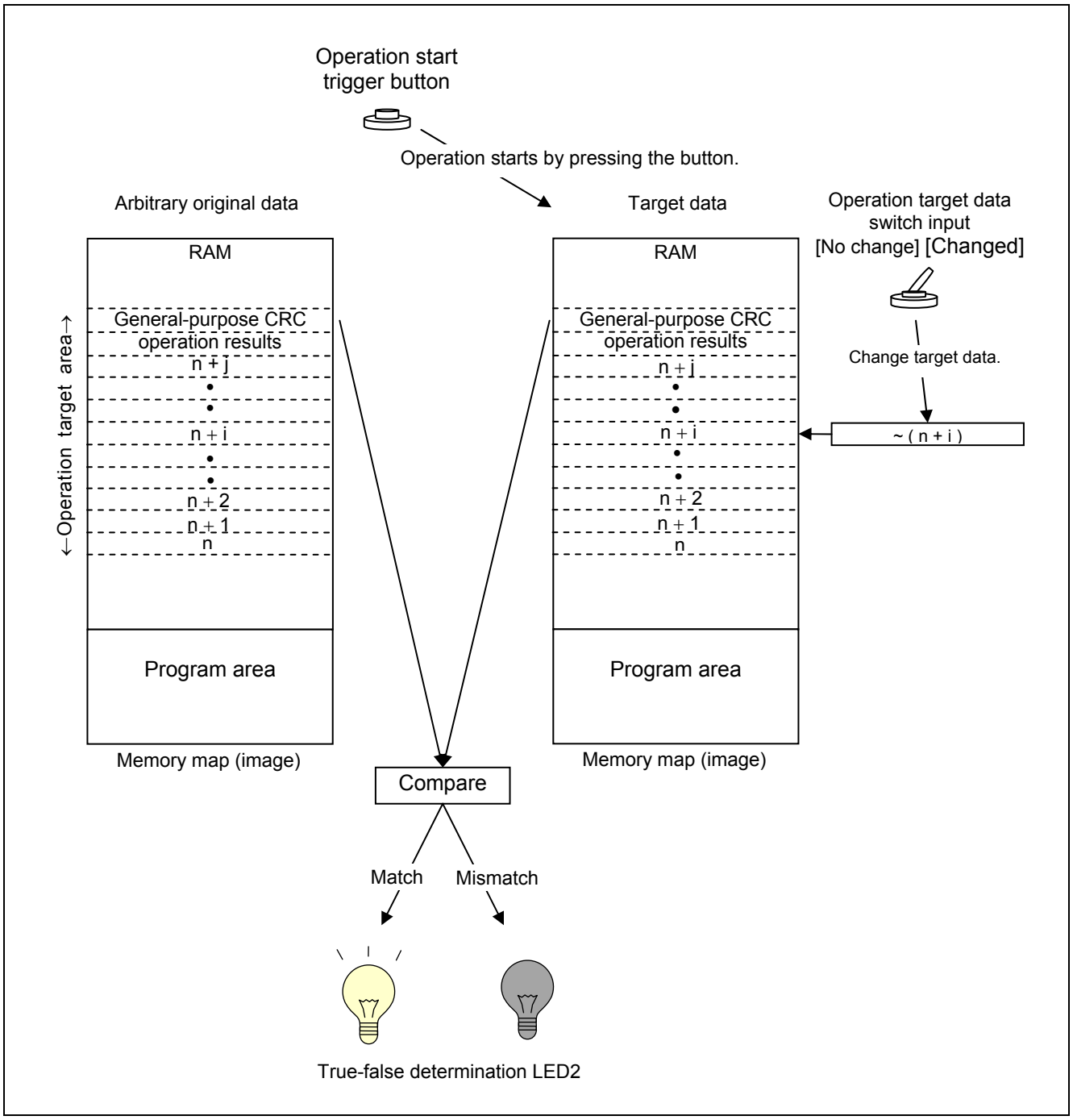


Figure 1.2 Outline of General-purpose CRC Operation

2. Operation Check Conditions

The sample code described in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G13 (R5F100LEA)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 32 MHz • CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0 V (Operation is possible over a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode which uses 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ V3.01.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V4.0.0.26 from Renesas Electronics Corp.
C Compiler (e^2 studio)	CC-RL V1.01.00 from Renesas Electronics Corp.
Flash memory programmer	E1 (R0E000010KCE00) from Renesas Electronics Corp.
Flash memory programming software	Renesas Flash Programmer V1.01.00 from Renesas Electronics Corp.

3. Related Application Note

The application note that is related to this application note is listed below for reference.

RL78/G13 Initialization (R01AN2575E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration used for this application note.

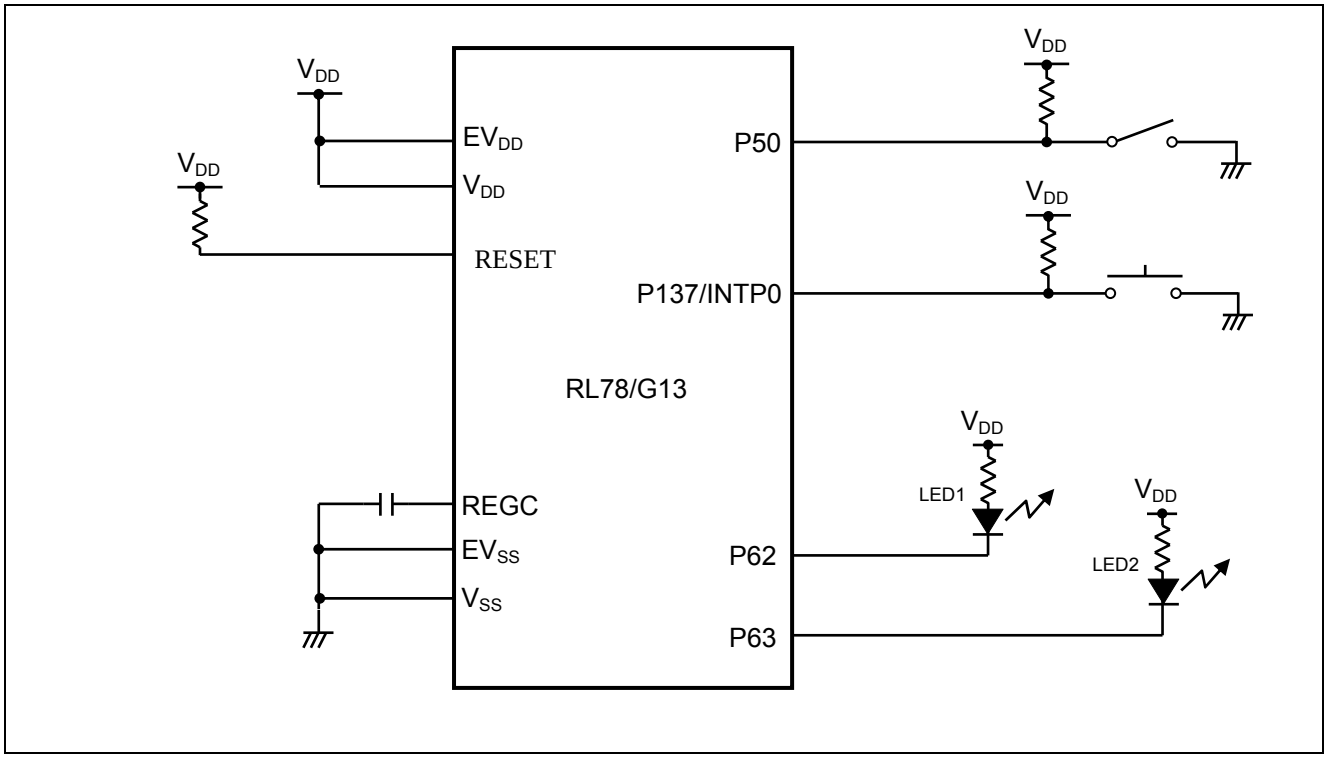


Figure 4.1 Hardware Configuration

Cautions:
1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).
2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their functions.

Table 4.1 Pins to be Used and their Functions

Pin Name	I/O	Description
P50	Input	General-purpose CRC operation target data switching input (changed/no change)
P62	Output	LED1 lighting control port (high-speed CRC operation result output)
P63	Output	LED2 lighting control port (general-purpose CRC operation result output)
P137/INTP0	Input	General-purpose CRC operation start trigger input

5. Description of the Software

5.1 Operation Outline

The sample application covered in this application note uses the flash memory CRC operation function, which is one of the safety functions incorporated in the RL78/G13.

The high-speed CRC performs operation on and compares the data in the code flash memory (addresses 00000H to 0FFFBH) with the results of the operation performed by the object converter.

The general-purpose CRC performs operation on the data in a part of the on-chip RAM and compares their results with the results of the operation performed again in the same area. The data to be operated on can be changed by using switch input.

Both of the high-speed CRC and general-purpose CRC turn on an LED when the results of the operation match.

(1) Initialize the flash memory CRC operation function.
<Conditions for setting>
- Set the range of the area on which high-speed CRC operation is to be performed to the flash memory (addresses 00000H to 0FFFBH).
- Set the operation mode of the high-speed CRC to "Start operation on the execution of a HALT instruction."

(2) Initialize the operation control ports.
<Conditions for setting>
- General-purpose CRC operation target data switching: Set up P50 as an input port (using an external pull-up resistor).
- LED1 /2 output (CRC operation true-false determination result): Set up P62 and P63 as output ports.
- General-purpose CRC operation start trigger button: Set up P137/INTP0 in INTP0 falling edge detection interrupt mode (using an external pull-up resistor).

(3) Perform high-speed CRC operation on the flash memory (addresses 00000H to 0FFFBH).
(4) Compare the results obtained in step (3) with the target values (specified in advance at build time) that are generated in the flash memory (addresses 0FFFCH to 0FFFDH) by the object converter and turns on LED1 if they match.
(5) Store arbitrary data and the results of general-purpose CRC operation in the general-purpose CRC operation target area (part of the on-chip RAM).
(6) Enter the HALT mode and waits for a general-purpose CRC operation start trigger (INTP0).
(7) Exit the HALT mode on the occurrence of a CRC operation start trigger and update the general-purpose CRC operation target data if the state of the general-purpose CRC operation target data switch is "Changed."
(8) Perform general-purpose CRC operation.
(9) Turn on LED2 if the results obtained in step (8) match the ones obtained in step (5). Otherwise, turn off the LED2.
(10) Repeat steps (5) to (9).

Cautions: 1. When building the application, disable on-chip debugging with the link option. This is because addresses 0FFFCH to 0FFFDH which are to be used to store the results of high-speed CRC operation as the target of comparison are also reserved for the on-chip debugger and a conflict would otherwise occur.
2. When checking the application for normal operation, write HEX data into the RL78/G13 using a flash memory programmer that is compatible with the RL78/G13.
3. For detailed usage notes on the product, refer to RL78/G13 User's Manual: Hardware.

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H/010C0H	11101111B	Disables the watchdog timer. (Stops counting after the release from the reset status.)
000C1H/010C1H	01111111B	LVD reset mode which uses 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	00000100B	Prohibits the on-chip debugger.

5.3 List of Constants

Table 5.2 lists the constants that are used in this sample program.

Table 5.2 Constants for the Sample Program

Constant	Setting	Description
HIGHSPEED_CALC_ADDR	0x0FFFC	Address at which the results of the high-speed CRC operation generated by the object converter are to be stored
GP_CALC_BUFF_SIZE	254	Size of the general-purpose CRC operation target buffer (excluding the 2 bytes in the area storing operation result)

5.4 List of Variables

Table 5.3 lists the global variable that is used by this sample program.

Table 5.3 Global Variable

Type	Variable Name	Contents	Function Used
uint8_t	calc_data[GP_CALC_BUFF_SIZE+2]	Area for storing the general-purpose CRC operation target data	main R_CreateDataForComparison R_GeneralPurposeCRCProc

5.5 List of Functions

Table 5.4 lists the global functions that are used by this sample program.

Table 5.4 Functions

Function Name	Outline
R_HighSpeedCRCProc	High-speed CRC operation processing
R_ExecHighSpeedCRC	Execution of high-speed CRC operation
R_CreateDataForComparison	Creation of general-purpose CRC operation target data
R_GeneralPurposeCRCProc	General-purpose CRC operation processing

5.6 Function Specifications

Shown below are the functions that are used in this sample program.

[Function Name]] R_HighSpeedCRCProc

Synopsis	High-speed CRC operation processing
Header	—
Declaration	uint16_t R_HighSpeedCRCProc(void)
Explanation	This function performs high-speed CRC operation and returns the results.
Arguments	None
Return value	Results of high-speed CRC operation
Remarks	None

[Function Name] R_ExecHighSpeedCRC

Synopsis	Execution of high-speed CRC operation
Header	—
Declaration	void R_ExecHighSpeedCRC(void)
Explanation	This function expands the HALT and RET instructions in the on-chip RAM (stack area) to start high-speed CRC operation. This function also executes the HALT and RET instructions that are expanded in the on-chip RAM.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_CreateDataForComparison

Synopsis	Creation of general-purpose CRC operation target data	
Header	—	
Declaration	void R_CreateDataForComparison(uint8_t *data, uint8_t size)	
Explanation	This function creates the target data to be subjected to general-purpose CRC operation. Performs general-purpose CRC operation on that data and places the results in the given area.	
Arguments	*data	Pointer to the area storing the target data
Return value	size	Size of the area storing the target data
Remarks	None	
Synopsis	None	

[Function Name] R_GeneralPurposeCRCProc

Synopsis	General-purpose CRC operation processing	
Header	—	
Declaration	uint16_t R_GeneralPurposeCRCProc(uint8_t *data, uint8_t size)	
Explanation	This function performs general-purpose CRC operation and returns the results.	
Arguments	*data	Pointer to the target data
	size	Size of the target data
Return value	Result of the general-purpose CRC operation	
Remarks	None	

5.7 Flowcharts

5.7.1 Overall Flow

Figure 5.1 shows the overall flow of the sample program described in this application note.

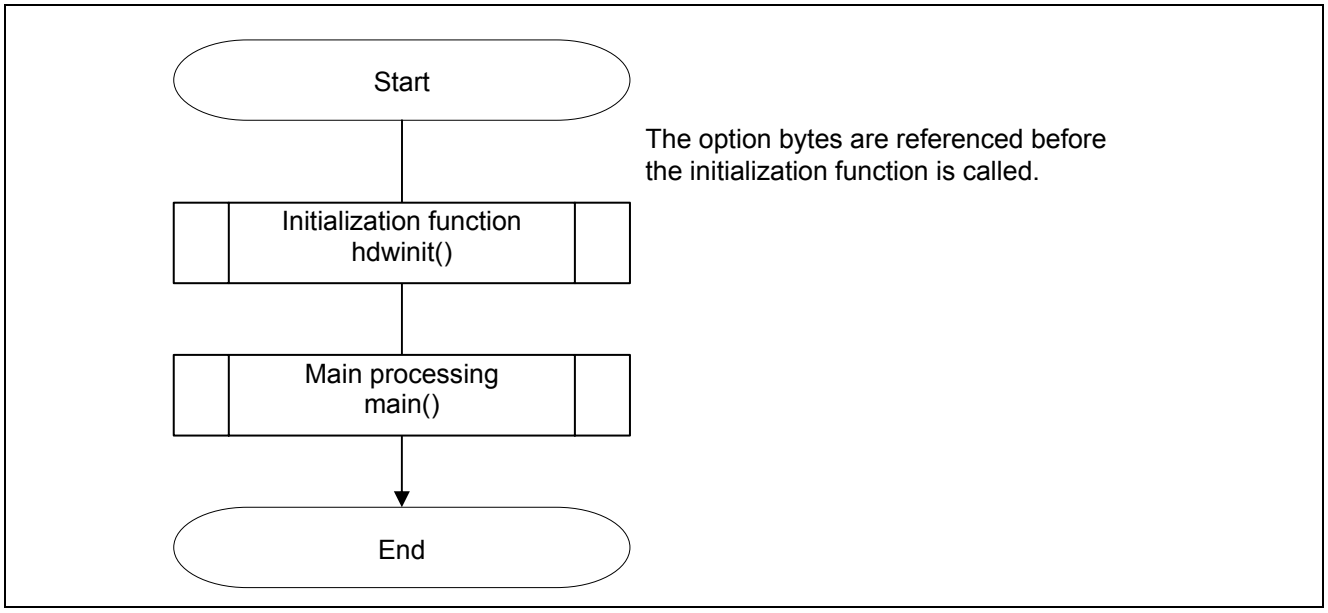


Figure 5.1 Overall Flow

5.7.2 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

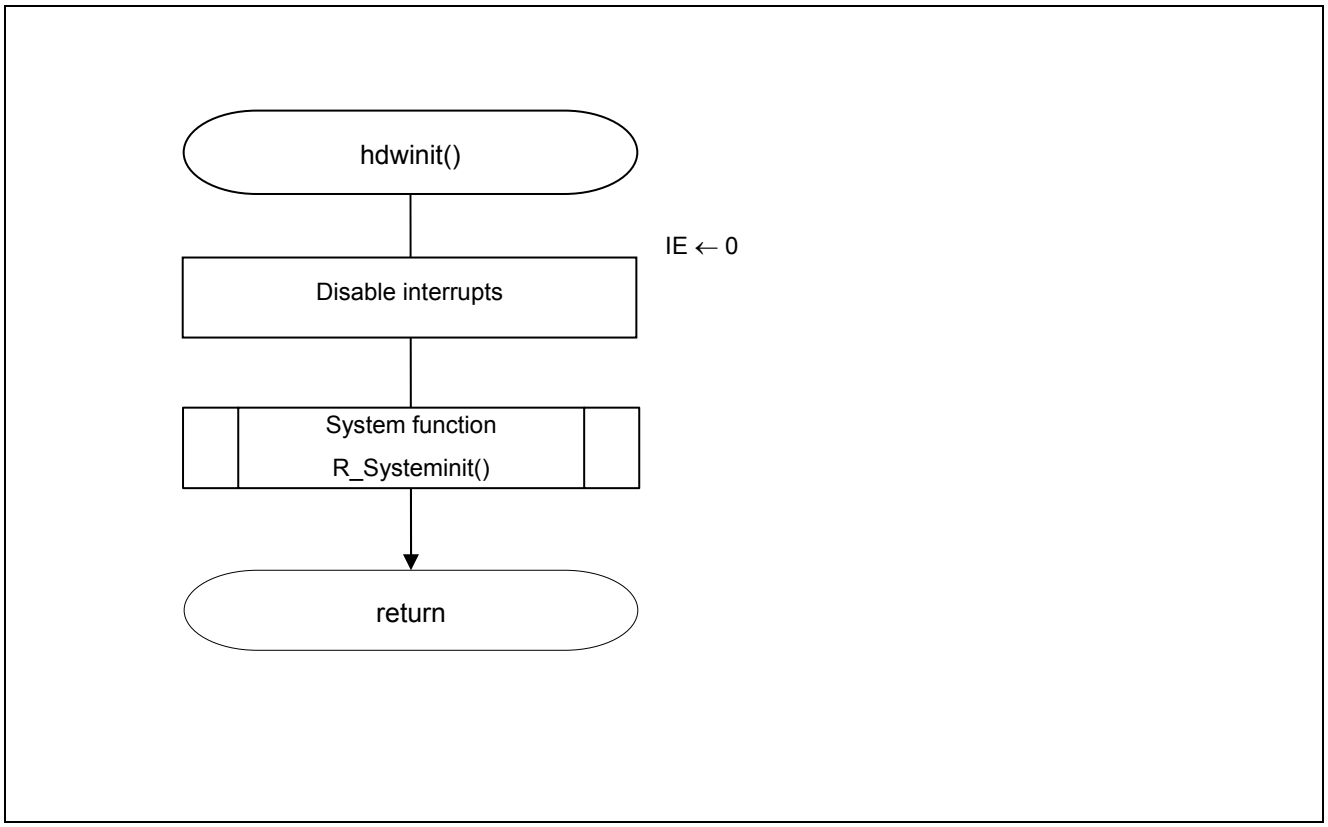


Figure 5.2 Initialization Function

5.7.3 System Function

Figure 5.3 shows the flowchart for the system function.

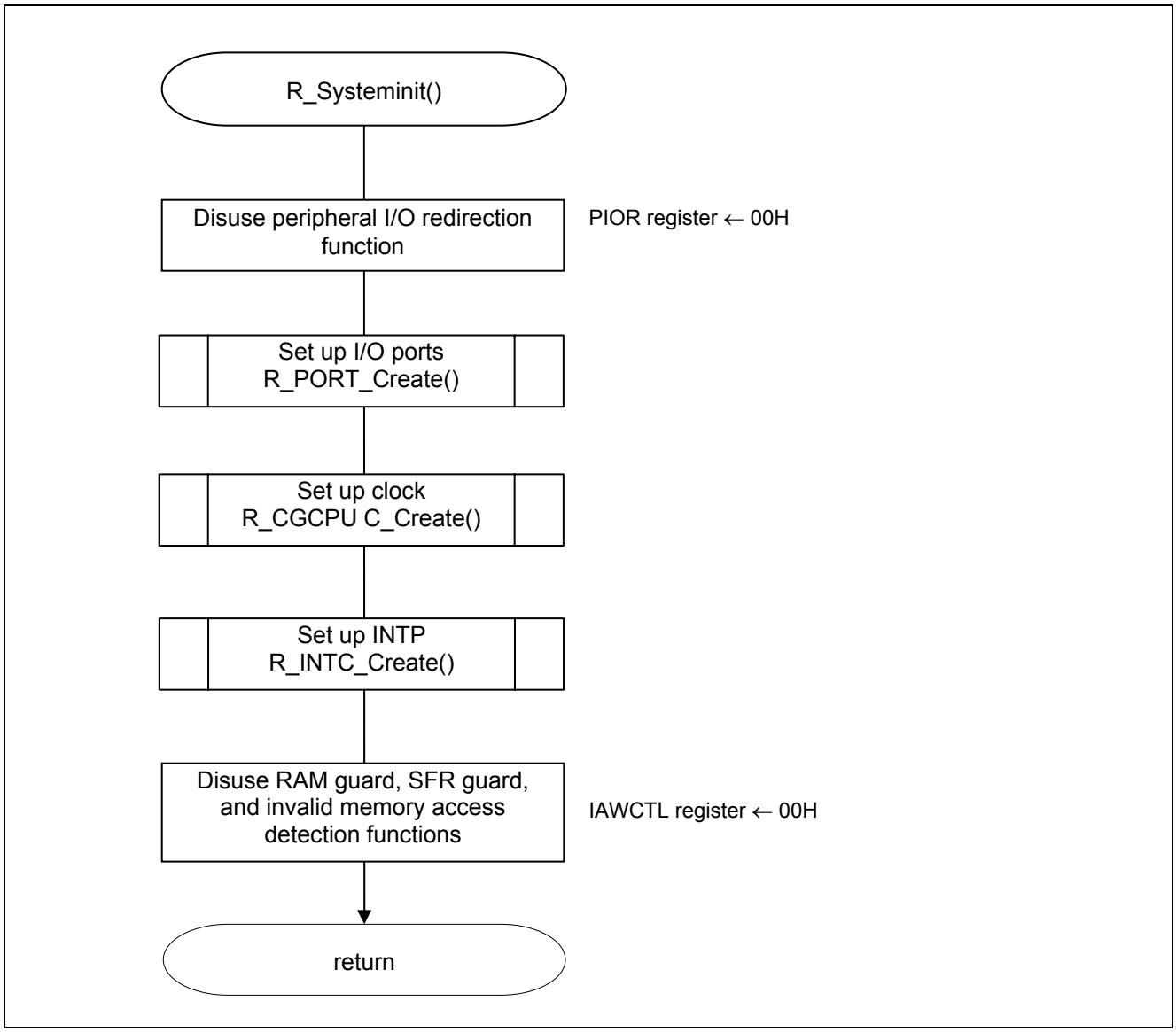


Figure 5.3 System Function

5.7.4 I/O Port Setup

Figure 5.4 shows the flowchart for setting up the I/O ports.

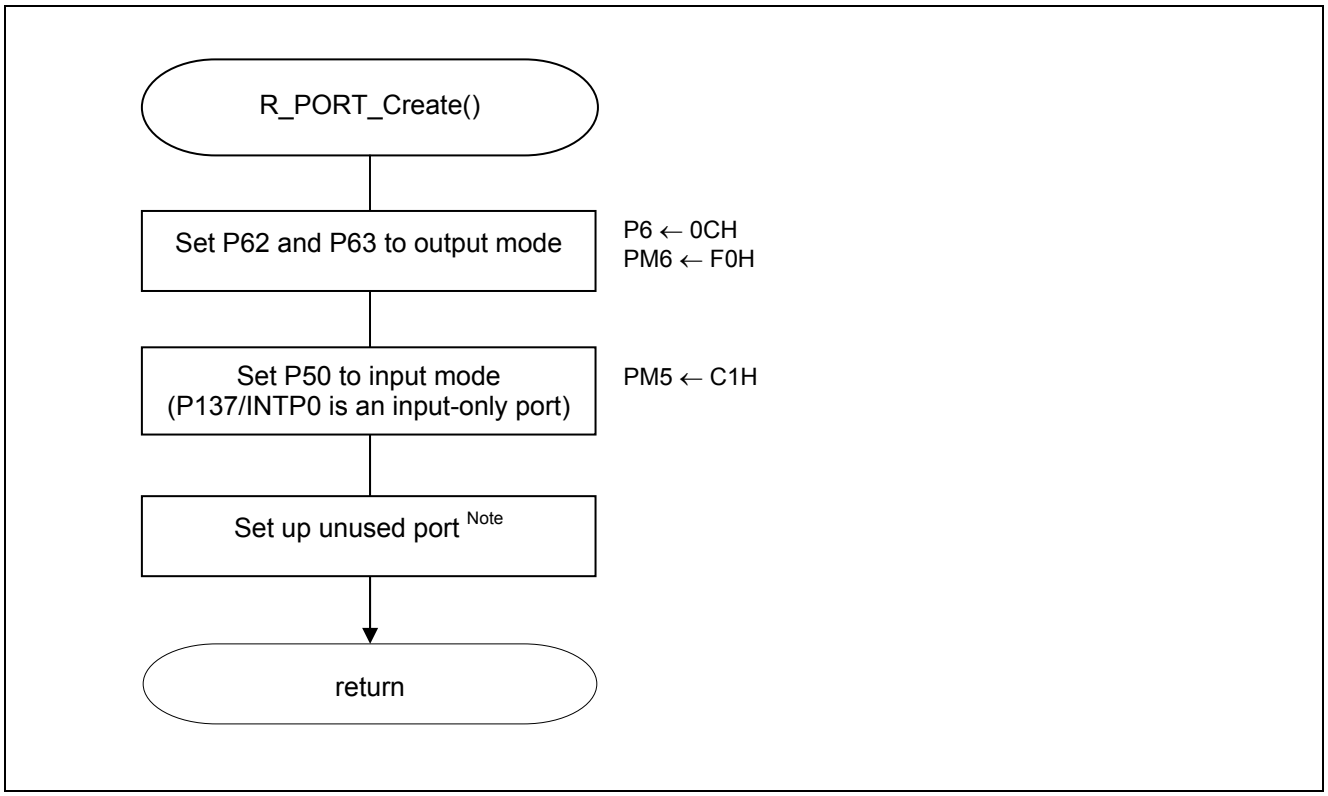


Figure 5.4 I/O Port Setup

Note: Refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E) for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are met. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

Setting up LED ports

- Port register (P6)
  Select the output level of P62 and P63.
- Port mode register (PM6)
  Select the I/O mode of the ports for PM62 and PM63.

Symbol: P6

7	6	5	4	3	2	1	0
P67	P66	P65	P64	P63	P62	P61	P60
x	x	x	x	**1**	**1**	x	x

Bit 3

P63	P63 output level selection
0	Low-level output
1	**High-level output**

Bit 2

P62	P62 output level selection
0	Low-level output
1	**High-level output**

Symbol: PM6

7	6	5	4	3	2	1	0
PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60
x	x	x	x	**0**	**0**	x	x

Bit 2

PM62	P62 I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Bit 3

PM63	P63 I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the general-purpose CRC operation target data switch

- Port mode register (PM5)
  Select the I/O mode of P50.

Symbol: PM5

7	6	5	4	3	2	1	0
PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50
x	x	x	x	x	x	x	**1**

Bit 0

PM50	P50 I/O mode selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.5 CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock.

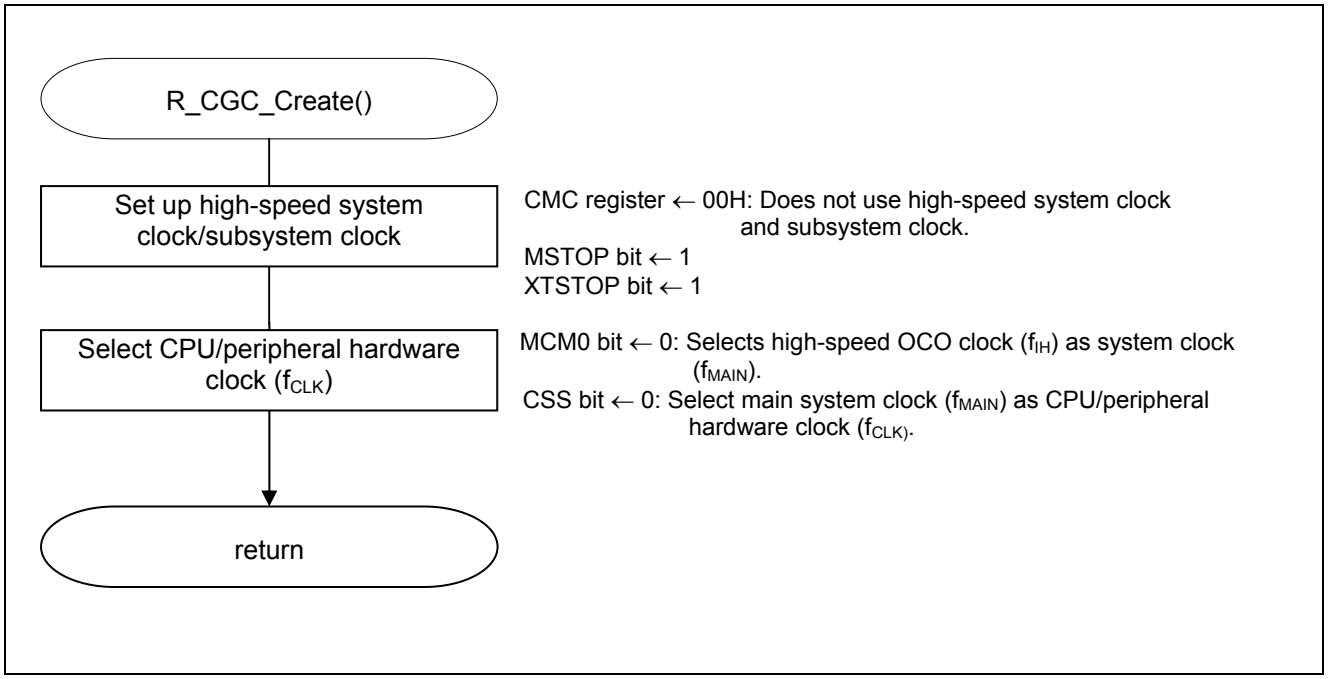


Figure 5.5 CPU Clock Setup

Caution: For details on the procedure for setting up the CPU clock (R_CGC_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E).

5.7.6 INTP0 Initialization

Figure 5.6 shows the flowchart for initializing INTP0.

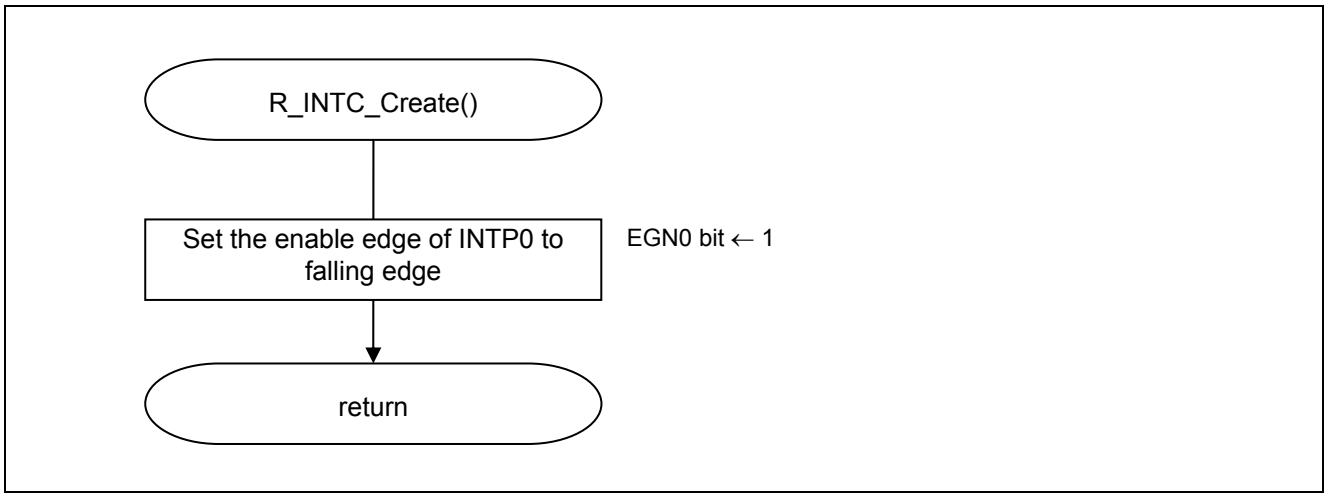


Figure 5.6 INTP0 Initialization

Setting up the INTP0 pin edge detection

- External interrupt rising edge enable register (EGP0)
- External interrupt falling edge enable register (EGN0)
  Enable edge of INTP0: Falling edge

Symbol: EGP0

7	6	5	4	3	2	1	0
EGP7	EGP6	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0
x	x	x	x	x	x	x	**0**

Symbol: EGN0

7	6	5	4	3	2	1	0
EGN7	EGN6	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0
x	x	x	x	x	x	x	**1**

Bit 0

EGP0	EGN0	INTP0 pin enable edge selection
0	0	Edge detection disabled
0	**1**	**Falling edge**
1	0	Rising edge
1	1	Both rising and falling edges

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.7 Main Processing

Figures 5.7 and 5.8 show the flowcharts for main processing.

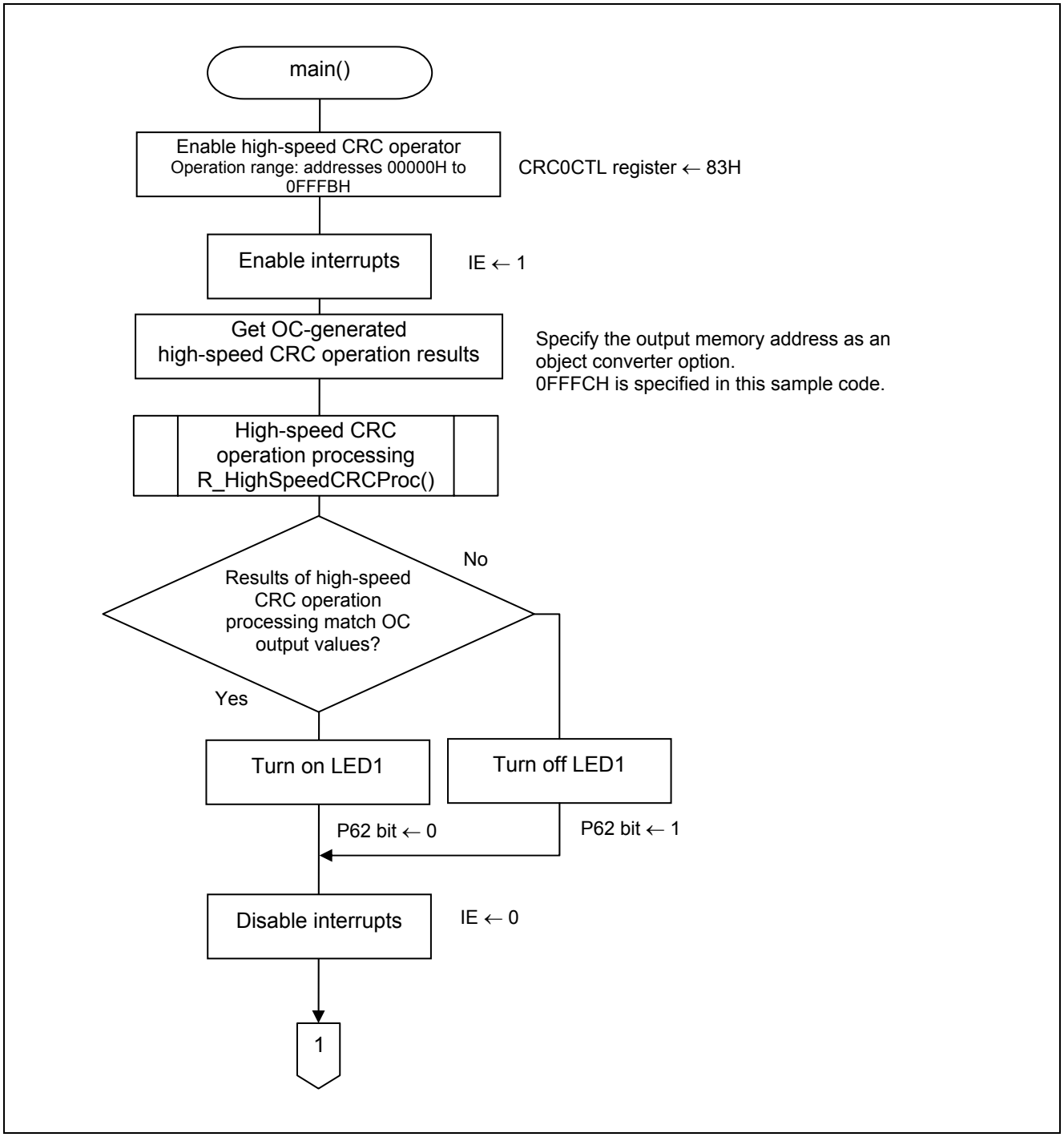


Figure 5.7 Main Processing (1/2)

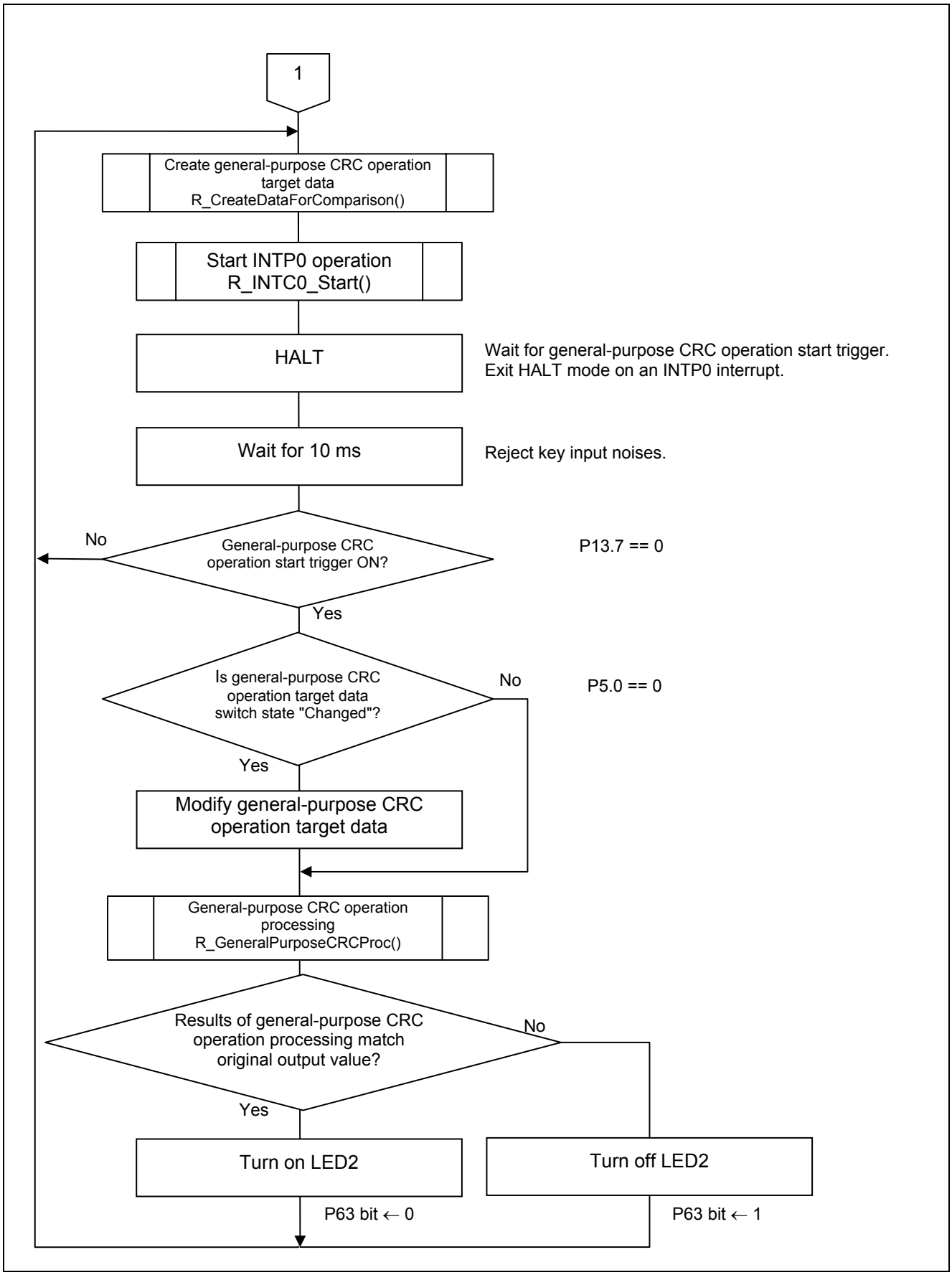


Figure 5.7 Main Processing (2/2)

Controlling the operation of the CRC circuit and specifying the operation range

- Flash memory CRC control register (CRC0CTL)
  Specifies the CRC circuit operation trigger.
  Specifies the CRC operation range.

Symbol: CRC0CTL

7	6	5	4	3	2	1	0
CRC0EN	0	FEA5	FEA4	FEA3	FEA2	FEA1	FEA0
1	0	**0**	**0**	**0**	**0**	**1**	**1**

Bit 7

CRC0EN	Control of CRC circuit operation
0	Stop the operation.
1	**Start the operation according to HALT instruction execution.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Bits 5 to 0

FEA5	FEA4	FEA3	FEA2	FEA1	FEA0	CRC Operation Range
0	0	0	0	0	0	00000H to 03FFBH (16 K to 4 bytes)
0	0	0	0	0	1	00000H to 07FFBH (32 K to 4 bytes)
0	0	0	0	1	0	00000H to 0BFFBH (48 K to 4 bytes)
0	**0**	**0**	**0**	**1**	**1**	**00000H to 0FFFBH (64 K to 4 bytes)**
0	0	0	1	0	0	00000H to 13FFBH (80 K to 4 bytes)
0	0	0	1	0	1	00000H to 17FFBH (96 K to 4 bytes)
0	0	0	1	1	0	00000H to 1BFFBH (112 K to 4 bytes)
0	0	0	1	1	1	00000H to 1FFFBH (128 K to 4 bytes)
0	0	1	0	0	0	00000H to 23FFBH (144 K to 4 bytes)
0	0	1	0	0	1	00000H to 27FFBH (160 K to 4 bytes)
0	0	1	0	1	0	00000H to 2BFFBH (176 K to 4 bytes)
0	0	1	0	1	1	00000H to 2FFFBH (192 K to 4 bytes)
0	0	1	1	0	0	00000H to 33FFBH (208 K to 4 bytes)
0	0	1	1	0	1	00000H to 37FFBH (224 K to 4 bytes)
0	0	1	1	1	0	00000H to 3BFFBH (240 K to 4 bytes)
0	0	1	1	1	1	00000H to 3FFFBH (256 K to 4 bytes)
0	1	0	0	0	0	00000H to 43FFBH (272 K to 4 bytes)
0	1	0	0	0	1	00000H to 47FFBH (288 K to 4 bytes)
0	1	0	0	1	0	00000H to 4BFFBH (304 K to 4 bytes)
0	1	0	0	1	1	00000H to 4FFFBH (320 K to 4 bytes)
0	1	0	1	0	0	00000H to 53FFBH (336 K to 4 bytes)
0	1	0	1	0	1	00000H to 57FFBH (352 K to 4 bytes)
0	1	0	1	1	0	00000H to 5BFFBH (368 K to 4 bytes)
0	1	0	1	1	1	00000H to 5FFFBH (384 K to 4 bytes)
0	1	1	0	0	0	00000H to 63FFBH (400 K to 4 bytes)
0	1	1	0	0	1	00000H to 67FFBH (416 K to 4 bytes)
0	1	1	0	1	0	00000H to 6BFFBH (432 K to 4 bytes)
0	1	1	0	1	1	00000H to 6FFFBH (448 K to 4 bytes)
0	1	1	1	0	0	00000H to 73FFBH (464 K to 4 bytes)
0	1	1	1	0	1	00000H to 77FFBH (480 K to 4 bytes)
0	1	1	1	1	0	00000H to 7BFFBH (496 K to 4 bytes)
0	1	1	1	1	1	00000H to 7FFFBH (512 K to 4 bytes)
Other than above						Setting prohibited

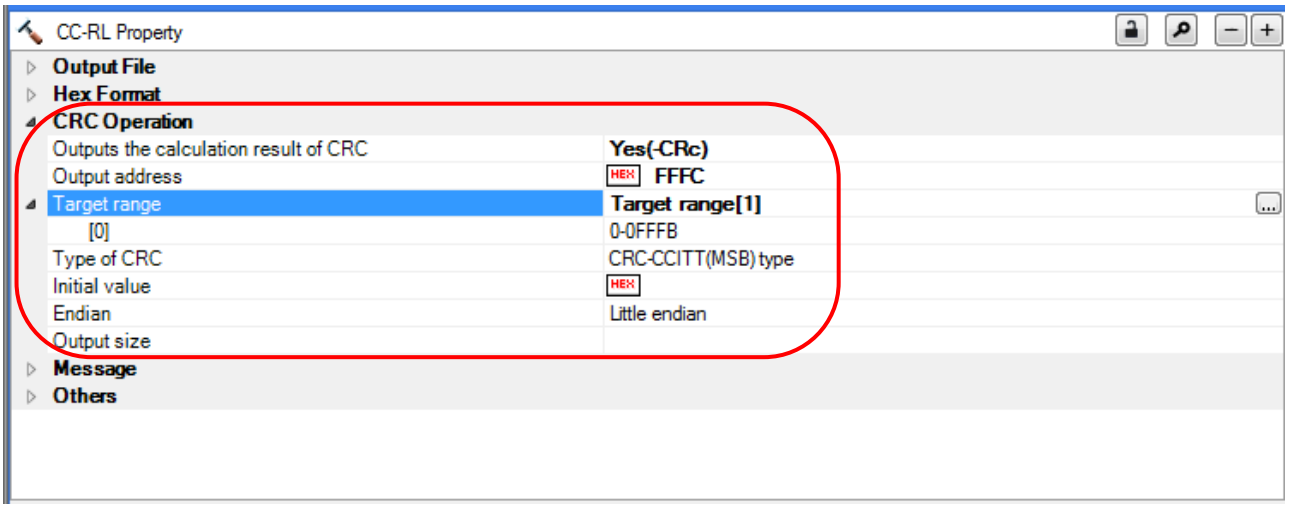
Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Remarks: Input the expected CRC operation value to be used for comparison in the lowest 4 bytes of the flash memory. Note that the operation range will thereby be reduced by 4 bytes.

Object converter option settings

- CRC operation
  Do CRC operation: Yes
  CRC result output address: 0FFFCH
  CRC operation range: Addresses 00000H to 0FFFBH
  CRC operation mode: CRC-CCITT(MSB) type

Object Converter Option Settings (Properties window of CS+ CC-RL build tool)



5.7.8 High-speed CRC Operation Processing

Figure 5. 9 shows the flowchart for the high-speed CRC operation processing.

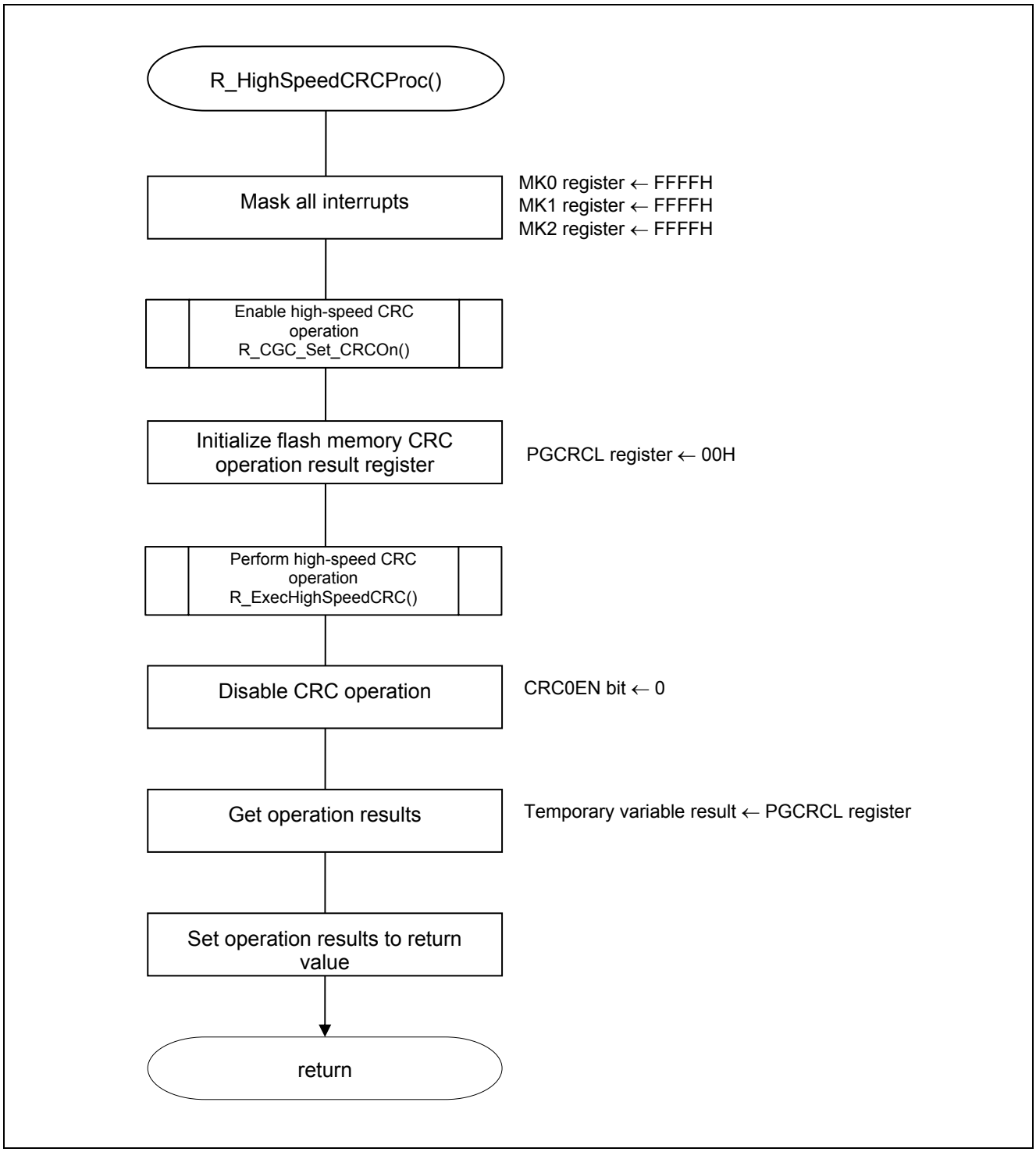
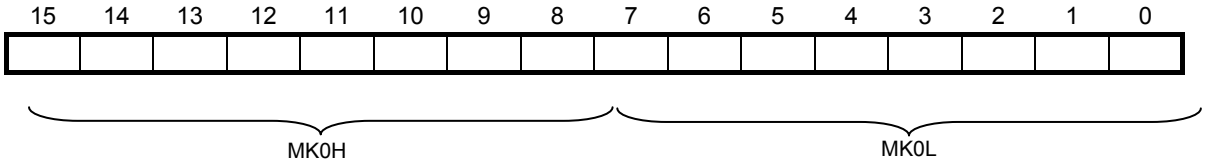


Figure 5.9 High-speed CRC Operation Processing

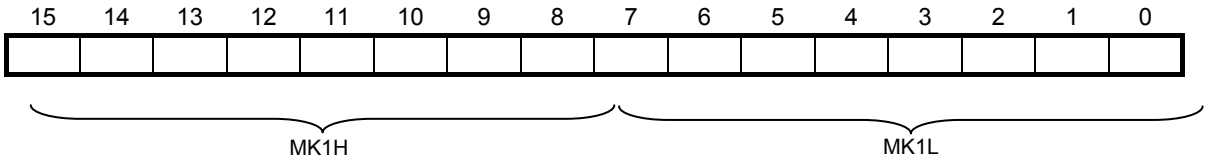
Masking on all interrupts

- Interrupt mask flag registers (MK0, MK1, and MK2)
  Set interrupt masks.

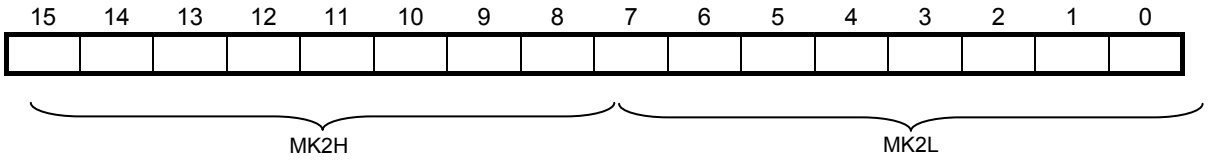
Symbol: MK0



Symbol: MK1



Symbol: MK2



Symbol: MK0L

7	6	5	4	3	2	1	0
PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIMK	WDTIMK
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Symbol: MK0H

7	6	5	4	3	2	1	0
SREMK0 TMMK01H	SRMK0 CSIMK01 IICMK01	STMK0 CSIMK00 IICMK00	DMAMK1	DMAMK0	SREMK2 TMMK11H	SRMK2 CSIMK21 IICMK21	STMK2 CSIMK20 IICMK20
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Symbol: MK1L

7	6	5	4	3	2	1	0
TMMK03	TMMK02	TMMK01	TMMK00	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Symbol: MK1H

7	6	5	4	3	2	1	0
TMMK04	TMMK13	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Symbol: MK2L

7	6	5	4	3	2	1	0
PMK10	PMK9	PMK8	PMK7	PMK6	TMMK07	TMMK06	TMMK05
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Symbol: MK2H

7	6	5	4	3	2	1	0
FLMK	IICAMK1	MDMK	SREMK3 TMMK13H	TMMK12	TMMK11	TMMK10	PMK11
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Bits 7 to 0

XXMKX	Interrupt processing control
0	Interrupt processing enabled
1	**Interrupt processing disabled**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Flash memory CRC operation results

- Flash memory CRC operation result register (PGCRCL)
  Store the high-speed CRC operation results.

Symbol: PGCRCL

15	14	13	12	11	10	9	8
PGCRC15	PGCRC14	PGCRC13	PGCRC12	PGCRC11	PGCRC10	PGCRC9	PGCRC8

7	6	5	4	3	2	1	0
PGCRC7	PGCRC6	PGCRC5	PGCRC4	PGCRC3	PGCRC2	PGCRC1	PGCRC0

Bits 15 to 0

PGCRC15 to 0	High-speed CRC operation results
0000H to FFFFH	Store the high-speed CRC operation results.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.9 Enabling High-speed CRC Operation

Figure 5.10 shows the flowchart for enabling high-speed CRC operation.

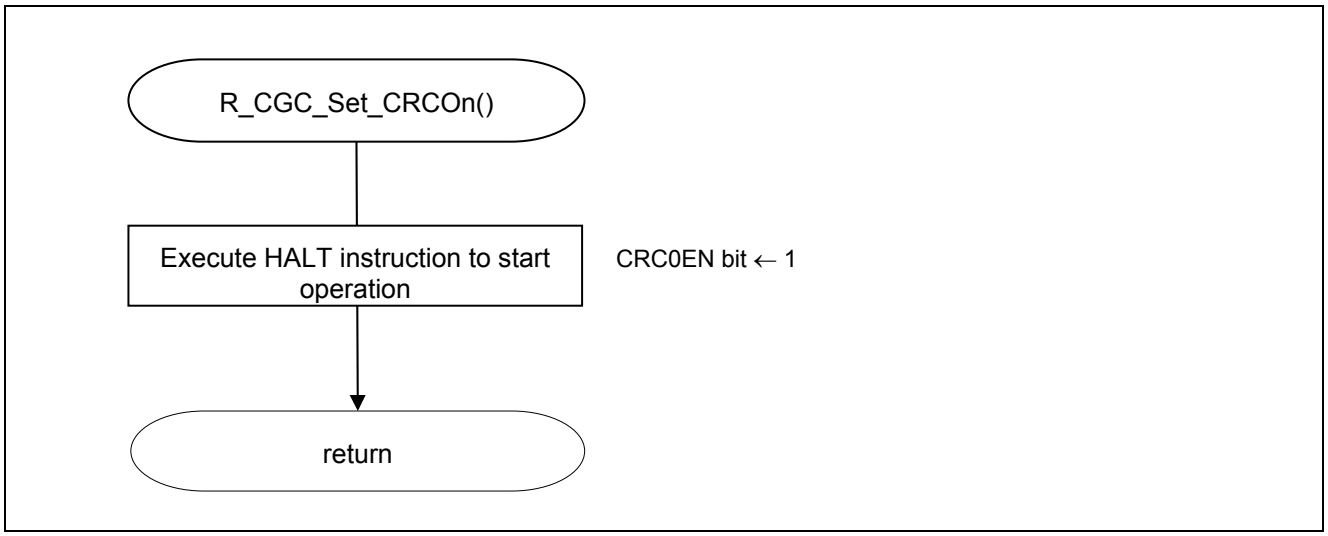


Figure 5.10 Enabling High-speed CRC Operation

5.7.10 Performing High-speed CRC Operation

Figure 5.11 shows the flowchart for performing high-speed CRC operation.

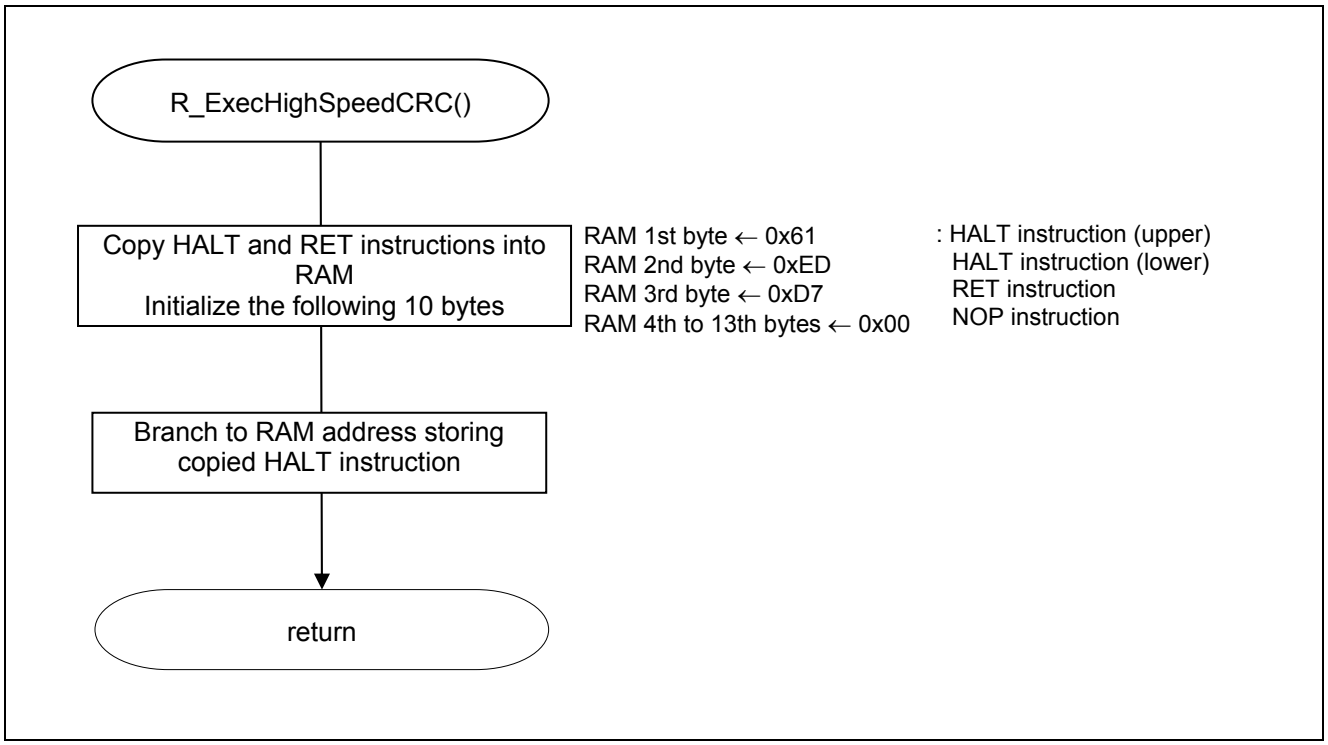


Figure 5.11 Performing High-speed CRC Operation

5.7.11 Creating General-purpose CRC Operation Target Data

Figure 5.12 shows the flowchart for creating general-purpose CRC operation target data.

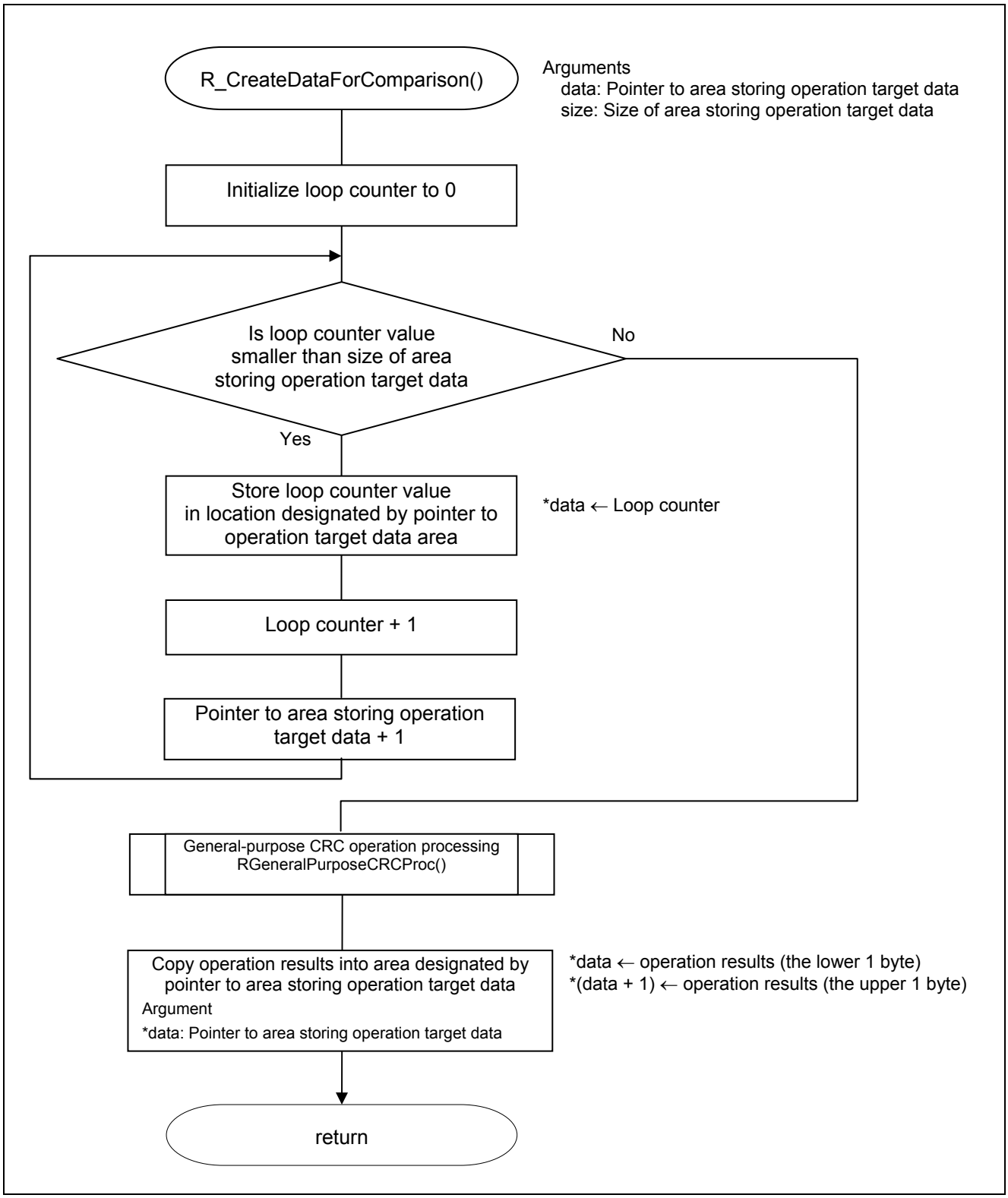


Figure 5.12 Creating General-purpose CRC Operation Target Data

5.7.12 General-purpose CRC Operation Processing

Figure 5.13 shows the flowchart for the general-purpose CRC operation processing.

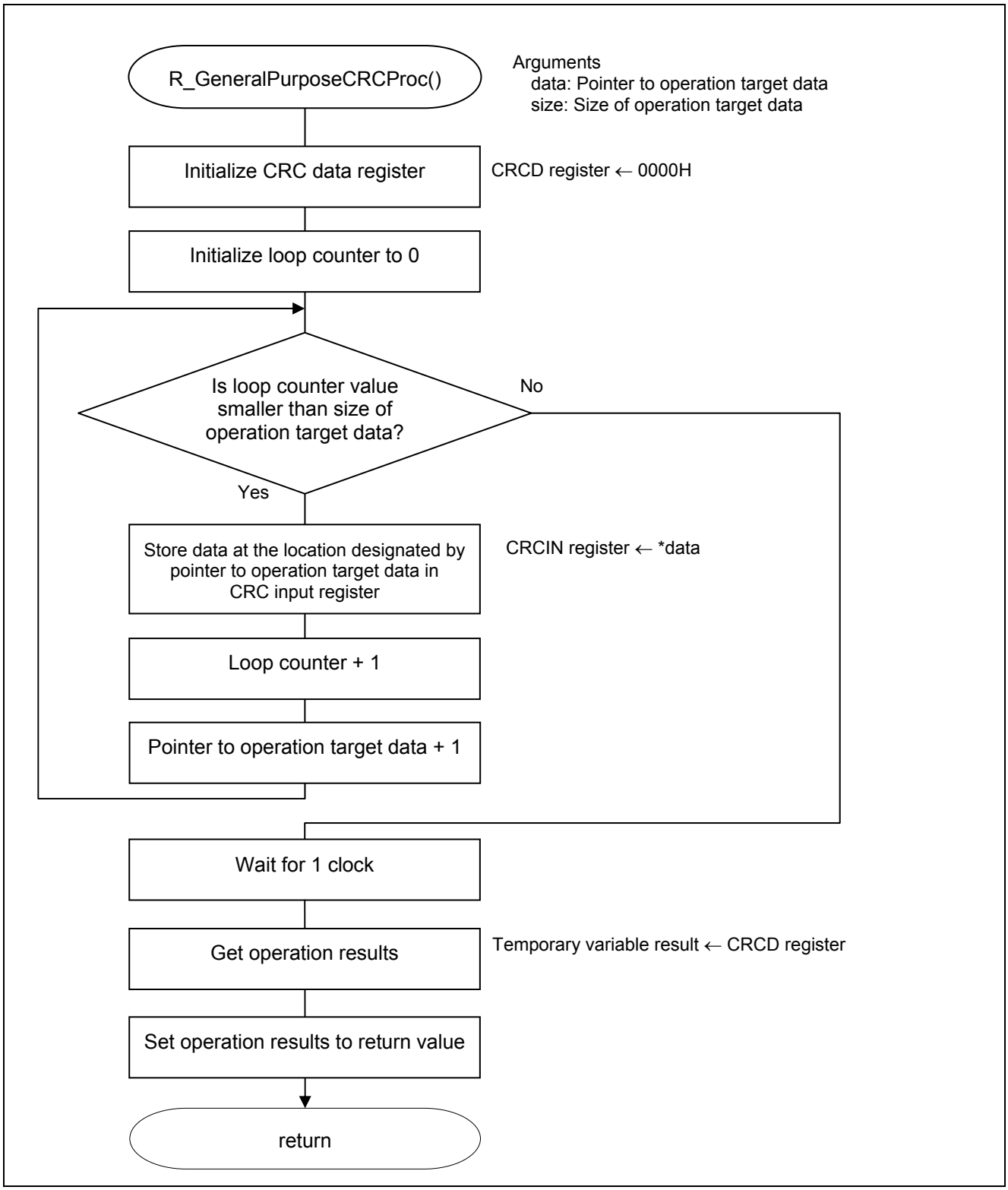


Figure 5.13 General-purpose CRC Operation Processing

General-purpose CRC operation results

- CRC data register (CRCD)
  Store general-purpose CRC operation results.

Symbol: CRCD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

General-purpose CRC calculation data

- CRC input register (CRCIN)
  Store the data to be subject to calculation by the general-purpose CRC.

Symbol: CRCIN

7	6	5	4	3	2	1	0

Bits 7 to 0

Bits 7 to 0	Description
00H to FFH	Input data

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.13 Starting INTP0 Operation

Figure 5.14 shows the flowchart for starting INTP0 operation.

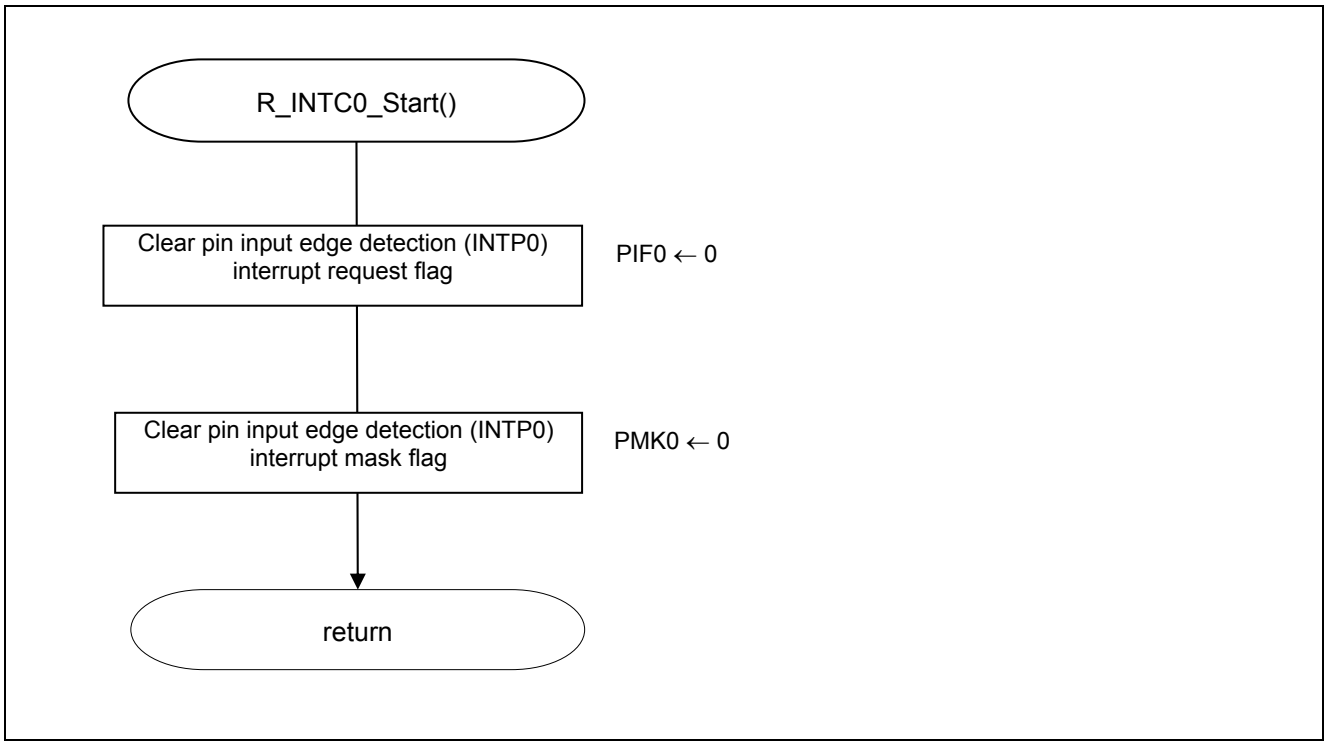


Figure 5.14 Starting INTP0 Operation

Making INTP0 interrupt settings

- Interrupt request flag register (IF0L)
  Clear interrupt request flag.
- Interrupt mask flag register (MK0L)
  Clear interrupt mask

Symbol: IF0L

7	6	5	4	3	2	1	0
PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIIF	WDTIIF
x	x	x	x	x	**0**	x	x

Bit 2

PIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request signal is generated, interrupt request status

Symbol: MK0L

7	6	5	4	3	2	1	0
PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIMK	WDTIMK
x	x	x	x	x	**0**	x	x

Bit 2

PMK0	Interrupt processing control
0	**Interrupt processing enabled**
1	Interrupt processing disabled

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G13 User's Manual: Hardware (R01UH0146E)

RL78 Family User's Manual: Software (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

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Revision Record	RL78/G13 Safety Function (Flash Memory CRC Operation Function)

Rev.	Date	Description	
		Page	Summary
1.00	May 28, 2015	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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