RL78/G13 Group

Multiple PWM generation using DMA CC-RL

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Introduction

In some applications it is required to have a small package with more PWM outputs than available in hardware in the device. The purpose of this application note is to show how to use a Timer and a DMA controller to generate additional PWM outputs.

Target Device

This application has been tested using RL78/G13 target board (QB-R5F100LE-TB) but it is easily portable to any other RL78 device having a DMA unit.

This example uses Timer TAU (Timer Array Unit) 0 Channel 0 and DMA Channel 0 but any other Timer or DMA channel can be used.

Related Application Note

Please refer to the following application note, on which this application note is based:

- RL78/G13 Multiple PWM generation using DMA (R01AN0717EE0100) Application Note

Contents

1. Multiple PWM Generation

1.1 The DMA

The Direct Memory Access controller, or DMA controller, is a peripheral that transfers data between the peripheral hardware supporting DMA, SFRs, and internal RAM without using the CPU. As a result, the normal internal operation of the CPU and data transfer can be executed in parallel allowing simultaneous transfer between the SFR and internal RAM, In addition, real-time control using communication, timer, and A/D can also be implemented.

In this application note eight separate PWM outputs are generated. However more could be added with minor modifications by using additional DMA channels. It is important to note that the PWM outputs have the same time base, so are not fully independent.

The DMA is activated by a peripheral function interrupt to perform data transfers. The DMA and CPU use the same bus, with the DMA taking bus priority over the CPU. Before use, the DMA controller needs a specific configuration to be initialized. This configuration includes a transfer source address, a transfer destination address and operating modes which are allocated in the DMA control registers.

1.2 Application overview

In this application an internal DMA channel is used to modify the contents of the Port7 data register in order to generate the PWM outputs.

Timer TAU (Timer Array Unit) in interval timer mode is used as the trigger source for DMA channel 0 configuration. The frequency of update of the PWM outputs is defined by the Timer TAU Unit 0 Channel 0 period. DMA transfers data from a RAM table, which is updated by the MCU application software, to the P7 port register.

Such operation described in **Figure 1** could also be used to generate specific signals for applications such as High brightness LED drive control, for example.

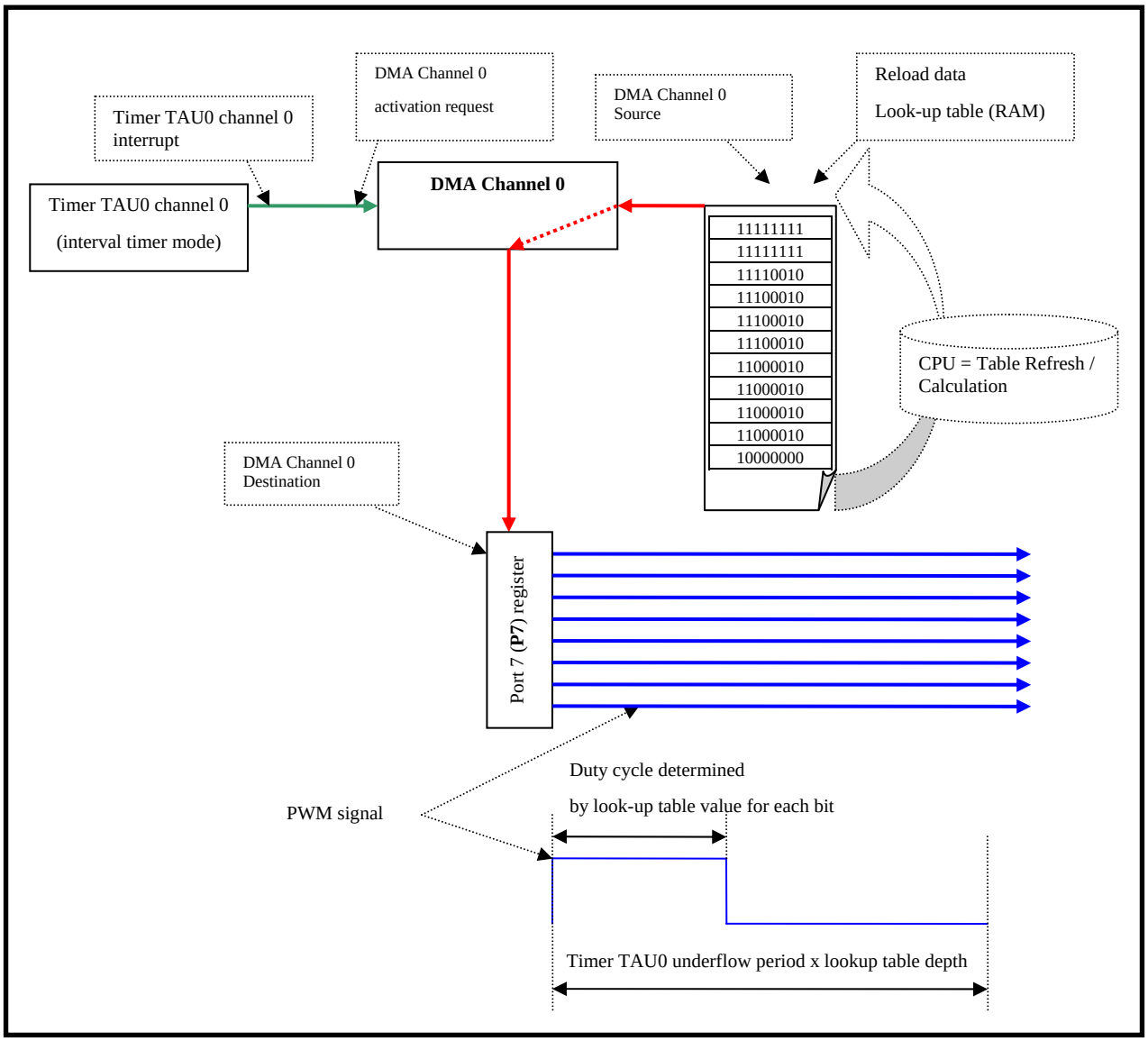


Figure 1 Operation Block Diagram

1.3 Principle

The DMA Channel 0 is configured in order to automatically transfer data from a “PWM look-up table” in RAM memory to the I/O port. The DMA counter is re-initialized by the CPU upon reaching the end of table after the DMA end of transfers interrupt is generated.

The required PWM resolution defines the depth of the “PWM look-up table”. Each PWM output is updated at each Timer TAU0 Channel 0 interrupt (here after called “time unit”). In this application note and code example, an arbitrary choice was made for 8-bit resolution and 8 PWM outputs to port P7, so 256 bytes are needed for the output RAM data.

The “time unit” is defined by Timer TAU0 Channel 0 which triggers DMA Channel 0 at each underflow.

The frequency of the PWM outputs is therefore determined by the frequency of update and the length of the table in RAM used to output to the P7 port register.

PWM frequency = 1/ ((TAU0 Channel 0 period) x (PWM look-up table size in bytes))

1.4 PWM look up table organization

For easier understanding of the PWM Look-up table stored in RAM that the DMA Channel 0 accesses, lets assume 8 PWM outputs are implemented to port P7 and 16 values are used, so the PWM will have a 4-bit resolution.**Table 1** shows a representation of RAM data which is transferred automatically every Timer TAU0 Channel 0 underflow period to P7 data register by the DMA. The relationship between the table values and PWM output generated is as shown in **Figure 2**. The coloured highlighted values indicate where a change in the PWM state occurs.

In this example, bit 7 (b7) will be output to port 7.7, bit 6 (b6) will be output to port 7.6 and bit 1 (b1) will be output to port 7.1.

An advantage for using the look-up table method is to permit different PWM frequencies for each output channel, using the same time base. Very flexible PWM waveforms can be created based on the PWM Look-up table data, extending the functionality from basic PWM to enhanced waveform generation.

The main function of the CPU is the initialization or modification of values in the table. Once this task is done, the DMA performs the transfer of data from the PWM Look-up table to the port independently.

Table 1 PWM Look-up table organization in RAM memory

Table index (address per each time base)	Look-up table data (in RAM)							
	b7	b6	b5	b4	b3	b2	b1	b0
0	1	0	X	X	X	X	1	X
1	1	0	X	X	X	X	1	X
2	1	0	X	X	X	X	1	X
3	1	**0**	X	X	X	X	1	X
4	1	**1**	X	X	X	X	1	X
5	1	1	X	X	X	X	1	X
6	**1**	1	X	X	X	X	1	X
7	**0**	**1**	X	X	X	X	1	X
8	0	**0**	X	X	X	X	1	X
9	0	0	X	X	X	X	1	X
10	0	0	X	X	X	X	1	X
11	0	**0**	X	X	X	X	1	X
12	0	**1**	X	X	X	X	**1**	X
13	0	1	X	X	X	X	**0**	X
14	0	1	X	X	X	X	0	X
15	0	1	X	X	X	X	0	X

Figure 2 shows how the port outputs respond to the data values in the PWM Look-up table after transfer by the DMA. For clarity colored vertical dotted lines are shown where the outputs change state corresponding to the same colored values in PWM loop-up **Table 1**.

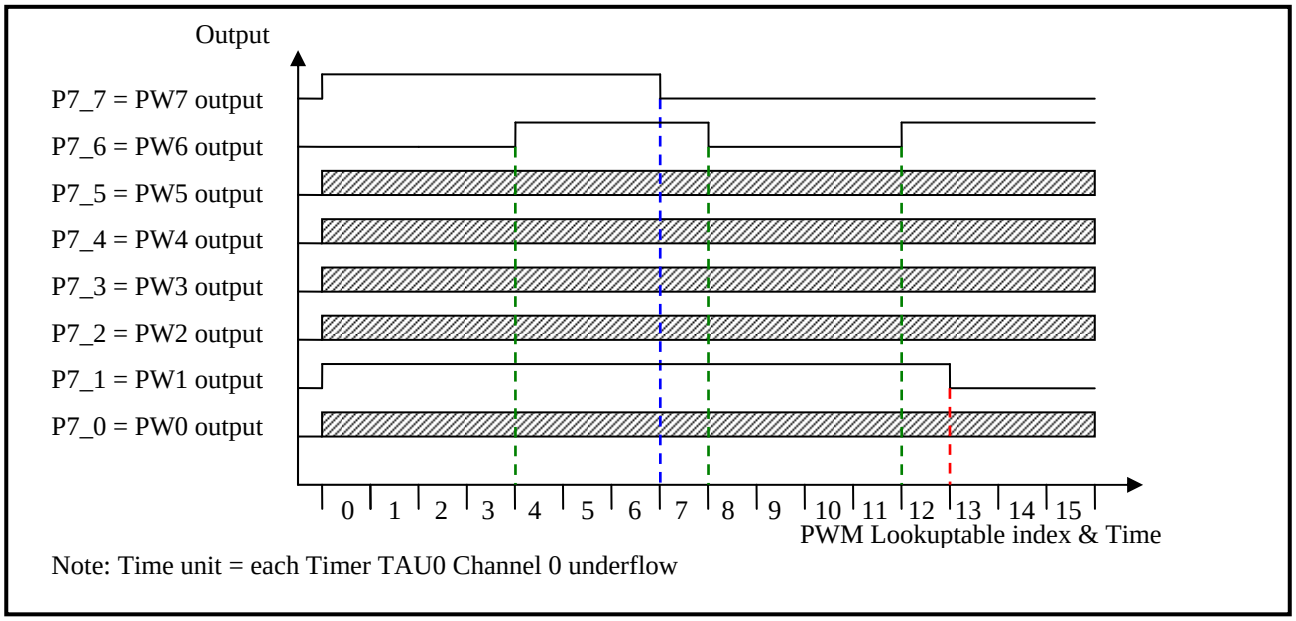


Figure 2 Port output states & PWM Look-up table relationship during DMA transfers

1.5 PWM look-up table calculation

Initialization of the PWM loop-up table is fairly straight forward. In the application software, for each PWM channel number, the look-up table has to be set to 1 from index 0 to N (which indicates high level of each PWM), and then cleared from index N+1 to the maximum index of table. Therefore, let's take an example that the PWM output number 7 is to set with a new value: 156. Let's assume in this example that the PWM resolution is 8-bit, here the PWM look-up table requires 256 entries or indexes. In this case, application software initializes the look-up table as described below:

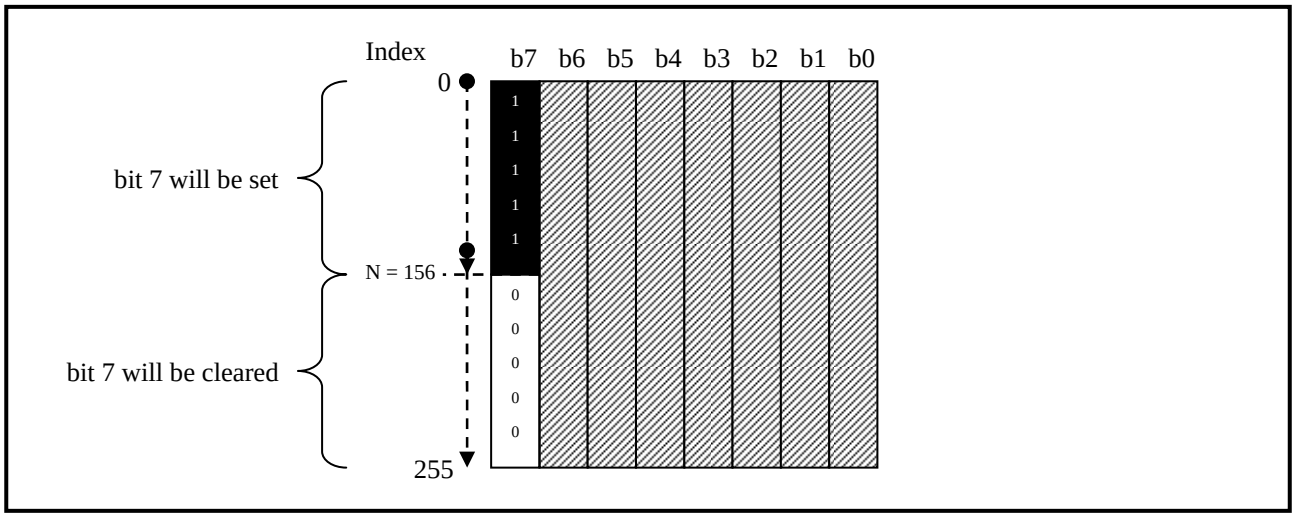


Figure 3 PWM Look-up table initialization for PWM generation

It is also possible to generate other signals waveforms by changing the values in the look-up table, as example programmable wait one-shot signal generation.

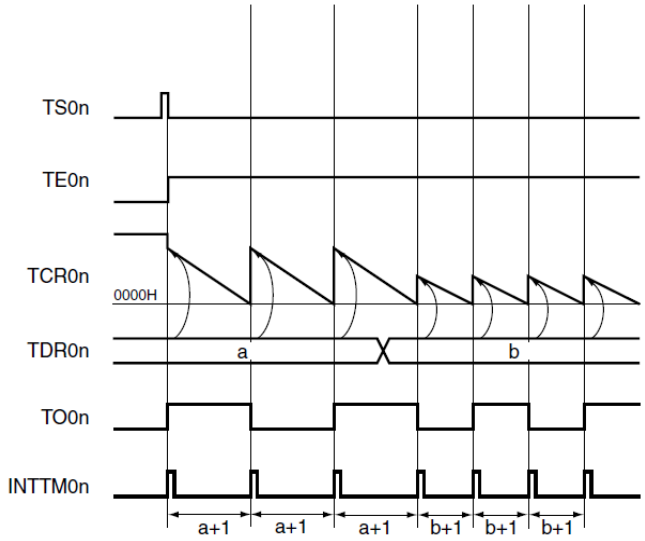
2. Peripheral architecture used for this application

2.1 Timer TAU0 Channel 0, operation timing in interval timer mode

The RL78/G13 has a number of timers integrated. The timer array unit has eight 16-bit timers. Each 16-bit timer is called a channel and can be used as an independent timer. Timer Array Unit 0 Channel 0 in interval timer mode is selected to trigger the DMA. In this mode TAU counts an internally generated count source and can be used as a reference timer that generates INTTM00 (timer interrupt) at fixed intervals. When the timer underflows, the contents of the TDR00 register is copied into the count source register and the count is then continued, as shown in the **Figure 4.**

The interrupt generation period can be calculated by the following expression:

Generation period of INTTM0n (timer interrupt) = Period of count clock x (Set value of TDR0n + 1)



Remarks 1. n: Channel number (n = 0 to 7)

2. TS0n: Bit n of timer channel start register 0 (TS0)
   TE0n: Bit n of timer channel enable status register 0 (TE0)
   TCR0n: Timer/counter register 0n (TCR0n)
   TDR0n: Timer data register 0n (TDR0n)
   TO0n: TO0n pin output signal

Figure 4 Operating Example of TAU when Counter Value (TDR0n) is Rewritten during Count Operation

The underflow period of TAU is the base of DMA activation for PWM generation in this application note. In addition, TAU configuration has to be carried out with consideration to its underflow frequency as this has an impact on the internal bus load. In other terms more frequently transfers are done, less bus bandwidth is left for CPU activity.

2.2 DMA, operation and configuration

When a software trigger (STG0 for DMA Channel 0) or a start source trigger specified by the IFC03 to IFC00 bits is input, a DMA transfer is started. At each trigger i.e. TAU0 Channel 0 underflow, the DMA transfers data from source address to destination address accordingly with registers DMC0 (DMA channel 0 mode control), DRC0 (DMA channel 0 operation control) and DBC0 (DMA channel 0 count) settings.

Here are the main RL78/G13 DMA characteristics and impact in this application note:

- The unit of transfer can be 8 or 16 bits. In this application note, the output port for PWM generation is port 7, as a consequence size of transfer is 8 bits.
- The maximum number of transfers is 1024. Each time a DMA transfer has been executed, a register representing this number is automatically decremented. It is the DBC0 register. By reading this DBC0 register during DMA

transfer, the remaining number transfer remaining can be indentified. However, this register cannot be modified by the application software during DMA transfer. In this application example, the number of transfer is chosen as 256.

- The Transfer type is 2-cycle as one transfer is processed in 2 clocks and the CPU stops during that processing.
- The transfer mode available with RL78/G13 DMA is single-transfer. In other words, at each trigger one transfer of data (8 or 16 bit) is done.
- The request for transfer is selectable from different peripheral hardware interrupts like A/D converter, serial interface and as in this application example timer TAU0 Channel 0.
- The transfer takes place between internal RAM and SFR.

2.3 Increasing PWM resolution

The number of transfers in this application example was selected to be 256, which equals 8-bit resolution for each PWM output.

The maximum PWM resolution is 10-bit, which corresponds to the maximum number of 1024 DMA transfers.

DMA operation and timings have to be taken in consideration as they impact the internal bus bandwidth and PWM generation capability.

2.4 Bus load

2 cycles are needed for each transfer every Timer TAU0 Channel 0 underflow. In addition DMA Channel 0 has to be reconfigured at each completion of total transfer). The DMA re-initialization is done in the DMA Channel 0 interrupt service routine.

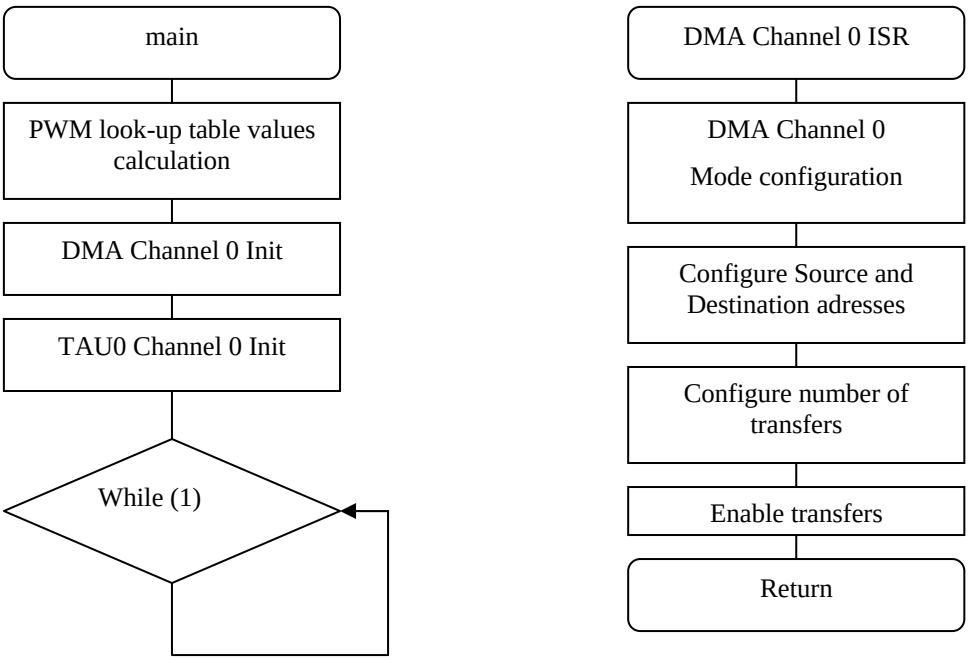
3. Conclusion

Use of the DMA, an I/O port and a PWM look-up table allows for additional PWM channels to be implemented at no additional cost.

Eight PWM's with 8-bit resolution at 2kHz can easily be produced, using a single DMA channel, an 8-bit I/O port, 1 timer and less than 10% CPU bus bandwidth (2cycles for transfer every Timer TAU0 Channel 0 underflow and DMA Channel 0 reconfiguration every 256 transfers).

Care has to be taken, though, that the frequency of the PWMs allows sufficient bandwidth for the CPU to execute the application software without impact.

4. Flowcharts



5. Appendix: Code listing

```
void main(void)
{
    uint8_t i = 0U;
    int bit_number = 0;
    int k = 0;

    __low_level_init();
    EI();// enable interrupt

    /* Set initial values for the 8 PWM channels */
    pwm_dutycycle[0U] = 1U;
    pwm_dutycycle[1U] = 64U;
    pwm_dutycycle[2U] = 96U;
    pwm_dutycycle[3U] = 128U;
    pwm_dutycycle[4U] = 160U;
    pwm_dutycycle[5U] = 192U;
    pwm_dutycycle[6U] = 224U;
    pwm_dutycycle[7U] = 250U;

    /* Scan 8 PWM channels */
    for (i = 0U, bit_number = 1; i < 8U; i++)
    {
        /* Start at high value */
        k = MAX_TABLE - 1;
        /* if PWM register content is different from highest value */
        if (pwm_dutycycle[i] < (MAX_TABLE - 1U))
        {
            for (;k >= pwm_dutycycle[i]; k--)
            {
                /* Clear bit to zero (0) from Max-table to PWM value */
                PWM0_7[k] &= ~bit_number;
            }
        }
        if (pwm_dutycycle[i] > 0U)
        {
            for (;k >= 0; k--)
            {
                /* Set bit to one (1) from PWM value to 0 */
                PWM0_7[k] |= bit_number;
            }
        }
        /* Next bit position */
        bit_number <<= 1;
    }

    DMA0_Init();
    TAU00_Init();

    while (1U)
    {
      ;
    }
}
```

```
/***********************************************************************
* Function Name : DMA0_Init
* Description : DMA Channel 0 initialization
* Argument : none
* Return Value : none
* Calling Functions : none
***********************************************************************/
void DMA0_Init(void)
{
  /* DMA operation enable
     b7 DMA operation enable bit
     b6:b1 Reserved set to 0
     b0 DMA transfer mode bit
  */
  DRC0 = 0x80U;

  NOP();// no operation
  NOP();// no operation

  /* Disable INTDMA0 interrupt */
  DMAMK0 = 1U;
  /* Set INTDMA0 low priority */
  DMAPR10 = 1U;
  DMAPR00 = 1U;
  /* Configure DMA
     b7 DMA transfer start software trigger
     b6 Selection of DMA transfer direction : RAM to SFR
     b5 Specification of transfer data size for DMA transfer : 8 bits
     b4 Pending of DMA transfer
     b3:b0 Selection of DMA start source (IFC03-0) : INTTM00
  */
  DMC0 = 0x42U;
  /* Configure DMA Channel 0 SFR address register : Port 7 */
  DSA0 = 0x07U;
  /* Configure DMA Channel 0 RAM address register : PWM0_7[MAX_TABLE] look-up table */
  DRA0 = (uint16_t)&PWM0_7;
  /* Configure DMA Channel 0 byte count register : 256 */
  DBC0 = 0x0100U;
  /* Clear INTDMA0 interrupt flag */
  DMAIF0 = 0U;
  /* Enable INTDMA0 interrupt */
  DMAMK0 = 0U;
  /* Start DMA Channel 0 operations */
  DST0 = 1U;
}
```

```
/***********************************************************************
* Function Name : TAU00_Init
* Description : TAU Unit 0 Channel 0 initialization
* Argument : none
* Return Value : none
* Calling Functions : none
***********************************************************************/
void TAU00_Init(void)
{
    /* Supplies input clock to TAU Unit 0 */
    TAU0EN = 1U;
    /* Configure format of Timer Clock Select register : fClk */
    TPS0 = 0x0000U;
    /* Stop all channels */
    TT0 = 0x0AFFU;
    /* Configure TAU0 Channel 0 in Interval timer mode */
    TMR00 = 0x0000U;
    /* Configure TAU0 Channel 0 period for PWM frequency around 2kHz */
    TDR00 = 0x003EU;
    /* Enable operation (start) trigger of channel 0 */
    TS0 |= 0x0001U;
}

/***********************************************************************
* Function Name : DMA0_isr
* Description : DMA Channel 0 interrupt service routine, relaunch each PWM period
* Argument : none
* Return Value : none
* Calling Functions : none
***********************************************************************/
static void __near r_dmac0_interrupt(void)
{
  /* Configure DMA
     b7 DMA transfer start software trigger
     b6 Selection of DMA transfer direction : RAM to SFR
     b5 Specification of transfer data size for DMA transfer : 8 bits
     b4 Pending of DMA transfer
     b3:b0 Selection of DMA start source (IFC03-0) : INTTM00
  */
  DMC0 = 0x42U;
  /* Configure DMA Channel 0 SFR address register : Port 7 */
  DSA0 = 0x07U;
  /* Configure DMA Channel 0 RAM address register : PWM0_7[MAX_TABLE] look-up table */
  DRA0 = (uint16_t)&PWM0_7;
  /* Configure DMA Channel 0 byte count register : 256 */
  DBC0 = 0x0100U;
  /* Start DMA Channel 0 operations */
  DST0 = 1U;
}
```

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		Description	
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