RL78/G13

High-speed On-chip Oscillator (HOCO) Clock Frequency Correction CC-RL

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Introduction

This application note explains how to correct the oscillation clock frequency of the high-speed on-chip oscillator (HOCO) by using the high-speed on-chip oscillator trimming register (HIOTRM) incorporated in RL78/G13.

An error in the oscillation frequency of the high-speed on-chip oscillator (HOCO) is detected using a subsystem clock or an external input signal and the high-speed on-chip oscillator trimming register (HIOTRM) is adjusted to set the oscillation frequency of the HOCO close to 32 MHz.

Target Device

RL78/G13

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

In this application note, an error in the clock oscillation frequency of the HOCO is detected using a subsystem clock or an external input signal. Then, the HIOTRM register is adjusted to set the oscillation frequency of the HOCO close to 32 MHz.

Whether to use the subsystem clock or the external input signal is determined by the parameter switch. When the start switch is pressed, the timer array unit (TAU) counts the frequency (pulse interval) or the pulse width of the subsystem clock or the external input signal. The HOCO is used for the count clock of the TAU. If the count value measured by the TAU is beyond the target range, the HIOTRM register is adjusted to set the oscillation frequency of the HOCO close to 32 MHz. The HIOTRM register is adjusted so that the count value is within the target range. The target range of the HOCO oscillation frequency is 32 MHz ± 0.1% (31.968 MHz to 32.032 MHz).

When the subsystem clock is used, the TAU measures the frequency (pulse interval) of the subsystem clock. To enhance accuracy, the pulse interval is measured four times to detect an error in the oscillation frequency of the HOCO.

When the external input signal is used, the TAU measures the low-level width of the timer input signal. A signal with a low-level width of 1.953125 ms (256 Hz, a duty cycle of 50%) is used as the timer input signal.

In this sample code, a pulse of 2 MHz ($f_{MAIN}/2^4$) is output from the clock output/buzzer output control circuit to always check correction results. To check the correction results, refer to the frequency of the output pulse on the PCLBUZ0 pin by using a frequency counter and the like.

Caution: Specified times and calibration methods in this sample code are used as examples. In this sample code, input from the start switch is used to start calibration, to simplify processing flows and to provide clear understanding. Adjust the timing of starting calibration and the intervals between start timings according to the system. This application note describes two calibration methods. Select the method most appropriate to the system for use.

Table 1.1 summarizes the peripheral functions to be used and their uses.

Table 1.1 Peripheral Functions to be Used and Their Uses

Peripheral Function	Use
Pin input edge detection interrupt	Used for the correction start switch.
Subsystem clock	Connects the subsystem clock to be used for calibration.
TAU0 channel 1	Used for calibration with the external input signal.
TAU0 channel 2	Used to prevent chattering on the correction start switch.
TAU0 channel 5	Used for calibration with the subsystem clock.
Clock output/buzzer output control circuit	Performs 2-MHz clock output.

1.1 Description of Calibration Methods

This section describes the two calibration methods to be used in this application note.

(1) Calibration with the subsystem clock
A calibration method with the subsystem clock is described below.

The subsystem clock cycle is measured on TAU0 channel 5.

The subsystem clock (32.768 kHz, a cycle of 30.517578125 µs) is selected as the timer input to be used on TAU0 channel 5, and the HOCO clock (32 MHz) is selected as the count clock. The subsystem clock cycle is measured using the input pulse interval measurement function of the TAU.

To enhance accuracy, the subsystem clock cycle is measured four times, and the four captured values are added up to calculate an error in the HOCO oscillation clock frequency.

The table below lists the calculated count values that are obtained through four times of capture when the frequency is 32 MHz, 32 MHz - 0.1% (31.968 MHz), or 32 MHz + 0.1% (32.032 MHz).

Table 1.2 Range of Count Values during the Use of Subsystem Clock

HOCO Clock Frequency (f_{IH})		Count Value Obtained through Four Times of Capture (Calculated Value)
32 MHz		3906.25
32 MHz – 0.1%	31.968 MHz	3902.34375
32 MHz + 0.1%	32.032 MHz	3910.15625

According to table 1.2, the target range of the count value obtained through four times of capture is set to 3903 to 3909 when the target frequency range is 32 MHz ± 0.1% (31.968 to 32.032 MHz). If the obtained count value is 3902 or less, this means that the HOCO clock is slower than the target frequency. If it is 3910 or more, this means that the HOCO clock is faster than the target frequency. Determine the direction of correction of the HIOTRM register value (speeding up/slowing down), according to the count value, and perform calibration by incrementing the HIOTRM register value by ±1. When the count value is within the target range, the calibration is completed.

Figure 1.1 gives an example of calibration in which the subsystem clock is used.

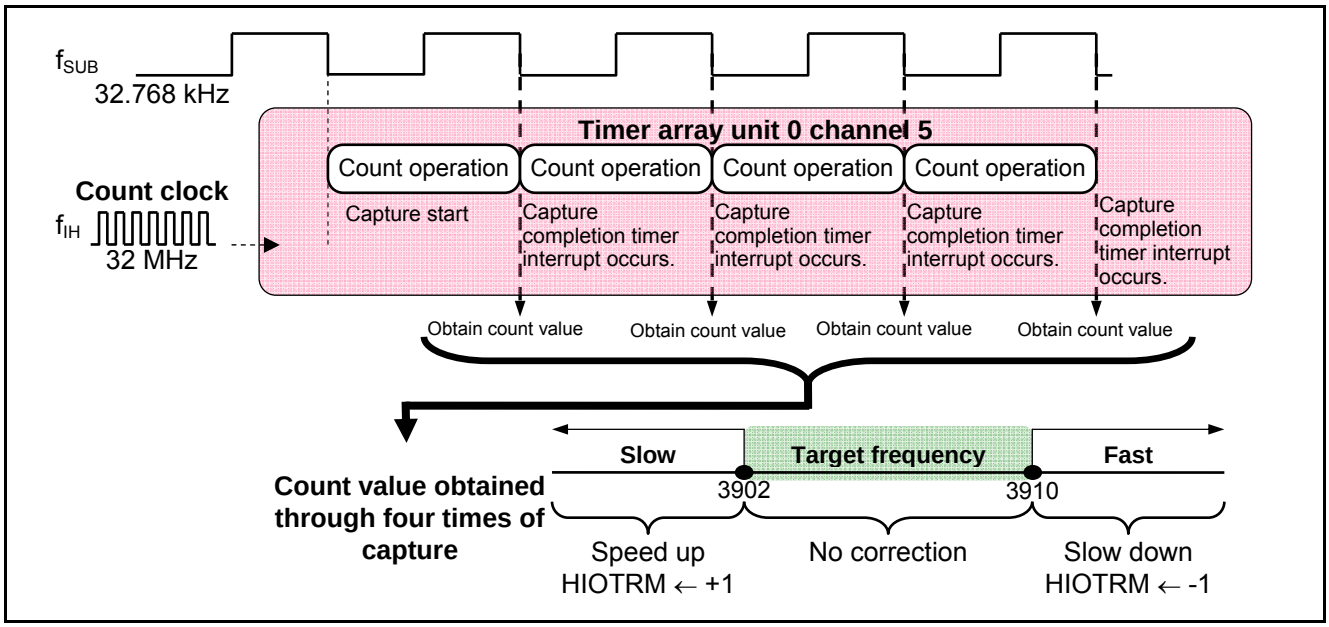

Figure 1.1 Example of Calibration in which the Subsystem Clock is Used

(2) Calibration with the external input signal
A calibration method with the external input signal is described below.

The low-level width of the external input signal is measured on TAU0 channel 1.

A signal with a low-level width of 1.953125 ms (256 Hz, a duty cycle of 50%) is input to the TI01 pin, and the HOCO clock (32 MHz) is selected as the count clock. The low-level width of the signal input to the TI01 pin is measured by using the TAU function of measuring the low-level width of input signal.

Accurate measurement of signal low-level width detects an error in the HOCO clock.

The table below lists the calculated count values that are obtained when the frequency is 32 MHz, 32 MHz - 0.1% (31.968 MHz), or 32 MHz + 0.1% (32.032 MHz).

Table 1.3 Count Values for Calibration with External Signal

HOCO Clock Frequency (f_{IH})		Count Value (Calculated Value)
32 MHz		62500
32 MHz – 0.1%	31.968 MHz	62437.5
32 MHz + 0.1%	32.032 MHz	62562.5

According to table 1.3, the target range of the count value is set to 62438 to 62561 for the target frequency range 32 MHz ± 0.1% (31.968 to 32.032 MHz). If the obtained count valued is 62437 or less, this means that the HOCO clock is slower than the target frequency. If it is 62562 or more, this means that the HOCO clock is faster than the target frequency. Determine the direction of correction of the HIOTRM register value (speeding up/slowing down), according to the count value, and perform calibration by incrementing the HIOTRM register value by ±1. When the count value is within the target range, the calibration is completed.

Figure 1.2 gives an example of calibration in which the external signal is used.

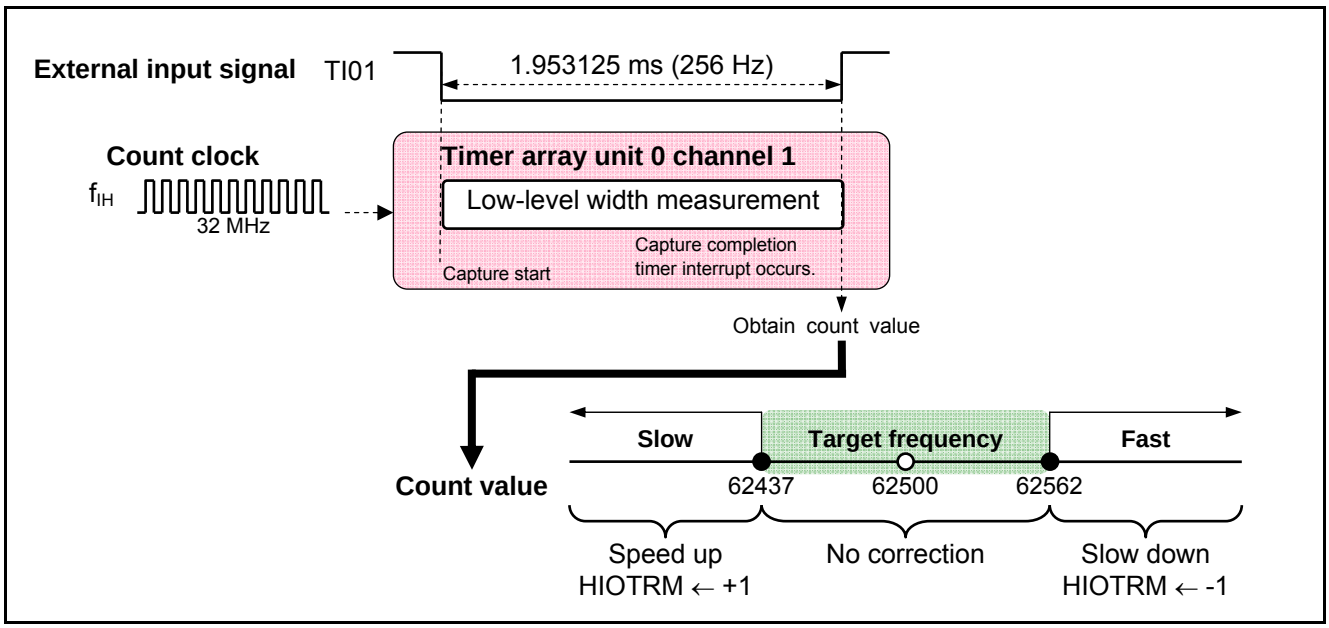

Figure 1.2 Example of Calibration in which the External Signal is Used

2. Operation Check Conditions

The sample code of this application note has been tested under the following conditions.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G13 (R5F100LEA)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 32 MHz • CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0 V (Operation is possible over a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode which uses 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ V3.01.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V4.0.0.26 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.01.00 from Renesas Electronics Corp.

3. Related Application Note

The application note that is related to this application note is shown below. Refer to it together with this application note.

- RL78/G13 Initialization (R01AN2575E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of hardware configuration that is used for this application note.

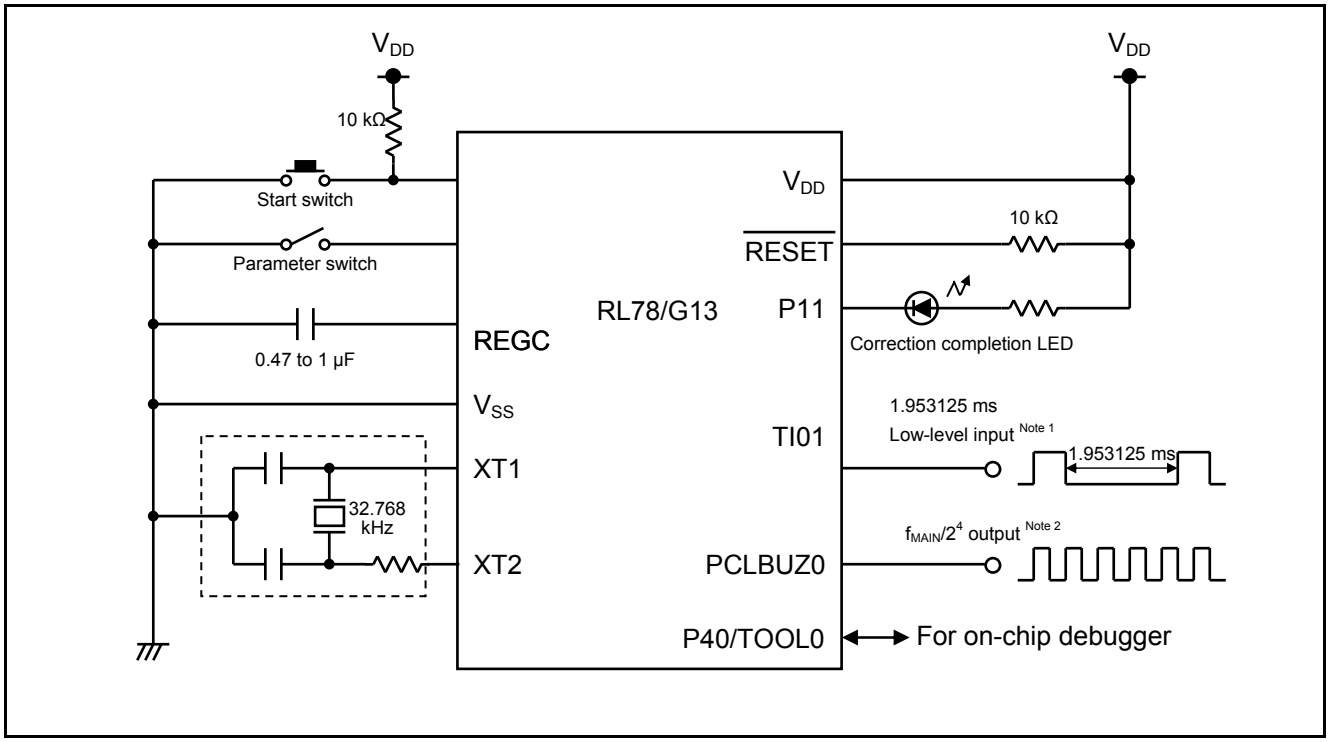

Figure 4.1 Hardware Configuration

Notes: 1. Input a signal with a low-level width of 1.953125 ms (256 Hz, a duty cycle of 50%).
2. Calibration sets the output frequency close to 2 MHz. Check the frequency using a frequency counter.

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).
2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their functions.

Table 4.1 Pins to be Used and Their Functions

Pin Name	I/O	Description
P137/INTP0	Input	Start switch: Connects the switch for starting calibration.
P10	Input	Parameter switch: Connects the switch for selecting a calibration method.
P11	Output	Correction completion LED: Connects the LED that indicates correction completion.
P123/XT1	Input	Subsystem clock: Connects a 32.768-kHz crystal oscillator.
P124/XT2	Input	
P16/TI01	Input	External input signal pin: Inputs a signal with a low-level width of 1.953125 ms (256 Hz, a duty cycle of 50%).
P140/PCLBUZ0	Output	Clock output: Always outputs $f_{MAIN}/2^4$ (2 MHz).

5. Description of Software

5.1 Operation Outline

In this application note, an error in the clock oscillation frequency of the HOCO is detected using a subsystem clock or an external input signal. Then, the HIOTRM register is adjusted to set the oscillation frequency of the HOCO close to 32 MHz.

Whether to use the subsystem clock or the external input signal is determined by the parameter switch. When the start switch is pressed, the TAU counts the frequency (pulse interval) or the pulse width of the subsystem clock or the external input signal. The HOCO is used for the count clock of the TAU. If the count value measured by the TAU is beyond the target range, the HIOTRM register is adjusted to set the oscillation frequency of the HOCO close to 32 MHz. The HIOTRM register is adjusted so that the count value is within the target range. The target range of the HOCO oscillation frequency is 32 MHz ± 0.1% (31.968 MHz to 32.032 MHz).

(1) Initialize TAU0 channel 1.
<Setting Conditions>

- Set the count clock as the operating clock (f_{MCK}= f_{CLK} = 32 MHz).
- Select the function of measuring the high/low-level width of input signal.
- Select both edges as the valid edge of the TI01 pin (for low-level width measurement).
  Falling edge and rising edge are selected as the start trigger and the capture trigger, respectively.
- Set the P16/TI01/TO01/INTP5 pin as the TI01 pin.

(2) Initialize TAU0 channel 2.
<Setting Conditions>

- Set the count clock to the operating clock/2^3 (f_{MCK} = f_{CLK}/23 = 4 MHz).
- Select the interval timer function.
- Select the software trigger only.
- Set the timer data register to 39999 (9C3FH).

(3) Initialize TAU0 channel 5.
<Setting Conditions>

- Set the count clock to the operating clock (f_{MCK} = f_{CLK} = 32 MHz).
- Select the function of measuring input pulse intervals.
- Use the valid edge of the TI05 pin for both start triggering and capture triggering.
- Select the subsystem clock (f_{SUB}) as the timer input to be used on channel 5.

(4) Initialize the clock output/buzzer output control circuit.
<Setting Conditions>

- Set the output clock to $f_{MAIN}/2^4$ (= 2 MHz).

(5) Initialize external interrupt.
<Setting Condition>

- Select the falling edges of the INTP0 pin as the valid edge for external interrupt requests.

(6) Enable clock output and external interrupt and then execute a HALT instruction to enter HALT mode.
(7) When the start switch is pressed, an external interrupt (INTP0) makes the system exit HALT mode. To eliminate chattering, wait for 10 ms by using TAU0 channel 2 and then check the level of the pin (P137/INTP0) to which the start switch is connected.
(8) If no chattering occurs, check the level of the pin (P10) to which the parameter switch is connected, and perform calibration by using the specified method. To use the subsystem clock, perform (9) to (12). To use the external input clock, perform (13) to (15).

Calibration with the Subsystem Clock

(9) Enable operation of TAU0 channel 5. Ignore the capture value when the first capture completion timer interrupt (INTTM05) occurs.
(10) After ignoring the first capture value, wait the second and subsequent timer interrupts (INTTM05).
(11) When an INTTM05 occurs, save the capture value and wait a capture completion timer interrupt again.
(12) On completion of four times of the measurement of the subsystem clock pulse interval, add up the four count values and perform (16).

Calibration with the External Input Signal

(13) Input to the TI01 pin a signal with a low-level width of 1.953125 ms (256 Hz, a duty cycle of 50%).
(14) Wait a capture completion timer interrupt (INTTM01) by TAU0 channel 1.
(15) After an INTTM01 occurs, save the capture value and then perform (16).

HOCO Correction

(16) Determine the necessity and correction direction (+1/-1) of the HOCO clock according to the value obtained in (12) or (15), and correct the HOCO clock frequency by adjusting the HIOTRM register value.
(17) Repeat (9) to (16) so that the HOCO clock frequency is within the target range.

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Setting	Description
000C0H/010C0H	11101111B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD reset mode 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger

5.3 List of Constants

Table 5.2 lists the constants that are used in this sample program.

Table 5.2 Constants for the Sample Program

Constant Name	Setting	Description
HIOTRM_MAX	0b00111111	Maximum value of the HIOTRM register
HIOTRM_MIN	0b00000000	Minimum value of the HIOTRM register
CCNT_XT1_MAX	3910	Upper threshold of subsystem clock count
CCNT_XT1_MIN	3902	Lower threshold of subsystem clock count
CCNT_EXT_MAX	62562	Upper threshold of external input signal count
CCNT_EXT_MIN	62437	Lower threshold of external input signal count

5.4 List of Variables

Table 5.3 lists the global variables.

Table 5.3 Global Variables

Type	Variable Name	Contents	Function Used
uint8_t	calibration_count	Calibration count value	R_Main_UseXT1() R_Main_ExternalClock() R_Trimming_OCO()
uint8_t	calibrate_history	Calibration history	R_Main_UseXT1() R_Main_ExternalClock() R_Trimming_OCO()
uint16_t	count_value	Count value (Used as an argument of R_Trimming_OCO)	R_Main_UseXT1() R_Main_ExternalClock() R_Trimming_OCO()
uint16_t	max	Upper threshold of count	R_Main_UseXT1() R_Main_ExternalClock() R_Trimming_OCO()
uint16_t	min	Lower threshold of count	R_Main_UseXT1() R_Main_ExternalClock() R_Trimming_OCO()

5.5 List of Functions

Table 5.4 lists the functions that are used in this sample program.

Table 5.4 Functions

Function Name	Outline
R_PCLBUZ0_Start	Clock output start
R_INTC0_Start	Pin input edge detection (INTP0) operation start
R_INTC0_Stop	Pin input edge detection (INTP0) operation stop
R_TAU0_TMIF02_Clear	TAU0 channel 2 interrupt request flag clear processing
R_TAU0_Channel2_Start	TAU0 channel 2 operation start
R_TAU0_Channel2_Stop	TAU0 channel 2 operation stop
R_Main_UseXT1	Calibration with the subsystem clock
R_TAU0_TMIF05_Clear	TAU0 channel 5 interrupt request flag clear processing
R_TAU0_Channel5_Start	TAU0 channel 5 operation start
R_TAU0_Channel5_Stop	TAU0 channel 5 operation stop
R_Main_ExternalClock	Calibration with the external input signal
R_TAU0_TMIF01_Clear	TAU0 channel 1 interrupt request flag clear processing
R_TAU0_Channel1_Start	TAU0 channel 1 operation start
R_TAU0_Channel1_Stop	TAU0 channel 1 operation stop
R_Trimming_OCO	HOCO clock correction

5.6 Function Specifications

This section describes the specifications for the functions that are used in this sample program.

[Function Name] R_PCLBUZ0_Start	
Synopsis	Clock output start
Header	r_cg_macrodriver.h, r_cg_pclbuz.h, r_cg_userdefine.h
Declaration	void R_PCLBUZ0_Start(void)
Explanation	This function enables clock output operation.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_INTC0_Start	
Synopsis	Pin input edge detection (INTP0) operation start
Header	r_cg_macrodriver.h, r_cg_intc.h, r_cg_userdefine.h
Declaration	void R_INTC0_Start(void)
Explanation	This function clears the INTP0 interrupt request flag and then enables INTP0 interrupts.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_INTC0_Stop	
Synopsis	Pin input edge detection (INTP0) operation stop
Header	r_cg_macrodriver.h, r_cg_intc.h, r_cg_userdefine.h
Declaration	void R_INTC0_Stop(void)
Explanation	This function disables INTP0 interrupts.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_TAU0_TMIF02_Clear	
Synopsis	TAU0 channel 2 interrupt request flag clear processing
Header	r_cg_macrodriver.h, r_cg_timer.h, r_cg_userdefine.h
Declaration	void R_TAU0_TMIF02_Clear(void)
Explanation	This function clears the TAU0 channel 2 interrupt request flag.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_TAU0_Channel2_Start	
Synopsis	TAU0 channel 2 operation start
Header	r_cg_macrodriver.h, r_cg_timer.h, r_cg_userdefine.h
Declaration	void R_TAU0_Channel2_Start(void)
Explanation	This function starts count operation on TAU0 channel 2.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_TAU0_Channel2_Stop	
Synopsis	TAU0 channel 2 operation stop
Header	r_cg_macrodriver.h, r_cg_timer.h, r_cg_userdefine.h
Declaration	void R_TAU0_Channel2_Stop(void)
Explanation	This function stops count operation on TAU 0 channel 2.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_Main_UseXT1	
Synopsis	Calibration with the subsystem clock
Header	r_cg_macrodriver.h, r_cg_cgc.h, r_cg_port.h, r_cg_intc.h, r_cg_timer.h, r_cg_pclbuz.h, r_cg_userdefine.h
Declaration	void R_Main_UseXT1(void)
Explanation	This function captures the subsystem clock count value and performs correction processing.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_TAU0_TMIF05_Clear	
Synopsis	TAU0 channel 5 interrupt request flag clear processing
Header	r_cg_macrodriver.h, r_cg_timer.h, r_cg_userdefine.h
Declaration	void R_TAU0_TMIF05_Clear(void)
Explanation	This function clears the TAU0 channel 5 interrupt request flag.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_TAU0_Channel5_Start	
Synopsis	TAU0 channel 5 operation start
Header	r_cg_macrodriver.h, r_cg_timer.h, r_cg_userdefine.h
Declaration	void R_TAU0_Channel5_Start(void)
Explanation	This function starts count operation on TAU 0 channel 5.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_TAU0_Channel5_Stop	
Synopsis	TAU0 channel 5 operation stop
Header	r_cg_macrodriver.h, r_cg_timer.h, r_cg_userdefine.h
Declaration	void R_TAU0_Channel5_Stop(void)
Explanation	This function stops count operation on TAU 0 channel 5.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_Main_ExternalClock	
Synopsis	Calibration with the external input signal
Header	r_cg_macrodriver.h, r_cg_cgc.h, r_cg_port.h, r_cg_intc.h, r_cg_timer.h, r_cg_pclbuz.h, r_cg_userdefine.h
Declaration	void R_Main_ExternalClock(void)
Explanation	This function captures the external input signal count value and performs correction processing.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_TAU0_TMIF01_Clear	
Synopsis	TAU0 channel 1 interrupt request flag clear processing
Header	r_cg_macrodriver.h, r_cg_timer.h, r_cg_userdefine.h
Declaration	void R_TAU0_TMIF01_Clear(void)
Explanation	This function clears the TAU0 channel 1 interrupt request flag.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_TAU0_Channel1_Start	
Synopsis	TAU0 channel 1 operation start
Header	r_cg_macrodriver.h, r_cg_timer.h, r_cg_userdefine.h
Declaration	void R_TAU0_Channel1_Start(void)
Explanation	This function starts count operation on TAU 0 channel 1.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_TAU0_Channel1_Stop	
Synopsis	TAU0 channel 1 operation stop
Header	r_cg_macrodriver.h, r_cg_timer.h, r_cg_userdefine.h
Declaration	void R_TAU0_Channel1_Stop(void)
Explanation	This function stops count operation on TAU 0 channel 1.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_Trimming_OCO	
Synopsis	HOCO clock correction
Header	r_cg_macrodriver.h, r_cg_cgc.h, r_cg_port.h, r_cg_intc.h, r_cg_timer.h, r_cg_pclbuz.h, r_cg_userdefine.h
Declaration	uint8_t R_Trimming_OCO(uint16_t count)
Explanation	This function sets the HIOTRM according to the argument and then determines whether to continue calibration.
Arguments	count : [Target clock count value]
Return value	[0]: Calibration ends. [1]: Calibration continues.
Remarks	None

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

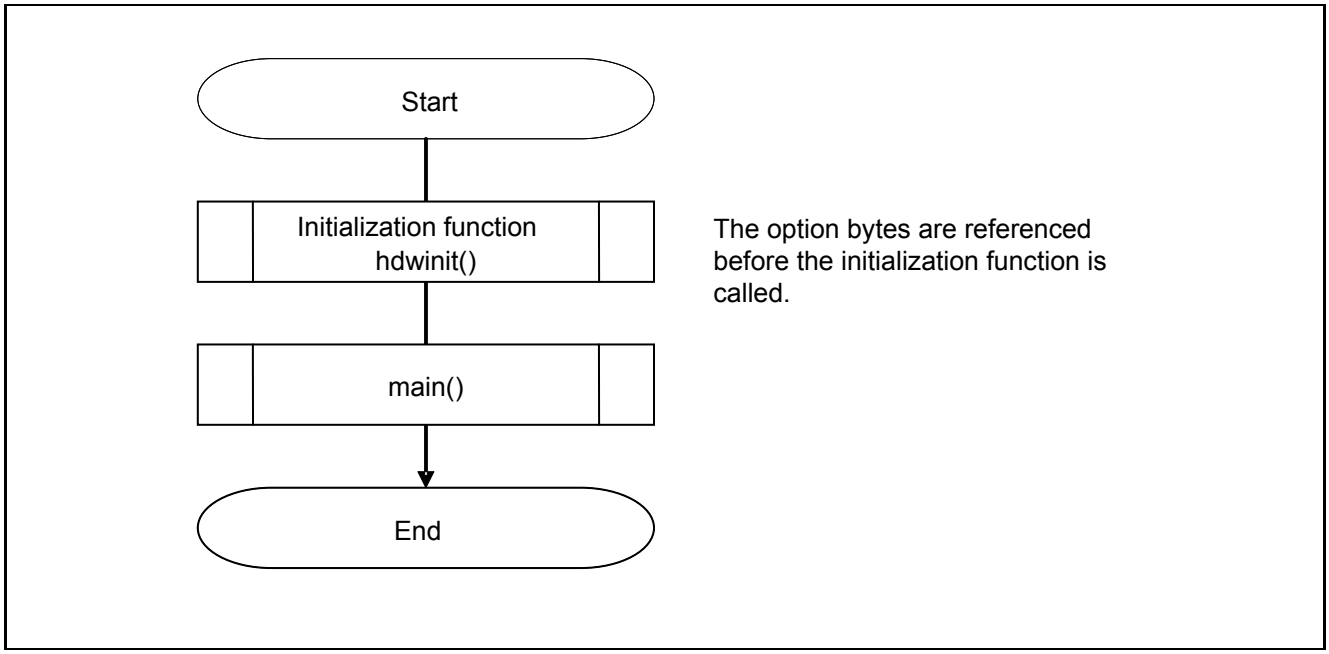

Figure 5.1 Overall Flow

5.7.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

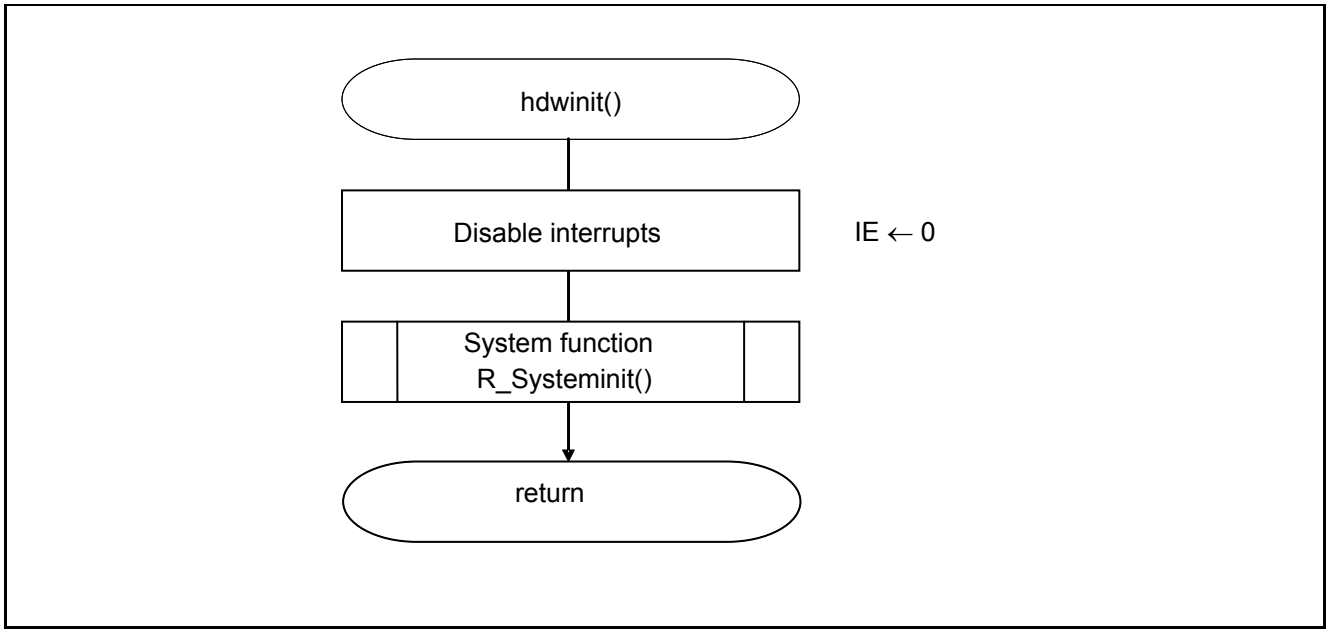

Figure 5.2 Initialization Function

5.7.2 System Function

Figure 5.3 shows the flowchart for the system function.

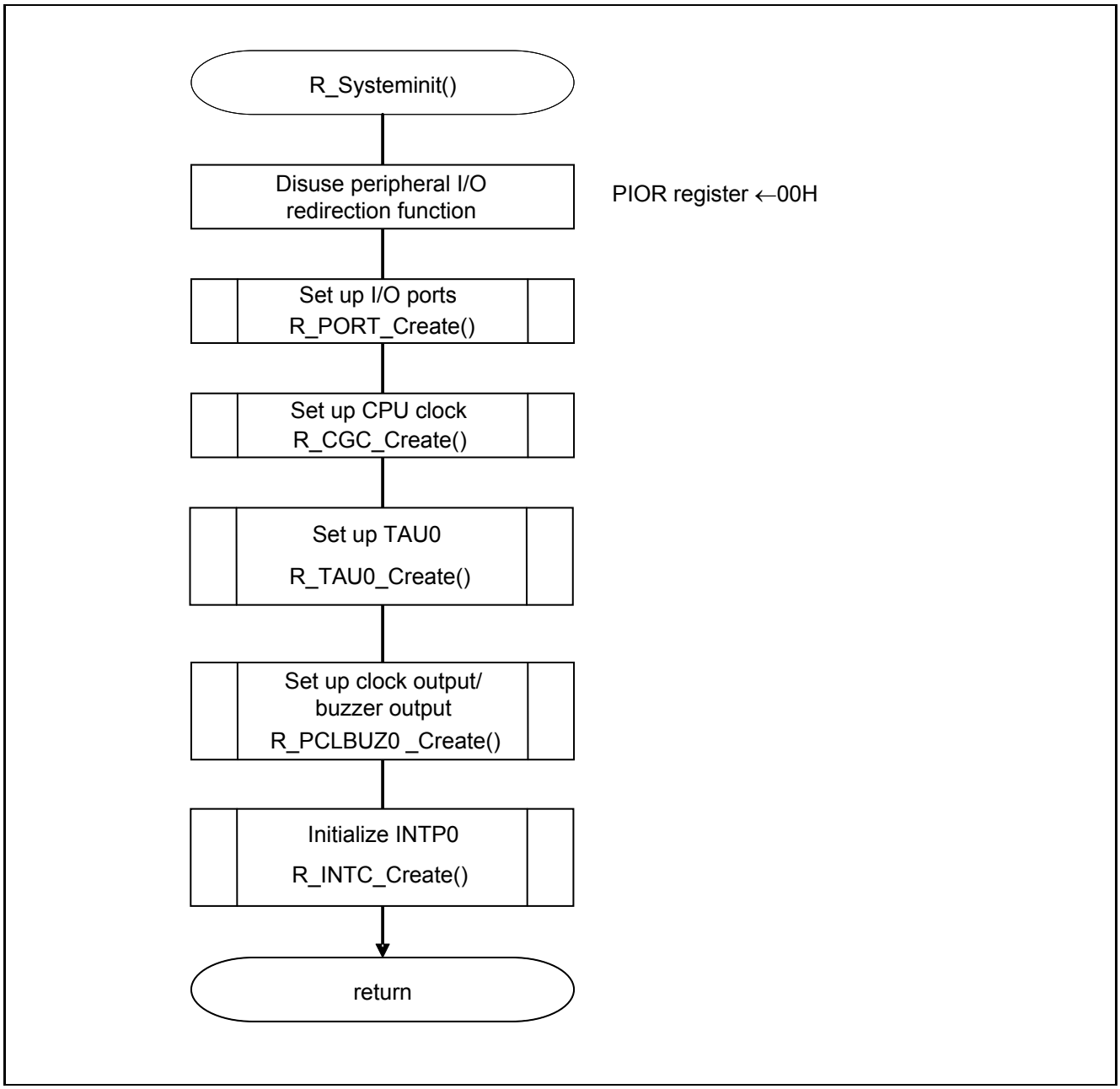

Figure 5.3 System Function

5.7.3 I/O Port Setup

Figure 5.4 shows the flowchart for setting up the I/O ports.

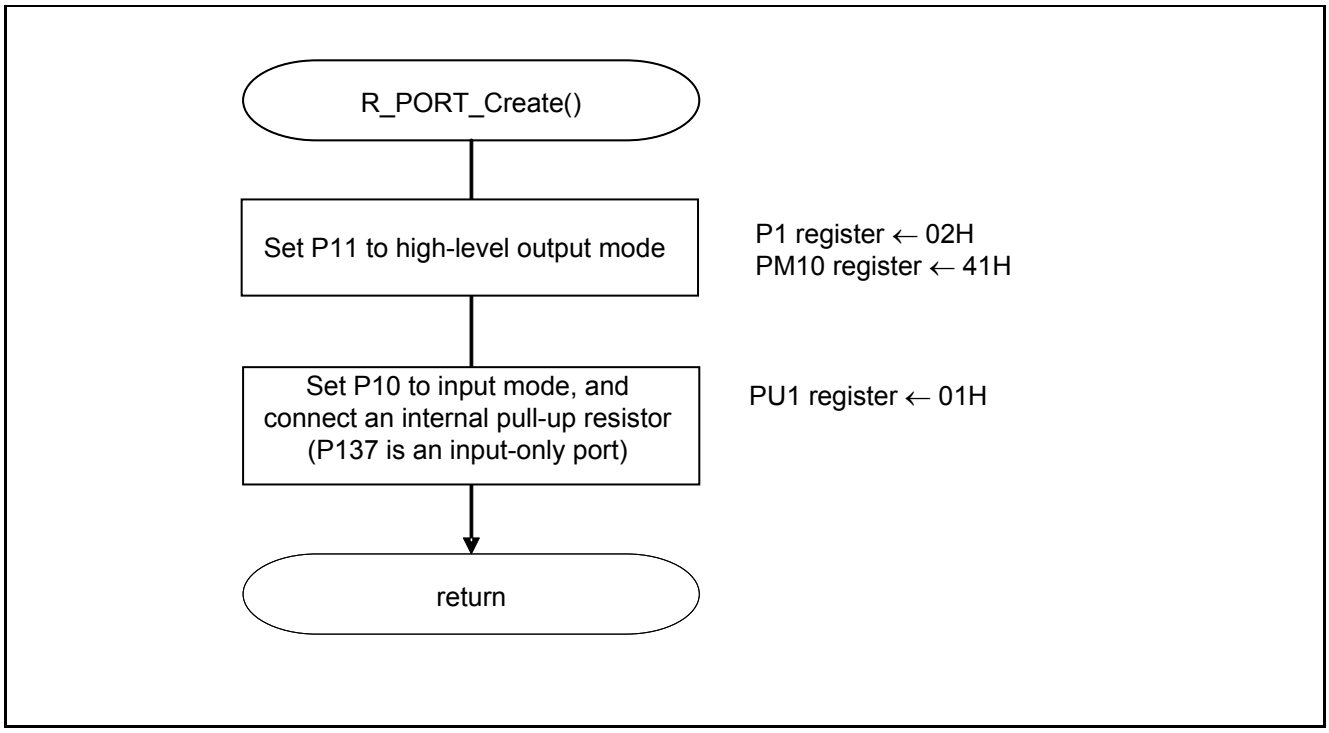

Figure 5.4 I/O Port Setup

Caution: Refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E) for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

Setting up the LED display pin

- Port register 1 (P1)
- Port mode register 1 (PM1)

Symbol: P1

7	6	5	4	3	2	1	0
P17	P16	P15	P14	P13	P12	P11	P10
x	x	x	x	x	x	**1**	x

Bit 1

P11	P11 output data control
0	Output 0
1	**Output 1**

Symbol: PM1

7	6	5	4	3	2	1	0
PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10
x	x	x	x	x	x	**0**	x

Bit 1

PM11	PM11 pin I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Caution For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.4 CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock.

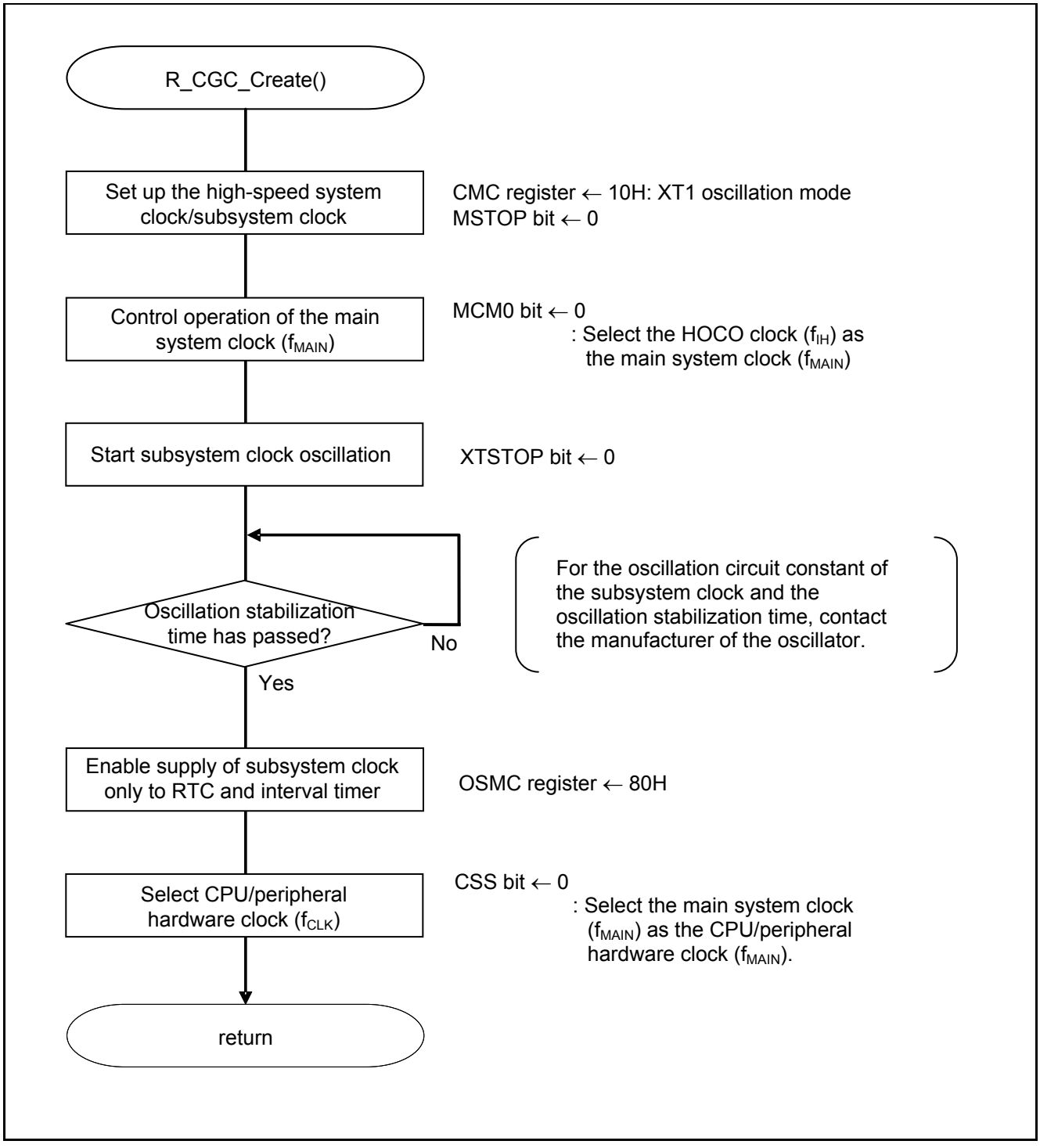

Figure 5.5 CPU Clock Setup

Remark: A wait time (about 1 s) is spent on stabilization of subsystem clock oscillation during CPU clock setup (R_CGC_Create()). The oscillation stabilization time is specified by the constant CGC_SUBWAITTIME in r_cg_cgc.h.

Caution: For details on the procedure for setting up the CPU clock (R_CGC_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E).

5.7.5 TAU0 Setup

Figures 5.6 and 5.7 show the flowcharts for setting up TAU0.

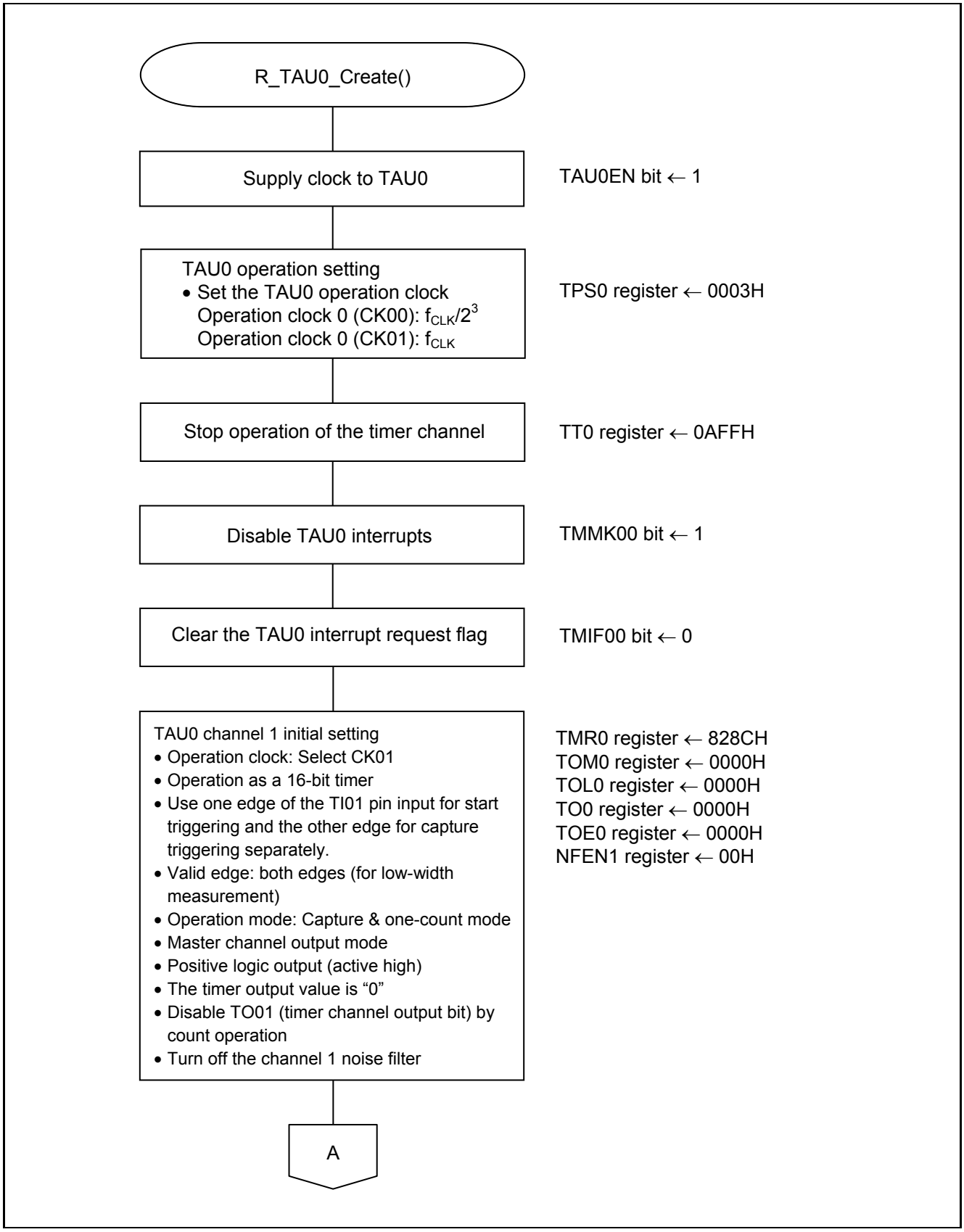

Figure 5.6 TAU0 Setup (1/2)

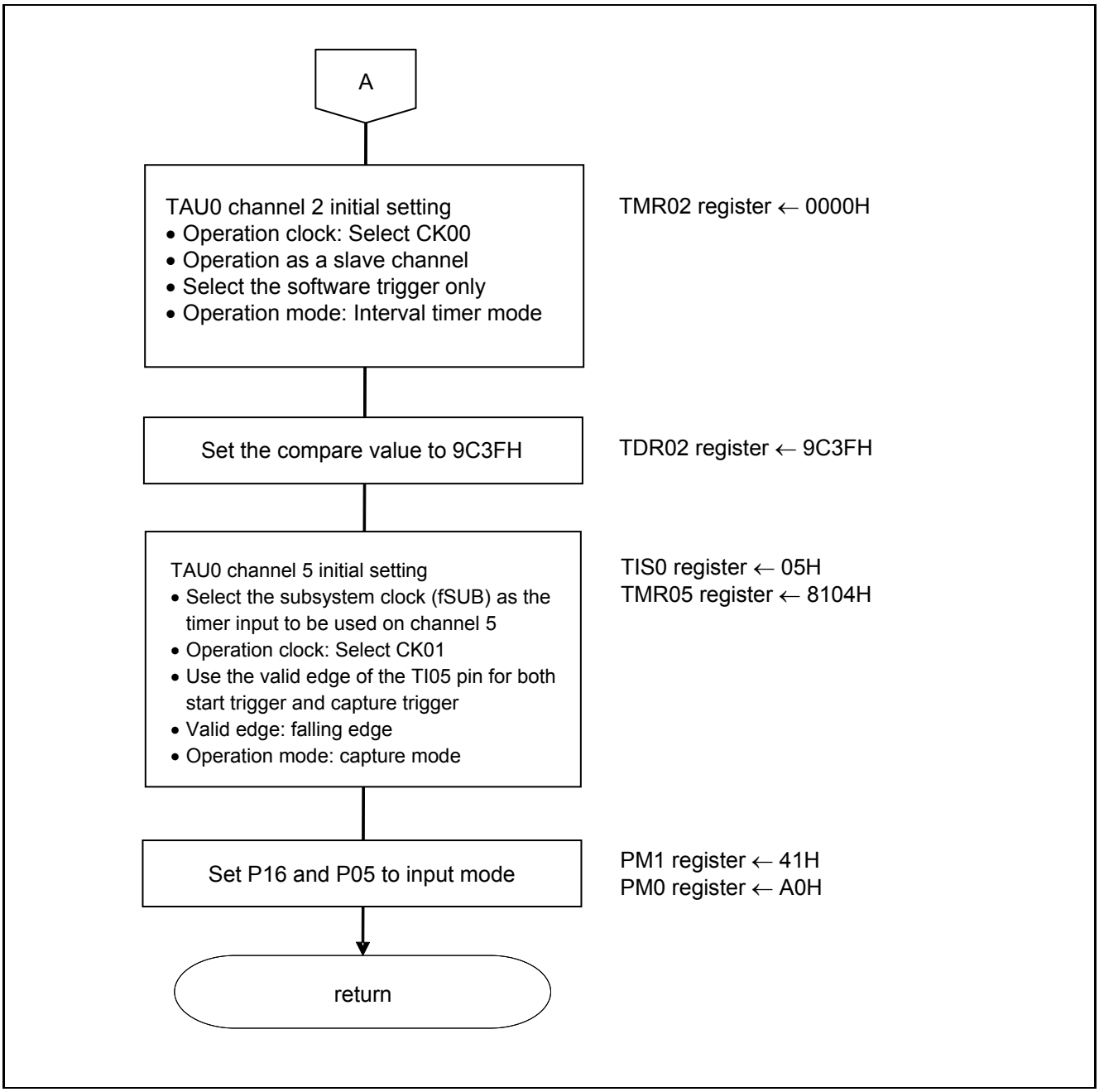

Figure 5.7 TAU0 Setup (2/2)

Enabling supply of clock signals to TAU0

- Peripheral enable register 0 (PER0)
  Enable supply of clock signals to the TAU0.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
x	x	x	x	x	x	x	**1**

Bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply. - SFR used by timer array unit 0 cannot be written. - Timer array unit 0 is in the reset status.
1	**Enables input clock supply.** **- SFR used by timer array unit 0 can be read and written.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Selecting the operation clock

- Timer clock select register 0 (TPS0)
  Select the timer operation clock (CK00 and CK01).

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS 031	PRS 030	0	0	PRS 021	PRS 020	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
0	0	x	x	0	0	x	x	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**

Bits 7 to 4

PRS 013	PRS 012	PRS 011	PRS 010		Selection of operation clock (CK01)				
					f_{CLK}= 2 MHz	f_{CLK}= 5 MHz	f_{CLK}= 10 MHz	f_{CLK}= 20 MHz	**f_{CLK}= 32 MHz**
0	**0**	**0**	**0**	**f_{CLK}**	2 MHz	5 MHz	10 MHz	20 MHz	**32 MHz**
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	16 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	8 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	4 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz	2 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156.2 kHz	312.5 kHz	625 kHz	1 MHz
0	1	1	0	$f_{CLK}/2^6$	31.25 kHz	78.1 kHz	156.2 kHz	312.5 kHz	500 kHz
0	1	1	1	$f_{CLK}/2^7$	15.62 kHz	39.1 kHz	78.1 kHz	156.2 kHz	250 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	125 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.76 kHz	19.5 kHz	39.1 kHz	62.5 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.76 kHz	19.5 kHz	31.25 kHz
1	0	1	1	$f_{CLK}/2^{11}$	976 Hz	2.44 kHz	4.88 kHz	9.76 kHz	15.63 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	7.81 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	3.91 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.95 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	976 Hz

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS 031	PRS 030	0	0	PRS 021	PRS 020	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
0	0	x	x	0	0	x	x	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**

Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000		Selection of operation clock (CK00)				
					f_{CLK}= 2 MHz	f_{CLK}= 5 MHz	f_{CLK}= 10 MHz	f_{CLK}= 20 MHz	**f_{CLK}= 32 MHz**
0	0	0	0	f_{CLK}	2 MHz	5 MHz	10 MHz	20 MHz	32 MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	16 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	8 MHz
0	**0**	**1**	**1**	**$f_{CLK}/2^3$**	250 kHz	625 kHz	1.25 MHz	2.5 MHz	**4 MHz**
0	1	0	0	$f_{CLK}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz	2 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156.2 kHz	312.5 kHz	625 kHz	1 MHz
0	1	1	0	$f_{CLK}/2^6$	31.25 kHz	78.1 kHz	156.2 kHz	312.5 kHz	500 kHz
0	1	1	1	$f_{CLK}/2^7$	15.62 kHz	39.1 kHz	78.1 kHz	156.2 kHz	250 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	125 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.76 kHz	19.5 kHz	39.1 kHz	62.5 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.76 kHz	19.5 kHz	31.25 kHz
1	0	1	1	$f_{CLK}/2^{11}$	976 Hz	2.44 kHz	4.88 kHz	9.76 kHz	15.63 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	7.81 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	3.91 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.95 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	976 Hz

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Stopping timers

- Timer channel stop register 0 (TT0)
  Stop the count operation.

Symbol: TT0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TTH03	0	TTH01	0	TT07	TT06	TT05	TT04	TT03	TT02	TT01	TT00
0	0	0	0	**1**	0	**1**	0	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Bit 11

TTH03	Trigger to stop operation of the upper-8-bit timer when channel 3 is in the 8-bit timer mode
0	No trigger operation
1	**Operation is stopped (stop trigger is generated).**

Bit 9

TTH01	Trigger to stop operation of the upper-8-bit timer when channel 1 is in the 8-bit timer mode
0	No trigger operation
1	**Operation is stopped (stop trigger is generated).**

Bits 7 to 0

TT0n	Operation stop trigger of channel n
0	No trigger operation
1	**Operation is stopped (stop trigger is generated).**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up timer interrupt

- Interrupt request flag registers 0H, 1L ,1H, and 2L (IF0H, IF1L, IF1H, and IF2L)
  Set interrupt request flags.
- Interrupt mask flag registers 0H, 1L ,1H, and 2L (MK0H, MK1L, MK1H, and MK2L)
  Set interrupt masks.

Symbol: IF0H

7	6	5	4	3	2	1	0
SREIF0 TMIF01H	SRIF0 CSIIF01 IICIF01	STIF0 CSIIF00 IICIF00	DMAIF1	DMAIF0	SREIF2 TMIF11H	SRIF2 CSIIF21 IICIF21	STIF2 CSIIF20 IICIF20
0	x	x	x	x	x	x	x

Symbol: IF1L

7	6	5	4	3	2	1	0
TMIF03	TMIF02	TMIF01	TMIF00	IICAIF0	SREIF0 TMIF03H	SRIF1 CSIIF11 IICIF11	STIF1 CSIIF10 IICIF10
0	**0**	**0**	**0**	x	**0**	x	x

Symbol: IF1H

7	6	5	4	3	2	1	0
TMIF04	TMIF13	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
0	x	x	x	x	x	x	x

Symbol: IF2L

7	6	5	4	3	2	1	0
PIF10	PIF9	PIF8	PIF7	PIF6	TMIF07	TMIF06	TMIF05
x	x	x	x	x	**0**	**0**	**0**

TMIF0n TMIF0nH	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request signal is generated, interrupt request status

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: MK0H

7	6	5	4	3	2	1	0
SREMK0 TMMK01H	SRMK0 CSIMK01 IICMK01	STMK0 CSIMK00 IICMK00	DMAMK1	DMAMK0	SREMK2 TMMK11H	SRMK2 CSMK21 IICMK21	STMK2 CSIMK20 IICMK20
1	x	x	x	x	x	x	x

Symbol: MK1L

7	6	5	4	3	2	1	0
TMMK03	TMMK02	TMMK01	TMMK00	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
1	**1**	**1**	**1**	x	**1**	x	x

Symbol: MK1H

7	6	5	4	3	2	1	0
TMMK04	TMMK13	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
1	x	x	x	x	x	x	x

Symbol: MK2L

7	6	5	4	3	2	1	0
PMK10	PMK9	PMK8	PMK7	PMK6	TMMK07	TMMK06	TMMK05
x	x	x	x	x	**1**	**1**	**1**

TMMK0n TMMK0nH	Interrupt handling control
0	Interrupt handling enabled
1	**Interrupt handling disabled**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up channel 1 operation mode

- Timer mode register 01 (TMR01)
  Select an operation clock (f_{MCK}).
  Select a count clock.
  Select 16/8-bit timer.
  Set up start trigger and capture trigger.
  Select the valid edge of timer input.
  Set up the operation mode.

Symbol: TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS011	CKS010	0	CCS01	SPLIT01	STS012	STS011	STS010	CIS011	CIS010	0	0	MD013	MD012	MD011	MD010
1	**0**	0	**0**	**0**	**0**	**1**	**0**	**1**	**0**	0	0	**1**	**1**	**0**	**0**

Bits 15 and 14

CKS011	CKS010	Selection of operation clock (f_{MCK}) of channel 1
0	0	Operation clock CK00 set by timer clock select register 0 (TPS0)
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	**0**	**Operation clock CK01 set by timer clock select register 0 (TPS0)**
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

CCS01	Selection of count clock (f_{TCLK}) of channel 1
0	**Operation clock (f_{MCK}) specified by the CKS010 and CKS011 bits**
1	Valid edge of input signal input from the TI01 pin

Bit 11

SPLIT01	Selection of 8 or 16-bit timer operation for channel 1
0	**Operates as 16-bit timer.** **(Operates in independent channel operation function or as slave channel in simultaneous channel operation function.)**
1	Operates as 8-bit timer.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS011	CKS010	0	CCS01	SPLIT01	STS012	STS011	STS010	CIS011	CIS010	0	0	MD013	MD012	MD011	MD010
1	**0**	0	**0**	**0**	**0**	**1**	**0**	**1**	**0**	0	0	**1**	**1**	**0**	**0**

Bits 10 to 8

STS012	STS011	STS010	Setting of start trigger or capture trigger of channel 1
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TI01 pin input is used as both the start trigger and capture trigger.
0	**1**	**0**	**Both the edges of the TI01 pin input are used as a start trigger and a capture trigger.**
1	0	0	Interrupt signal of the master channel is used (when channel 1 is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Bits 7 and 6

CIS11	CIS10	Selection of TI01 pin input valid edge
0	0	Falling edge
0	1	Rising edge
1	**0**	**Both edges (when low-level width is measured)** **Start trigger: Falling edge, Capture trigger: Rising edge**
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS011	CKS010	0	CCS01	SPLIT01	STS012	STS011	STS010	CIS011	CIS010	0	0	MD013	MD012	MD011	MD010
1	**0**	0	**0**	**0**	**0**	**1**	**0**	**1**	**0**	0	0	**1**	**1**	**0**	**0**

Bits 3 to 0

MD013	MD012	MD011	MD010	Operation mode of channel 1	Corresponding function	Count operation of TCR
0	0	0	1/0	Interval timer mode	Interval timer / Square wave output / divider function / PWM output (master)	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	**1**	**0**	**0**	**Capture & one-count mode**	**Measurement of high-/low-level width of input signal**	**Counting up**
Other than above				Setting prohibited		

The operation of the MD010 bit varies depending on each operation mode (see the table below).

Operation mode (Value set by the MD013 to MD011 bits (see table above))	MD010	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• Capture mode (0, 1, 0)	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
• **Capture & one-count mode (1, 1, 0)**	**0**	**Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.**
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up channel 1 timer output mode

- Timer output mode register 0 (TOM0)
  Control timer output mode.

Symbol: TOM0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TOM07	TOM06	TOM05	TOM04	TOM03	TOM02	TOM01	0
0	0	0	0	0	0	0	0	x	x	x	x	x	x	**0**	0

Bit 1

TOM01	Control of timer output mode of channel 1
0	**Master channel output mode**
1	Slave channel output mode

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Specifying the channel 1 timer output value

- Timer output value register 0 (TO0)
  Specify a timer output value.

Symbol: TO0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TO07	TO06	TO05	TO04	TO03	TO02	TO01	TO00
0	0	0	0	0	0	0	0	x	x	x	x	x	x	**0**	x

Bit 1

TO01	Timer output of channel 1
0	**Timer output value is "0".**
1	Timer output value is "1".

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Enabling channel 1 timer output

- Timer output enable register 0 (TOE0)
  Enable timer output.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TOE07	TOE06	TOE05	TOE04	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	0	0	x	x	x	x	x	x	**0**	x

Bit 1

TOE01	Timer output enable/disable of channel 1
0	**The TO01 operation stopped by count operation (timer channel output bit).**
1	The TO01 operation enabled by count operation (timer channel output bit).

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up channel 1 noise filter

- Noise filter enable register 1 (NFEN1)
  Enable or disable noise filtering on input signal from the timer input pin

Symbol: NFEN1

7	6	5	4	3	2	1	0
TNFEN07	TNFEN06	TNFEN05	TNFEN04	TNFEN03	TNFEN02	TNFEN01	TNFEN00
x	x	x	x	x	x	**0**	x

Bit 1

TNFEN01	Use of noise filter of TI01/TO01/P16 pin input signal
0	**Noise filter OFF**
1	Noise filter ON

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up channel 2 operation mode

- Timer mode register 02 (TMR02)
  Select an operation clock (f_{MCK}).
  Select a count clock.
  Select 16/8-bit timer.
  Set up start trigger and capture trigger.
  Select the valid edge of timer input.
  Set up the operation mode.

Symbol: TMR02

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS021	CKS020	0	CCS02	MASTER02	STS022	STS021	STS020	CIS021	CIS020	0	0	MD023	MD022	MD021	MD020
0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	0	0	**0**	**0**	**0**	**0**

Bits 15 and 14

CKS021	CKS020	Selection of operation clock (f_{MCK}) of channel 2
0	**0**	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

CCS02	Selection of count clock (f_{TCLK}) of channel 2
0	**Operation clock (f_{MCK}) specified by the CKS010 and CKS011 bits**
1	Valid edge of input signal input from the TI02 pin

Bit 11

MASTER02	Selection between using channel 2 independently or simultaneously with another channel (as a slave or master)
0	**Operates in independent channel operation function or as slave channel in simultaneous channel operation function.**
1	Operates as master channel in simultaneous channel operation function.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: TMR02

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS021	CKS020	0	CCS02	MASTER02	STS022	STS021	STS020	CIS021	CIS020	0	0	MD023	MD022	MD021	MD020
0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	0	0	**0**	**0**	**0**	**0**

Bits 10 to 8

STS022	STS021	STS020	Setting of start trigger or capture trigger of channel 2
0	**0**	**0**	**Only software trigger start is valid (other trigger sources are unselected).**
0	0	1	Valid edge of the TI02 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI02 pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when channel 2 is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: TMR02

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS021	CKS020	0	CCS02	MASTER02	STS022	STS021	STS020	CIS021	CIS020	0	0	MD023	MD022	MD021	MD020
0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	0	0	**0**	**0**	**0**	**0**

Bits 3 to 0

MD023	MD022	MD021	MD020	Operation mode of channel 2	Corresponding function	Count operation of TCR
0	**0**	**0**	1/**0**	**Interval timer mode**	**Interval timer / Square wave output / divider function / PWM output (master)**	**Counting down**
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The operation of the MD020 bit varies depending on each operation mode (see the table below).

Operation mode (Value set by the MD023 to MD021 bits (see table above))	MD020	Setting of starting counting and interrupt
• **Interval timer mode (0, 0, 0)**	**0**	**Timer interrupt is not generated when counting is started (timer output does not change, either).**
• Capture mode (0, 1, 0)	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Specifying the channel 2 count value

- Timer data register 02 (TDR02)
  Specify the interval timer compare register value.

Symbol: TDR02

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	1	1	0	0	0	0	1	1	1	1	1	1

Set the interval timer compare value to 39999 (0x9C3F).

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Selecting channel 5 timer input

- Timer input select register 1 (TIS0)
  Select the channel 5 of TAU0 timer input.

Symbol: TIS0

7	6	5	4	3	2	1	0
0	0	0	0	0	TIS02	TIS01	TIS00
0	0	0	0	0	**1**	**0**	**1**

Bits 2 to 0

TIS02	TIS01	TIS00	Selection of timer input used with channel 5
0	0	0	Input signal of timer input pin (TI05)
0	0	1	
0	1	0	
0	1	1	
1	0	0	Internal low-speed on-chip oscillator (LOCO) clock (f_{IL})
1	**0**	**1**	**Subsystem clock (f_{SUB})**
Other than above			Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up channel 5 operation mode

- Timer mode register 05 (TMR05)
  Select an operation clock (f_{MCK}).
  Select a count clock.
  Set up start trigger and capture trigger.
  Select the valid edge of timer input.
  Set up the operation mode.

Symbol: TMR05

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS051	CKS050	0	CCS05	0	STS052	STS051	STS050	CIS051	CIS050	0	0	MD053	MD052	MD051	MD050
1	**0**	0	**0**	0	**0**	**0**	**1**	**0**	**0**	0	0	**0**	**1**	**0**	**0**

Bits 15 and 14

CKS051	CKS050	Selection of operation clock (f_{MCK}) of channel 5
0	0	Operation clock CK00 set by timer clock select register 0 (TPS0)
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	**0**	**Operation clock CK01 set by timer clock select register 0 (TPS0)**
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

CCS05	Selection of count clock (f_{TCLK}) of channel 5
0	**Operation clock (f_{MCK}) specified by the CKS050 and CKS051 bits**
1	Valid edge of input signal input from the TI05 pin

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: TMR05

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS051	CKS050	0	CCS05	0	STS052	STS051	STS050	CIS051	CIS050	0	0	MD053	MD052	MD051	MD050
1	**0**	0	**0**	0	**0**	**0**	**1**	**0**	**0**	0	0	**0**	**1**	**0**	**0**

Bits 10 to 8

STS052	STS051	STS050	Setting of start trigger or capture trigger of channel 5
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	**0**	**1**	**Valid edge of the TI05 pin input is used as both the start trigger and capture trigger.**
0	1	0	Both the edges of the TI05 pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when channel 5 is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Bits 7 and 6

CIS51	CIS50	Selection of TI05 pin input valid edge
0	**0**	**Falling edge**
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: TMR05

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 051	CKS 050	0	CCS 05	0	STS 052	STS 051	STS 050	CIS0 51	CIS0 50	0	0	MD0 53	MD0 52	MD0 51	MD0 50
1	**0**	0	**0**	0	**0**	**0**	**1**	**0**	**0**	0	0	**0**	**1**	**0**	**0**

Bits 3 to 0

MD0 53	MD0 52	MD0 51	MD0 50	Operation mode of channel 5	Corresponding function	Count operation of TCR
0	0	0	1/0	Interval timer mode	Interval timer / Square wave output / divider function / PWM output (master)	Counting down
0	**1**	**0**	1/**0**	**Capture mode**	**Input pulse interval measurement**	**Counting up**
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The operation of the MD050 bit varies depending on each operation mode (see the table below).

Operation mode (Value set by the MD053 to MD051 bits (see table above))	MD050	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0)	**0**	**Timer interrupt is not generated when counting is started (timer output does not change, either).**
• **Capture mode (0, 1, 0)**	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up TI01 and TI05 pin ports

- Port mode register 0 (PM0)
- Port mode register 1 (PM1)
  Select the I/O modes of the TI01 pin (P16) and the TI05 pin (P05).

Symbol: PM1

7	6	5	4	3	2	1	0
PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10
x	**1**	x	x	x	x	x	x

Bit 6

PM16	P16 pin I/O mode selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

Symbol: PM0

7	6	5	4	3	2	1	0
PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00
x	x	**1**	x	x	x	x	x

Bit 5

PM05	P05 pin I/O mode selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.6 Clock Output/Buzzer Output Control Circuit Setup

Figure 5.8 shows the flowchart for setting up the clock output/buzzer output control circuit.

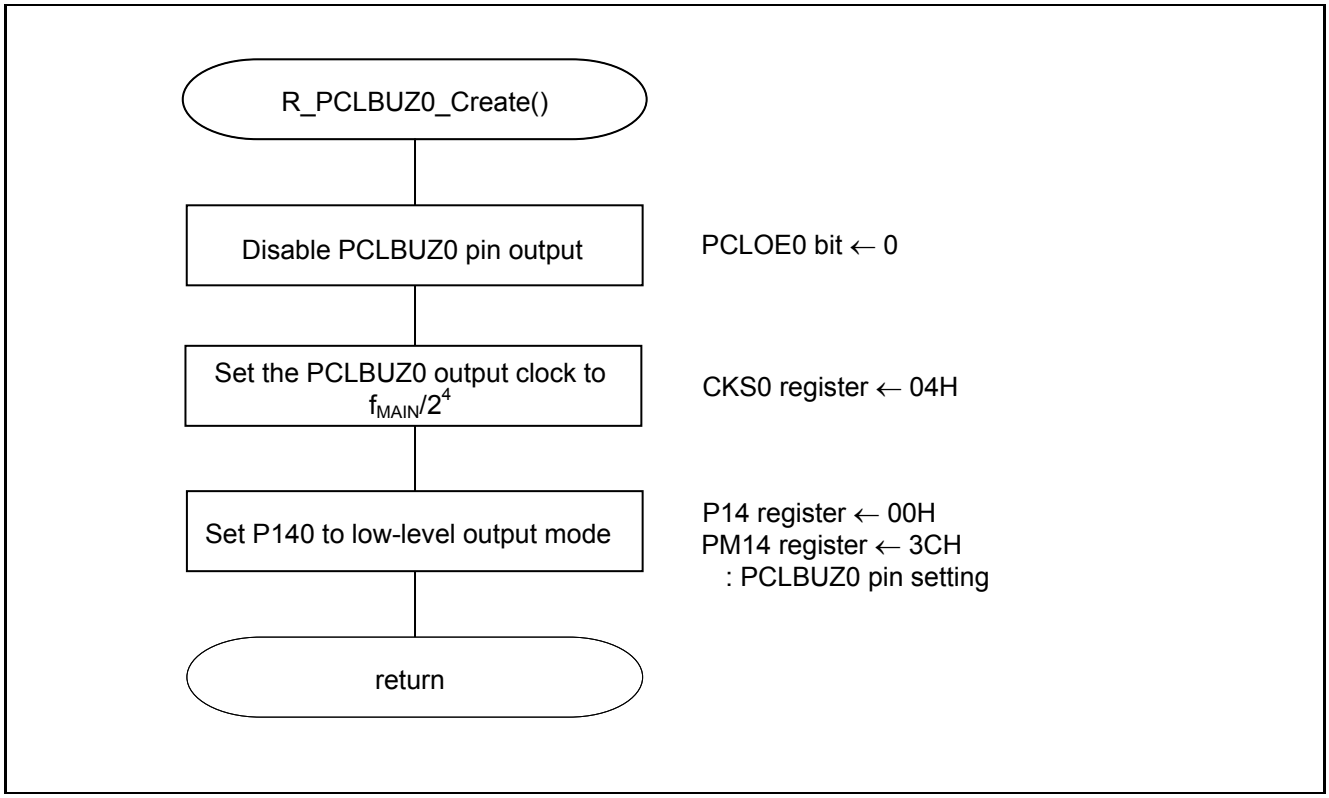

Figure 5.8 Clock Output/Buzzer Output Control Circuit Setup

Selecting output clock

- Clock output select register 0 (CKS0)
  Select PCLBUZ0 pin output clock.

Symbol: CKS0

7	6	5	4	3	2	1	0
PCLOE0	0	0	0	CSEL0	CCS02	CCS01	CCS00
0	0	0	0	**0**	**1**	**0**	**0**

Bit 7

PCLOE0	PCLBUZ0 pin output enable/disable specification
0	**Output disabled.**
1	Output enabled.

Bits 3 to 0

CSEL0	CCS02	CCS01	CCS00	PCLBUZ0 pin output clock selection				
					f_{MAIN} = 5 MHz	f_{MAIN} = 10 MHz	f_{MAIN} = 20 MHz	**f_{MAIN} = 32 MHz**
0	0	0	0	f_{MAIN}	5 MHz	10 MHz	Setting prohibited	Setting prohibited
0	0	0	1	$f_{MAIN}/2$	2.5 MHz	5 MHz	10 MHz	16 MHz
0	0	1	0	$f_{MAIN}/2^2$	1.25 MHz	2.5 MHz	5 MHz	8 MHz
0	0	1	1	$f_{MAIN}/2^3$	625 kHz	1.25 MHz	2.5 MHz	4 MHz
0	**1**	**0**	**0**	**$f_{MAIN}/2^4$**	312.5 kHz	625 kHz	1.25 kHz	**2 MHz**
0	1	0	1	$f_{MAIN}/2^{11}$	2.44 kHz	4.88 kHz	9.77 kHz	15.63 kHz
0	1	1	1	$f_{MAIN}/2^{12}$	1.22 kHz	2.44 kHz	4.88 kHz	7.81 kHz
1	0	0	0	$f_{MAIN}/2^{13}$	610 Hz	1.22 kHz	2.44 kHz	3.91 kHz
1	0	0	0	f_{SUB}	32.768 kHz			
1	0	0	1	$f_{SUB}/2$	16.384 kHz			
1	0	1	0	$f_{SUB}/2^2$	8.192 kHz			
1	0	1	1	$f_{SUB}/2^3$	4.096 kHz			
1	1	0	0	$f_{SUB}/2^4$	2.048 kHz			
1	1	0	1	$f_{SUB}/2^5$	1.024 kHz			
1	1	1	0	$f_{SUB}/2^6$	512 Hz			
1	1	1	1	$f_{SUB}/2^7$	**256 Hz**			

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up PCLBUZ0 pin port

- Port mode register 14 (PM14)
- Port register 14 (P14)
  Set up the PCLBUZ0 (P140) I/O mode and output data.

Symbol: PM14

7	6	5	4	3	2	1	0
PM147	PM146	1	1	1	1	PM141	PM140
x	x	1	1	1	1	x	**0**

Bit 0

PM140	PM140 pin I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Symbol: P14

7	6	5	4	3	2	1	0
P147	P146	P145	P144	P143	P142	P141	P140
x	x	x	x	x	x	x	**0**

Bit 0

P140	P140 output data control
0	**Output 0**
1	Output 1

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.7 Initialization of INTP0

Figure 5.9 shows the flowchart for initializing INTP0.

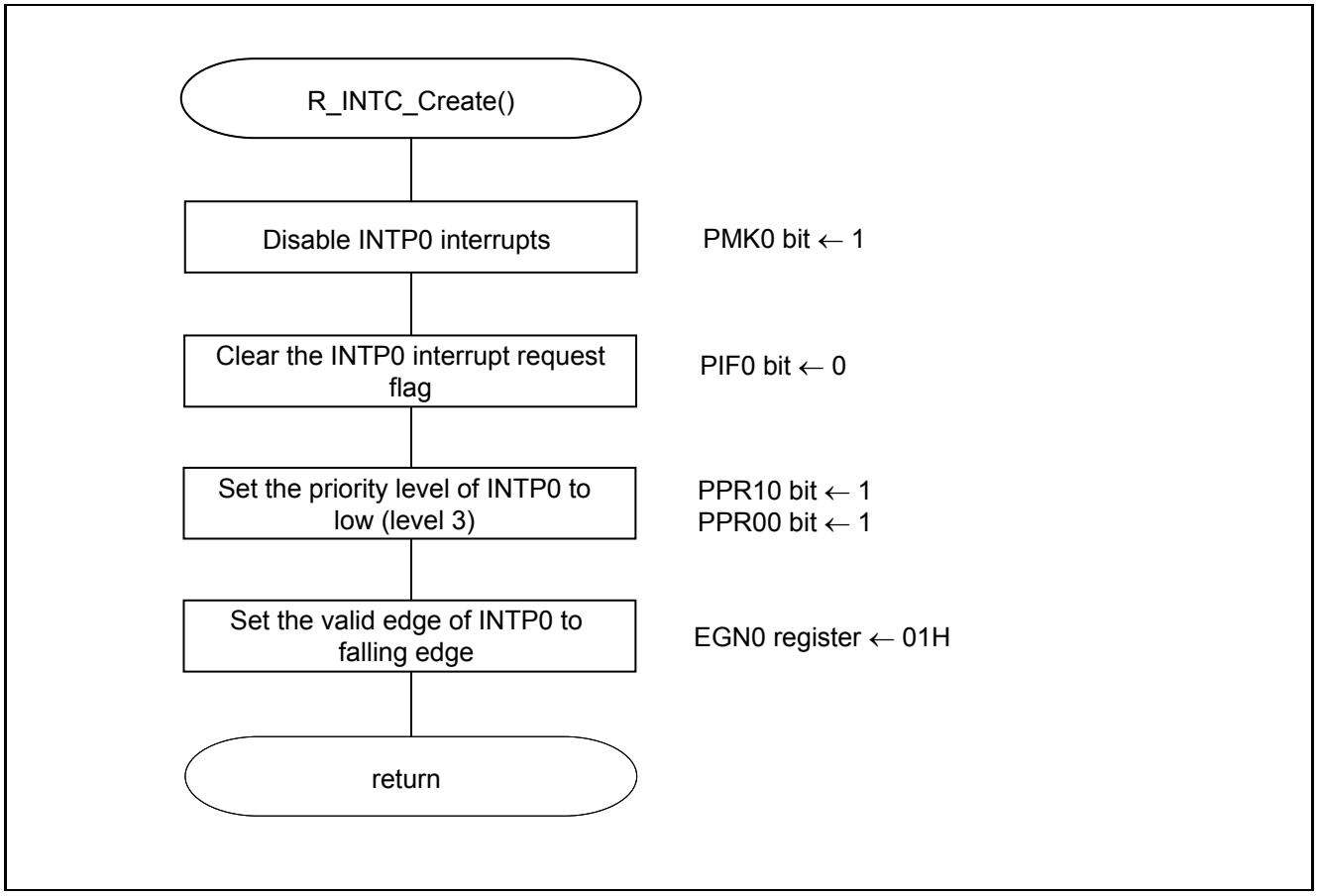

Figure 5.9 Initialization of INTP0

Setting up INTP0 interrupt handling

- Interrupt mask flag register (MK0L, MK2L, and MK2H)
  Mask interrupts.

Symbol: MK0L

7	6	5	4	3	2	1	0
PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIMK	WDTIMK
x	x	x	x	x	**1**	x	x

PMK0	Interrupt handling control
0	Interrupt handling is enabled
1	**Interrupt handling is disabled**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up INTP0 interrupt request flag

- Interrupt request flag register (IF0L, IF2L, IF2H)
  Set up interrupt request.

Symbol: IF0L

7	6	5	4	3	2	1	0
PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIIF	WDTIIF
x	x	x	x	x	**0**	x	x

PIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request signal is generated, interrupt request status

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting the priority level of INTP0

- Priority specification flag register (PR00L and PR10L)
  Set interrupt priority levels.

Symbol: PR00L

7	6	5	4	3	2	1	0
PPR05	PPR04	PPR03	PPR02	PPR01	PPR00	LVIPR0	WDTIPR0
x	x	x	x	x	**1**	x	x

Symbol: PR10L

7	6	5	4	3	2	1	0
PPR15	PPR14	PPR13	PPR12	PPR11	PPR10	LVIPR1	WDTIPR1
x	x	x	x	x	**1**	x	x

PPR10	PPR00	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	**1**	**Specify level 3 (low priority level)**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Selecting the valid edge of INTP0

- External interrupt rising edge enable register (EGP0)
- External interrupt falling edge enable register (EGN0)
  Select the valid edge of an external interrupt.

Symbol: EGP0

7	6	5	4	3	2	1	0
EGP7	EGP6	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0
x	x	x	x	x	x	x	**0**

Symbol: EGN0

7	6	5	4	3	2	1	0
EGN7	EGN6	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0
x	x	x	x	x	x	x	**1**

EGP0	EGN0	INTP0 pin valid edge selection
0	0	Edge detection disabled
0	**1**	**Falling edge**
1	0	Rising edge
1	1	Both falling and rising edges

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.8 Main Processing

Figures 5.10 and 5.11 show the flowcharts for the main processing.

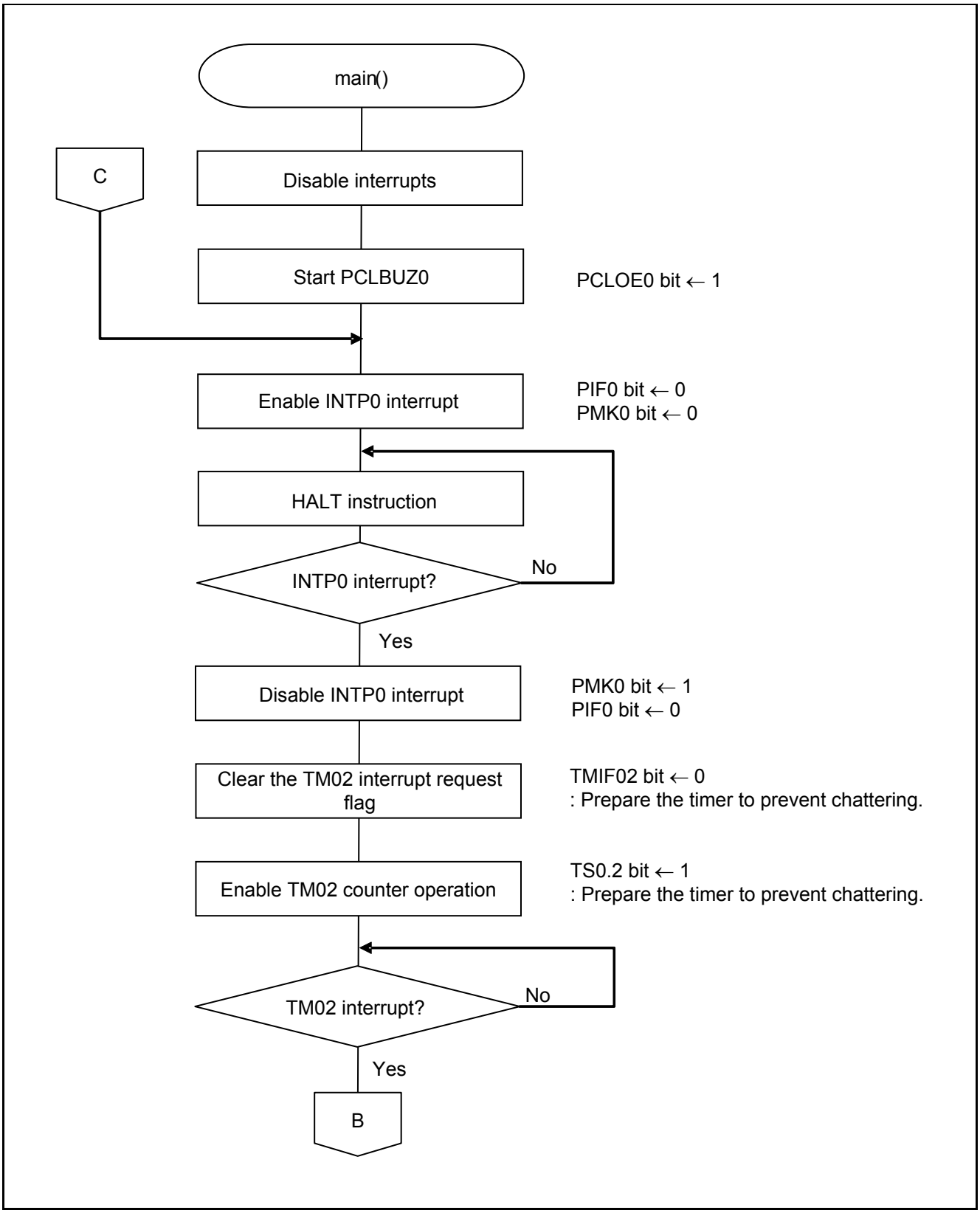

Figure 5.10 Main Processing (1/2)

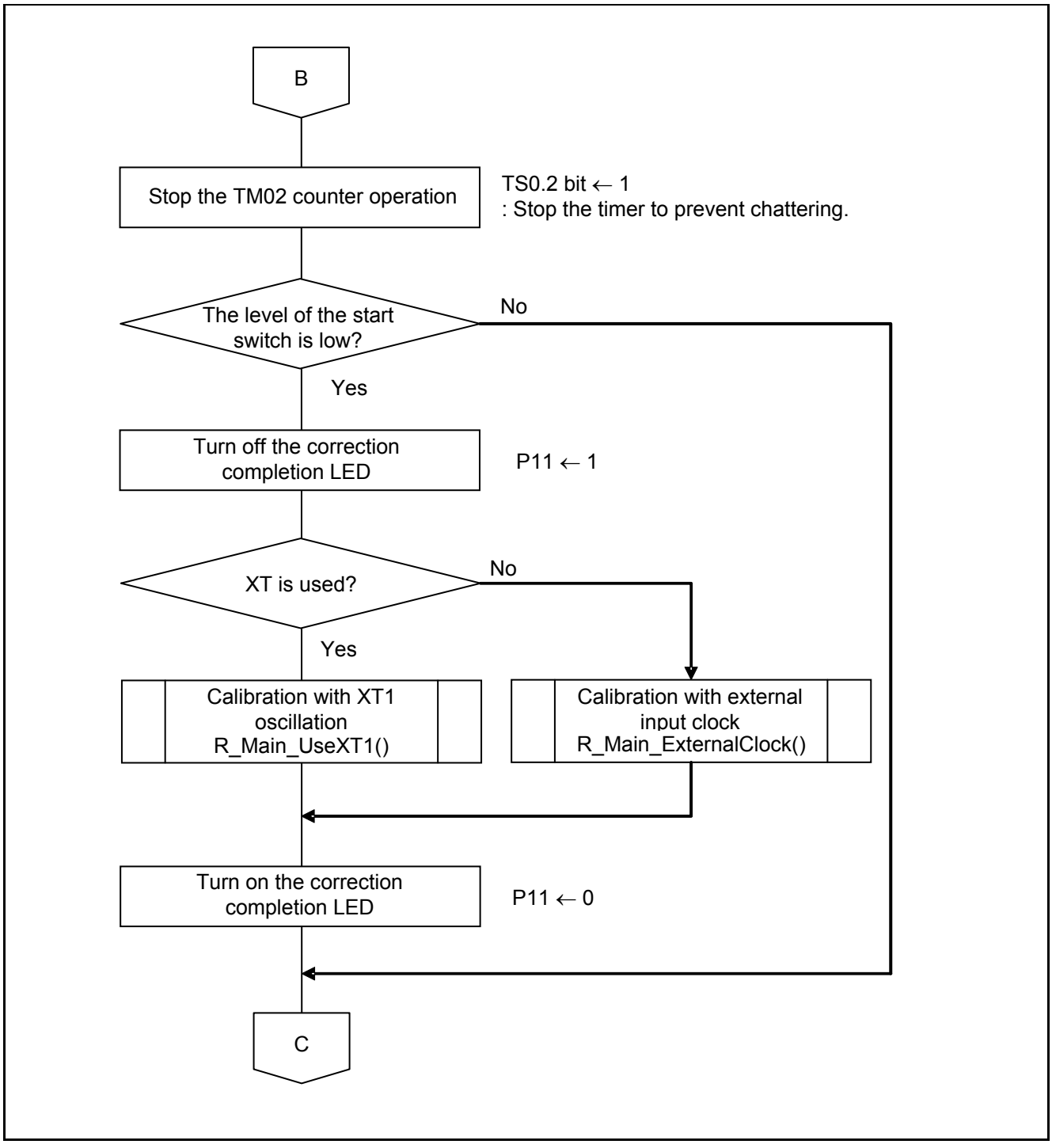

Figure 5.11 Main Processing (2/2)

5.7.9 Calibration with XT1 Oscillation

Figures 5.12 and 5.13 show the flowcharts for calibration with XT1 oscillation.

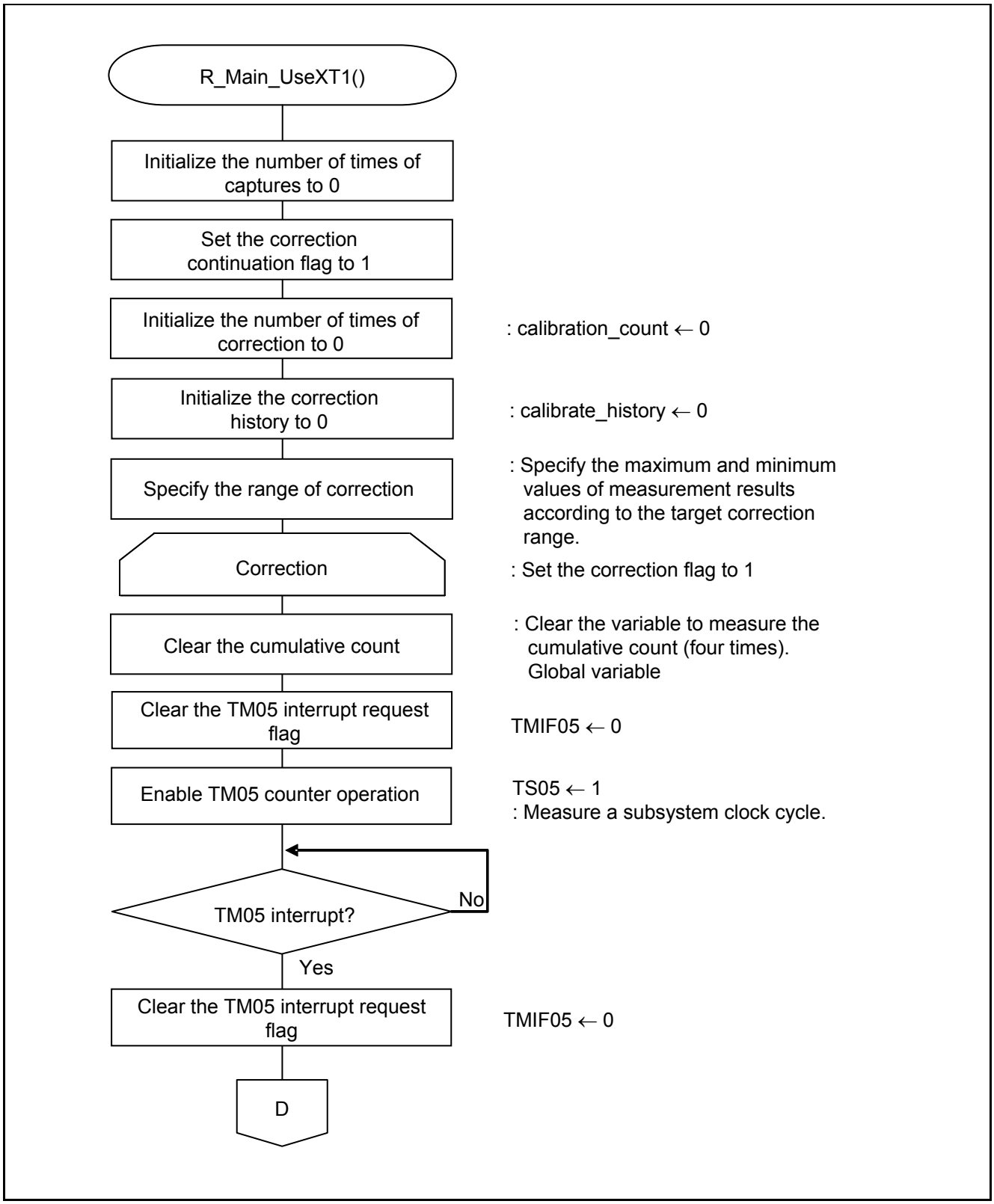

Figure 5.12 Calibration with XT1 Oscillation (1/2)

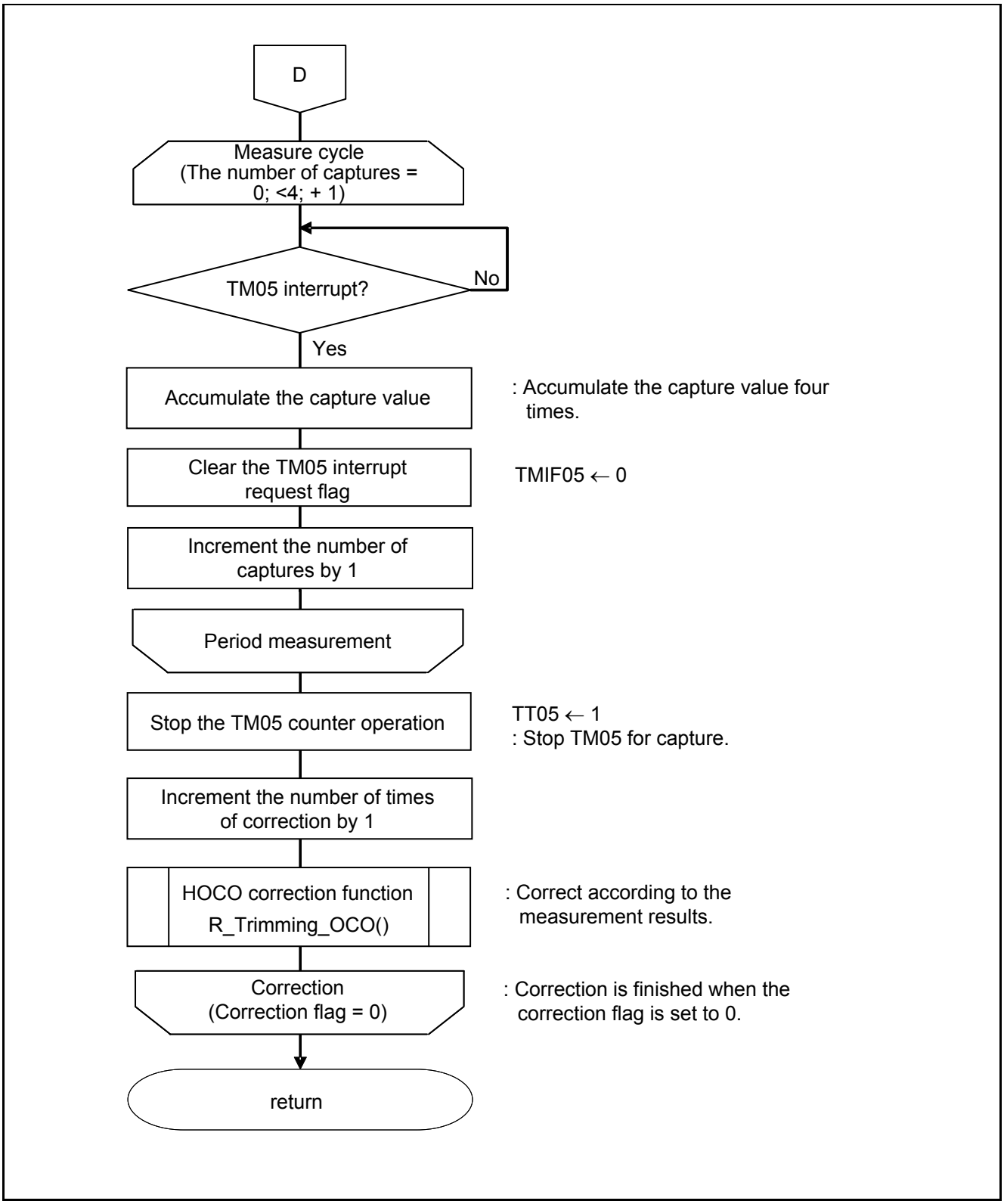

Figure 5.13 Calibration with XT1 Oscillation (2/2)

5.7.10 Calibration with External Input Clock

Figure 5.14 shows the flowchart for calibration with an external input clock.

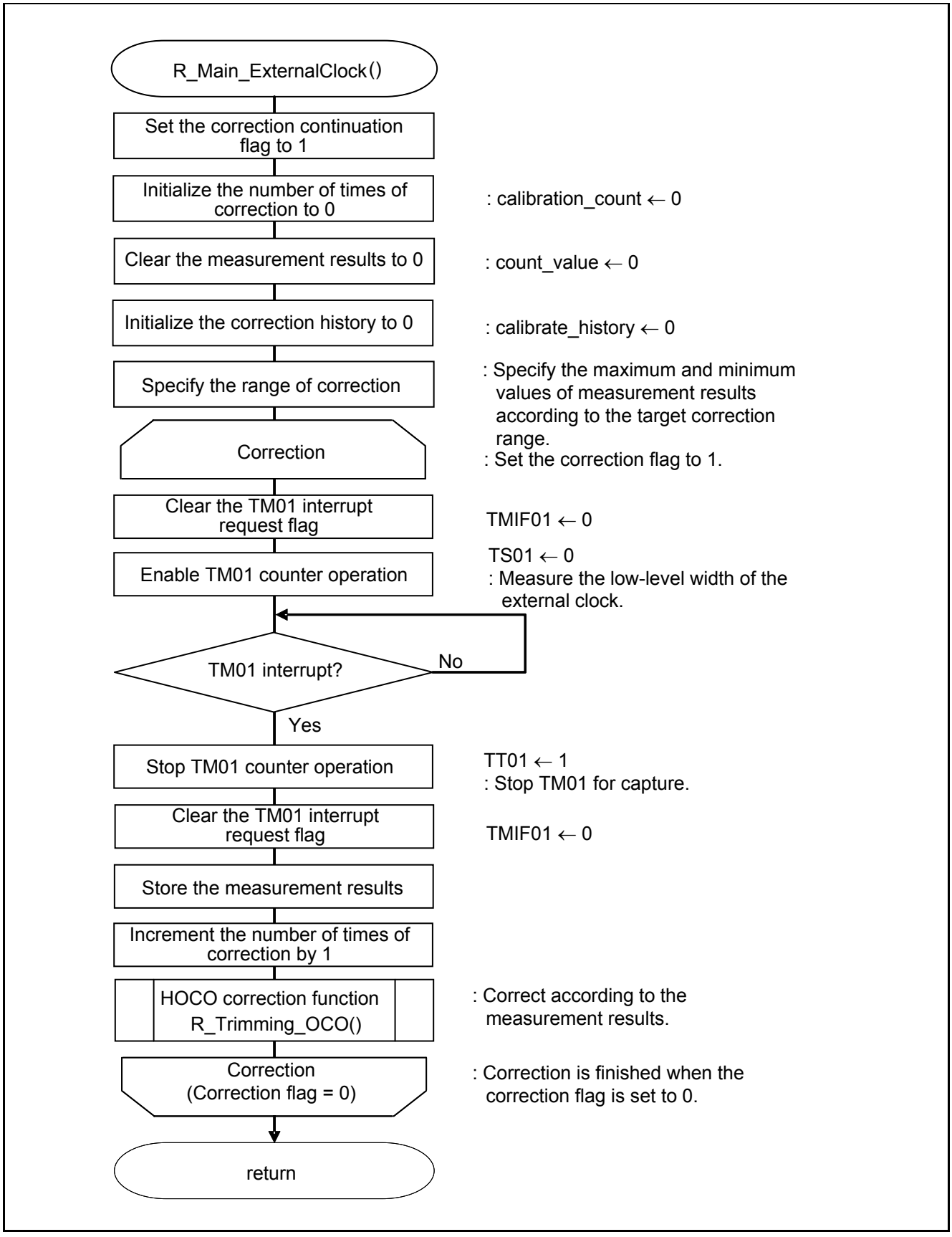

Figure 5.14 Calibration with External Input Clock

Obtaining the TAU0 capture value

- Timer data register 05 (TDR05)
  Measurement results of the subsystem clock pulse interval
- Timer data register 01 (TDR01)
  Measurement results of the low-level width of the TI01 pin pulse

Symbol: TDR05

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

The count of the pulse interval of the subsystem clock is (TDR05 register value + 1).

Symbol: TDR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

The count of the low-level width of the TI01 pin pulse is (TDR01 register value + 1).

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Starting timer channel operation

- Timer channel start register 0 (TS0)
  Timer start setting

Symbol: TS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TSH03	0	TSH01	0	TS07	TS06	TS05	TS04	TS03	TS02	TS01	TS00
0	0	0	0	0	0	0	0	x	x	**1/0**	x	x	x	**1/0**	x

Bit 5

TS05	Operation enable (start) trigger of channel 5
0	No trigger operation
1	**The TE05 bit is set to 1 and the count operation becomes enabled.**

Bit 1

TS01	Operation enable (start) trigger of channel 1
0	No trigger operation
1	**The TE01 bit is set to 1 and the count operation becomes enabled.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Stopping timer channel operation

- Timer channel stop register 0 (TT0)
  Timer stop setting

Symbol: TT0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TTH03	0	TTH01	0	TT07	TT06	TT05	TT04	TT03	TT02	TT01	TT00
0	0	0	0	0	0	0	0	x	x	**1/0**	x	x	x	**1/0**	x

Bit 5

TT05	Operation stop trigger of channel 5
0	No trigger operation
1	**Operation is stopped (stop trigger is generated).**

Bit 1

TT01	Operation stop trigger of channel 1
0	No trigger operation
1	**Operation is stopped (stop trigger is generated).**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.11 HOCO Correction Function

Figures 5.15 and 5.16 show the flowcharts for the HOCO correction function.

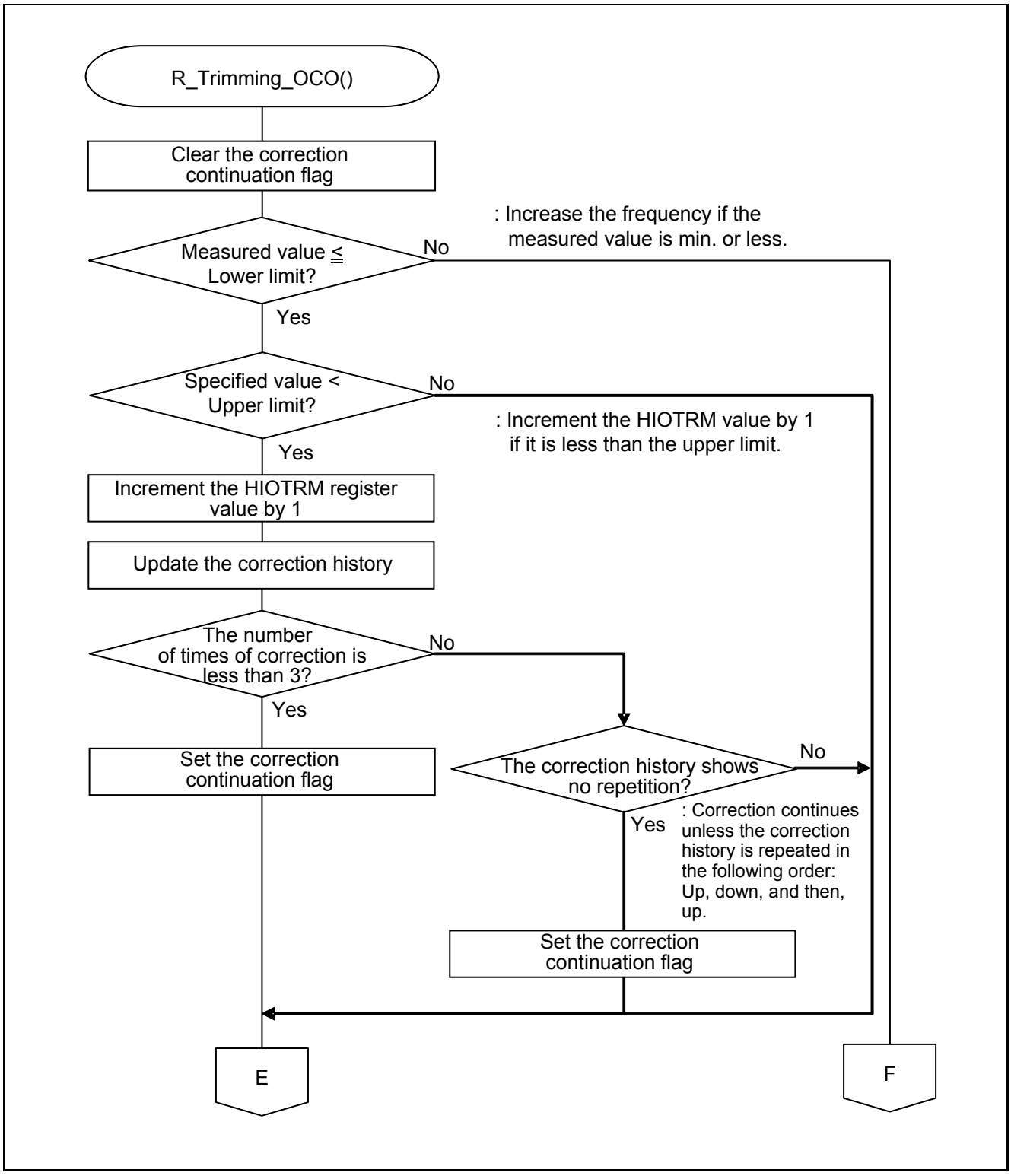

Figure 5.15 HOCO Correction Function (1/2)

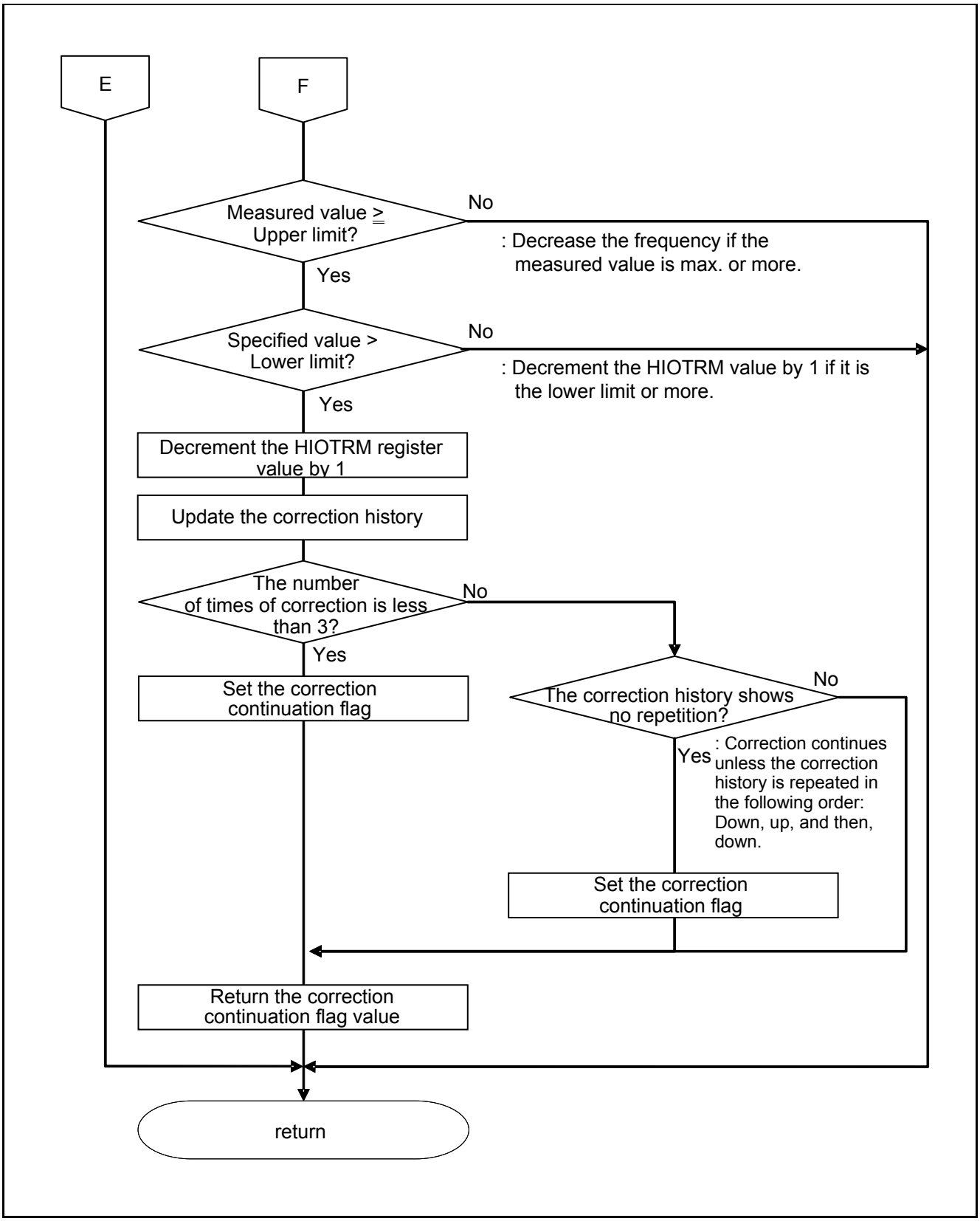

Figure 5.16 HOCO Correction Function (2/2)

Correcting the HOCO clock frequency

- High-speed on-chip oscillator trimming register (HIOTRM)
  Correct the HOCO clock frequency.

Symbol: HIOTRM

7	6	5	4	3	2	1	0
0	0	HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0
0	0	**1/0**	**1/0**	**1/0**	**1/0**	**1/0**	**1/0**

Bits 5 to 0

HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0	Internal high-speed oscillator
0	0	0	0	0	0	Minimum speed
0	0	0	0	0	1	▲
0	0	0	0	1	0	
0	0	0	0	1	1	
0	0	0	1	0	0	
			.			
			.			
			.			
1	1	1	1	1	0	▼
1	1	1	1	1	1	Maximum speed

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

User's Manual:

RL78/G13 User's Manual: Hardware (R01UH0146E)
RL78 Family User's Manual: Software (R01US0015E)
The latest version can be downloaded from the Renesas Electronics website.

Technical Updates/Technical News

The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics Website

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Inquiries

http://www.renesas.com/contact/

Revision Record	RL78/G13 High-speed On-chip Oscillator (HOCO) Clock Frequency Correction

Rev.	Date	Description	
		Page	Summary
1.00	Feb. 15, 2016	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

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