RL78/G13

EEPROM Control by Microwire Communications

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Introduction

Microwire interface is one of serial communication interfaces. This application note shows how to realize Microwire communications by using three-wire serial I/O of RL78/G13 serial array unit.

Target Device

RL78/G13

When applying the sample program covered in this application note to another RL78 microcontroller, conduct an extensive evaluation to use.

Contents

1. Specifications

This application note shows how to realize Microwire communications by using three-wire serial I/O of serial array unit. CSI of RL78/G13 operates as a master and controls Atmel EEPROM (AT93C46D) of slave side by Microwire communications. Write and Read of data are performed according to the instruction set of AT93C64D, and it is confirmed that the written contents can be read correctly.

Table 1.1 shows peripherals to be used and purposes and Figure 1.1 shows operations of Microwire.

Table 1.1 Peripherals and Purposes

Peripheral	Purpose
Chanel 0 of serial array unit 0	Master transmission/reception of CSI00
Port output	Output of chip select

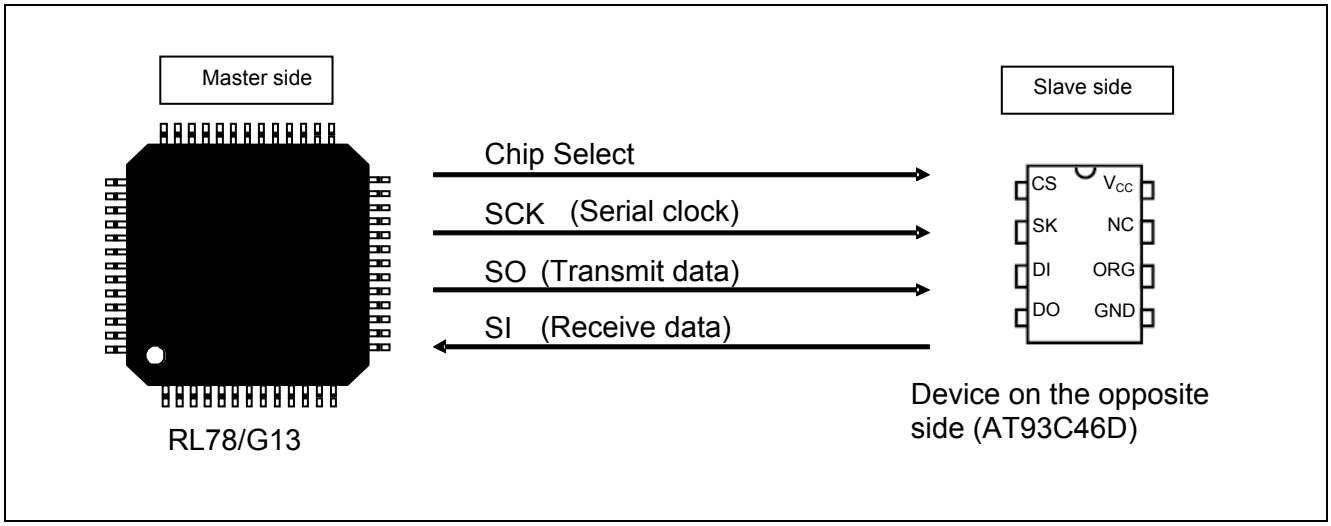


Figure 1.1 Operation of Microwire

ATMEL AT93C46D as device on the opposite side is an 8-pin EEPROM device in which the Microwire is equipped as a communication interface. Its capacity is 1024 bits and can choose the two modes shown in Table 1.2 by processing of ORG pin of AT93C46D. In this application, ORG pin is connected to V_{CC} and data width is 16 bits. Refer to the latest version datasheet of AT93C46D for the newest and exact information.

Table 1.2 Mode Switching of AT93C46D

	Data width per unit address	Address space	Address width
ORG pin: GND	8 bits	Addresses 0 to 127 (0 to 7FH)	7 bits
ORG pin: V_{CC}	16 bits	Addresses 0 to 63 (0 to 3FH)	6 bits

Table 1.3 shows instruction sets of AT93C46D to be used in this application. All of numerical values and characters are denoted by the binary system, and it is a bit string which continues to the right from the left (from SB column to Address column (or Data column)) of Table 1.3. Refer to the latest version datasheet of AT93C46D for the newest and exact information.

Table 1.3 Control Instruction Sets of AT93C46D

Instruction	SB	OpC	Address						Data	Note
READ	1	10	A_5	A_4	A_3	A_2	A_1	A_0		The value read from DO pin begins from 0 of a dummy bit.
WRITE	1	01	A_5	A_4	A_3	A_2	A_1	A_0	D_{15} - D_0	CS pin is set as Low after transmission, and it is reflected in AT93C46D by standing by for 250 ns. It is a setting success, if CS is again set as High after that and DO pin is High.
ERAL	1	00	1	0	X	X	X	X		
EWEN	1	00	1	1	X	X	X	X		
EWDS	1	00	0	0	X	X	X	X		

SB: Start Bit

OpC: Operation Code

X: Don't Care

Figure 1.2 shows AT93C46D digital timing diagram of CS pin. In Microwire communication, when a chip select signal is set to High, it means valid (selected), and when a chip select signal is set to Low, it means invalid (non-selected). Please keep in mind that it differs from SPI communication. If 50 ns or more passes after setting CS as High, the clock receiving of SK pin will be available. It can fill with 2 clocks or more of a CPU clock (f_{CPU}) by clock setup in this application. This time required changes with V_{CC} voltage. Refer to the latest version datasheet of AT93C46D for the newest and exact information.

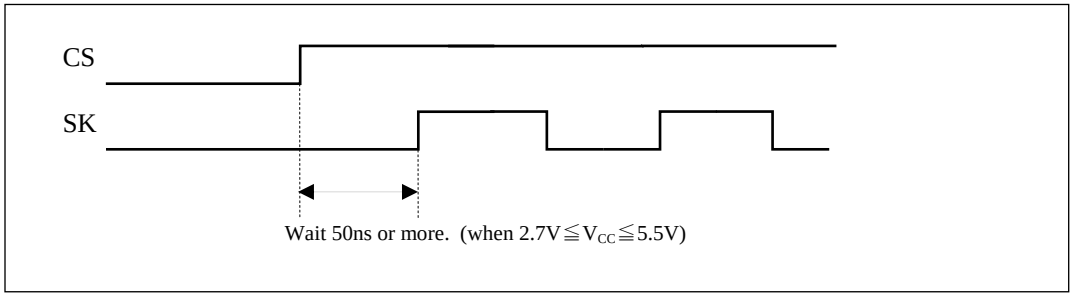


Figure 1.2 Digital Timing Diagram of CS Pin

Figure 1.3 shows the setup timing of AT93C46D DI pin (data input pin). Setup value of DI pin is obtained at the timing of the clock's rising edge and taken into AT93C46D. Therefore, the data setup (data change) for DI pin needs to avoid just before and immediately after of clock rising timing as shown in Figure 1.3. The time required for this processing changes with V_{CC} voltage. Refer to the latest version datasheet of AT93C46D for the newest and exact information.

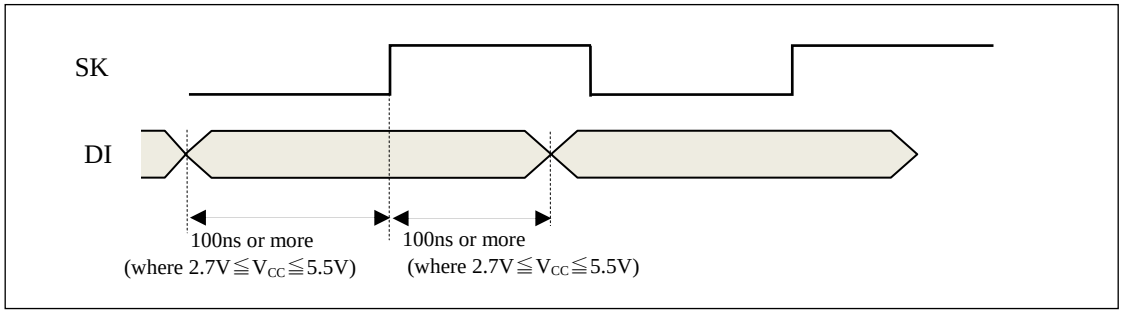


Figure 1.3 Digital Timing Diagram of DI Pin

Figure 1.4 shows the timing to read data from DO pin (data output pin) by AT93C46D READ instruction. In order to make it easy to understand, the timing that output value of DO pin is 0 is presented as an example. Since the clock rising of SK pin serves as an output and both DI pin and DO pin make the rising of clock the trigger, when communicating by a CSI function, it needs to be cautious of a phase setup. The time required for this processing changes with V_{CC} voltage. Refer to the latest version datasheet of AT93C46D for the newest and exact information.

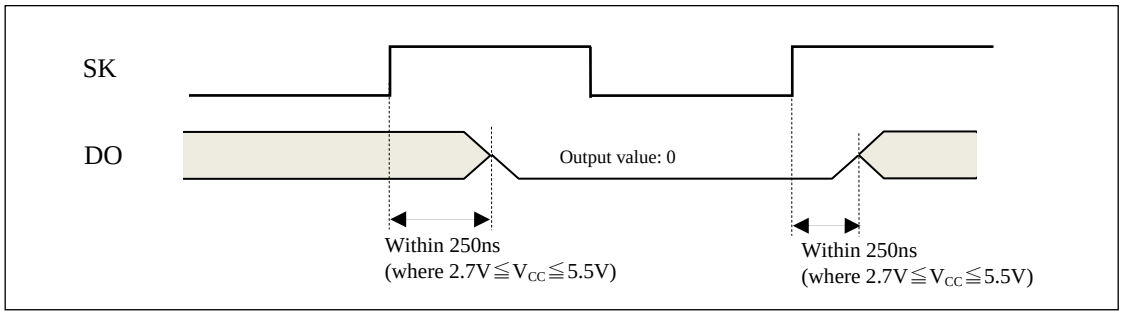


Figure 1.4 Digital Timing Diagram of DO Pin

2. Operation Check Conditions

The sample code described in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G13 (R5F100LE)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 32 MHz • CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0 V (Operation is possible over a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode which uses 2.81 V (2.76 V to 2.87V)
Integrated development environment	Cube Suite+V2.00.00 from Renesas Electronics Corp.
C compiler	CA78K0R V1.60 from Renesas Electronics Corp.
Board to be used	RL78/G13 target board (QB-R5F100LE-TB) + AT93C46D

3. Related Application Notes

The application notes that are related to this application note are listed below for reference.

- RL78/G13 Initialization (R01AN0451E) Application Note
- RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Master Transmission/Reception) (R01AN0460E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows the Microwire connection example of RL78/G13 and EEPROM (AT93C46D).

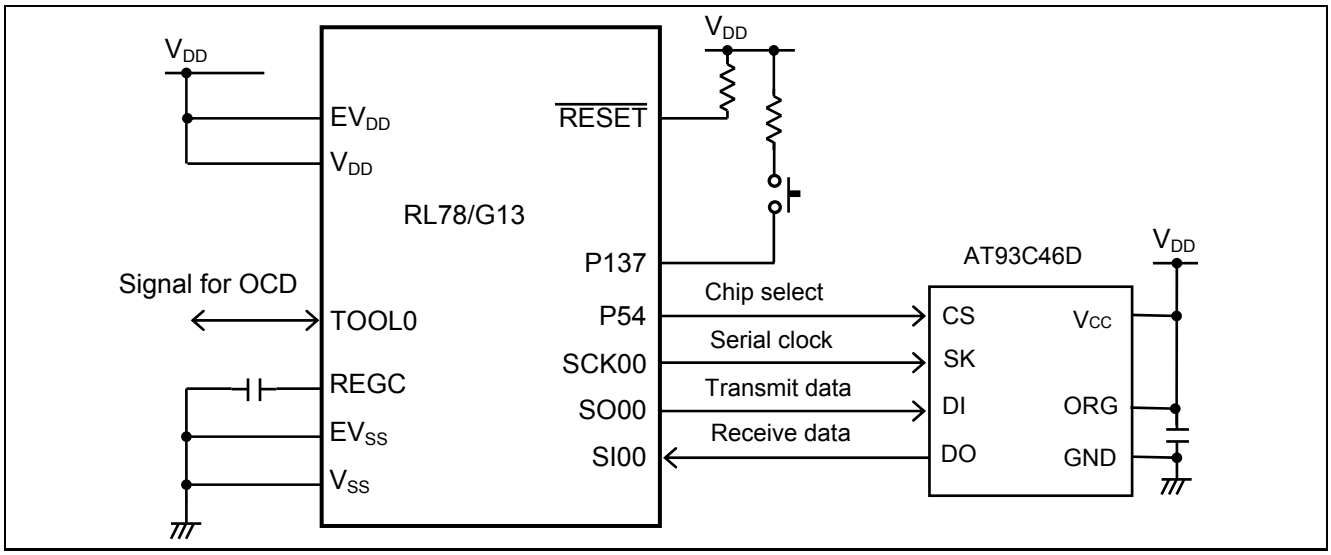


Figure 4.1 Microwire Connection Example of RL78/G13 and EEPROM (AT93C46D)

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. When there is a pin of the name which starts with EV_{SS}, connects with V_{SS}, and when there is a pin of the name which starts with EV_{DD}, connects with V_{DD}.

3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

4.2 List of Pins to be Used

Table4.1 lists pins to be used and their functions.

Table4.1 Pins to be Used and their Functions

Pin Name	I/O	Description
P54	Output	Output of chip select
P10/SCK00/SCL00	Output	Provide for serial clock
P12/SO00/TxD0/TOOLTxD	Output	Data transmit (MCU → EEPROM)
P11/SI00/RxD0/TOOLRxD/SDA00	Input	Data receive (MCU ← EEPROM)
P137/INTP0	Input	Restart switch

5. Description of Software

5.1 Operation Outline

In this application note, CSI (master transmission and reception) performs transmission and reception to device on the opposite side (slave side). Providing clock to the slave side, data transmission of 128 bytes, and data receiving of 128 bytes from slave side are performed. Due to the communication interface of device on the opposite side (slave side) is Microwire, the half-duplex is adopted in this application note.

(1) The SAU0 is initialized.

<Setting conditions>

- Uses the SAU0 channel 0 as CSI.
- Sets a serial clock as 32MHHz.
- INTCSI00 type: Uses the transfer end interrupt (single-transfer mode)
- A start factor is a software trigger.
- CSI communication mode is transmission/reception mode.
- Phase of clock and data is type 4.
- MSB first transfer
- Baud rate: 500kbps (32MHz is divided by 64)
- Data length is 8-bit data length.
- Initial state of SCK00 pin: low level
- Initial state of SO00 pin: low level

(2) An EWEN command (writing/delete permission) is executed to device on the opposite side (AT93C46D). Thereby, a WRITE command (writing) and an ERAL command (all the area deletion) become usable.

(3) An ERAL command (all the area deletion) is executed to device on the opposite side (AT93C46D). Then, the CS pin of device on the opposite side (AT93C46D) is set to Low (non-selected state), and the DO pin (status) is checked after standby of a specified period of time. This is repeated until confirming High (all the area deletion is completed) of the DO pin.

(4) A WRITE command (data writing) is executed to device on the opposite side (AT93C46D). Then, the CS pin of device on the opposite side (AT93C46D) is set to Low (non-selected state), and the DO pin (status) is checked after standby of a specified period of time. This is repeated until confirming High (all the area deletion is completed) of the DO pin. After the confirmation, the address for writing and the data to be written are updated respectively, and this is repeated 64 times from address 0 to address 63 of device on the opposite side (AT93C46D).

The data to be written is 2 bytes for one address. Because total 9 bits of a start bit (1), OpC (2), and an address (6) accompany the data to be written in advance, a total of 25 bits are right-aligned (LSB) in “unsigned char” type 4 bytes and transmitted. The 1st byte is set to 00000001B, the 2nd byte is set to 01A5A4A3A2A1A0B, the 3rd byte is set to D15D14D13D12D11D10D9D8, the 4th byte is set to D7D6D5D4D3D2D 1D0, and they are transmitted by MSB first. Because device on the opposite side (AT93C46D) reads the data of the DI pin in the rising edge of clock timing, the phase type 4 can respond in CSI of RL78/G13. Figure 5.1 shows the timing of WRITE command execution.

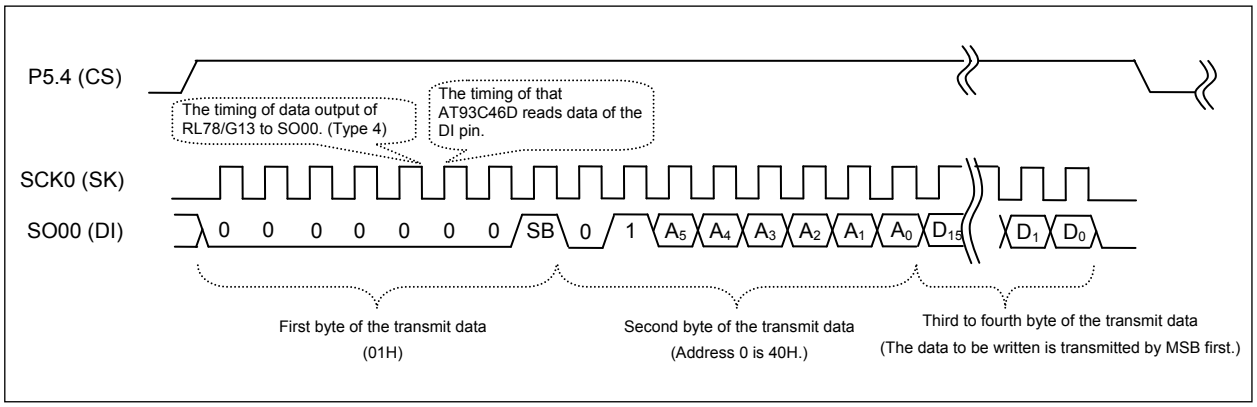


Figure 5.1 The Timing of WRITE Command Execution

(5) An READ command (data reading) is executed to device on the opposite side (AT93C46D). It checks that the data from address 0 to address 63 was read in order, and the same contents as the written-in data can be read on the screen of a debugger (CubeSuite+). Since the read-out range is from address 0 to address 63 of device on the opposite side (AT93C46D), a READ command is executed 64 times**.** Figure 5.2 shows the timing of READ command execution.

The data to be written is 2 bytes for one address. A total of 26 bits (a start bit (1), OpC (2), an address (6), dummy bit [value 0] (1) for timing adjustment, and dummy bit [value FFFFH] (16) for urging the clock supply under data reading) are right-aligned (LSB) in “unsigned char” type 4 bytes and transmitted. In other words, the 1st byte is set to 00000010B, the 2nd byte is set to $1A_5A_4A_3A_2A_1A_00$B, the 3rd byte is set to FFH, the 4th byte is set to FFH, and they are transmitted by MSB first. Although device on the opposite side (AT93C46D) reads the data of DI pin in the rising edge of a clock timing, the data output to DO pin also synchronizes with the timing of a clock standup. Therefore, under ordinary circumstances, the right method will change a phase into Type 2 from Type 4 from the 3rd byte of command, but phase type 4 transmission and reception are continued in this application on the grounds that the output delay time of AT93C46D is 250 ns at the maximum, and it is a large enough compared with the hold time of CSI00. However, as this is a strictly experimental trial, in a customer's development, please confirm the datasheet of communication device on the opposite side and design according to the specification. Figure 5.2 shows the timing of READ command execution.

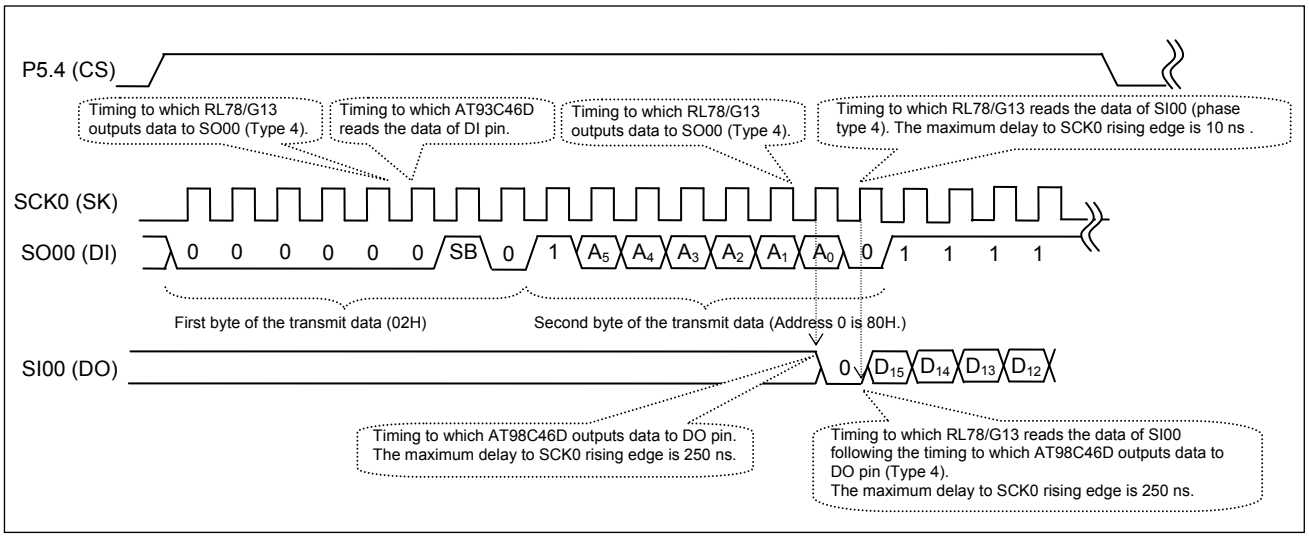


Figure 5.2 The Timing of READ Command Execution

5.2 List of Option Byte Settings

Table 5.1 shows the option byte settings. Please set up the optimal value for a customer's system if needed.

Table 5.1 Option Byte Settings to be Used in This Sample Code

Address	Setting	Description
000C0H	11101110B	Stops the watchdog timer. (Stops counting after the end of reset status.)
000C1H	01111111B	LVD reset mode 2.81 V (2.76 V to 2.87 V)
000C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H	10000101B	Enables the on-chip debugger

5.3 List of Constants

Table5.2 shows the constants list for the sample code.

Table5.2 Constants for the Sample Code

Constant	Setting	Description
_0000_SAU_CK00_FCLK_0	0000H	Operation clock CK00 is undivided (CK00=f_{CLK}).
_0000_SAU_CK01_FCLK_0	0000H	Operation clock CK01 is undivided (CK01=f_{CLK}).
_0004_SAU_SIRMN_FECTMN	0004H	Clears the framing error flag.
_0002_SAU_SIRMN_PECTMN	0002H	Clears the parity error flag.
_0001_SAU_SIRMN_OVCTMN	0001H	Clears the overrun error detection flag.
_0020_SAU_SMRMN_INITIALVALUE	0020H	Initial value of SMR00 register
_0000_SAU_CLOCK_SELECT_CK00	0000H	Selects CK00 to the operation clock.
_0000_SAU_CLOCK_MODE_CKS	0000H	Selects an operation clock to the transfer clock.
_0000_SAU_TRIGGER_SOFTWARE	0000H	Only software trigger is valid as the start trigger.
_0000_SAU_MODE_CSI	0000H	Setting of CSI mode
_0000_SAU_TRANSFER_END	0000H	Selects the transfer end interrupt for the interrupt source.
_C000_SAU_RECEPTION_TRANSMISSION	C000H	Sets the transmission/reception mode.
_3000_SAU_TIMING_4	3000H	Data and clock phase of CSI mode is type 4.
_0000_SAU_MSB	0000H	Inputs/outputs data with MSB first.
_0007_SAU_LENGTH_8	0007H	8-bit data length (stored in bits 0 to 7 of the SDRmn register)
_3E00_CSI00_DIVISOR	3E00H	Transfer clock is the operation clock divided by 64.
~_0100_SAU_CH0_CLOCK_OUTPUT_1	FEFFH	Initial output value of the serial clock is 0.
~_0001_SAU_CH0_DATA_OUTPUT_1	FFFEH	Initial output value of the data clock is 0.
_0001_SAU_CH0_OUTPUT_ENABLE	0001H	Serial output enable register
_0001_SAU_CH0_START_TRG_ON	0001H	Enters the communication wait status.
_0001_SAU_CH0_STOP_TRG_ON	0001H	Stops the communication operation.
~_0001_SAU_CH0_OUTPUT_ENABLE	FFFEH	Stops output by serial communication operation.

5.4 List of Variables

Table5.3 shows the global variables list.

Table5.3 Global Variables

Type	Variable Name	Contents	Function Used
uint8_t	tx_bufA [4]	Stores commands to EEPROM, addresses, and transmit data.	S_MICRO_EWEN, S_MICRO_EWDS, S_MICRO_ERAL, S_MICRO_ERASE, S_MICRO_READ, S_MICRO_WRITE
uint8_t	rx_bufA [4]	Stores receive data from EEPROM.	S_MICRO_READ
uint8_t	tx_numA	Number of communications with EEPROM.	S_MICRO_EWEN, S_MICRO_EWDS, S_MICRO_ERAL, S_MICRO_ERASE, S_MICRO_READ, S_MICRO_WRITE
uint16_t	READDATA[64]	The final storage location of received data	main
volatile uint8_t	g_csi00_comflag	Communication state flag of CSI00	S_COMUNICATION, R_CSI00_Send_Receive, r_csi00_interrupt
volatile uint16_t	g_csi00_tx_count	Number of transmit data	R_CSI00_Send_Receive r_csi00_interrupt
volatile uint8_t *	gp_csi00_tx_address	Transmit data pointer	R_CSI00_Send_Receive r_csi00_interrupt
volatile uint8_t *	gp_csi00_rx_address	Transmit data pointer	R_CSI00_Send_Receive r_csi00_interrupt

5.5 List of Functions

Table5.4 shows the functions list.

Table5.4 List of Functions

Function Name	Outline
S_MICRO_EWEN	Makes EEPROM write-enable state.
S_MICRO_EWDS	Makes EEPROM write-disable state.
S_MICRO_ERAL	The whole chip of EEPROM is deleted.
S_MICRO_READ	Reads data from specified address of EEPROM.
S_MICRO_WRITE	Writes data to specified address of EEPROM.
S_COMUNICATION	The function including from starting access to completion to EEPROM.
S_CHKEND	Writing/deletion state (Ready or Busy) check processing of EEPROM.
S_WAITTSV	Waiting processing
R_CSI00_Start	CSI00 setting processing to communication standby state (for code generated amount)
R_CSI00_Send_Receive	Starting communication of CSI00 (for code generated amount)
r_csi00_interrupt	Communication end interrupt of CSI00 (for code generated amount)

5.6 Function Specifications

This section describes the specifications for the functions that are used in the sample code.

[Function Name] S_MICRO_EWEN	
Synopsis	Makes serial EEPROM write-enable state by sending EWEN command.
Header	–
Declaration	void S_MICRO_EWEN(void)
Explanation	Makes serial EEPROM write-enable state by sending EWEN command.
Arguments	None
Return value	None

[Function Name] S_MICRO_EWDS	
Synopsis	Write-disable setup processing
Header	–
Declaration	void S_MICRO_EWDS(void)
Explanation	Makes serial EEPROM write-disable by sending EWDS command.
Arguments	None
Return value	None

[Function Name] S_MICRO_ERAL	
Synopsis	Chip erasing start trigger processing
Header	–
Declaration	void S_MICRO_ ERAL (void)
Explanation	Triggers chip erasing by sending ERAL command to serial EEPROM. (Confirming completion of erasing is another processing.)
Arguments	None
Return value	None

[Function Name] S_MICRO_READ	
Synopsis	Data read from specified address processing
Header	r_cg_macrodriver.h
Declaration	uint16_t S_MICRO_READ(uint8_t address8)
Explanation	Reads out data from specified address by sending READ command to serial EEPROM.
Arguments	uint8_t address8 : An address in which data to be read is stored
Return value	Read data (uint16_t type)

[Function Name] S_MICRO_WRITE	
Synopsis	Data writing to specified address trigger processing
Header	r_cg_macrodriver.h
Declaration	void S_MICRO_WRITE(uint8_t address8,uint16_t write_data)
Explanation	Triggers data writing to specified address by sending WRITE command to serial EEPROM. (Confirming completion of writing is another processing.)
Arguments	uint8_t address8 : An address in which data to be read is stored uint16_t write_data : Data to be written
Return value	None

[Function Name] S_COMUNICATION	
Synopsis	Access to serial EEPROM processing
Header	r_cg_macrodriver.h
Declaration	void S_COMUNICATION(void)
Explanation	Sends commands or data to serial EEPROM on conditions as required by tx_bufA, tx_numA, rx_bufA. Returns after completion of communications.
Arguments	None
Return value	None

[Function Name] S_CHKEND	
Synopsis	Erasing/writing to serial EEPROM state confirmation processing
Header	r_cg_macrodriver.h
Declaration	uint8_t S_CHKEND(void)
Explanation	Returns actual processing state after erasing or writing.
Arguments	None
Return value	State of EEPROM (uint8_t type) 0x00: Completion (EEPROM is in Ready state.) 0xFF: In processing (EEPROM is in Busy state.)

[Function Name] S_WAITTSV	
Synopsis	Waiting processing
Header	−
Declaration	void S_WAITTSV(void)
Explanation	Waits after executing of seven NOP commands.
Arguments	None
Return value	None

[Function Name] R_CSI00_Start	
Synopsis	CSI00 timer operation enabled processing
Header	r_cg_macrodriver.h
Declaration	void R_CSI00_Start(void)
Explanation	Makes CSI00 timer operation enabled state.
Arguments	None
Return value	None

[Function Name] R_CSI00_Send_Receive	
Synopsis	CSI00 starting communication processing
Header	r_cg_macrodriver.h
Declaration	MD_STATUS R_CSI00_Send_Receive(uint8_t * const tx_buf, uint8_t tx_num, uint8_t * const rx_buf)
Explanation	Starts transmission processing of CS100 on conditions as required by tx_buf, tx_num, rx_buf, and send the first data. Sets a transmissions state flag.
Arguments	uint8_t* const tx_buf : Transmission data pointer uint8_t tx_num : Number of transmission data uint8_t* const rx_buf : Pointer for storing receive data
Return value	MD_STATUS value: Normal / abnormal judging of an argument

[Function Name] r_csi00_interrupt	
Synopsis	CSI00 transfer end interrupt processing
Header	−
Declaration	__interrupt static void r_csi00_interrupt(void)
Explanation	Transfer end interrupt (INTCSI00) activates it. Stores receive data into a buffer in which received data is stored, and starts transmission processing of the next data. Clears the transmission state flag at the final data receiving.
Arguments	None
Return value	None

5.7 Flowcharts

Figure 5.3 shows the overall flow of the sample program described in this application note.

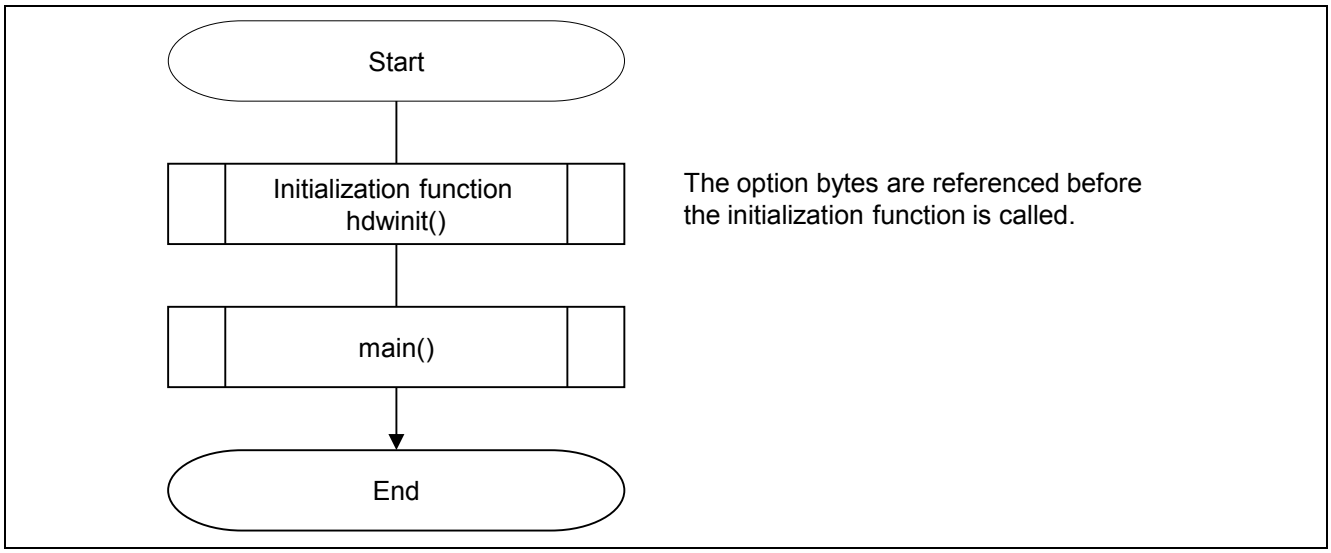


Figure 5.3 Overall Flow

5.7.1 Initialization Function

Figure 5.4 shows the flowchart for the initialization function.

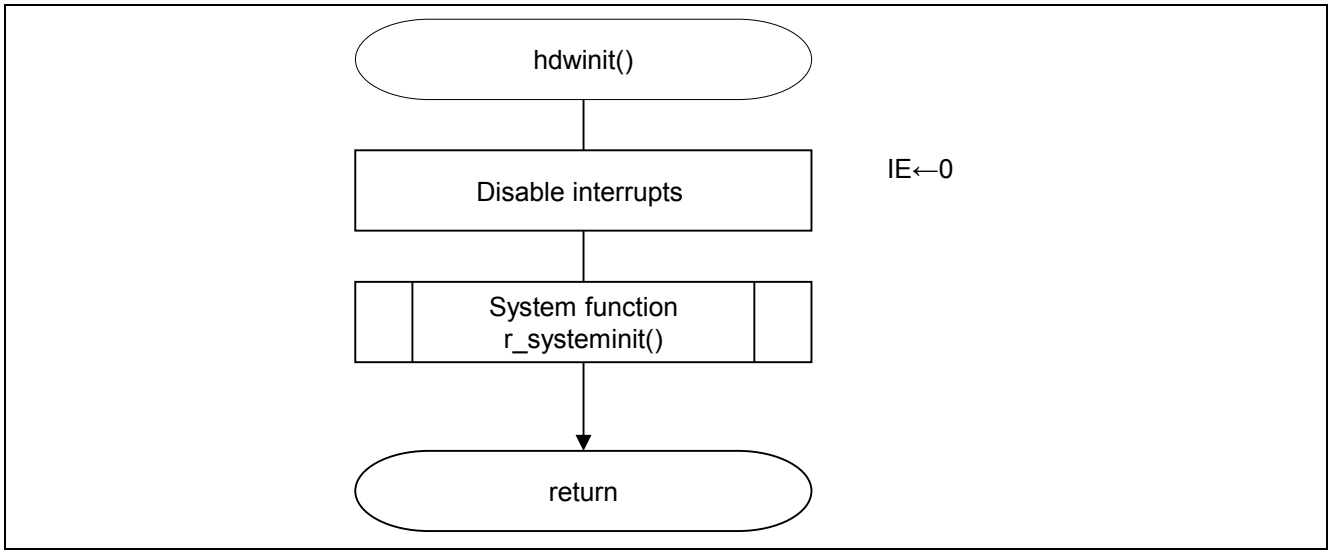


Figure 5.4 Initialization Function

5.7.2 System Function

Figure 5.5 shows the flowchart for the system function.

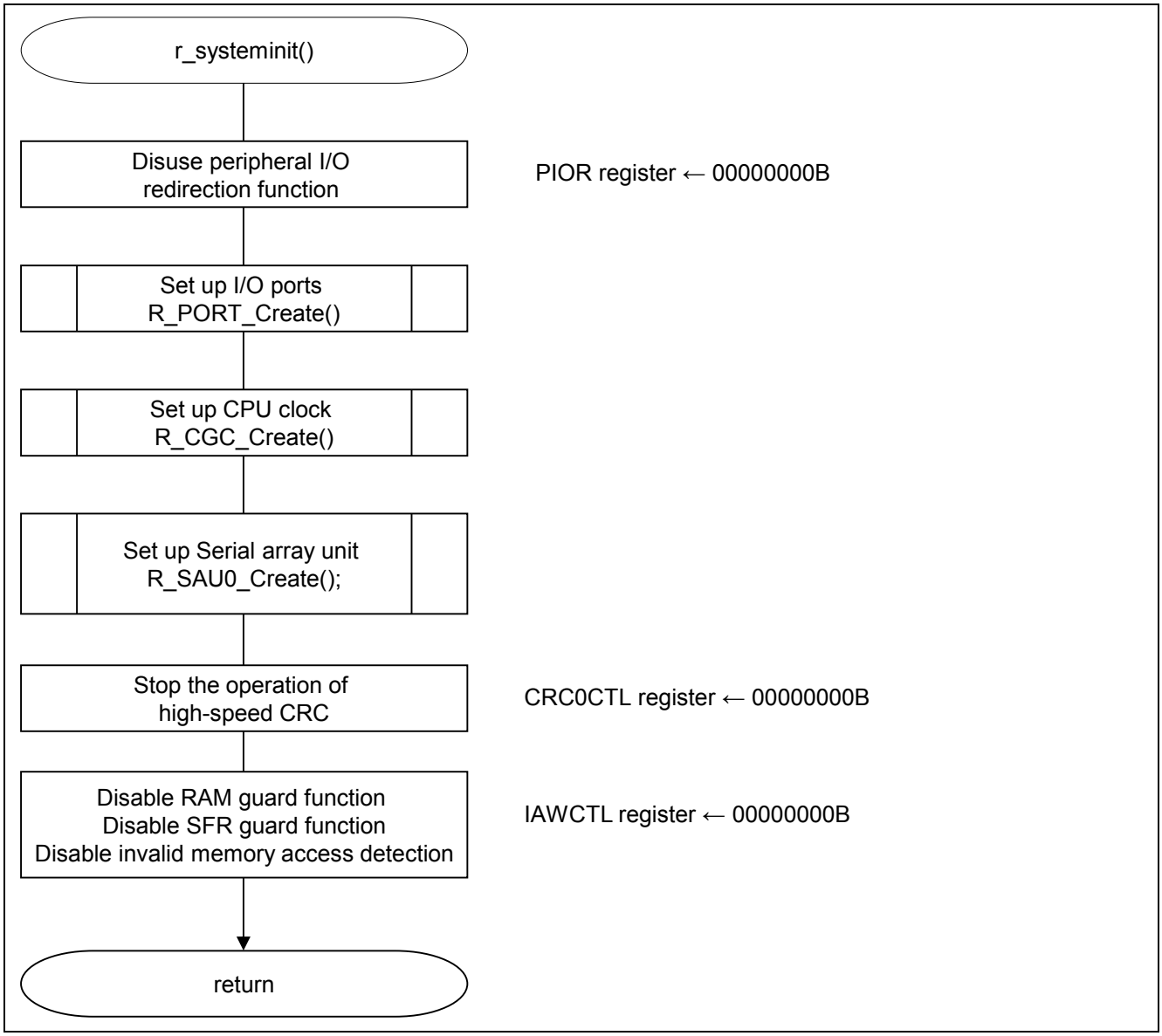


Figure 5.5 System Function

5.7.3 I/O Port Setup

Figure 5.6 shows the flowchart for I/O port setup.

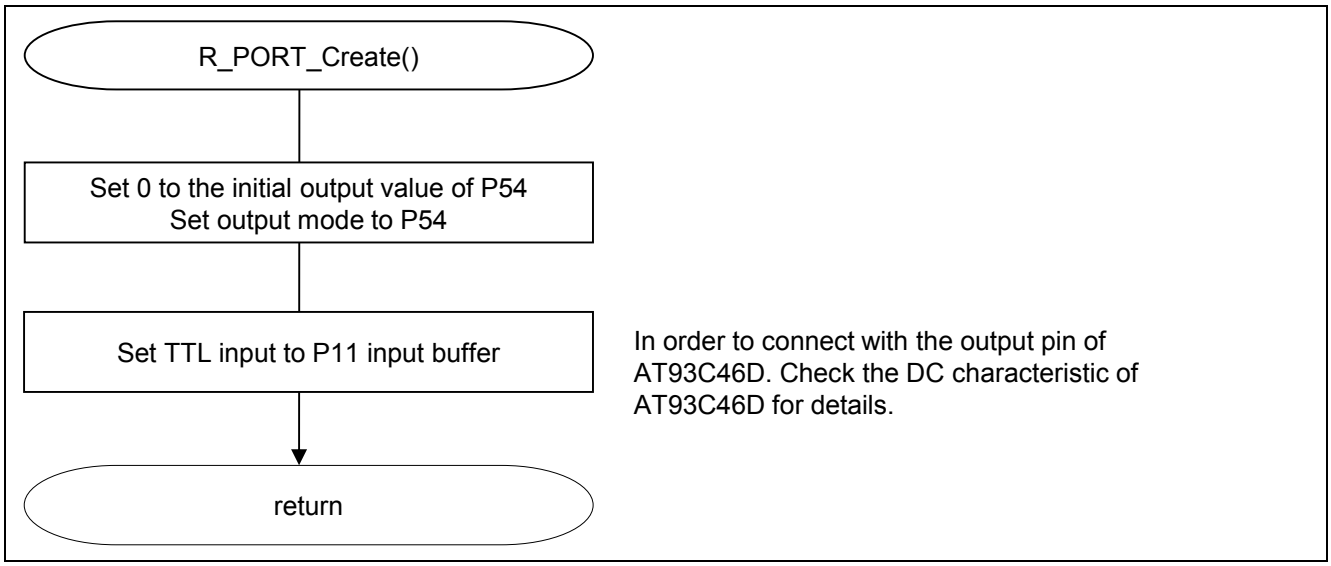


Figure 5.6 I/O Port Setup

Note: Refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN0451E) for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

Setup of ports for chip select signal output.

- Port register 5 (P5)
- Port mode register 5 (PM5)
  Select an I/O mode and output latch for each port.

Symbol: P5

7	6	5	4	3	2	1	0
P57	P56	P55	P54	P53	P52	P51	P50
x	x	x	**0**	x	x	x	x

Bit 4

P54	Output data control (in output mode)	Input data read (in input mode)
0	**Output 0**	**Input low level**
1	Output 1	Input high level

Symbol: PM5

7	6	5	4	3	2	1	0
PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50
x	x	x	**0**	X	x	x	x

Bit 4

PM54	P54 I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Input mode setup of serial data input pin.

- Port input mode register 1 (PIM1)
- Selects input buffer type of port.

Symbol: PIM1

7	6	5	4	3	2	1	0
PIM17	PIM16	PIM15	PIM14	PIM13	PIM12	PIM11	PIM10
x	x	x	x	x	0	**1**	x

Bit 1

PIM11	P11 pin input buffer selection
0	Normal input buffer
1	**TTL Input buffer**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware

5.7.4 CPU Clock Setup

Figure 5.7 shows the flowchart for setting up the CPU clock.

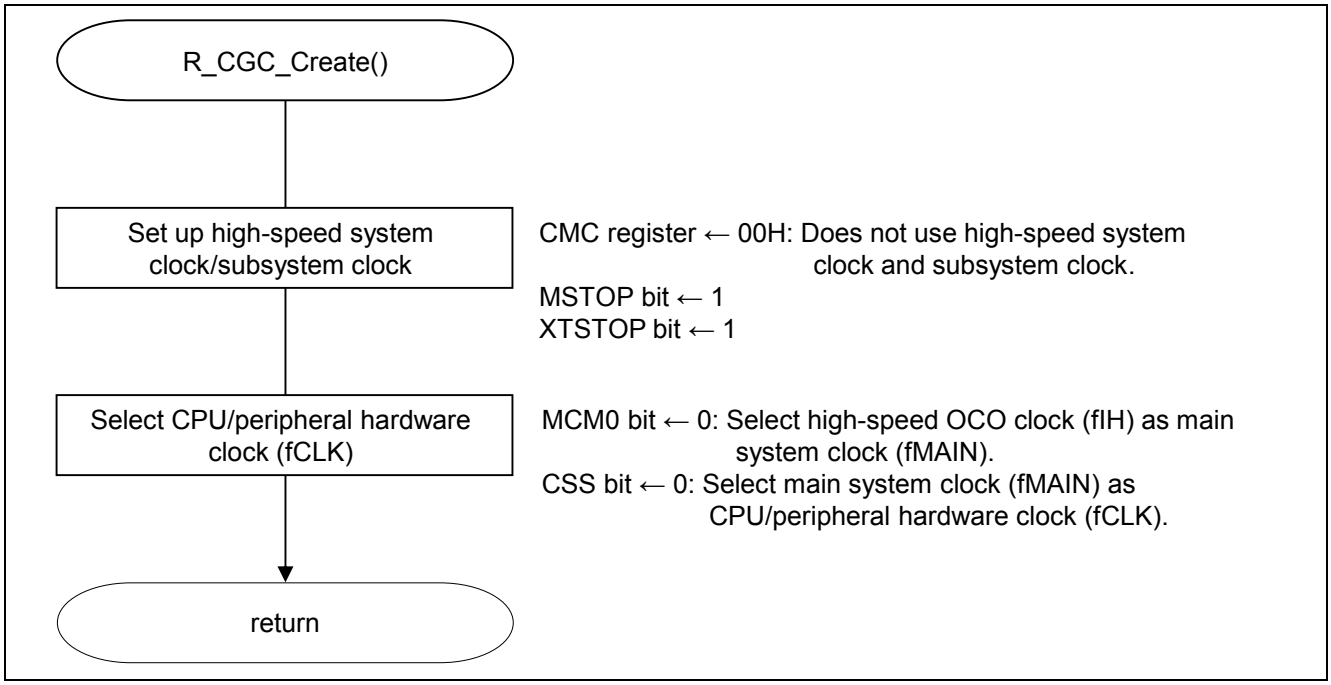


Figure 5.7 CPU Clock Setup

Caution: For details on the procedure for setting up the CPU clock (R_CGC_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN0451E).

5.7.5 SAU0 Setup

Figure 5.8 shows the flowchart for SAU0 setup.

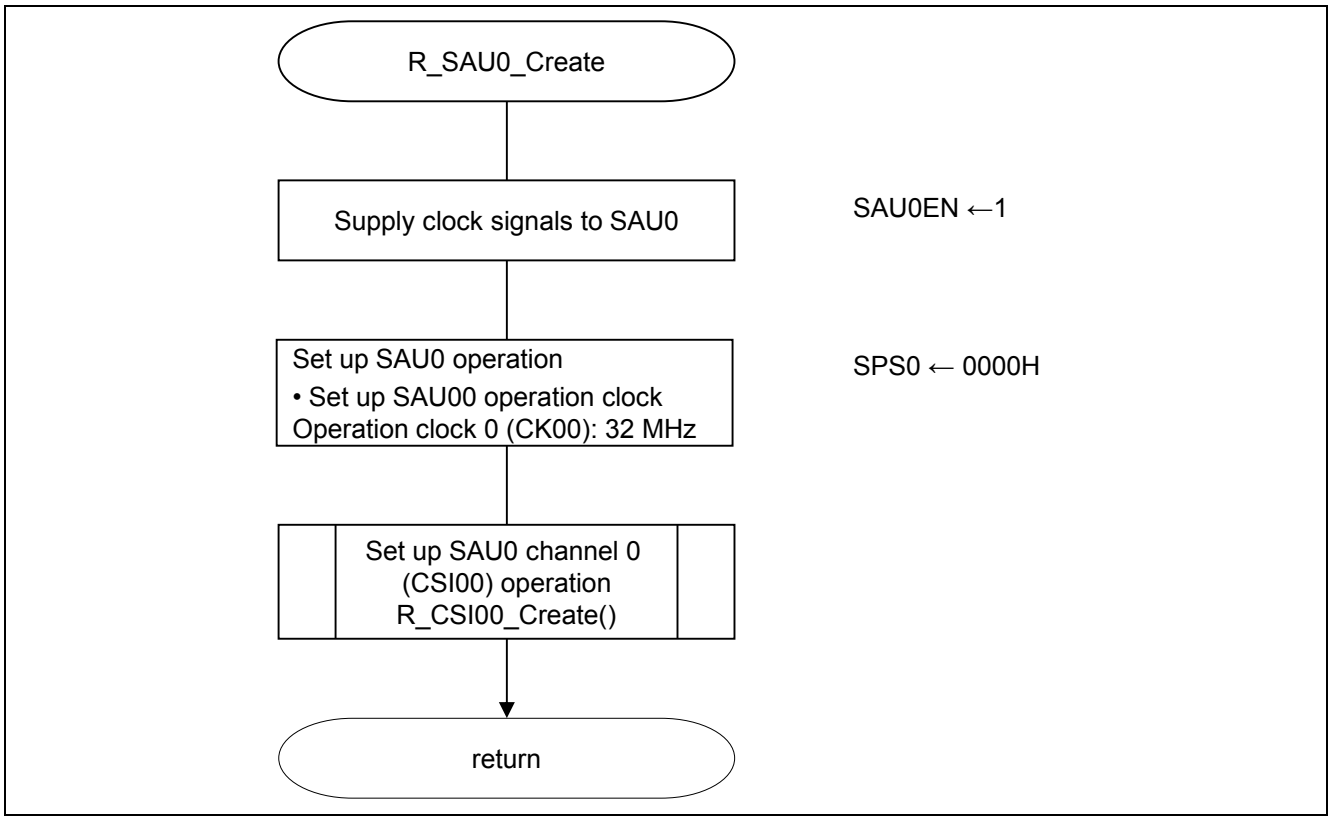


Figure 5.8 SAU0 Setup

Enabling supply of clock signals to the SAU0.

- Peripheral enable register 0 (PER0)
  Enable supply of clock signals to SAU0.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
x	x	x	x	x	**1**	x	x

Bit 2

SAU0EN	Control of serial array unit 0 and input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Selecting a serial clock.

- Serial clock select register 0 (SPS0)
  Select an operation clock for SAU0.

Symbol: SPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
0	0	0	0	0	0	0	0	x	x	x	x	**0**	**0**	**0**	**0**

Bit 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000	Selection of operation clock (CK00)					
					f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz	**f_{CLK} = 32 MHz**
0	**0**	**0**	**0**	**f_{CLK}**	2 MHz	5 MHz	10 MHz	20 MHz	**32 MHz**
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	16 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1,25 MHz	2.5 MHz	5 MHz	8 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	4 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	313 kHz	625 kHz	1.25 MHz	2 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156 kHz	313 kHz	625 kHz	1 MHz
0	1	1	0	$f_{CLK}/2^6$	31.3 kHz	78.1 kHz	156 kHz	313 kHz	500 kHz
0	1	1	1	$f_{CLK}/2^7$	15.6 kHz	39.1 kHz	78.1 kHz	156 kHz	250 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	125 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.77 kHz	19.5 kHz	39.1 kHz	62.5 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.77 kHz	19.5 kHz	31.3 kHz
1	0	1	1	$f_{CLK}/2^{11}$	977 Hz	2.44 kHz	4.88 kHz	9.77 kHz	15.6 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	7.81 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	3.91 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.95 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61Hz	153Hz	305 Hz	610 Hz	977 Hz

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.6 SAU0 Channel 0 (CSI00) Operation Setup

Figure 5.9 shows the flowchart for setting up SAU0 channel 0 (CSI00) operation.

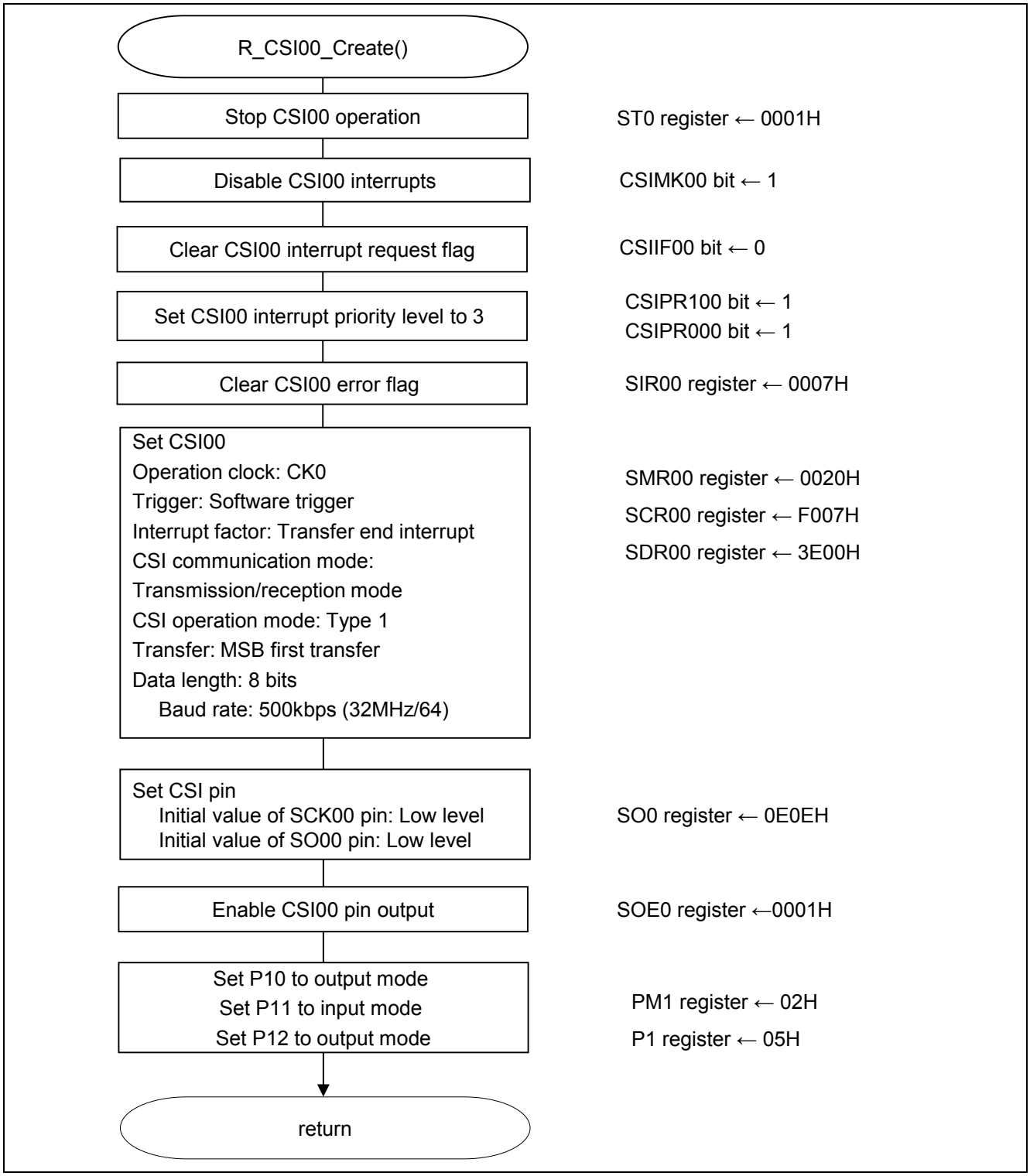


Figure 5.9 SAU0 Channel 0 (CSI00) Operation Setup

Setting up the SAU0 channel 0 operation mode.

- Serial communication operation setting register 00 (SCR00)
  Select an operation clock (f_{MCK}).
  Specify whether to make the serial clock (f_{SCK}) input available.
  Set up the start trigger and operation mode.
  Select an interrupt source.

Symbol: SMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS00	CCS00	0	0	0	0	0	STS00	0	SIS000	1	0	0	MD002	MD001	MD000
0	**0**	0	0	0	0	0	**0**	0	0	1	0	0	**0**	**0**	**0**

Bit 15

CKS00	Selection of operation clock (f_{MCK}) of channel 0
0	**Operation clock CK00 set by the SPS0 register**
1	Operation clock CK01 set by the SPS0 register

Bit 14

CCS00	Selection of transfer clock (f_{TCLK}) of channel 0
0	**Divided operation clock f_{MCK} specified by the CKS00 bit**
1	Clock input f_{SCK} from the SCK00 pin (slave transfer in CSI mode)

Bit 8

STS00	Selection of start trigger source
0	**Only software trigger is valid**
1	Valid edge of the RxDq pin (selected for UART reception)

Bit 2 and 1

MD002	MD001	Setting of operation mode of channel 0
0	**0**	**CSI mode**
0	1	UART mode
1	0	Simplified I2C mode
1	1	Setting prohibited

Bit 0

MD000	Selection of interrupt source of channel 0
0	**Transfer end interrupt**
1	Buffer empty interrupt

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the SAU0 channel 0 operation mode.

- Serial communication operation setting register 00 (SCR00)
  Selection of data transmission/reception mode.
  Phase of data and clock.
  First bit
  Data length

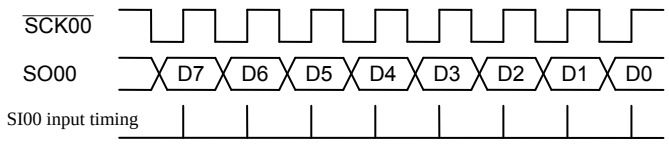
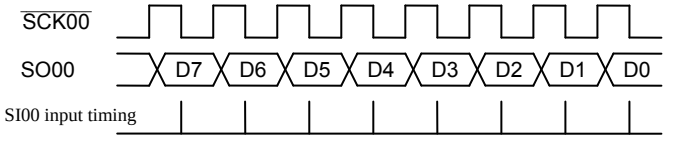
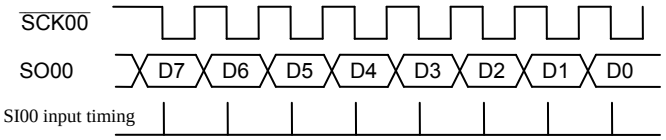
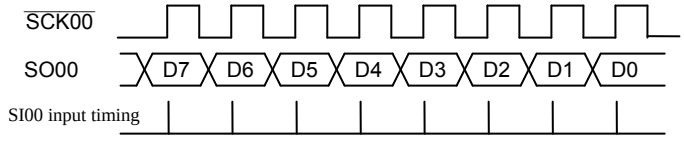
Symbol: SCR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXE 00	RXE 00	DAP 00	CKP 00	0	EOC 00	PTC 001	PTC 000	DIR 00	0	SLC 001	SLC 000	0	1	DLS 001	DLS 000
1	**1**	**1**	**1**	0	0	0	0	**0**	0	0	0	0	1	**1**	**1**

Bit 15 and 14

TXE00	RXE00	Setting of operation mode of channel 0
0	0	Disable communication
0	1	Reception only
1	0	Transmission only
1	**1**	**Transmission/reception**

Bit 13 and 12

DAP00	CKP00	Selection of data and clock phase in CSI mode	Type
0	0		1
0	1		2
1	0		3
1	**1**		**4**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: SCR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXE 00	RXE 00	DAP 00	CKP 00	0	EOC 00	PTC 001	PTC 000	DIR 00	0	SLC 001	SLC 000	0	1	DLS 001	DLS 000
1	**1**	**1**	**1**	0	0	0	0	**0**	0	0	0	0	1	**1**	**1**

Bit 7

DIR00	Selection of data transfer sequence in CSI and UART modes
0	**Inputs/outputs data with MSB first.**
1	Inputs/outputs data with LSB first.

Bit 1 and 0

DLS001	DLS000	Setting of data length in CSI and UART modes
0	0	9-bit data length (stored in bits 0 to 8 of the SDR00 register) (can be set in UART0 mode only.)
1	0	7-bit data length (stored in bits 0 to 6 of the SDR00 register)
1	**1**	**8-bit data length (stored in bits 0 to 7 of the SDR00 register)**
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Selecting an operation clock frequency divisor.

- Serial data register 00 (SDR00)
  Set the division ratio of the operation clock (f_{MCK}) frequency.

Symbol: SDR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits 15 to 9

SDR00[15:9]							Transfer clock setting by dividing the operation clock (f_{MCK})
0	0	0	0	0	0	0	$f_{MCK}/2$
0	0	0	0	0	0	1	$f_{MCK}/4$
0	0	0	0	0	1	0	$f_{MCK}/6$
0	0	0	0	0	1	1	$f_{MCK}/8$
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
0	**0**	**1**	**1**	**1**	**1**	**1**	**$f_{MCK}/64$**
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	1	1	1	0	$f_{MCK}/254$
1	1	1	1	1	1	1	$f_{MCK}/256$

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Specifying the output values for the SCK00 and SO00 pins.

- Serial output register 0 (SO0)
  Specify the output values for the serial data output pin and serial clock output pin.

Symbol: SO0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	CKO 03	CKO 02	CKO 01	CKO 00	0	0	0	0	SO 03	SO 02	SO 01	SO 00
0	0	0	0	x	x	x	**0**	0	0	0	0	x	x	x	**0**

Bit 8

CKO00	Serial clock output of channel 0
0	Serial clock output value is “0”.
1	Serial clock output value is “1”.

Bit 0

SO00	Serial data output of channel 0
0	**Serial clock output value is “0”.**
1	Serial clock output value is “1”.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Enabling output of serial communication operation.

- Serial output enable register 0 (SOE0)
  Enable output of serial communication operation.

Symbol: SOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	SOE 03	SOE 02	SOE 01	SOE 00
0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	**1**

Bit 0

SOE00	Serial output enable/stop of channel 0
0	Stops output by serial communication operation.
1	**Enables output by serial communication operation.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the ports of the SCK00, SO00 and SI00 pins.

- Port register 1 (P1)
- Port mode register 1 (PM1)
  Select an input/output mode and output latch for each port.

Symbol: P1

7	6	5	4	3	2	1	0
P17	P16	P15	P14	P13	P12	P11	P10
x	x	x	x	x	**1**	x	**1**

Bit 2

P12	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	**Output 1**	**Input high level**

Bit 0

P10	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	**Output 1**	**Input high level**

Symbol: PM1

7	6	5	4	3	2	1	0
PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10
x	x	x	x	x	**0**	**1**	**0**

Bit 2

PM12	P12 pin I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Bit 1

PM11	P11 pin I/O mode selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

Bit 0

PM10	P10 pin I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Note: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.7 Main Function

Figure 5.10 and Figure 5.11 show the flowchart for main function.

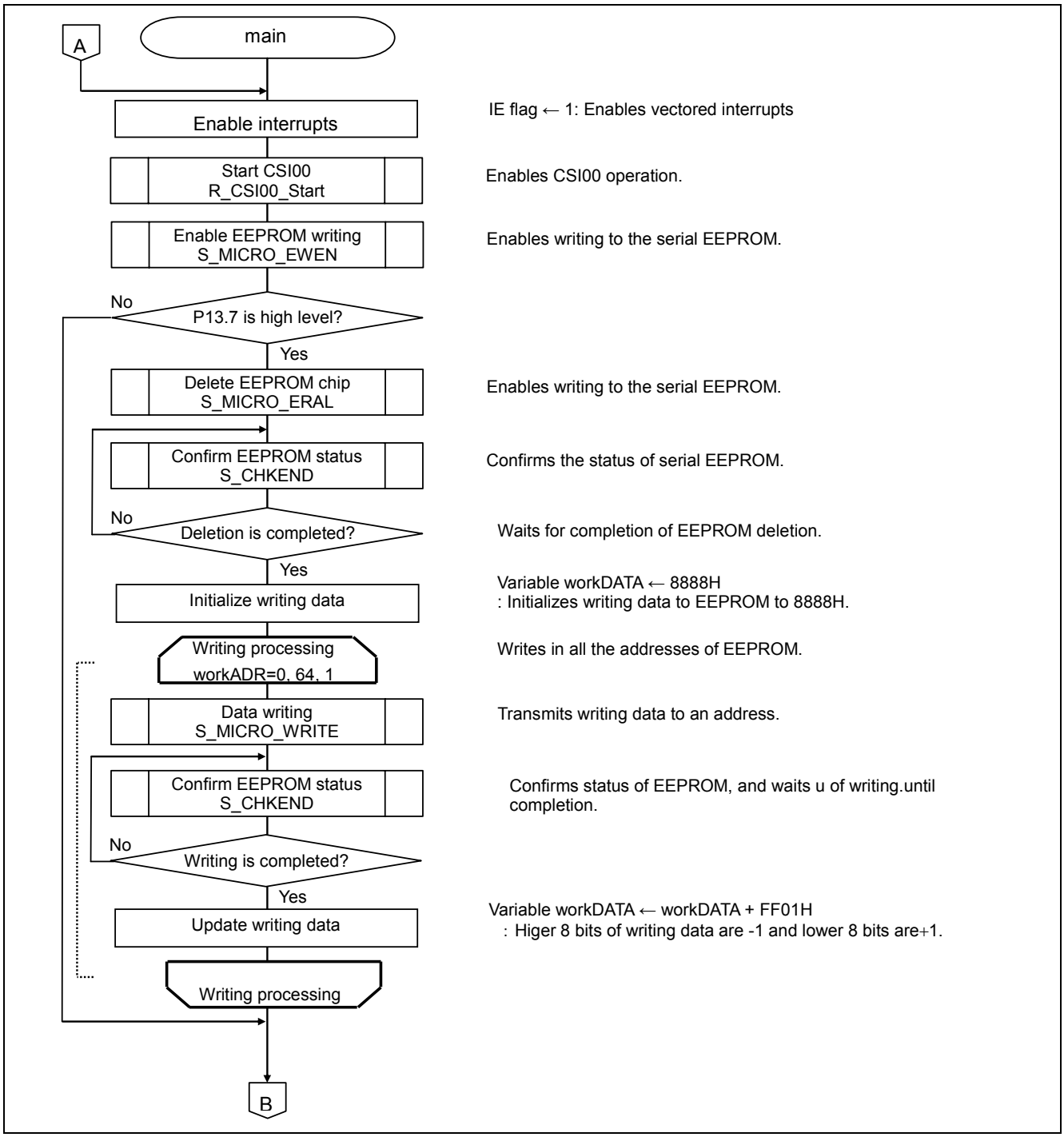
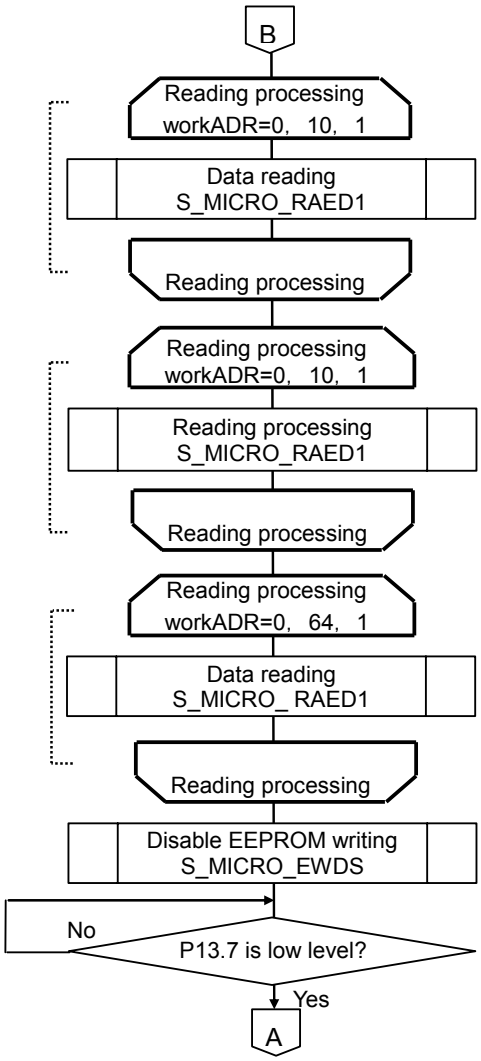


Figure 5.10 Main Function (1/2)



In order to check stability of operation, reads the address 0's contents 10 times.

In order to check stability of operation, reads the address 1's contents 10 times.

Reads all the data of serial EEPROM.

Variable DTCDATA ← EEPROM reading data

Disables writing to EEPROM.

Waites to set P13.7 to a low level.

Figure 5.11 Main Function (2/2)

5.7.8 Setting CSI00 to the Communication Standby Status

Figure 5.12 shows the flowchart for processing offsetting CSI00 to the communication wait status.

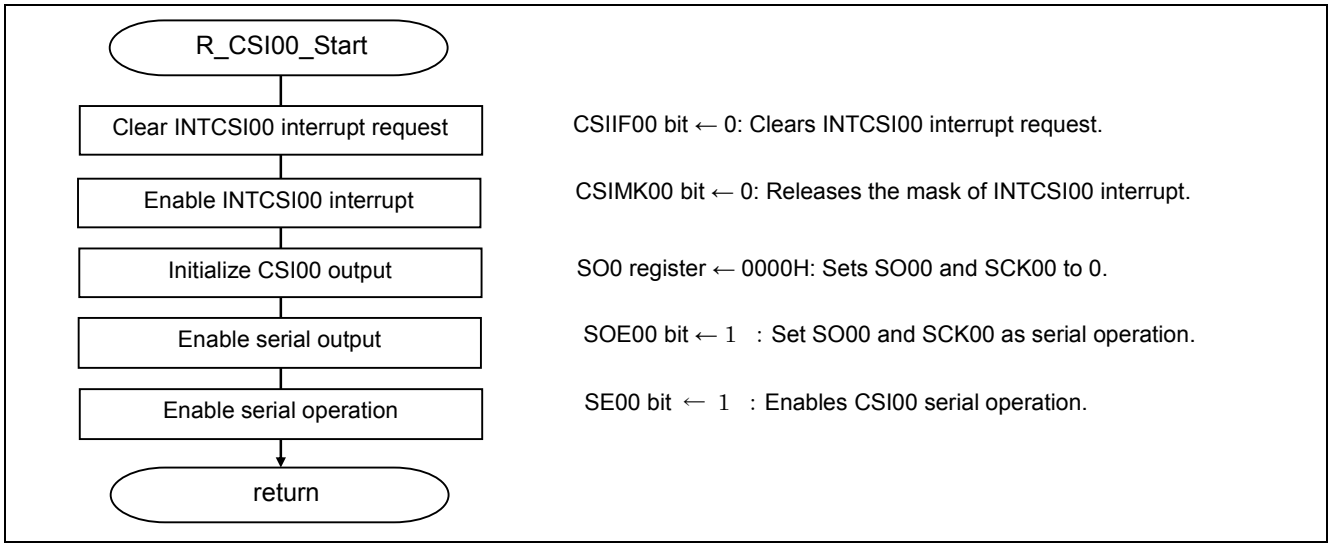


Figure 5.12 Setting CSI00 to the Communication Standby Status

Setting the interrupt request flag.

- Interrupt request flag register 0H (IF0H)

  Clear the interrupt request flag.

Symbol: IF0H

7	6	5	4	3	2	1	0
SREIF0 TMIF01H	SRIF0 CSIIF01 IICIF01	STIF0 CSIIF00 IICIF00	DMAIF1	DMAIF0	SREIF2	SRIF2 CSIIF21 IICIF21	STIF2 CSIIF20 IICIF20
x	x	**0**	x	x	x	x	x

CSIIF00	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Setting the interrupt mask

- Interrupt mask flag register 0H (MK0H)
  Enable interrupt processing.

Symbol: MK0H

7	6	5	4	3	2	1	0
SREMK0 TMMK01H	SRMK0 CSIMK01 IICMK01	STMK0 CSIMK00 IICMK00	DMAMK1	DMAMK0	SREMK2	SRMK2 CSIMK21 IICMK21	STMK2 CSIMK20 IICMK20
x	x	**0**	x	x	x	x	x

CSIMK00	Interrupt processing control
0	**Enables interrupt processing.**
1	Disables interrupt processing

Setting the initial output level.

- Serial output register m (SOm)

Symbol: SOm

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	CKO m3	CKO m2	CKO m1	CKO m0	0	0	0	0	SO m3	SO m2	SO m1	SO m0
0	0	0	0	**0/1**	**0/1**	**0/1**	**0**	0	0	0	0	**0/1**	**0/1**	**0/1**	**0**

Bit 0, 8

SOmn	Serial data output of channel n
0	**Serial data output value is “0**
1	Serial data output value is “1

Enabling data output of the targeted channel.

- Serial output enabling register 0 (SOE0)
  Enables output.

  Symbol: SOEm

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	SOE m3	SOE m2	SOE m1	SOE m0
0	0	0	0	0	0	0	0	0	0	0	0	**0/1**	**0/1**	**0/1**	**1**

  Bit 0

SOE mn	Serial output enable/stop of channel n
0	Stops output by serial communication operation.
1	Enables output by serial communication operation.

Enters the communication wait status.

- Serial channel start register m (SSm)

  Starts the operation.

  Symbol: SSm

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	SSm3	SSm2	SSm1	SSm0
0	0	0	0	0	0	0	0	0	0	0	0	**0/1**	**0/1**	**0/1**	**1**

  Bit 0

SSm0	Operation start trigger of channel n
0	No trigger operation
1	Sets the SEmn bit to 1 and enters the communication wait status.

5.7.9 To Make EEPROM Write-Enable State

Figure 5.13 shows the flowchart for processing to enable writing to EEPROM.

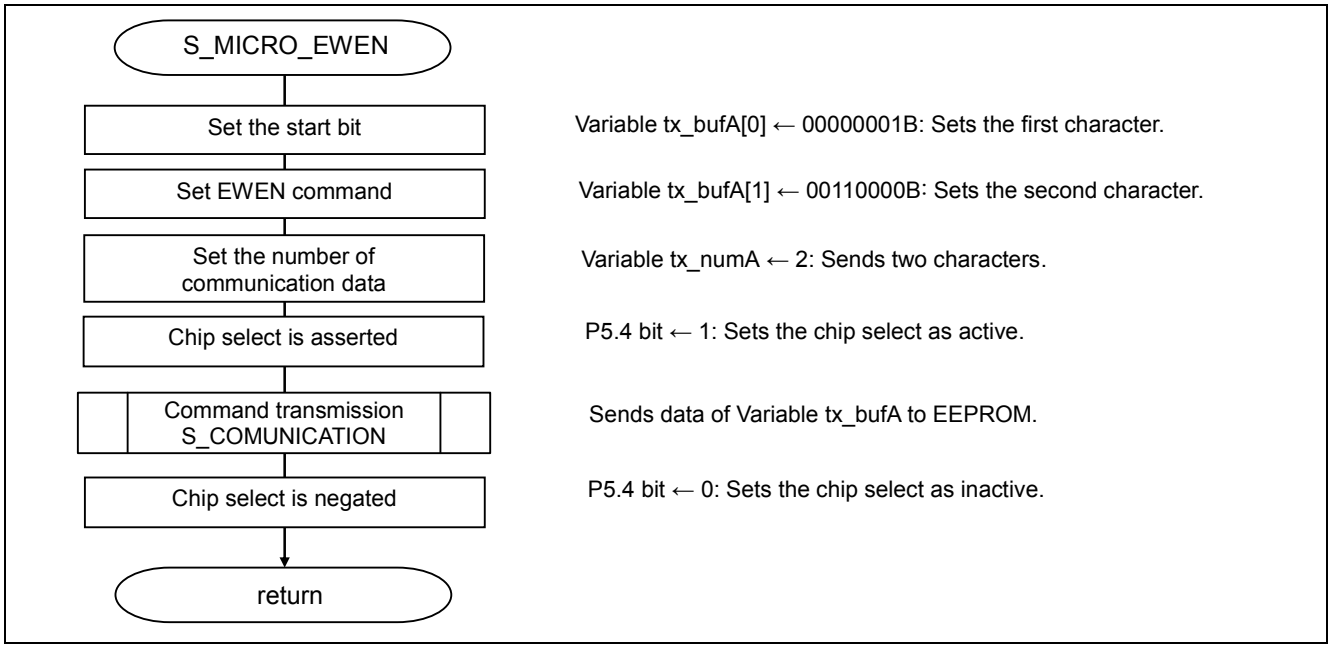


Figure 5.13 To Make EEPROM Write-Enable State

5.7.10 Deletion of Whole EEPROM Chip

Figure 5.14 shows the flowchart for processing to delete the whole chip of EEPROM.

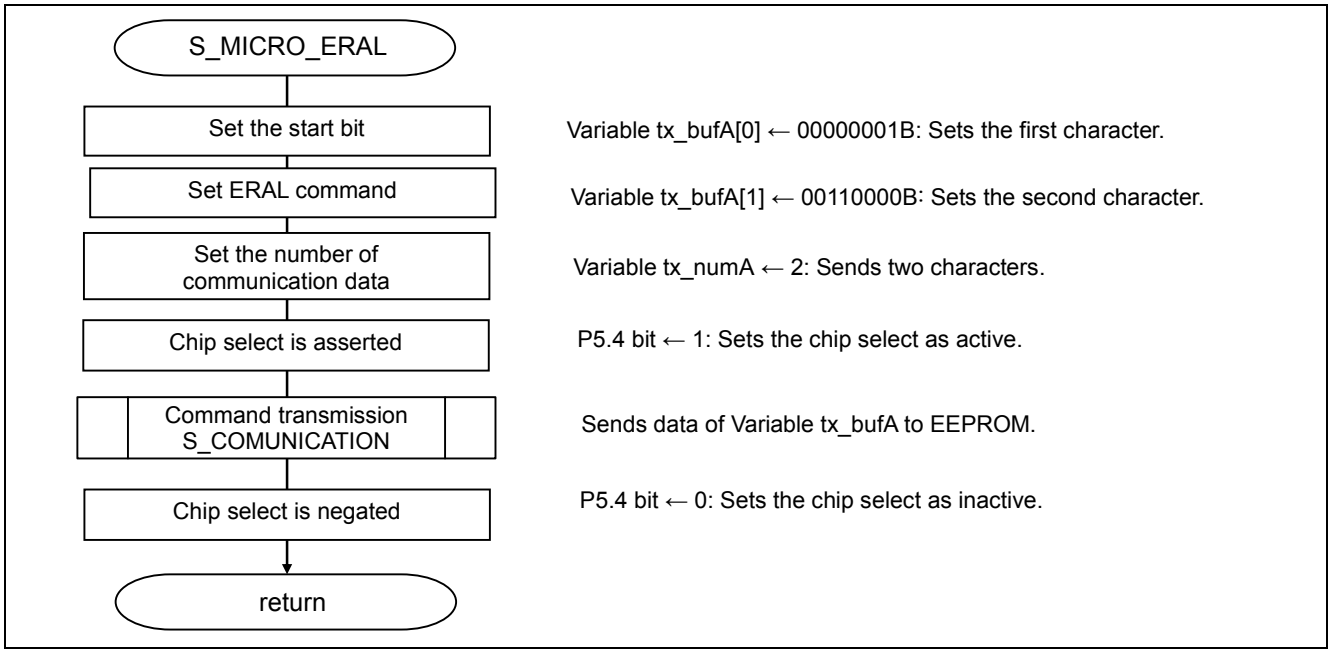


Figure 5.14 Deletion of Whole EEPROM Chip

5.7.11 Writing/deletion state (Ready or Busy) check processing of EEPROM

Figure 5.15 shows the flowchart for processing to check writing/deletion state (ready or busy) of EEPROM.

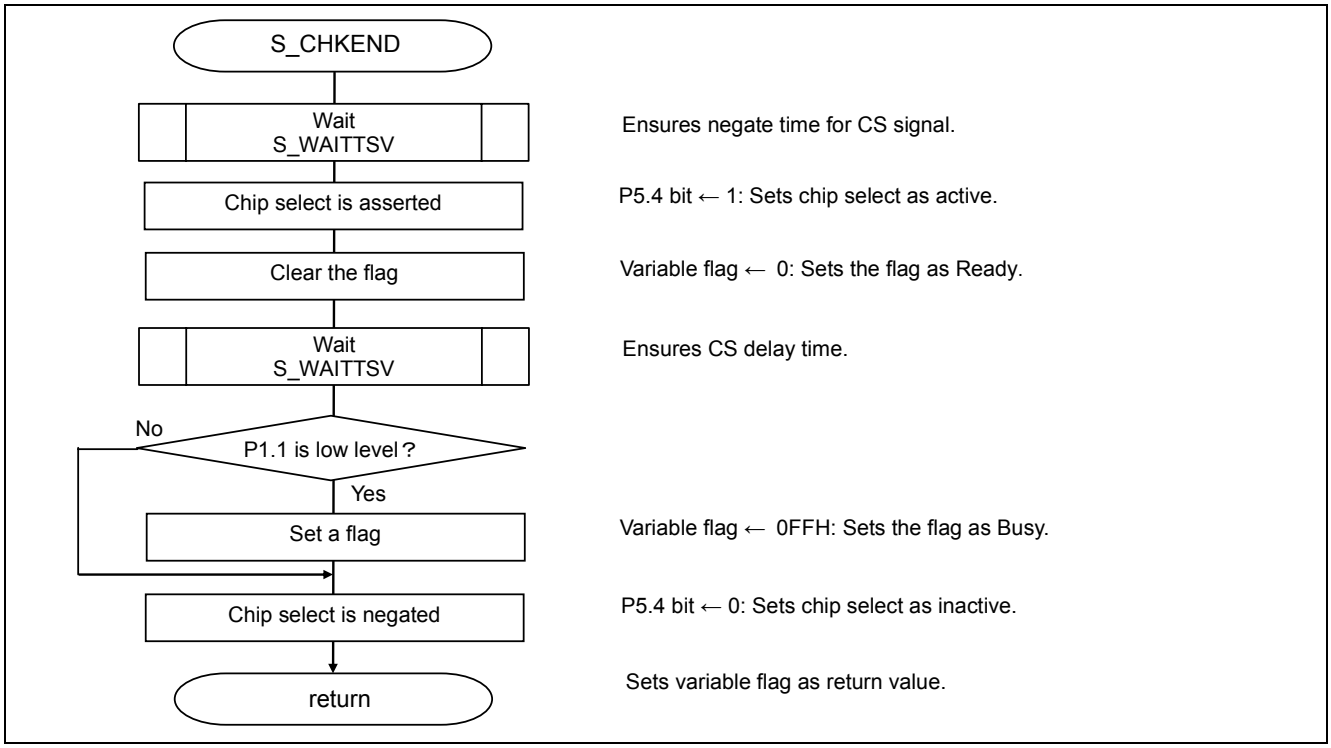


Figure 5.15 Writing/deletion state (Ready or Busy) check processing of EEPROM

5.7.12 Writing Data to Specified Address of EEPROM

Figure 5.16 shows the flowchart for processing to write data to specified address of EEPROM.

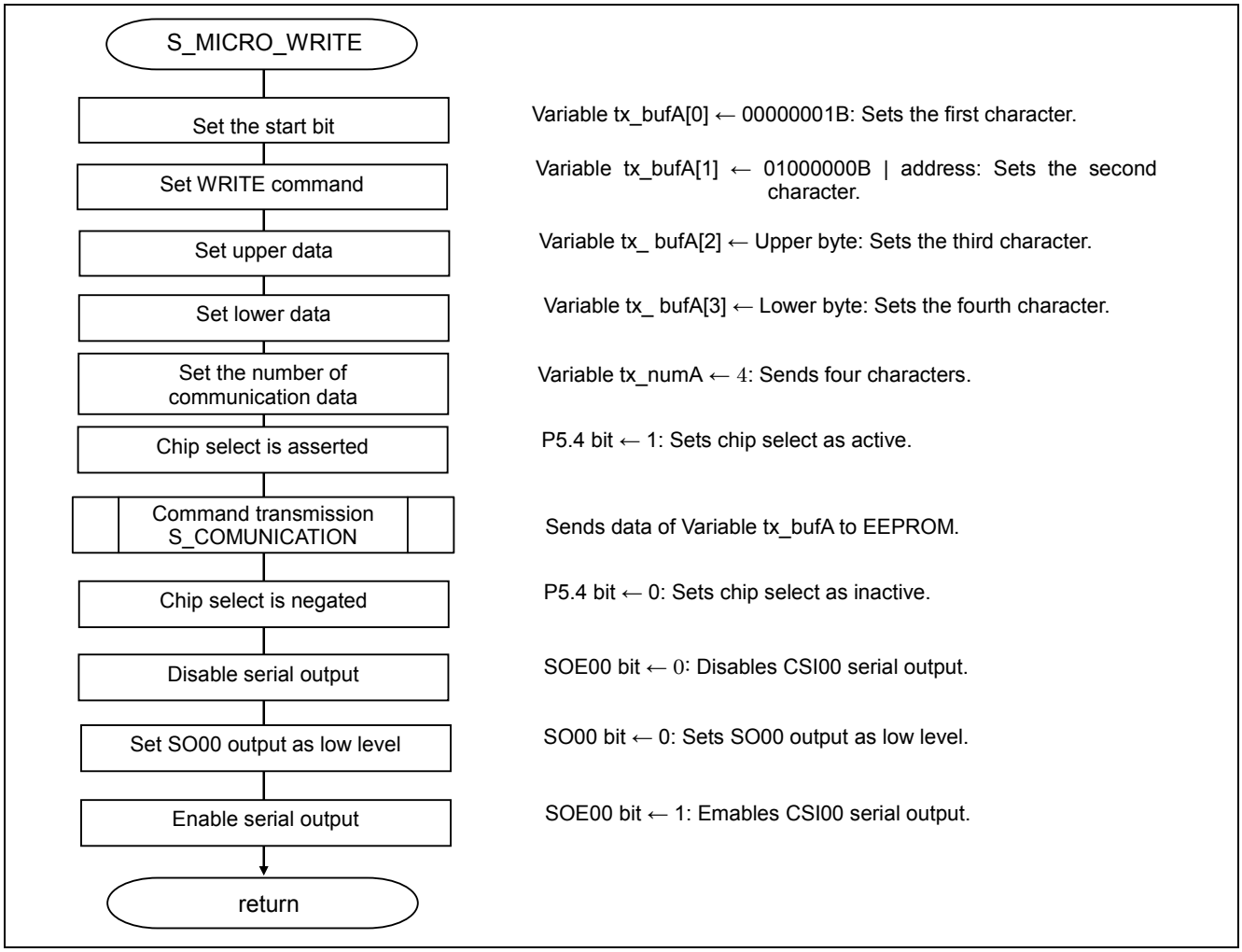


Figure 5.16 Writing Data to Specified Address of EEPROM

5.7.13 Reading Data from Specified Address of EEPROM

Figure 5.17 shows the flowchart for processing to read data from specified address of EEPROM.

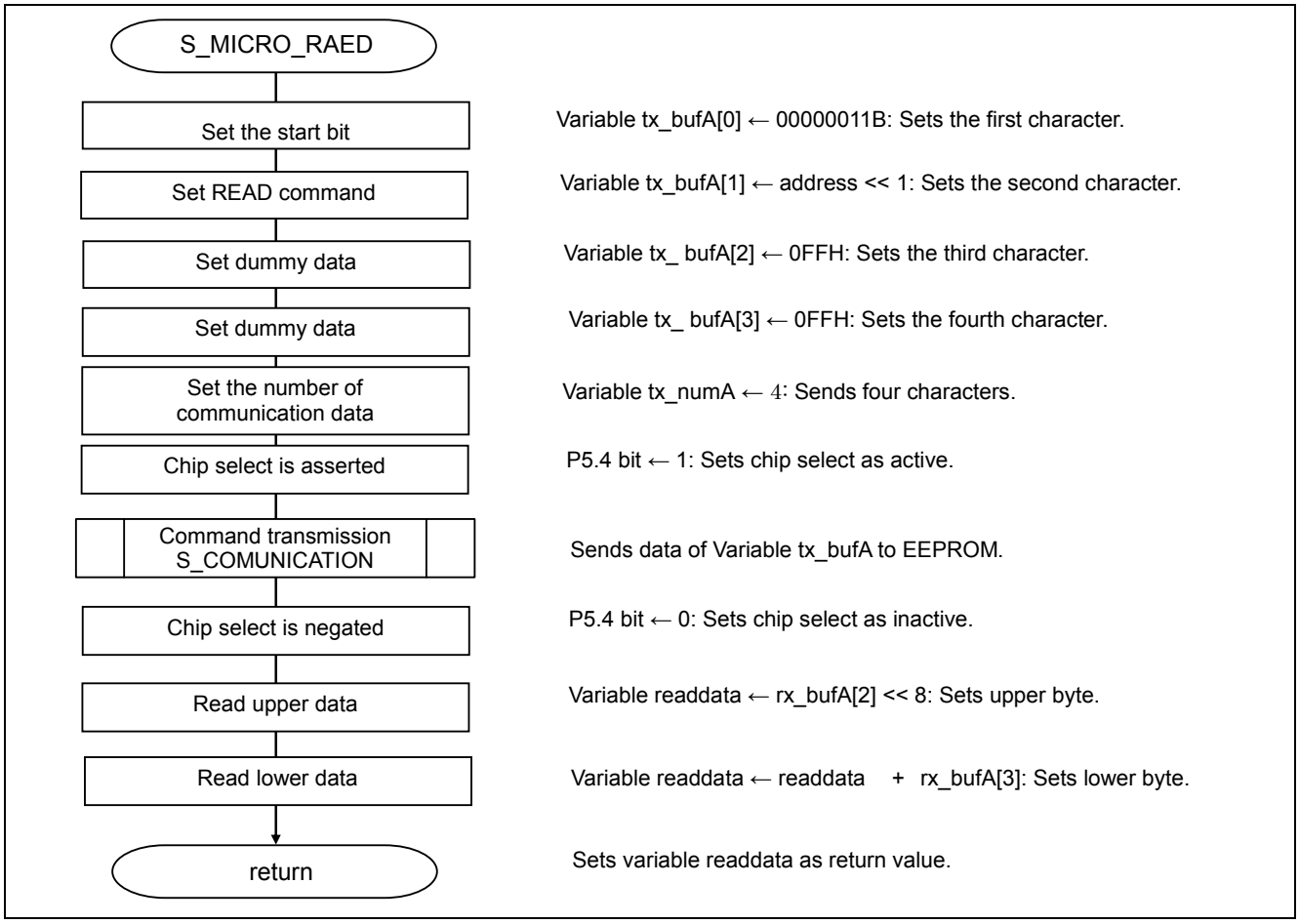


Figure 5.17 Reading Data from Specified Address of EEPROM

5.7.14 To Make EEPROM Write-Disable State

Figure 5.18 shows the flowchart for processing to disable writing to EEPROM.

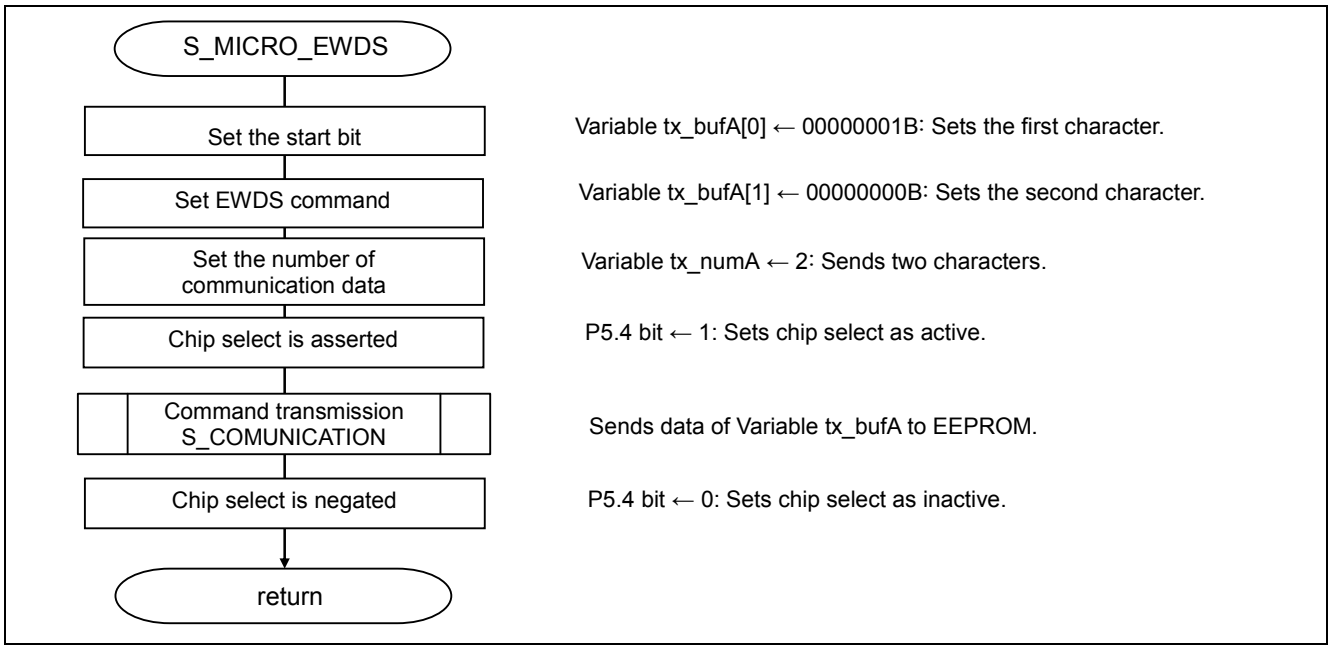


Figure 5.18 To Make EEPROM Write-Disable State

5.7.15 Function Including from Starting Access to Completion to EEPROM

Figure 5.19 shows the flowchart of the function including from starting access to completion to EEPROM.

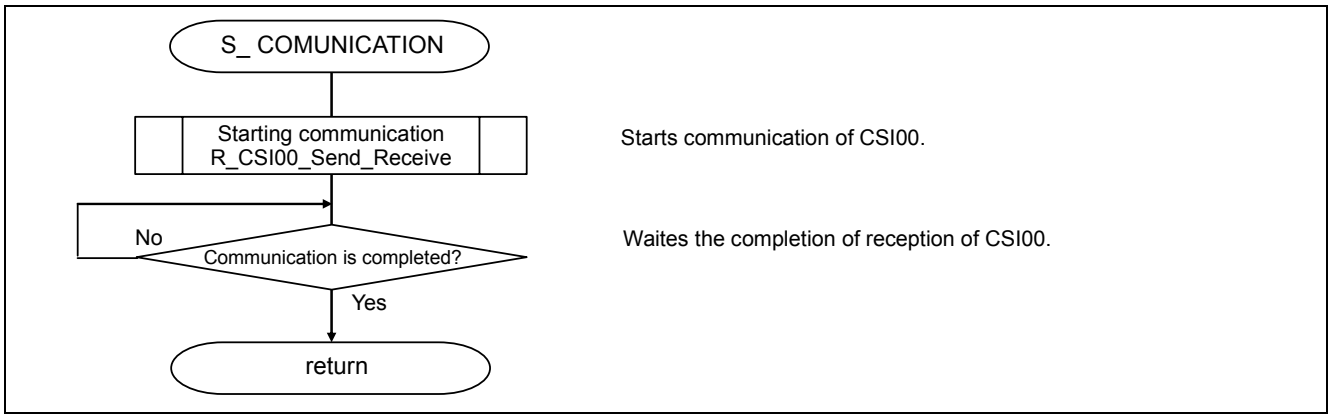


Figure 5.19 Function Including from Starting Access to Completion to EEPROM

5.7.16 Waiting Processing

Figure 5.20 shows the flowchart for processing of waiting processing.

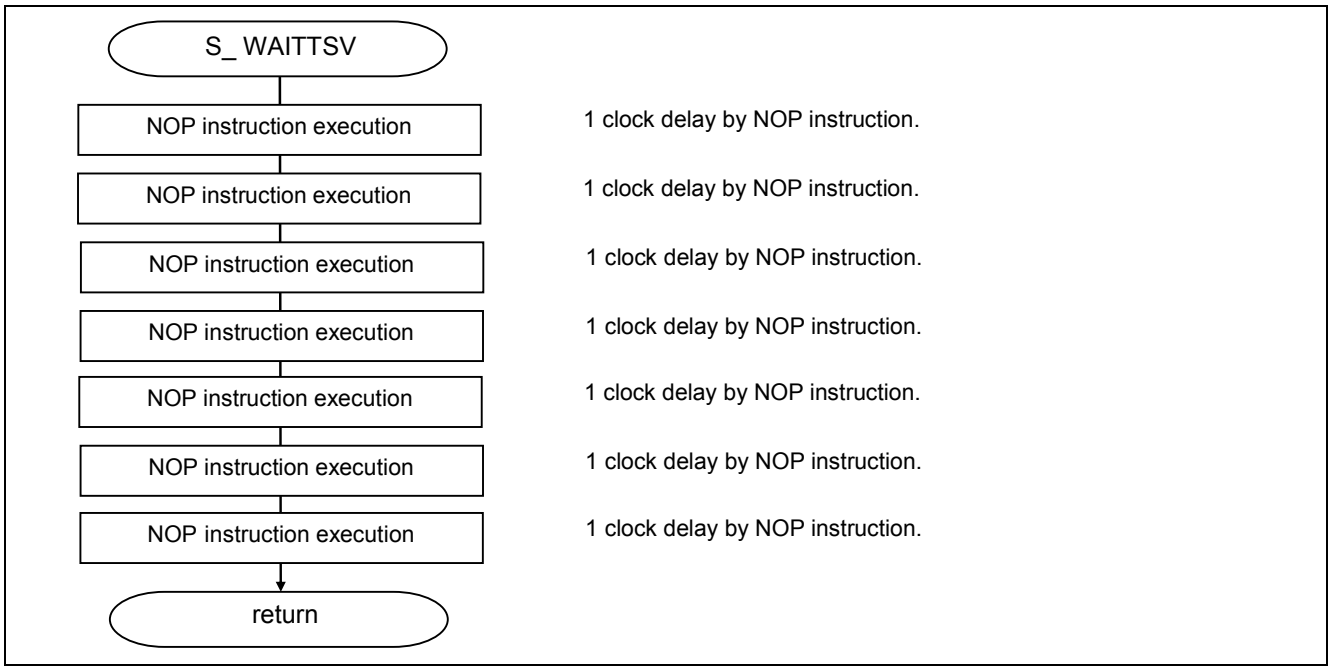


Figure 5.20 Waiting Processing

5.7.17 Starting Communication of CSI00

Figure 5.21 shows the flowchart for processing of Starting communication of CSI00.

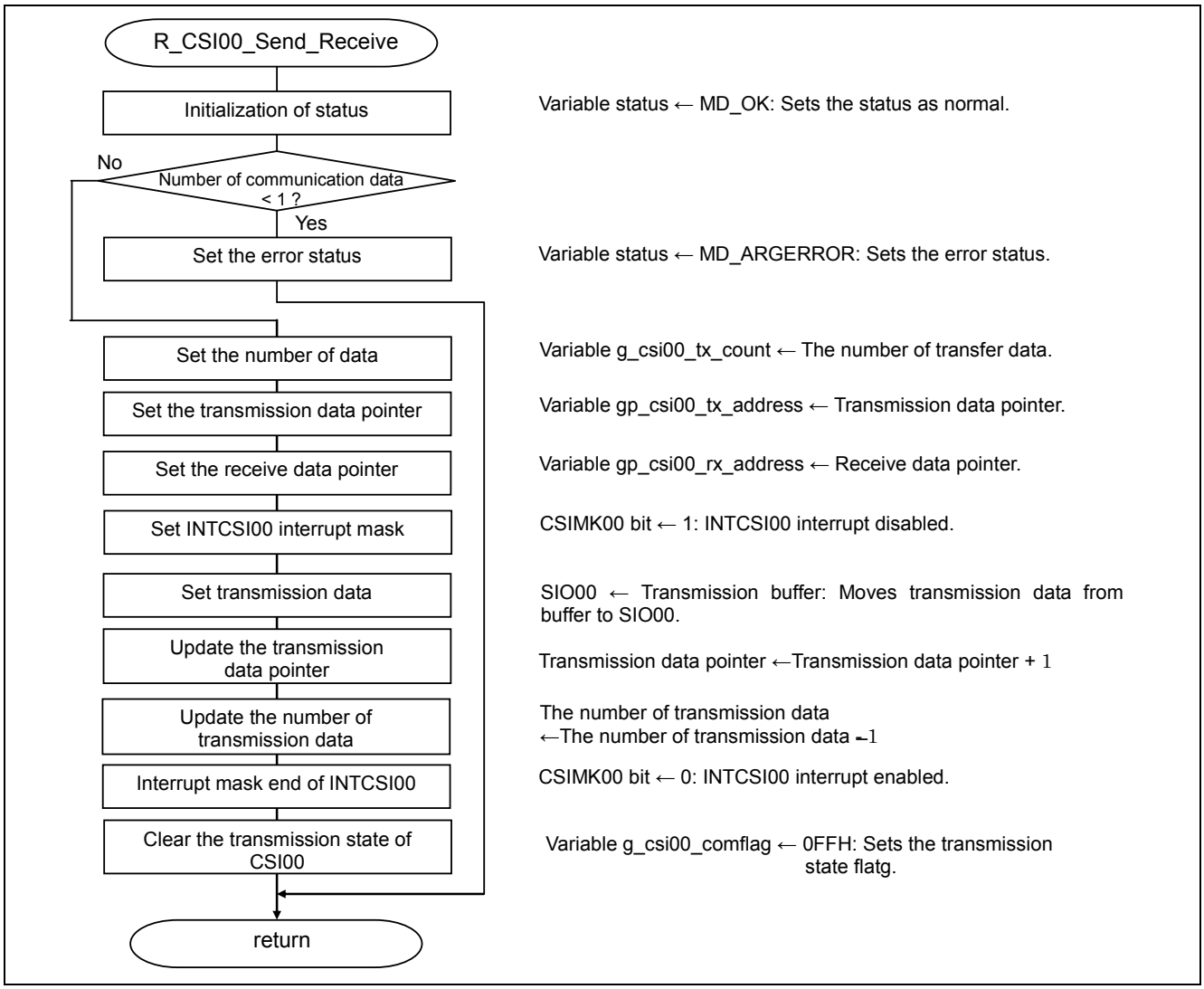


Figure 5.21 Starting Communication of CSI00

5.7.18 Communication End Interrupt of CSI00

Figure 5.22 shows the flowchart for processing of communication end interrupt of CSI00.

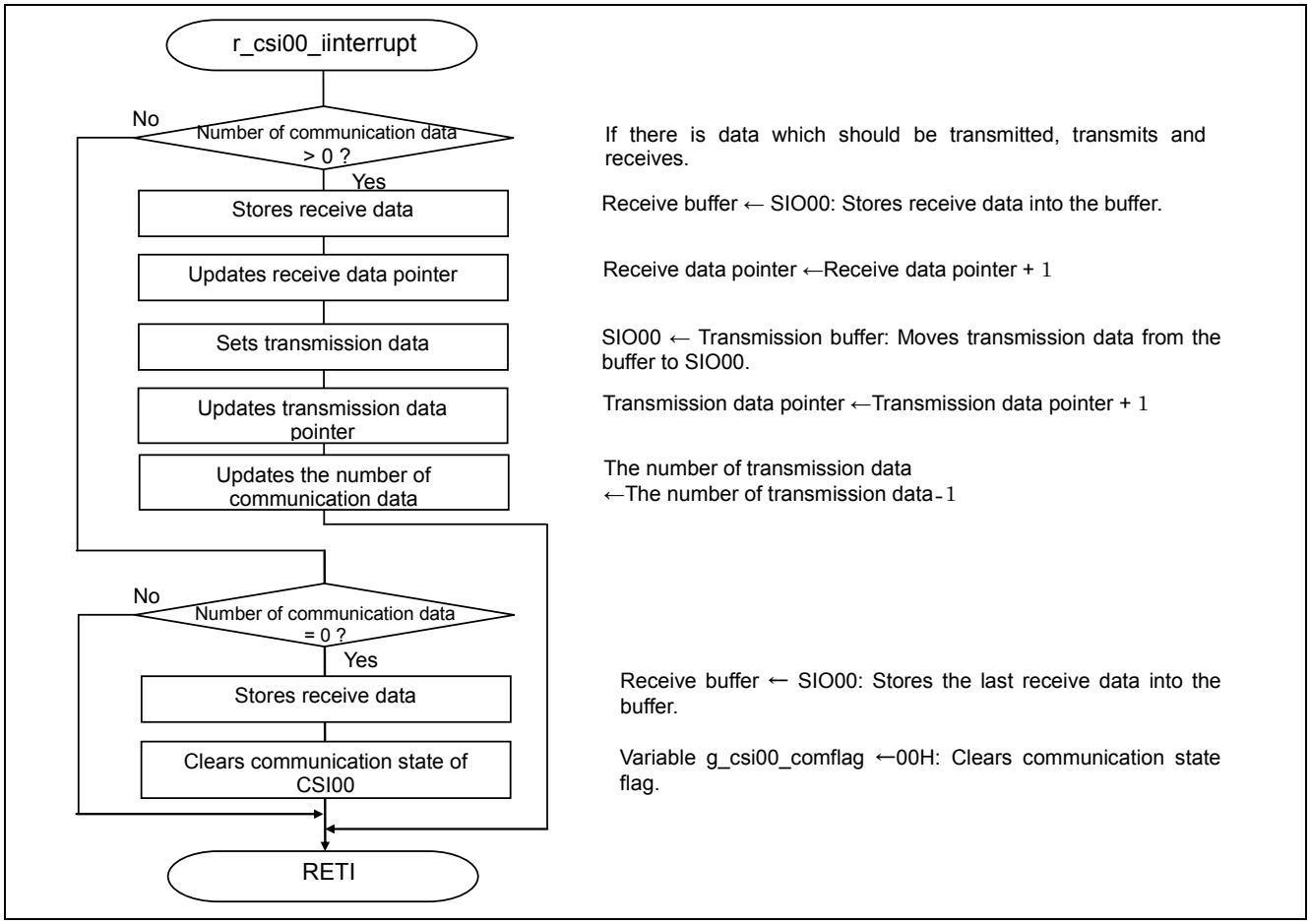


Figure 5.22 Communication End Interrupt of CSI00

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G13 User's Manual: Hardware (R01UH0146E)
RL78 Family User's Manual: Software (R01US0015E)
(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

Website and Support

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Revision History: RL78/G13 EEPROM Control by Microwire Communications

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	July 7, 2014	—	First edition issued
1.10	Dec. 22. 2015	37	A table was corrected.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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