RL78/G13

DMA Controller (UART Sequential Reception) CC-RL

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Introduction

This application note explains how to use the RL78/G13 DMA controller for sequential reception through the UART. The sample application covered in this application note stores data that is received using the UART communication in the on-chip RAM sequentially through the DMA controller.

Target Device

RL78/G13

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

This application note explains how to use the RL78/G13 DMA controller for sequential reception through the UART. The sample application covered in this application note receives ASCII data (one byte × five times) from an other device through UART communication using the serial array unit (SAU). The DMA controller is used to transfer the data from an SFR to the on-chip RAM. The receive data is stored in the on-chip RAM as triggered by the UART reception end interrupt. When the number of bytes to be transferred specified by the application (five times) is reached, the application regards the receive data as an ASCII code representing a five-digit decimal number and converts it into a numeric value. When the accumulated value of the receive data exceeds a threshold (100,000), the application turns on the LED.

Table 1.1 lists the peripheral functions and their uses. Figure 1.1 shows the outline of the operation. Figure 1.2 shows the timing chart of the DMA controller.

Table 1.1 Peripheral Functions to be Used and their Uses

Peripheral Function	Use
DMA controller	Transfers data received through the UART to the on-chip RAM.
Serial array unit	Used for UART reception.

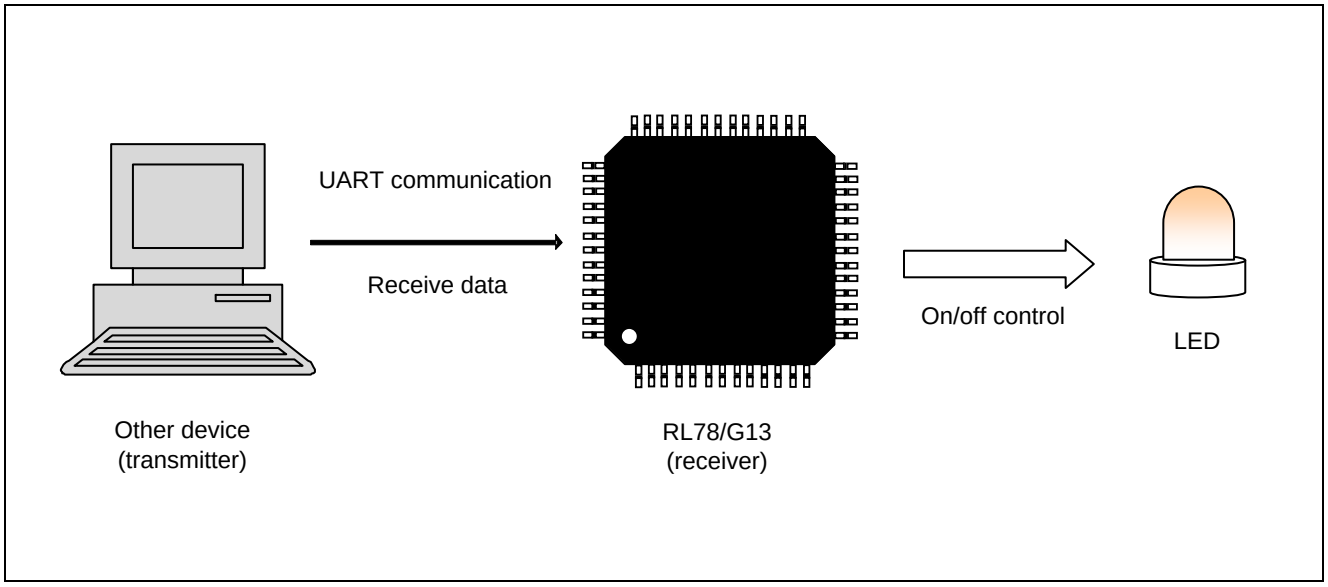

Figure 1.1 Outline of Operation

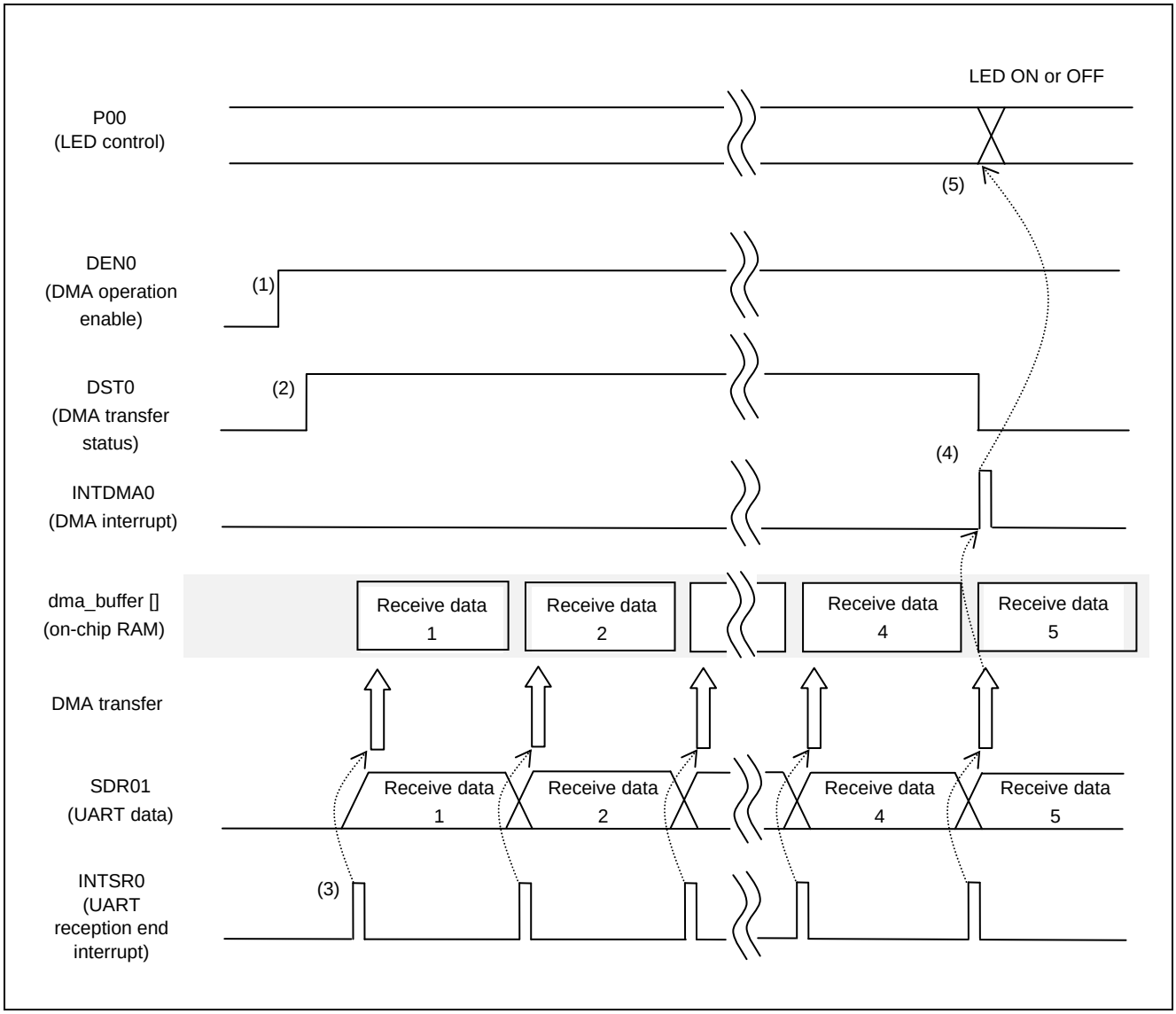

Figure 1.2 DMA Controller Timing Chart

(1) Set DEN0 to 1 to enable the operation of DMA.
(2) After making settings for the DMA controller, set DST0 to 1 to place the DAM controller in the DMA trigger wait mode.
(3) Transfer the value of the serial data register 01 (SDR01) to dma_buffer (on-chip RAM) using the UART reception transfer end interrupt (INTSR0) as a DMA trigger.
(4) When the number of times of DMA transfer reaches the specified number (five), the DMA controller exits the DMA trigger wait mode (DST0 = 0) and a DMA interrupt (INTDMA0) is generated.
(5) After a DMA interrupt (INTDMA0) occurs, the receive data stored in dma_buffer is converted into a numeric value. Control the output at P00 according to the accumulated value of the receive data to turn on or off the LED.

2. Operation Check Conditions

The sample code described in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G13 (R5F100LEA)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 32 MHz • CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0 V (can run on a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS + V3.01.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V4.0.0.26 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.01.00 from Renesas Electronics Corp.

3. Related Application Note

The application notes that are related to this application note are listed below for reference.

RL78/G13 Initialization (R01AN2575E) Application Note
RL78/G13 Serial Array Unit (UART Communication) (R01AN2517E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of hardware configuration that is used for this application note.

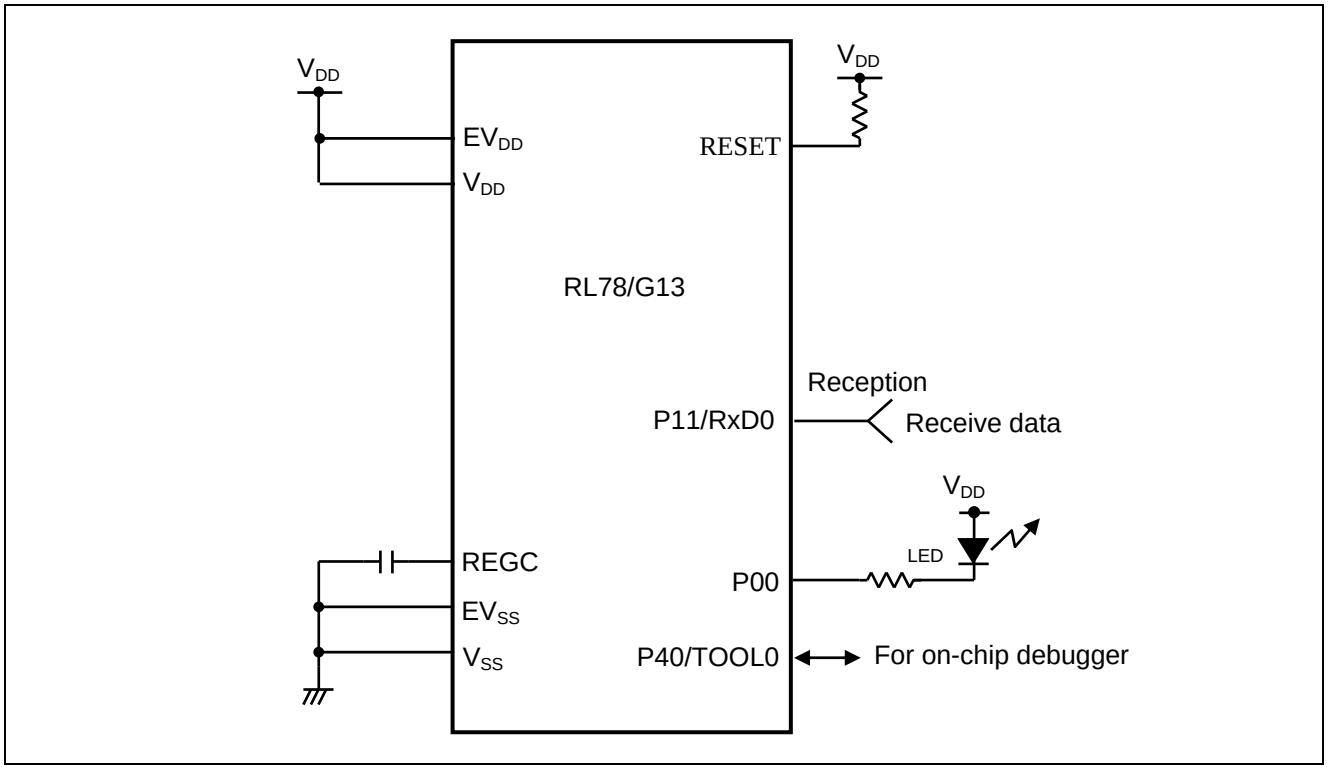

Figure 4.1 Hardware Configuration

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their functions.

Table 4.1 Pins to be Used and their Functions

Pin Name	I/O	Description
P11/RxD0	Input	Serial data reception pin
P00	Output	LED lighting control port

5. Description of the Software

5.1 Operation Outline

The sample application covered in this application note uses the DMA controller to store the data that is received through the UART in the on-chip RAM. Upon the completion of the transfer of 5-byte data by the DMA controller, the application converts the receive data stored in the on-chip RAM to a 5-digit numeric value. It turns on the LED when the accumulated value of the receive data exceeds 100,000 and turns off otherwise.

(1) Initialize the DMA controller.
<Conditions for Setting>

- Set the DMA transfer direction to "SFR to on-chip RAM."
- Use the UART reception transfer end interrupt request (INTSR0) as the DMA startup source.
- Set the transfer data size to 8 bits.
- Select the SDR01 address (0x000FFF12) as the address of the transfer source SFR.
- Set the transfer destination RAM address to the start address of variable dma_buffer [].
- Set the number of times of transfer to five.

(2) Initialize the SAU0.
<Conditions for setting>

- Use the SAU0 in UART mode, receive only.
- Use even parity as the parity setting.
- Set the data transfer order to LSB first.
- Set the data length to 8 bits.
- Set the receive data level to standard.
- Set the transfer rate to 9600 bps
- Use the error interrupt (INTSRE0).
- Set the priority level of the INTSRE0 interrupt to low.
- Use the UART reception transfer end interrupt (INTSR0) as the interrupt source.

(3) Set operation start trigger of channel 1 (SS01 bit) to 1 to place the UART in the communication wait status. Mask the transfer end interrupt (SRMK0 = 1) to disable INTSR0 interrupt processing. The vector interrupt processing for error interrupts (INTSRE0) is enabled to prevent overrun errors due to reception errors.
(4) Place the DMA controller in the trigger wait mode.
(5) Execute the HALT instruction to turn on the HALT mode and wait for a DMA transfer end interrupt (INTDMA0).
(6) The DMA controller updates the receive data on each occurrence of a transfer end interrupt request (INTSR0).

(7) When an error interrupt (INTSRE0) occurs, the error status is stored within the vector interrupt processing and DMA transfer is carried out via a software trigger.
(8) The HALT mode is exited on the occurrence of a DMA transfer end interrupt (INTDMA0) (even if a UART reception error occurs, a DMA0 transfer end interrupt (INTDMA0) is generated after the transfer of 5-byte data including the byte that is received when the error occurred is completed). Subsequently, the error status is examined. If no UART reception error has occurred, the processing described in step (9) is performed. If a UART reception error has occurred, the error status is cleared and the processing described in step (11) is performed.
(9) Convert the receive data (5 bytes) into a numeric value regarding it as a 5-digit decimal number represented in ASCII code.
(10) When the accumulated value computed in step (9) exceeds 100,000, the accumulated value is cleared and the LED which is connected to P00 is turned on. Otherwise, the accumulated value is retained and the LED connected to P00 is turned off.
(11) Initialize the DMA setting and wait for a trigger again.
(12) Turn on the HALT mode again and wait for DMA transfer end interrupt (INTDMA0).

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H/010C0H	11101111B	Disables the watchdog timer. (Stops counting after the release from the reset status.)
000C1H/010C1H	01111111B	LVD reset mode which uses 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

5.3 List of Constants

Table 5.2 lists the constants that are used in this sample program.

Table 5.2 Constants for the Sample Program

Constant	Setting	Description
_0002_SAU_CH1_START_TRG_ON	0x0002	Setting to enable the operation of serial channel enable status register 0 (SE0)
TOTAL_LIMIT	100000	Upper limit of total received values
_0005_DMA0_BYTE_COUNT	0x0005	Number of times of DMA transfer
P_LED	P0_bit.no0	LED lighting control port

5.4 List of Variables

Table 5.3 lists the global variables that are used by this sample program.

Table 5.3 Global Variables

Type	Variable Name	Contents	Function Used
uint8_t	g_DmaUartError	UART reception error variable	R_DMAC0_Create_UserInit r_dmac0_interrupt r_uart0_interrupt_error
uint8_t	dma_buffer[5]	Data receive buffer	R_DMAC0_Create_UserInit r_dmac0_interrupt
uint32_t	rx_total	Receive data accumulated value buffer	R_DMAC0_Create_UserInit r_dmac0_interrupt

5.5 List of Functions

Table 5.4 lists the functions that are used in this sample program.

Table 5.4 Functions

Function Name	Outline
R_UART0_MaskStart	UART0 communication start processing (interrupt masking)
R_DMAC0_Start	DMA0 transfer enabling
r_dmac0_interrupt	DMA0 transfer end interrupt
r_uart0_interrupt_error	UART0 reception error interrupt
R_DMAC0_Set_SoftwareTriggerOn	DMA0 software trigger transfer start processing

5.6 Function Specifications

Shown below are the functions that are used in this sample program.

[Function Name] R_UART0_MaskStart

Synopsis	UART0 communication start processing (interrupt masking)
Header	r_cg_serial.h
Declaration	void R_UART0_MaskStart(void)
Explanation	This function starts UART communication with the UART0 transfer end interrupt (INTSR0) masked.
Arguments	None
Return value	None
Remarks	Although R_UART0_Start which serves a similar purpose is available, this function is used because it is necessary to mask the required interrupt.

[Function Name R_DMAC0_Start

Synopsis	DMA0 transfer enabling
Header	r_cg_dmac.h
Declaration	void R_DMAC0_Start(void)
Explanation	This function starts controlling DMA transfer. It performs the following processing: • Clears the end interrupt request. • Enables DMA transfer end interrupts. • Enables the DMA transfer and switches the CPU to the DMA transfer wait status.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_dmac0_interrupt

Synopsis	DMA0 transfer end interrupt
Header	r_cg_dmac.h
Declaration	static void __near r_dmac0_interrupt (void)
Explanation	This function performs the interrupt processing when the specified number of DMA transfer have been performed. The function adds the receive data to the past accumulated value. When the specified count of 100,000 is exceeded, the function clears the accumulated value and turns on the LED that is connected to P00. Subsequently, the function restarts the DMA.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_uart0_interrupt_error

Synopsis	UART0 reception error interrupt
Header	None
Declaration	static void __near r_uart0_interrupt_error (void)
Explanation	This function clears the error status and reads the contents of the SDR01 register.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_DMAC0_Set_SoftwareTriggerOn

Synopsis	DMA0 software trigger transfer start processing
Header	None
Declaration	void R_DMAC0_Set_SoftwareTriggerOn(void)
Explanation	This function sets up the DMA0 software trigger and starts DMA transfer (once).
Arguments	None
Return value	None
Remarks	None

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

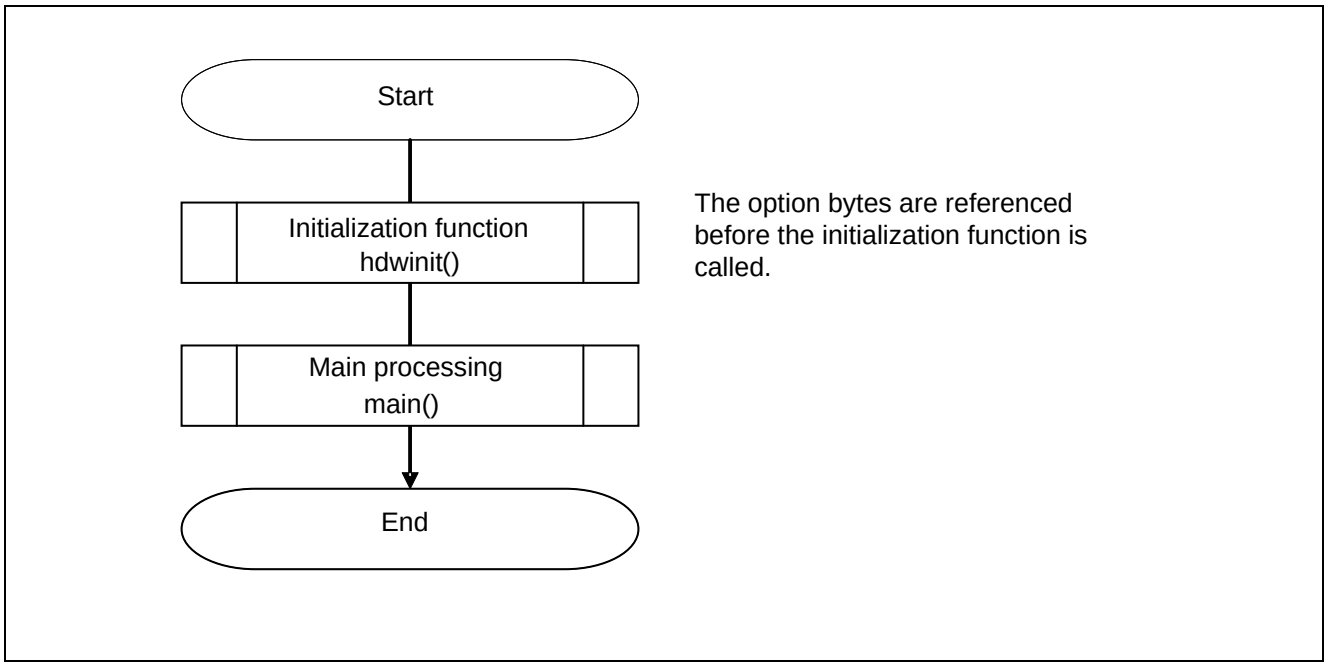

Figure 5.1 Overall Flow

5.7.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

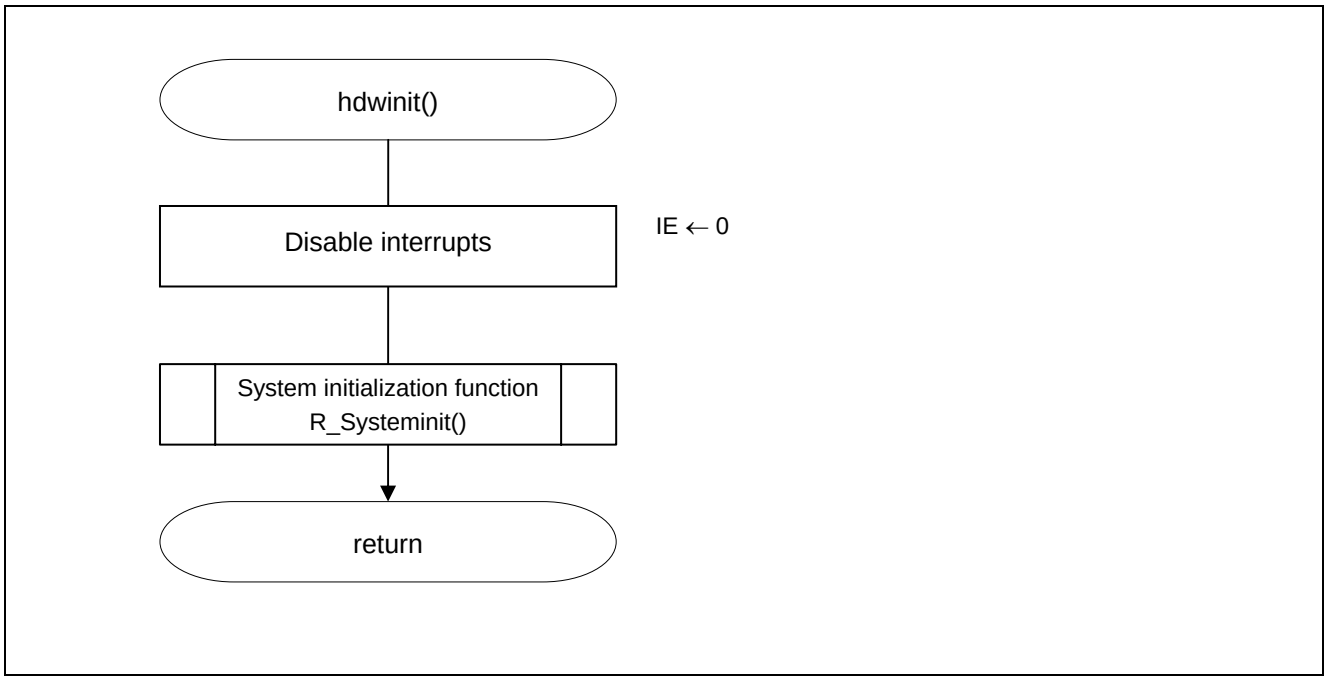

Figure 5.2 Initialization Function

5.7.2 System Initialization Function

Figure 5.3 shows the flowchart for the system initialization function.

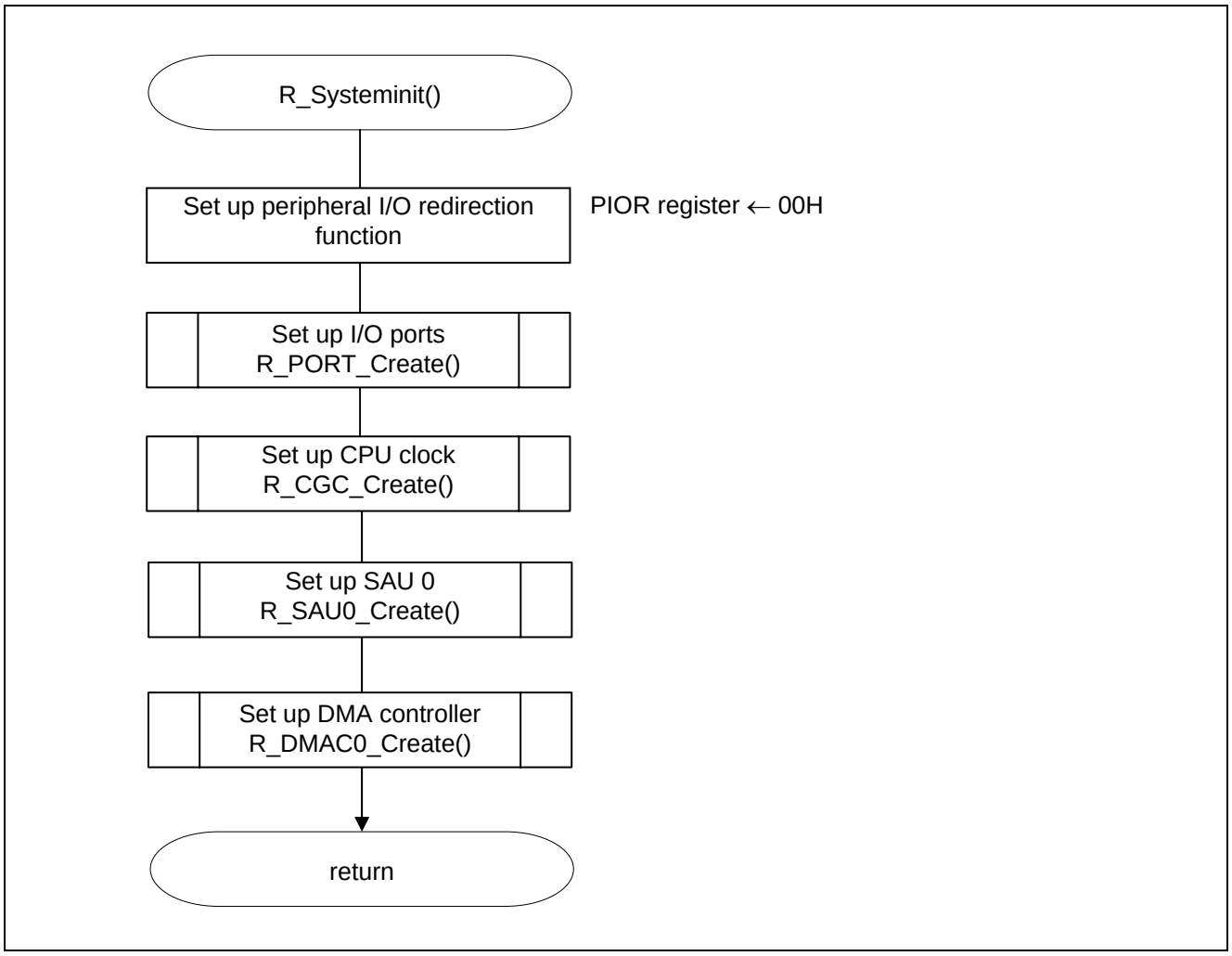

Figure 5.3 System Initialization Function

5.7.3 I/O Port Setup

Figure 5.4 shows the flowchart for setting up the I/O ports.

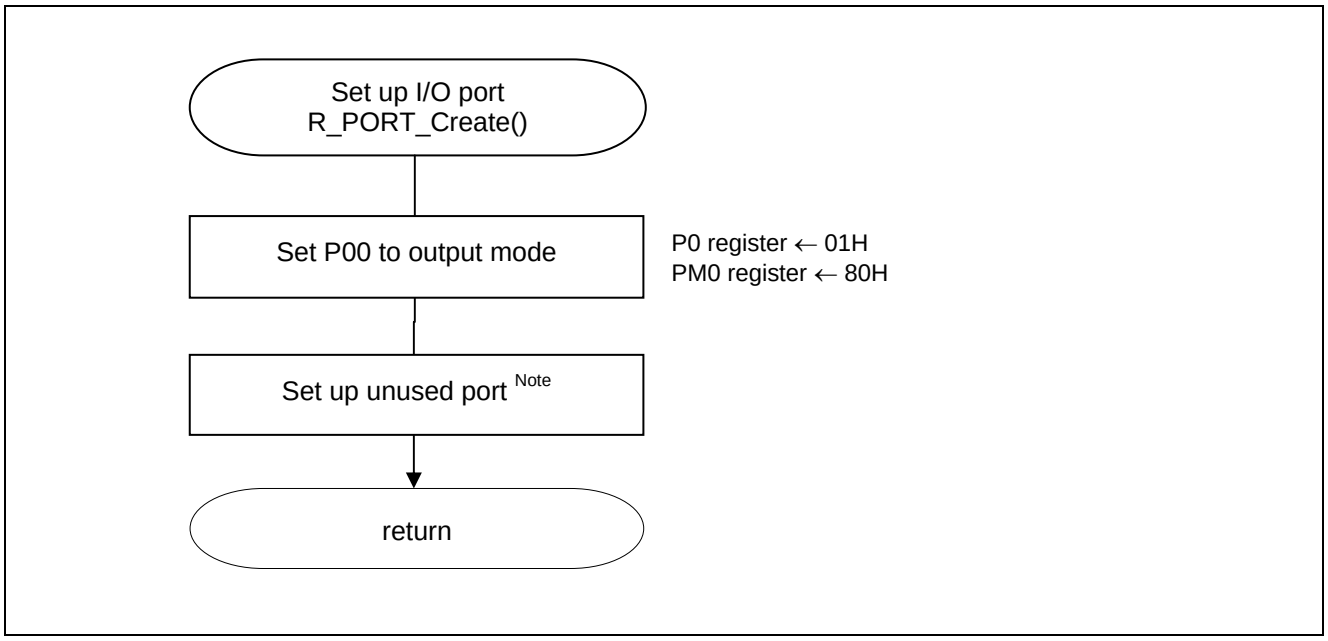

Figure 5.4 I/O Port Setup

Note: Refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E) for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are met. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

Setting up the LED port

- Port register 0 (P0)
- Port mode register 0 (PM0)

Symbol: P0

7	6	5	4	3	2	1	0
P07	P06	P05	P04	P03	P02	P01	P00
0	0	0	0	0	0	0	**1**

Bit 0

P00	P00 pin output data control (in output mode)
0	Output 0
1	**Output 1**

Symbol: PM0

7	6	5	4	3	2	1	0
PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00
1	0	0	0	0	0	0	**0**

Bit 0

PM00	P00 pin I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.4 CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock.

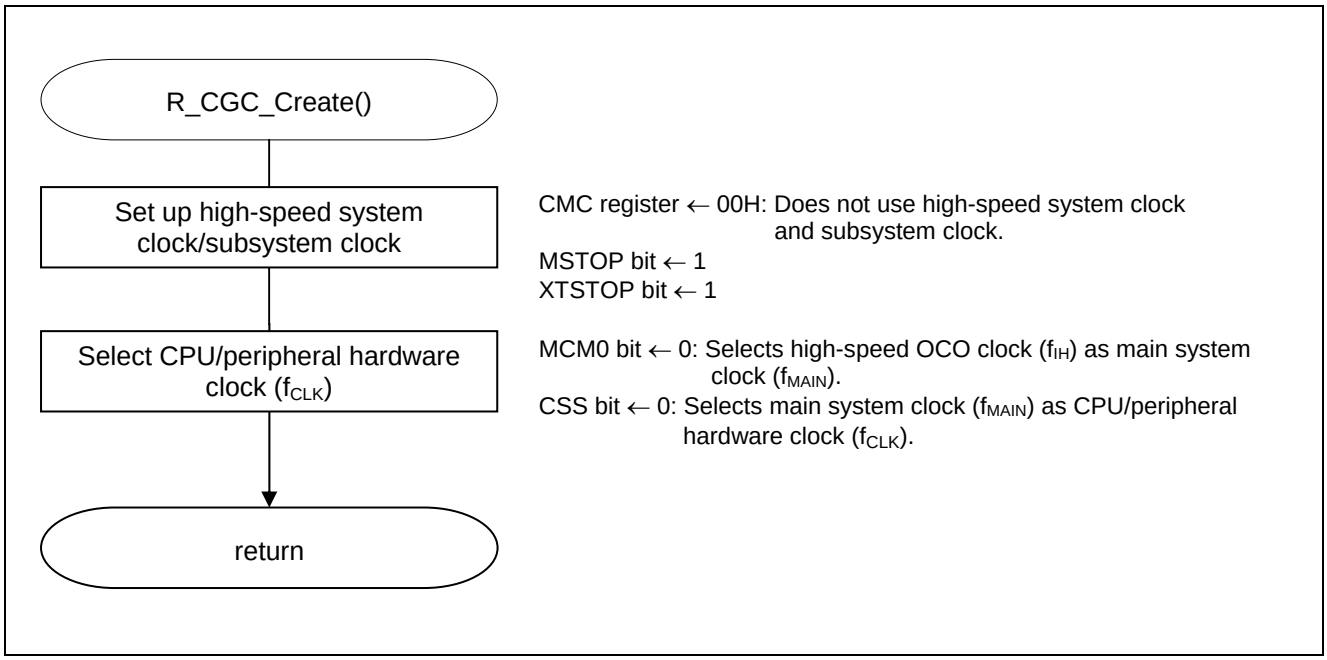

Figure 5.5 CPU Clock Setup

Caution: For details on the procedure for setting up the CPU clock (R_CGC_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E).

5.7.5 Serial Array Unit 0 Setup

Figure 5.6 shows the flowchart for setting up the serial array unit 0.

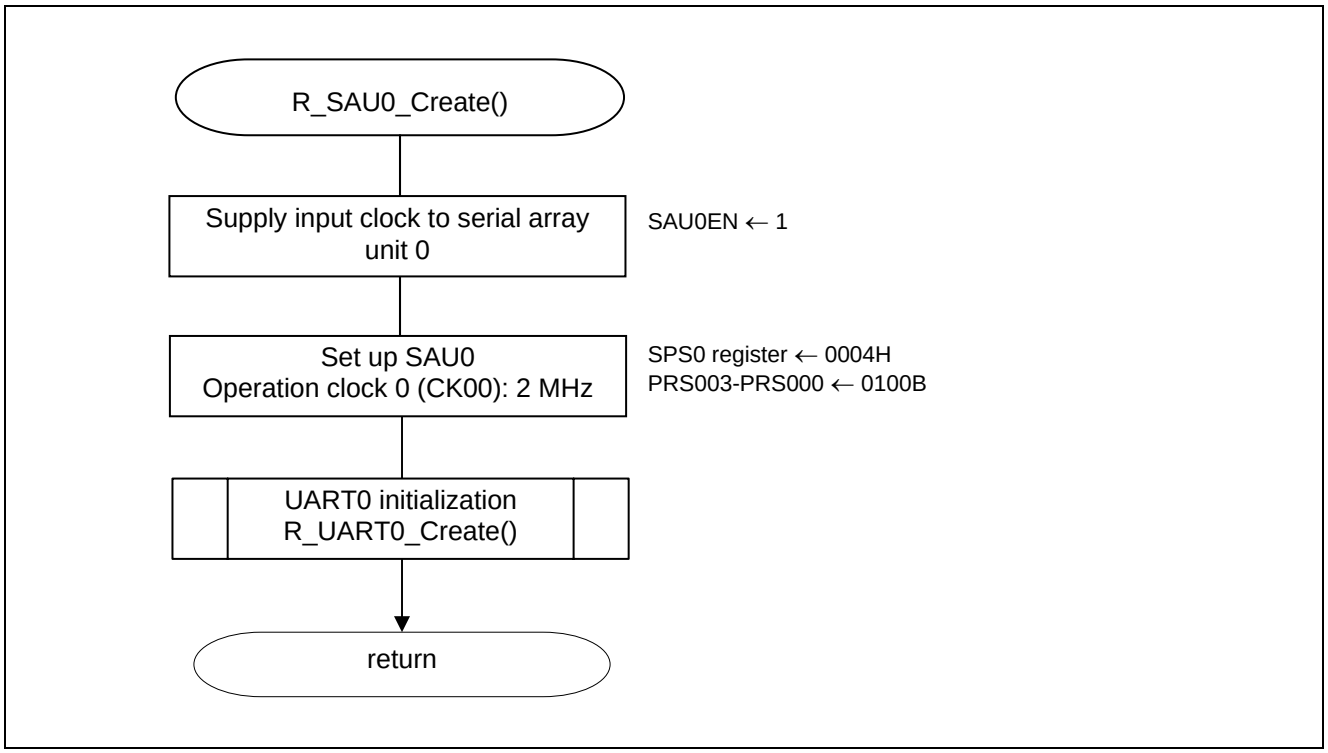

Figure 5.6 Serial Array Unit 0 Setup

Caution: For details on the procedure for setting up the SAU0 (R_SAU0_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Serial Array Unit (UART Communication) Application Note (R01AN2517E).

5.7.6 UART0 Setup

Figure 5.7 shows the flowchart for setting up the UART0.

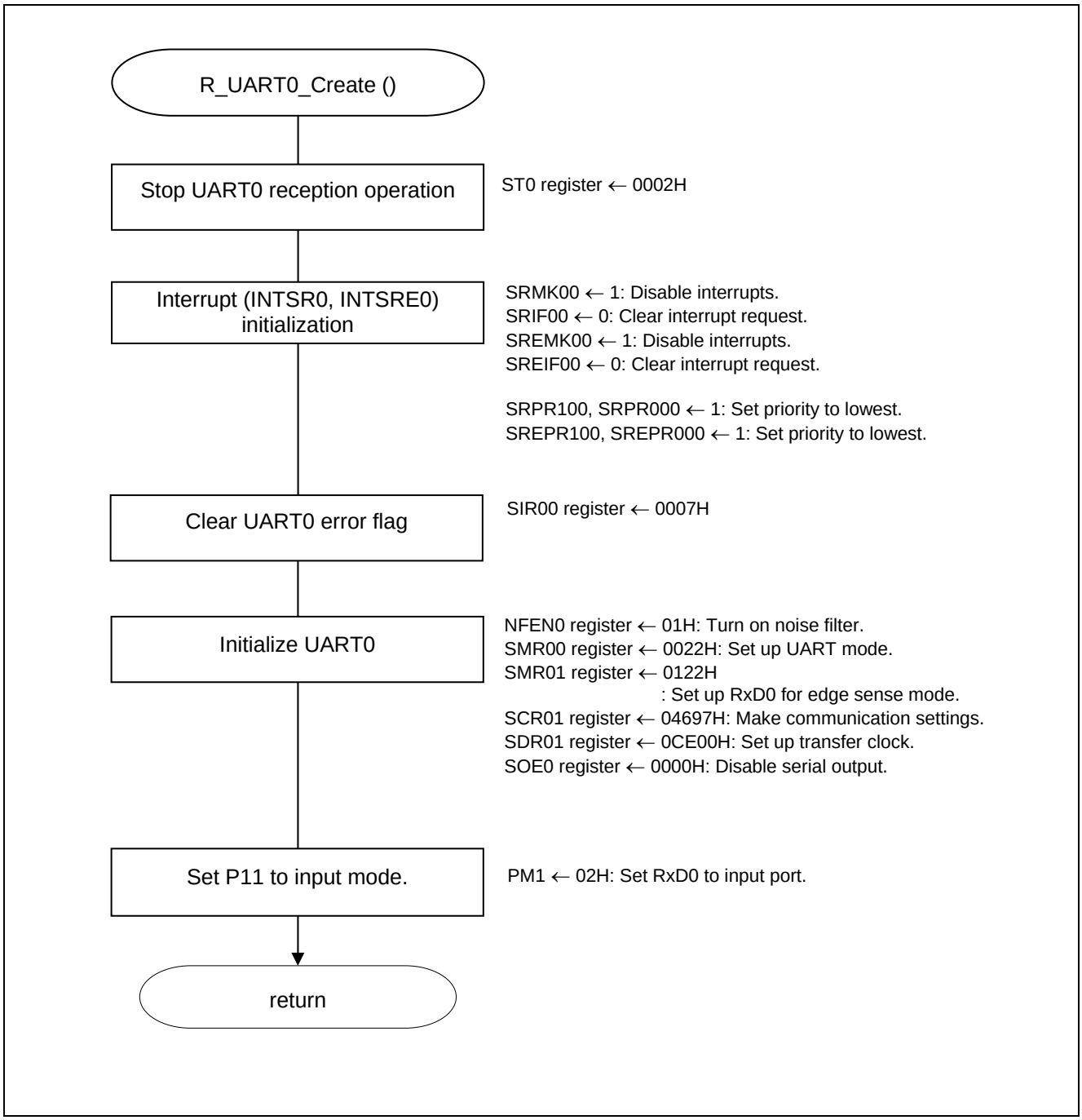

Figure 5.7 UART0 Setup

Caution: For details on the procedure for setting up the UART0 (R_UART0_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Serial Array Unit (UART Communication) Application Note (R01AN2517E).

5.7.7 DMA Controller Initialization

Figure 5.8 shows the flowchart for initializing the DMA controller.

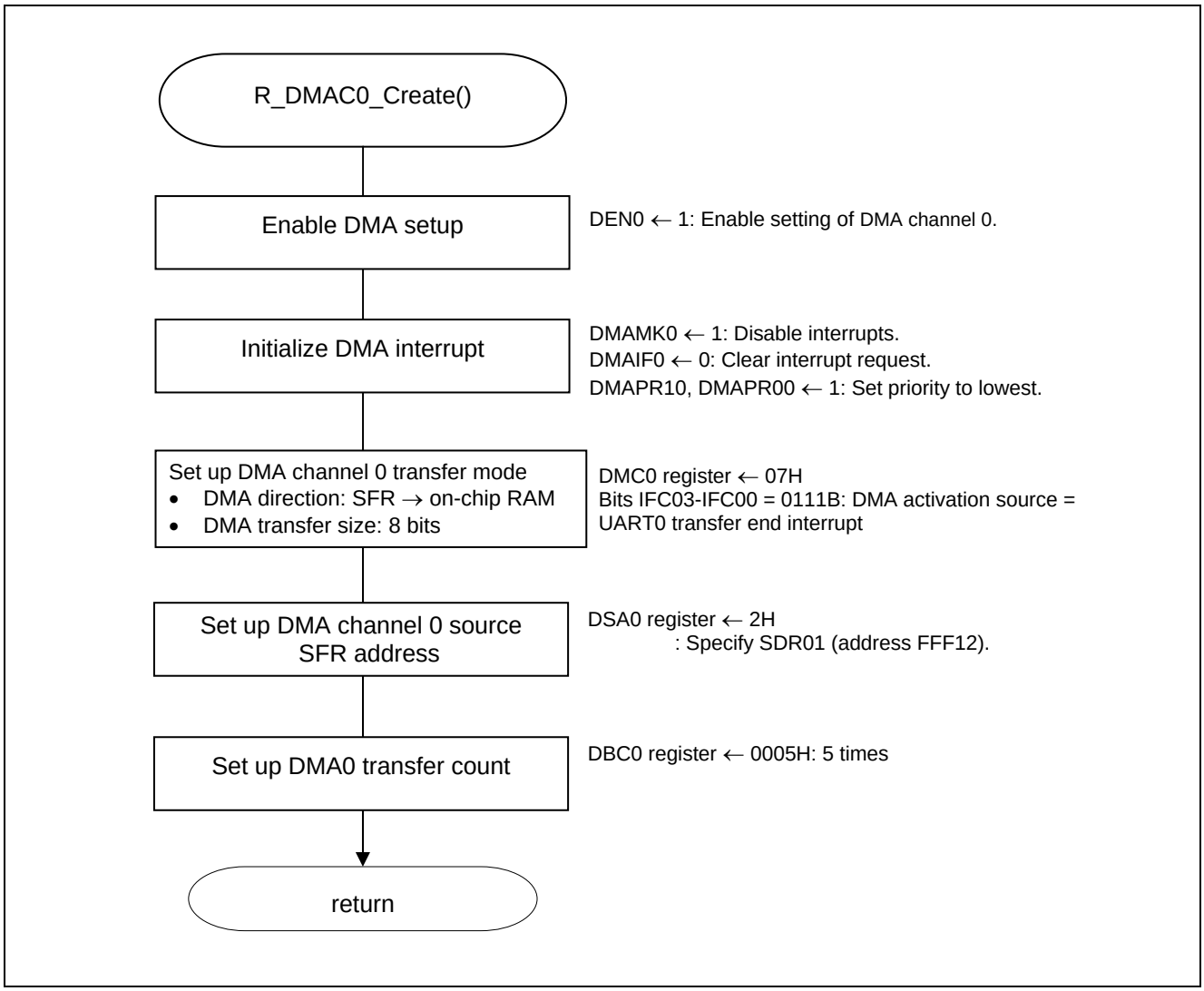

Figure 5.8 DMA Controller Initialization

Disabling DMA channel 0

- DMA operation control register (DRC0)

Symbol: DRC0

7	6	5	4	3	2	1	0
DEN0	0	0	0	0	0	0	DST0
1/0	0	0	0	0	0	0	**0**

Bit 7

DEN0	DMA operation enable flag
0	**Disables operation of DMA channel 0 (stops operating clock of DMA).** Disables DMA setup processing.
1	Enables operation of DMA channel 0. **Enables DMA setup processing.**

Bit 0

DST0	DMA transfer mode flag
0	**DMA transfer of DMA channel 0 is completed.**
1	DMA transfer of DMA channel 0 is not completed (still under execution).

Initializing DMA transfer end interrupts

- Interrupt request flag register (IF0H)
  Clear interrupt request flag.
- Interrupt mask flag register (MK0H)
  Clear interrupt mask.
- Priority specification flag register (PR00H, PR10H)
  Interrupt level = Level 3 (lowest level)

Symbol: IF0H

7	6	5	4	3	2	1	0
SREIF0 TMIF01H	SRIF0 CSIIF01 IICIF01	STIF0 CSIIF00 IICIF00	DMAIF1	DMAIF0	SREIF2 TMIF11H	SRIF2 CSIIF21 IICIF21	STIF2 CSIIF20 IICIF20
x	x	x	x	**0**	x	x	x

Bit 3

DMAIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: MK0H

7	6	5	4	3	2	1	0
SREMK0 TMMK01 H	SRMK0 CSIMK01 IICMK01	STMK0 CSIMK00 IICMK00	DMAMK1	DMAMK0	SREMK2 TMMK11 H	SRMK2 CSIMK21 IICMK21	STMK2 CSIMK20 IICMK20
x	x	x	x	**1**	x	x	x

Bit 3

DMAMK0	Interrupt processing control
0	Enables interrupt processing.
1	**Disables interrupt processing.**

Symbol: PR00H

7	6	5	4	3	2	1	0
SREPR00 TMPR001 H	SRPR00 CSIPR001 IICPR001	STPR00 CSIPR000 IICPR000	DMAPR01	DMAPR00	SREPR02 TMPR011 H	SRPR02 CSIPR021 IICPR021	STPR02 CSIPR020 IICPR020
x	x	x	x	**1**	x	x	x

Symbol: PR10H

7	6	5	4	3	2	1	0
SREPR10 TMPR101 H	SRPR10 CSIPR101 IICPR101	STPR10 CSIPR100 IICPR100	DMAPR11	DMAPR10	SREPR12 TMPR111 H	SRPR12 CSIPR121 IICPR121	STPR12 CSIPR120 IICPR120
x	x	x	x	**1**	x	x	x

Bit 3

DMAPR10	DMAPR00	Priority level selection
0	0	Specify level 0 (highest level)
0	1	Specify level 1
1	0	Specify level 2
1	**1**	**Specify level 3 (lowest level)**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up DMA channel 0 transfer mode

- DMA mode control register (DMC0)
  Use no software trigger.
  Set DMA transfer direction to SFR to on-chip RAM.
  Set transfer data size to 8 bits.
  Specify DMA transfer on DMA startup request.
  Select UART0 transfer end interrupt as DMA startup source.

Symbol: DMC0

7	6	5	4	3	2	1	0
STG0	DRS0	DS0	DWAIT0	IFC03	IFC02	IFC01	IFC00
0	**0**	**0**	**0**	**0**	**1**	**1**	**1**

Bit 7

STG0	DMA transfer start software trigger
0	**No trigger operation**
1	DMA transfer is started when DMA operation is enabled (DEN0 = 1).

Bit 6

DRS0	Selection of DMA transfer direction
0	**SFR to on-chip RAM**
1	On-chip RAM to SFR

Bit 5

DS0	Specification of transfer data size for DMA transfer
0	**8 bits**
1	16 bits

Bit 4

DWAIT0	Pending of DMA transfer
0	**Executes DMA transfer upon DMA start request (no held pending).**
1	Holds DMA start request pending if any.

Bits 3 to 0

IFC03	IFC02	IFC01	IFC00	Selection of DMA start source	
				Trigger Signal	Trigger contents
0	0	0	0	—	Disables DMA transfer by interrupt. (Only software trigger is enabled.)
0	0	0	1	INTAD	A/D conversion end interrupt
0	0	1	0	INTTM00	End of timer channel 0 count end or capture end interrupt
0	0	1	1	INTTM01	End of timer channel 1 count end or capture end interrupt
0	1	0	0	INTTM02	End of timer channel 2 count end or capture end interrupt
0	1	0	1	INTTM03	End of timer channel 3 count end or capture end interrupt
0	1	1	0	INTST0/INTCSI00	UART0 transmission transfer end or buffer empty interrupt/CSI00 transfer end or buffer empty interrupt
0	**1**	**1**	**1**	**INTSR0/INTCSI01**	**UART0 reception transfer end interrupt/CSI01 transfer end or buffer empty interrupt**
1	0	0	0	INTST1/INTCSI10	UART1 transmission transfer end or buffer empty interrupt/CSI10 transfer end or buffer empty interrupt
1	0	0	1	INTSR1/INTCSI11	UART1 reception transfer end interrupt/CSI11 transfer end or buffer empty interrupt
1	0	1	0	INTST2/INTCSI20	UART2 transmission transfer end or buffer empty interrupt/CSI20 transfer end or buffer empty interrupt
1	0	1	1	INTSR2/INTCSI21	UART2 reception transfer end interrupt/CSI21 transfer end or buffer empty interrupt
Other than above				Setting prohibited	

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up DMA channel 0 transfer SFR

- DMA SFR address register 0 (DSA0)
  Set up the source SFR of DMA transfer.

  Symbol: DSA0

7	6	5	4	3	2	1	0
0	**0**	**0**	**1**	**0**	**0**	**1**	**0**

  Set the lower 8 bits of RXD0/SIO01 (SFR address: 0x000FFF12).

  Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up DMA channel 0 destination RAM address

- DMA RAM address register 0 (DRA0)
  Set up the RAM address of DMA transfer destination.

  Symbol: DRA0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

  Set the start address of array dma_buffer[].

  Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up DMA channel 0 transfer count

- DMA byte count register 0 (DBC0)
  Specify DMA transfer count.

  Symbol: DBC0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**

  Set the number of times of DMA transfer to 5.

  Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.8 Main Processing

Figure 5.9 shows the flowchart for main processing.

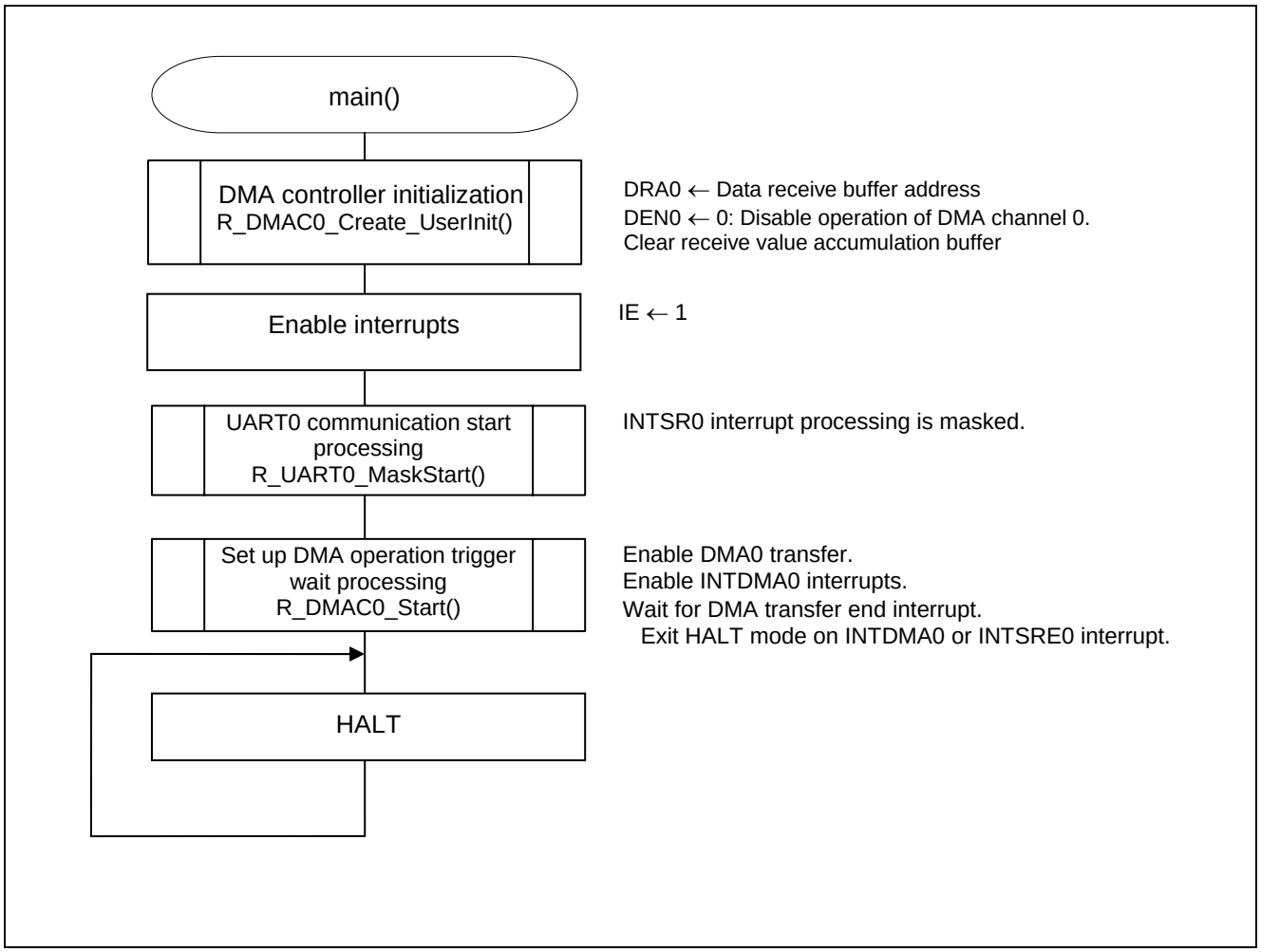

Figure 5.9 Main Processing

5.7.9 UART0 Communication Start Processing

Figure 5.10 shows the flowchart for UART0 communication start processing.

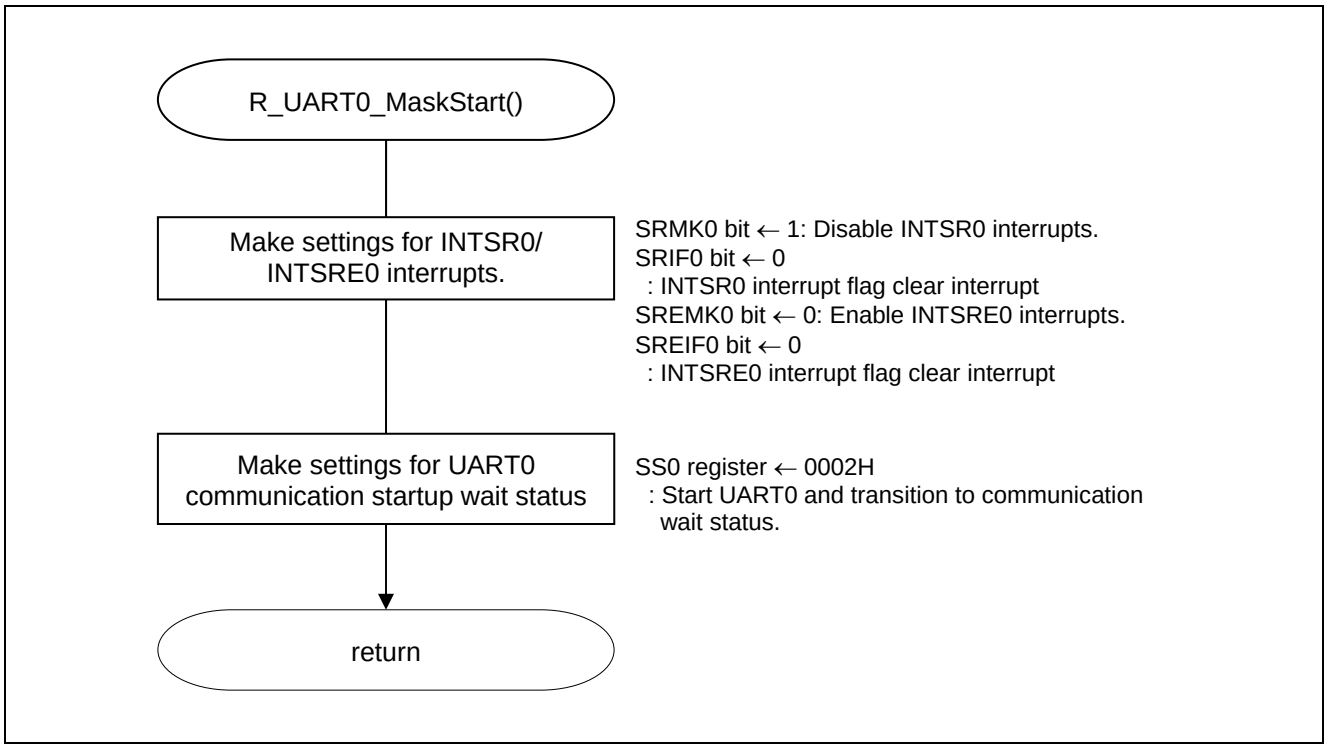

Figure 5.10 UART0 Communication Start Processing

Preparing for enabling DMA transfer end interrupts

- Interrupt request flag register (IF0H)
  Clear interrupt request flags.
- Interrupt mask flag register (MK0H)
  Clear interrupt masks.

Symbol: IF0H

7	6	5	4	3	2	1	0
SREIF0 TMIF01H	SRIF0 CSIIF01 IICIF01	STIF0 CSIIF00 IICIF00	DMAIF1	DMAIF0	SREIF2 TMIF11H	SRIF2 CSIIF21 IICIF21	STIF2 CSIIF20 IICIF20
0	**0**	x	x	x	x	x	x

Bit 7

SREIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Bit 6

SRIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK0H

7	6	5	4	3	2	1	0
SREMK0 TMMK01H	SRMK0 CSIMK01 IICMK01	STMK0 CSIMK00 IICMK00	DMAMK1	DMAMK0	SREMK2 TMMK11H	SRMK2 CSIMK21 IICMK21	STMK2 CSIMK20 IICMK20
0	**1**	x	x	x	x	x	x

Bit 7

SREMK0	Interrupt processing control
0	**Enables interrupt processing.**
1	Disables interrupt processing.

Bit 6

SRMK0	Interrupt processing control
0	Enables interrupt processing.
1	**Disables interrupt processing.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Starting serial channel 0

- Serial channel start register 0 (SS0)
  Start serial channel 0 communication/counting.

Symbol: SS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	SS03	SS02	SS01	SS00
0	0	0	0	0	0	0	0	0	0	0	0	x	x	**1**	x

Bit 1

SS01	Operation start trigger of channel 1
0	No trigger operation
1	**Sets the SE01 bit to 1 and enters the communication wait status.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.10 DMA Transfer Enable Processing

Figure 5.11 shows the flowchart for the DMA transfer enable processing.

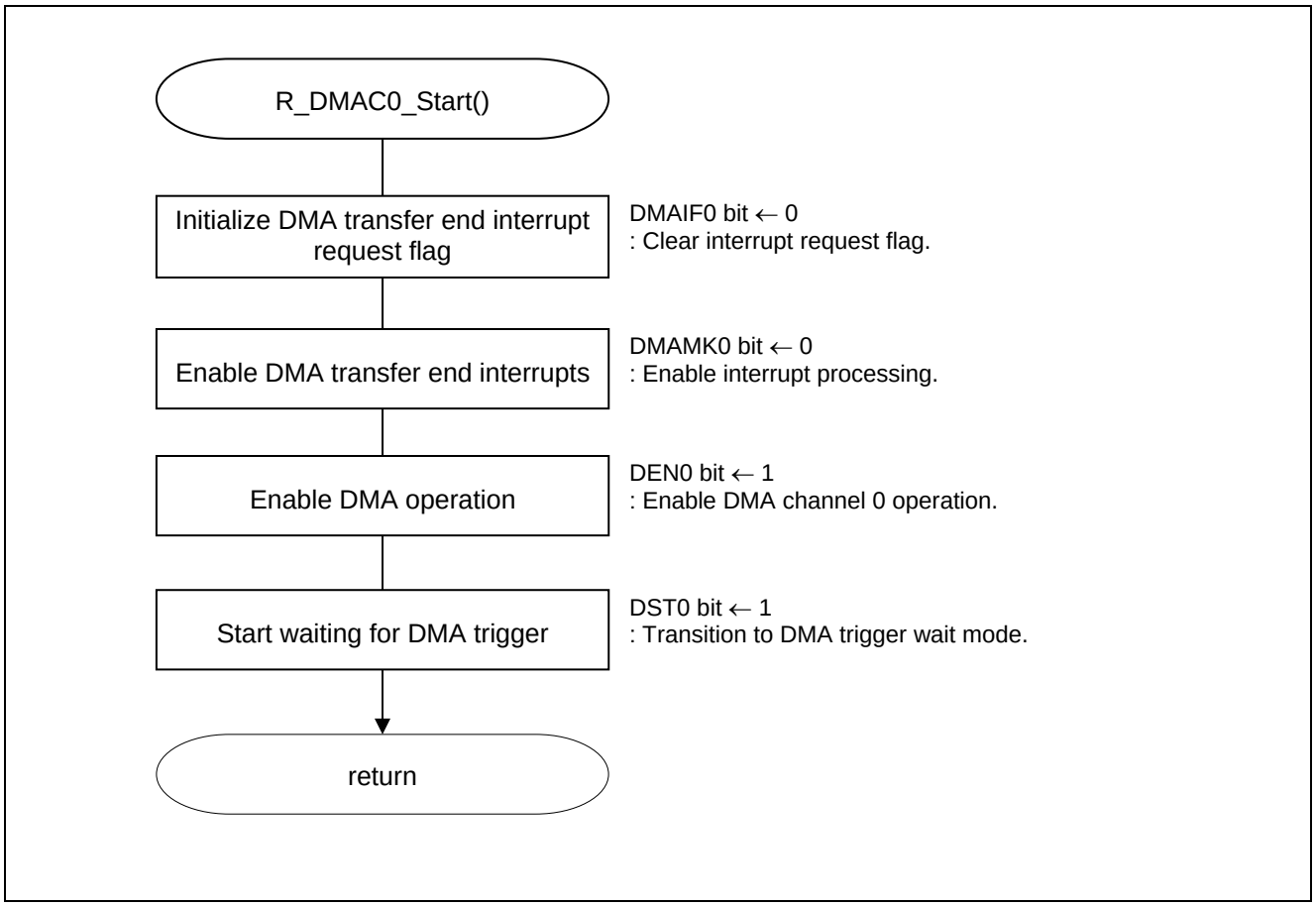

Figure 5.11 DMA Transfer Enable Processing

Preparing for DMA transfer end interrupt enable processing

- Interrupt request flag register (IF0H)
  Clear interrupt request flags.
- Interrupt mask flag register (MK0H)
  Clear interrupt masks.

Symbol: IF0H

7	6	5	4	3	2	1	0
SREIF0 TMIF01H	SRIF0 CSIIF01 IICIF01	STIF0 CSIIF00 IICIF00	DMAIF1	DMAIF0	SREIF2 TMIF11H	SRIF2 CSIIF21 IICIF21	STIF2 CSIIF20 IICIF20
x	x	x	x	**0**	x	x	x

Bit 3

DMAIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK0H

7	6	5	4	3	2	1	0
SREMK0 TMMK01H	SRMK0 CSIMK01 IICMK01	STMK0 CSIMK00 IICMK00	DMAMK1	DMAMK0	SREMK2 TMMK11H	SRMK2 CSIMK21 IICMK21	STMK2 CSIMK20 IICMK20
x	x	x	x	**0**	x	x	x

Bit 3

DMAMK0	Interrupt processing control
0	**Enables interrupt processing.**
1	Disables interrupt processing.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up DMA channel 0 operation trigger wait mode

- DMA operation control register (DRC0)

Symbol: DRC0

7	6	5	4	3	2	1	0
DEN0	0	0	0	0	0	0	DST0
1	0	0	0	0	0	0	**1**

Bit 7

DEN0	DMA operation enable flag
0	Disables operation of DMA channel 0 (stops operating clock of DMA). Disables DMA setup processing.
1	**Enables operation of DMA channel 0.** **Enables DMA setup processing.**

Bit 0

DST0	DMA transfer mode flag
0	DMA transfer of DMA channel 0 DMA is completed.
1	**DMA transfer of DMA channel 0 is not completed (still under execution).**

The DMA trigger wait mode is entered by setting DST0 to 1 after enabling DMA operation (DEN0 = 1).

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.11 DMA0 transfer End Interrupt Processing

Figure 5.12 shows the flowchart for the DMA0 transfer end interrupt processing.

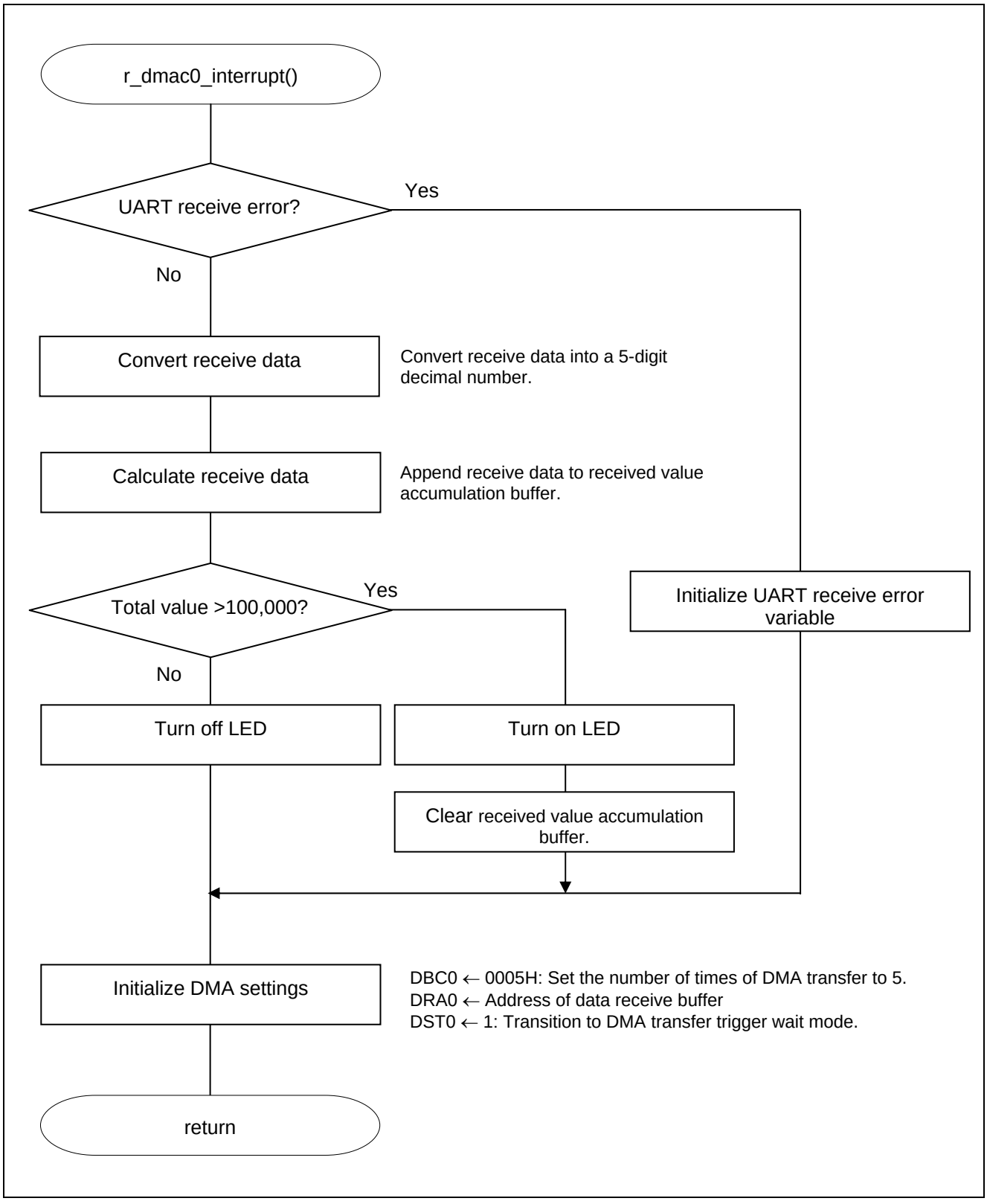

Figure 5.12 DMA0 Transfer End Interrupt Processing

5.7.12 UART0 Reception Error Interrupt Processing

Figure 5.13 shows the flowchart for the UART0 reception error interrupt processing.

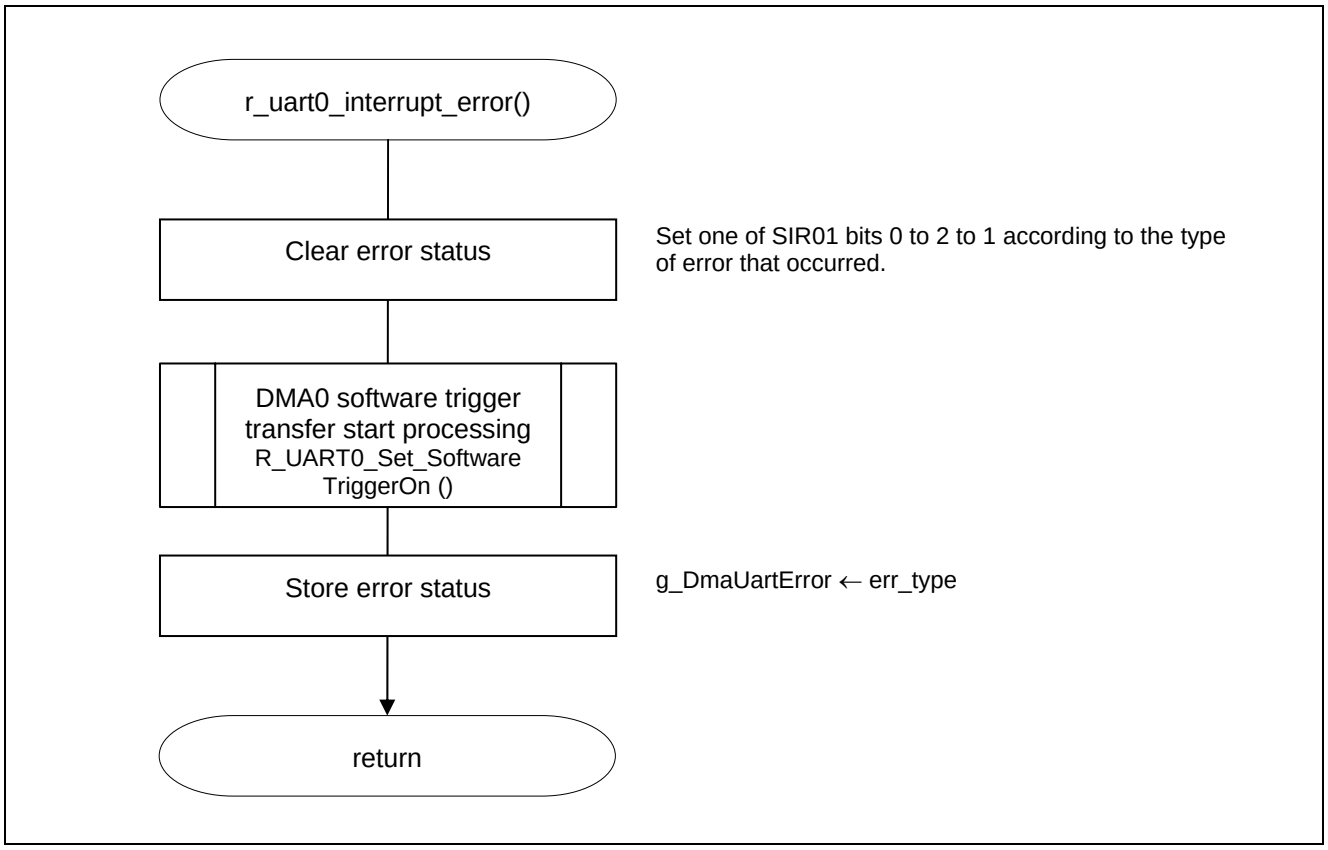

Figure 5.13 UART0 Reception Error Interrupt Processing

5.7.13 DMA0 Software Trigger Transfer Start Processing

Figure 5.14 shows the flowchart for the DMA0 software trigger transfer start processing.

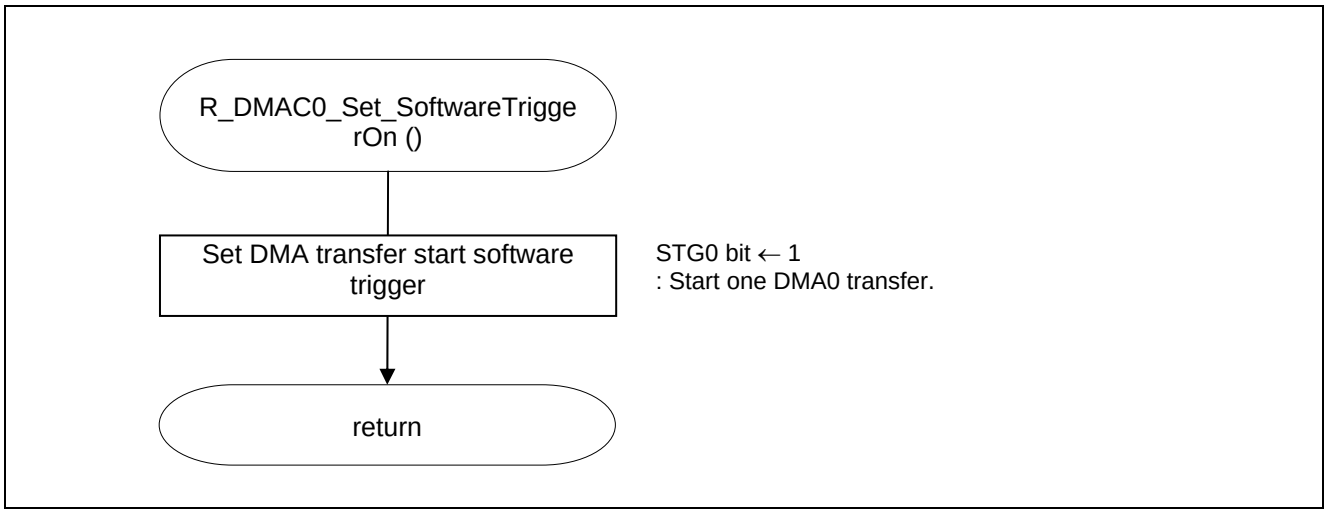

Figure 5.14 DMA0 Software Trigger Transfer Start Processing

Setting up DMA channel 0 transfer start software trigger

- DMA mode control register (DMC0)
  Set up DMA transfer start software trigger.

  Symbol: DMC0

7	6	5	4	3	2	1	0
STG0	DRS0	DS0	DWAIT0	IFC03	IFC02	IFC01	IFC00
1	0	0	0	0	1	1	1

  Bit 7

STG0	DMA transfer start software trigger
0	No trigger operation
1	**DMA transfer is started when DMA transfer operation is enabled (DEN0 = 1).**

  Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G13 User's Manual: Hardware (R01UH0146E)

RL78 Family User's Manual: Software (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

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Revision Record	RL78/G13 DMA Controller (UART Sequential Reception)

Rev.	Date	Description	
		Page	Summary
1.00	May 28, 2015	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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