RL78/G12

Key Interrupt Function

R01AN1462EJ0100
Rev. 1.00
Aug 28, 2013

Introduction

This application note explains how to use the key interrupt function.

A 4 x 4 key matrix is scanned to show the numbers of key switches being pressed in binary on five LED displays.

Target Device

RL78/G12

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

This application note shows the use of a key interrupt function for a 4 x 4 key matrix. A key interrupt (INTKR) is used as a trigger for key scan.

When any key is pressed with all scan lines activated to enable all key inputs, an INTKR is generated. After the generation of the INTKR, the number of the pressed key is identified through key scan. A key detection is performed every 30 ms, and if detected key numbers match each other twice, the corresponding key is recognized to be pressed (chattering prevention processing). The number of the recognized key is shown on five LED displays. When multiple keys are pressed simultaneously, all the LEDs are turned on. When no key is pressed, all the LEDs are turned off.

Table 1.1 lists the peripheral functions to be used and their uses. Figure 1.1 illustrates the outline of the key scan operation

Table 1.1 Peripheral Functions to be Used and Their Uses

Peripheral Function	Use
P122/KR2/X2/EXCLK/(TI02)/(INTP2) P121/KR3/X1/(TI03)/(INTP3) P60/KR4/SCLA0/(TxD0) P61/KR5/SDAA0/(RxD0)	Key interrupt detection
P20/ANI0/AVREFP P21/ANI1/AVREFM P22/ANI2 P23/ANI3	Key scanning output
Timer array unit 0 channel 0	Interval timer for timing of key scanning
P10/ANI16/PCLBUZ0/SCK00/SCL00 P11/ANI17/SI00/RxD0/SDA00/TOOLRxD P12/ANI18/SO00/TxD0/TOOLTxD P13/ANI19/TI00/TO00/INTP2 P14/ANI20/TI01/TO01/INTP3	LED display data output

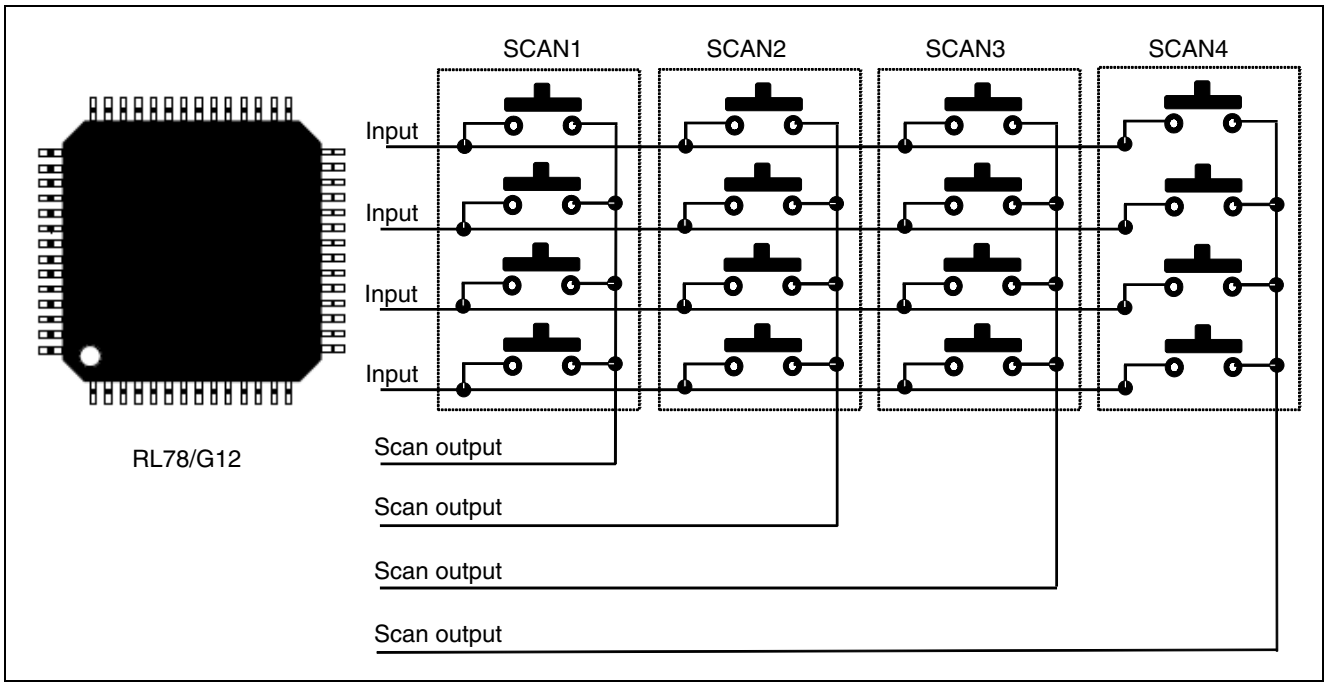

Figure 1.1 Outline of Key Scan Operation

Reference

Generally, N-ch open drain output is used for key scan. Here, however, CMOS output is used. As shown in Figure 4.1, diode is mounted for each key to prevent the conflict of scan outputs when multiple keys are pressed simultaneously.
Key scanning with N-ch open drain pins does not allow reduction of the intervals between scans. This is because the use of pull-up resistors of several tens of k-ohms causes scan line signals to take several microseconds to several tens of microseconds to rise. Here, port high-level output is used to shorten the time for the signals to rise.

2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G12 (R5F1026A)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 24 MHz • CPU/peripheral hardware clock: 24 MHz
Operating voltage	5.0 V (Operation is possible over a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVI}): Reset mode which uses 2.81 V (2.76 V to 2.87 V)
Integrated development environment	CubeSuite + V1.03.00 from Renesas Electronics Corp.
Assembler	RA78K0R V1.70 from Renesas Electronics Corp.
Board to be used	RL78/G12 target board (QB-R5F1026A-TB)

Caution This sample code supports 20-pin products (R5F1026A) only.

3. Related Application Notes

The application notes that are related to this application note are listed below for reference.

RL78/G12 Initialization (R01AN1030E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 gives an example of hardware configuration used in this application note.

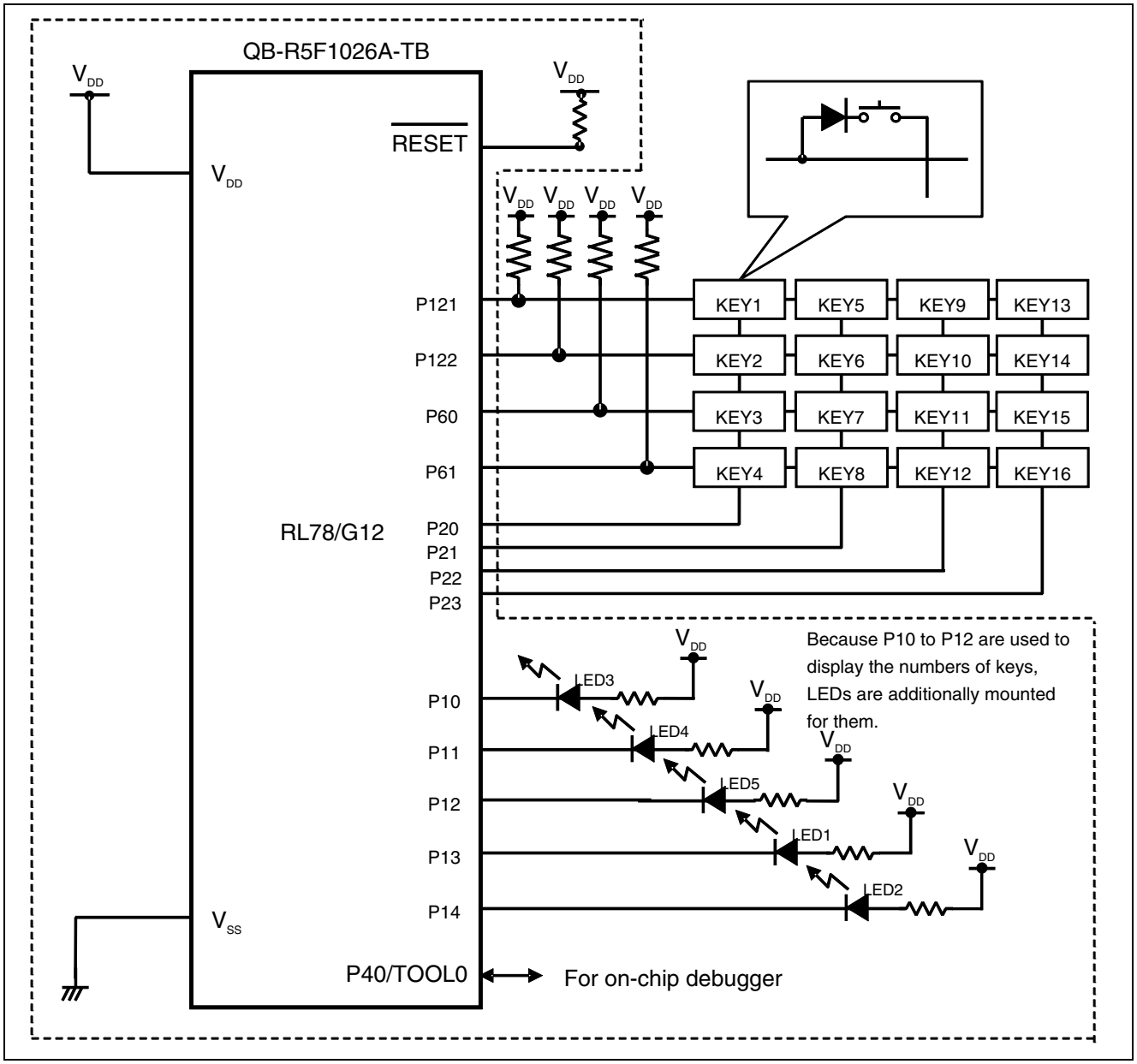

Figure 4.1 Hardware Configuration

Cautions 1 The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2 V_{DD} must be held at not lower than the reset release voltage (V_{LVI}) that is specified as LVD.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their functions.

Table 4.1 Pins to be Used and their Functions

Pin Name	I/O	Description
P121, P122, P60, and P61	Input	Key interrupt detection
P20 to P23	Output	Key scan output
P10 to P14	Output	LED display data output

5. Description of the Software

5.1 Operation Overview

This application note shows the use of key interrupt (INTKR) and timer interrupt (INTTM00).

When any key is pressed in a key input wait state (with all scan lines activated to enable all key inputs), an INTKR is generated. After the generation of the INTKR, the number of the pressed key is identified through key scan. A key detection is performed twice at an interval of 30 ms, and if detected key numbers match each other twice, the corresponding key is recognized to be pressed (chattering prevention processing). The number of the recognized key is shown in binary on five LED displays. When multiple keys are pressed simultaneously, all the LEDs are turned on. When no number of key is detected, all the LED displays are turned off to return the system to a key input wait state.

(1) Make initial setting.

<Setting Conditions>

- Set channel 0 of TAU0 to a 30-ms-period interval timer.
- Set the key interrupt detection pins to an interrupt enable state.
- Set all the key scan output pins to an output state.

(2) Wait until a key is pressed.

(3) Perform key scan after an INTKR is generated.

(4) Perform key scan twice at an interval of 30 ms and perform chattering prevention processing.

(5) When a key number is recognized, the LED display indicates that the corresponding key is pressed.

(6) When no number of key is detected, all the scan lines are activated to return the system to a key input wait state in (2).

This application note represents P10 as bit 10 and P14 as bit 4. The numbers of pressed keys are shown in binary on LED displays connected to P10 to P14.

Table 5.1 shows the relationship between LED-connected ports and bits.

Table 5.1 Relationship between LED-connected Ports and Bits

	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port	P14 (LED2)	P13 (LED1)	P12 (LED5)	P11 (LED4)	P10 (LED3)

Table 5.2 shows the relationship between the numbers of pressed keys and LED displays.

Table 5.2 Relationship between Numbers of Pressed Keys and LED Displays

		LED2 (P14)	LED1 (P13)	LED5 (P12)	LED4 (P11)	LED3 (P10)
Number of Key	No Key is Pressed	OFF	OFF	OFF	OFF	OFF
	1	OFF	OFF	OFF	OFF	**ON**
	2	OFF	OFF	OFF	**ON**	OFF
	3	OFF	OFF	OFF	**ON**	**ON**
	4	OFF	OFF	**ON**	OFF	OFF
	5	OFF	OFF	**ON**	OFF	**ON**
	6	OFF	OFF	**ON**	**ON**	OFF
	7	OFF	OFF	**ON**	**ON**	**ON**
	8	OFF	**ON**	OFF	OFF	OFF
	9	OFF	**ON**	OFF	OFF	**ON**
	10	OFF	**ON**	OFF	**ON**	OFF
	11	OFF	**ON**	OFF	**ON**	**ON**
	12	OFF	**ON**	**ON**	OFF	OFF
	13	OFF	**ON**	**ON**	OFF	**ON**
	14	OFF	**ON**	**ON**	**ON**	OFF
	15	OFF	**ON**	**ON**	**ON**	**ON**
	16	**ON**	OFF	OFF	OFF	OFF
	Multiple Keys are Pressed	**ON**	**ON**	**ON**	**ON**	**ON**

5.2 List of Option Byte Settings

Table 5.3 summarizes the settings of the option bytes.

Table 5.3 Option Byte Settings

Address	Value	Description
000C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H	01111111B	LVD reset mode, 2.81 V (2.76 to 2.87 V)
000C2H	11100000B	HS mode HOCO: 24 MHz
000C3H	10000101B	Enables the on-chip debugger.

5.3 List of Functions (Subroutines)

Table 5.4 gives a list of functions that are used by this sample program.

Table 5.4 Functions

Function (Subroutine) Name	Outline
RESET_START	Initializes the hardware and calls the main function.
SINIPORT	Sets the I/O ports.
SINICLK	Sets the clock generation circuit.
SINITAU	Sets the timer array unit
SINIKEY	Sets key interrupt
SWAIT30MS	30-ms wait processing
SSTRTKEY	Enables key interrupt
SSCANKEY	Key scan processing
SGETKEY	Gets key return
SLEDOUT	LED display control

5.4 Function (Subroutine) Specifications

This section describes the specifications for the functions that are used in the sample code.

[Function Name] RESET_START

Synopsis	Initializes the CPU at reset start.
Declaration	-
Explanation	Calls the main function after setting the stack pointer and initializing the hardware.
Arguments	None
Return value	None
Remarks	None

[Function Name] SINIPORT

Synopsis	Sets the I/O ports.
Declaration	-
Explanation	Sets P10 to P14 to output (high-level output). Sets the other ports to output (low-level output).
Arguments	None
Return value	None
Remarks	None

[Function Name] SINICLK

Synopsis	Sets the clock generation circuit.
Declaration	-
Explanation	Initializes the registers related to the clock generation circuit.
Arguments	None
Return value	None
Remarks	None

[Function Name] SINITAU

Synopsis	Sets the timer array unit.
Declaration	-
Explanation	Sets the timer array unit.
Arguments	None
Return value	None
Remarks	None

[Function Name] SINIKEY

Synopsis	Sets key interrupt.
Declaration	-
Explanation	Sets key interrupt.
Arguments	None
Return value	None
Remarks	None

[Function Name] SWAIT30MS

Synopsis	30-msec wait processing
Declaration	-
Explanation	Waits in HALT mode for 30 msec.
Arguments	None
Return value	None
Remarks	None

[Function Name] SSTRTKEY

Synopsis	Enables key interrupt.
Declaration	-
Explanation	Enables key interrupt.
Arguments	None
Return value	None
Remarks	None

[Function Name] SSCANKEY

Synopsis	Key scan processing	
Declaration	-	
Explanation	Checks the key press status of the key matrix.	
Arguments	None	: [Key scan result]
Return value	BC	
Remarks	None	

[Function Name] SGETKEY

Synopsis	Gets key return.	
Declaration	-	
Explanation	Reads P6 and P12 registers and gets the values of return ports.	
Arguments	None	: [Value of return port] Values of P61, P60, P122, and P121
Return value	C	
Remarks	None	

[Function Name] SLEDOUT

Synopsis	LED display control	
Declaration	-	
Explanation	Shows the numbers of pressed keys in binary on LED displays.	
Arguments	BC	: [Key scan result] : [Number of pressed key]
Return value	E	
Remarks	None	

5.5 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

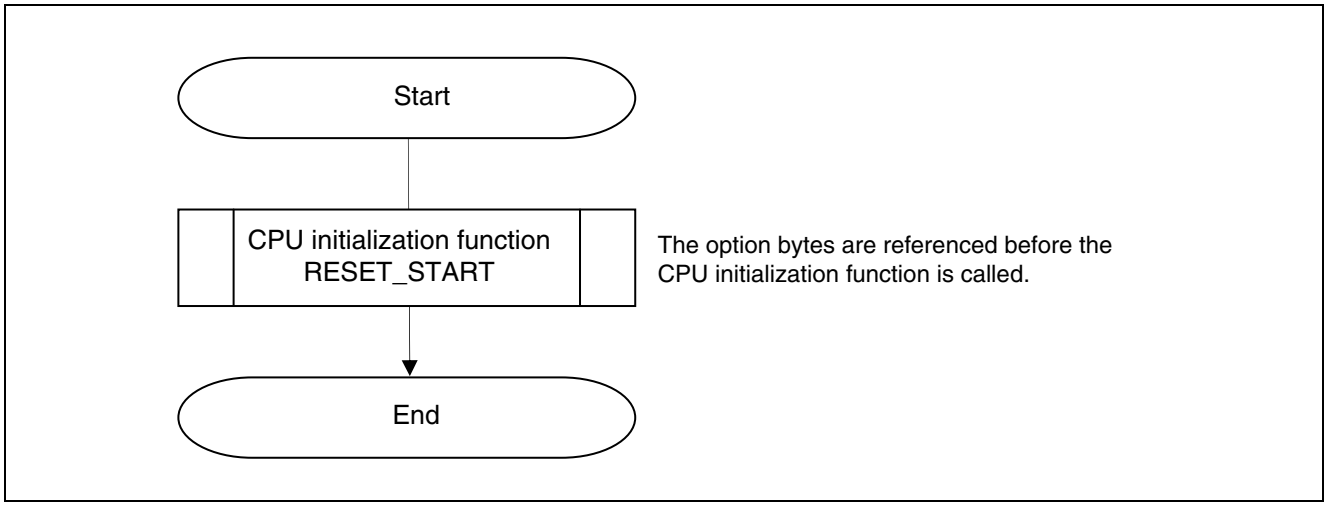

Figure 5.1 Overall Flow

5.5.1 CPU Initialization Function

Figure 5.2 shows the flowchart for the CPU initialization function.

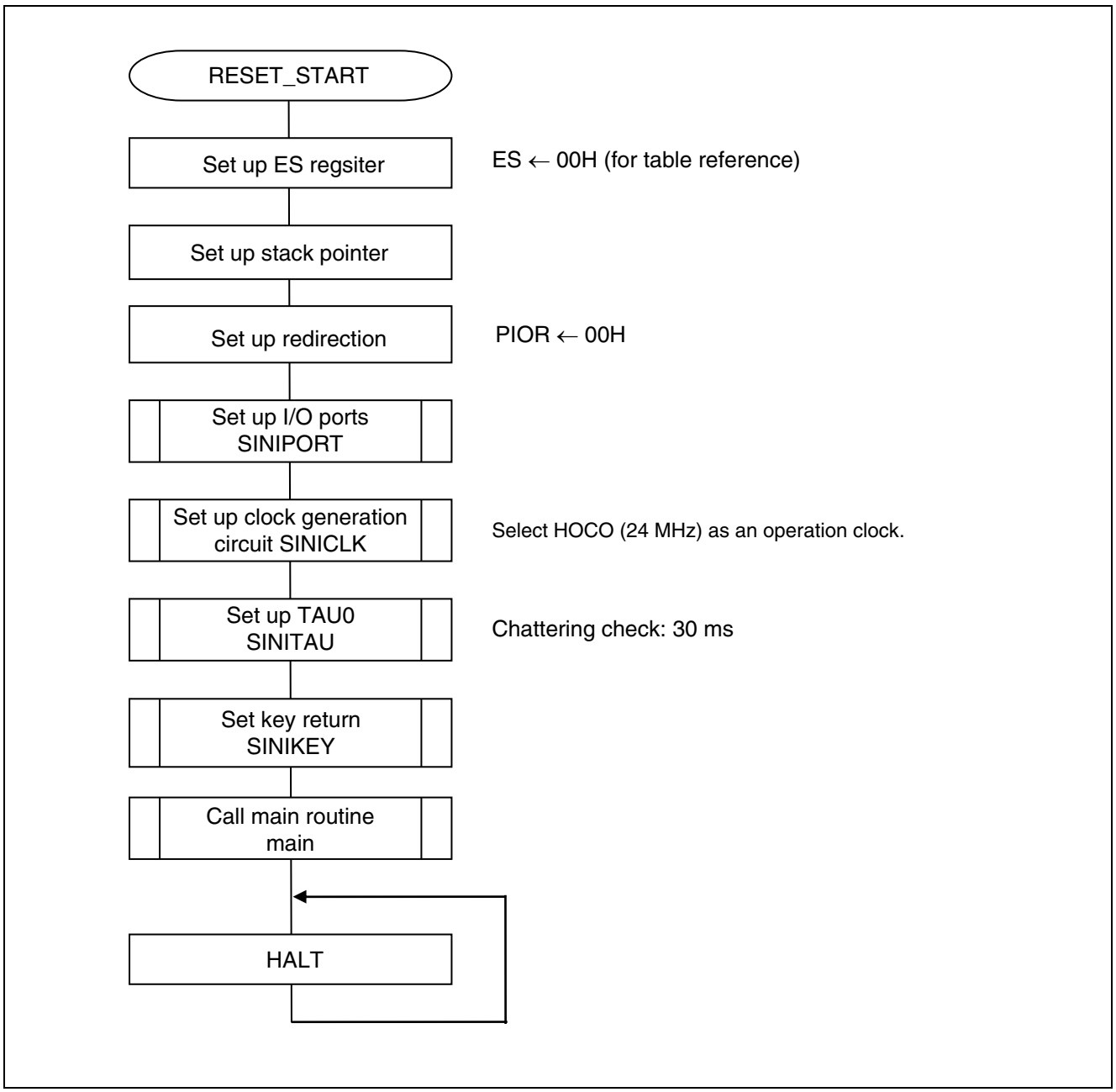

Figure 5.2 CPU Initialization Function

5.5.2 I/O Port Setup

Figure 5.3 shows the flowchart for setting up the I/O port.

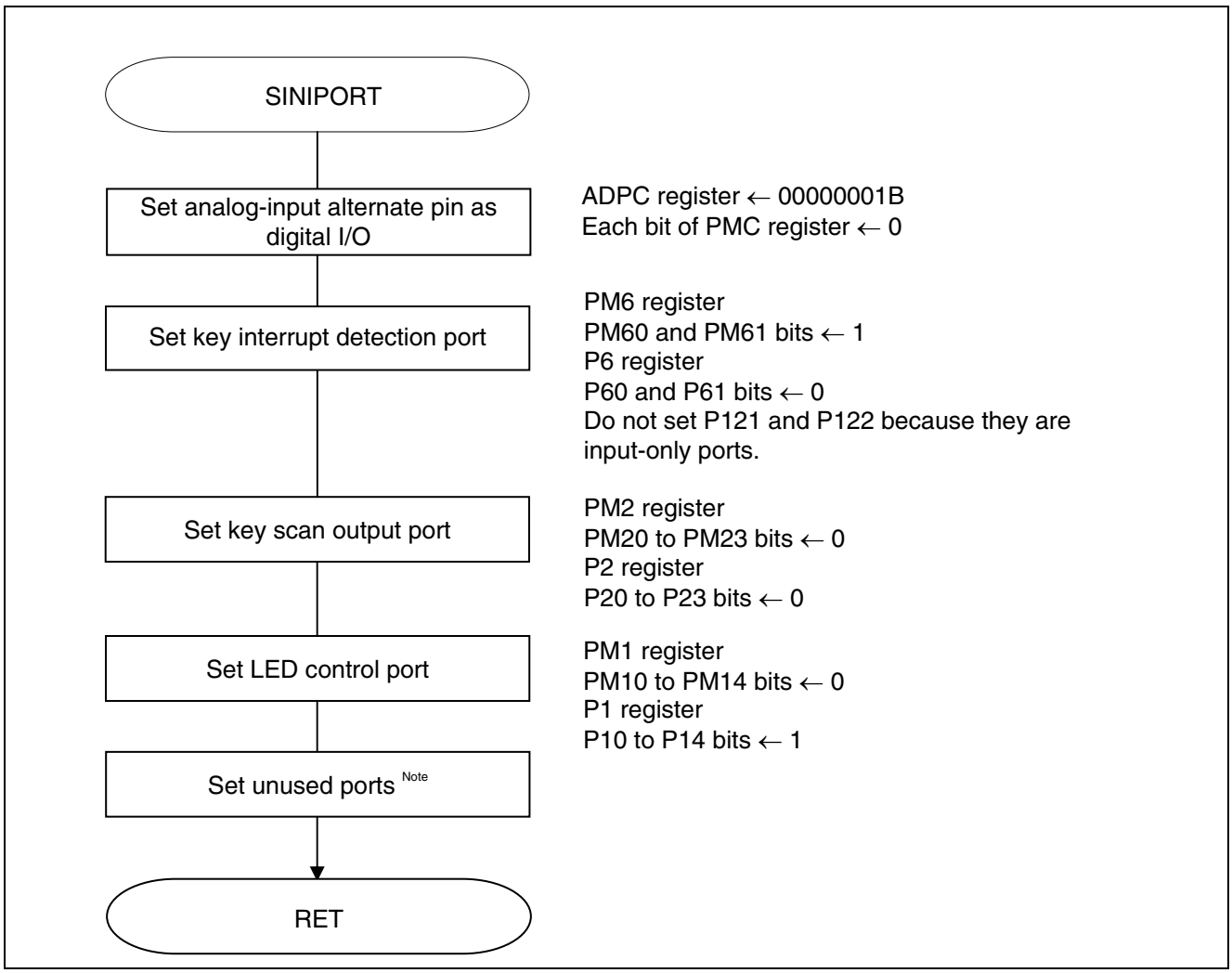

Figure 5.3 I/O Port Setup

Note For the configuration of the unused ports, refer to RL78/G12 User's Manual: Hardware.

Caution Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

Key Interrupt Input Pin Setting

- Port mode register (PM7)
  Set to input mode the pins with which key interrupt is to be used.

Symbol: PM6

7	6	5	4	3	2	1	0
1	1	1	1	1	1	PM61	PM60
1	1	1	1	1	1	**1**	**1**

Bits 1 and 0

PM6n	P6n pin I/O mode selection (n = 0 and 1)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Caution For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

5.5.3 Clock Generation Circuit Setup

Figure 5.4 shows the flowchart for setting up the clock generation circuit.

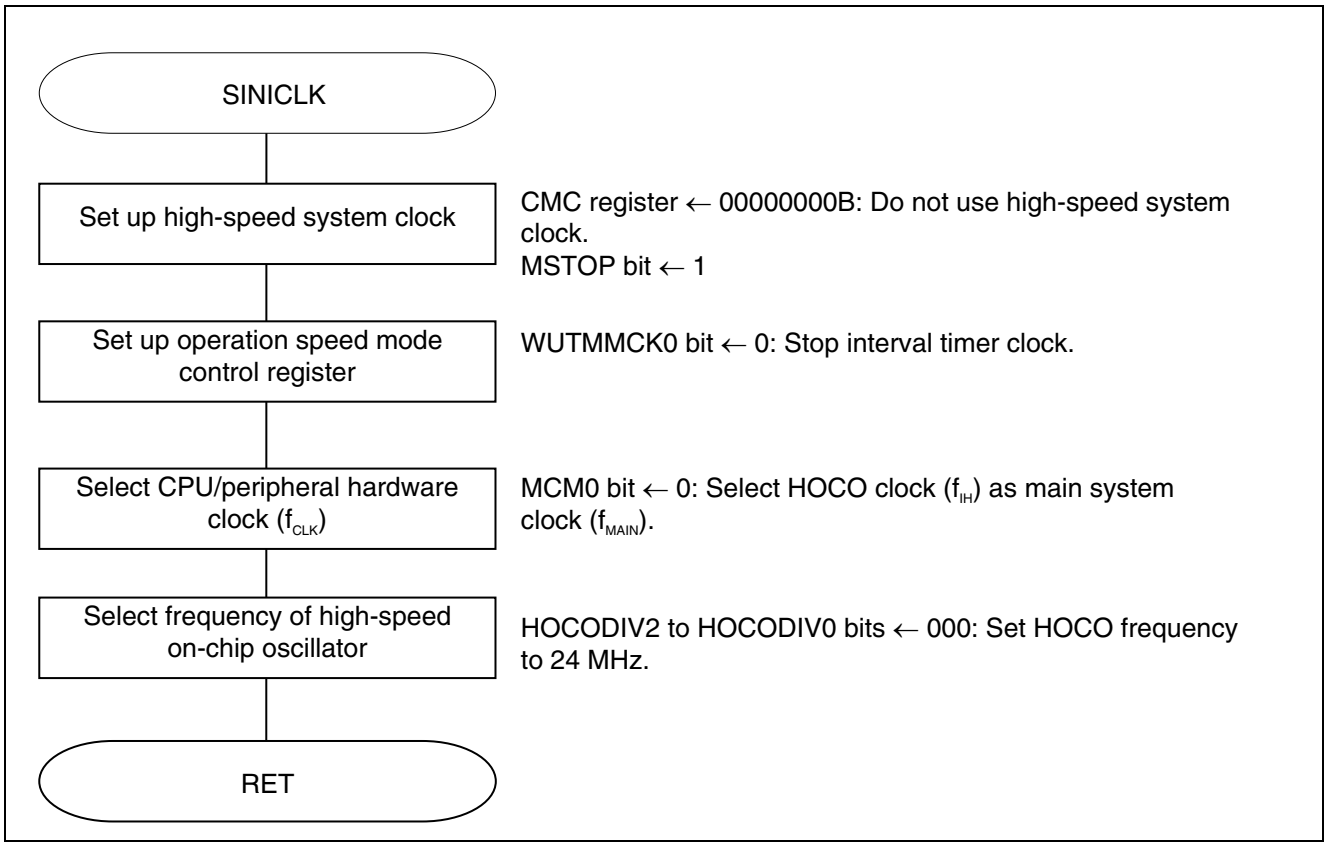

Figure 5.4 Clock Generation Circuit Setup

Caution For details on the procedure for setting up the clock generation circuit (SINICLK), refer to the section entitled "Flowcharts" in RL78/G12 Initialization Application Note (R01AN1030E).

5.5.4 Timer Array Unit Setup

Figure 5.5 shows the flowchart for setting up the timer array unit.

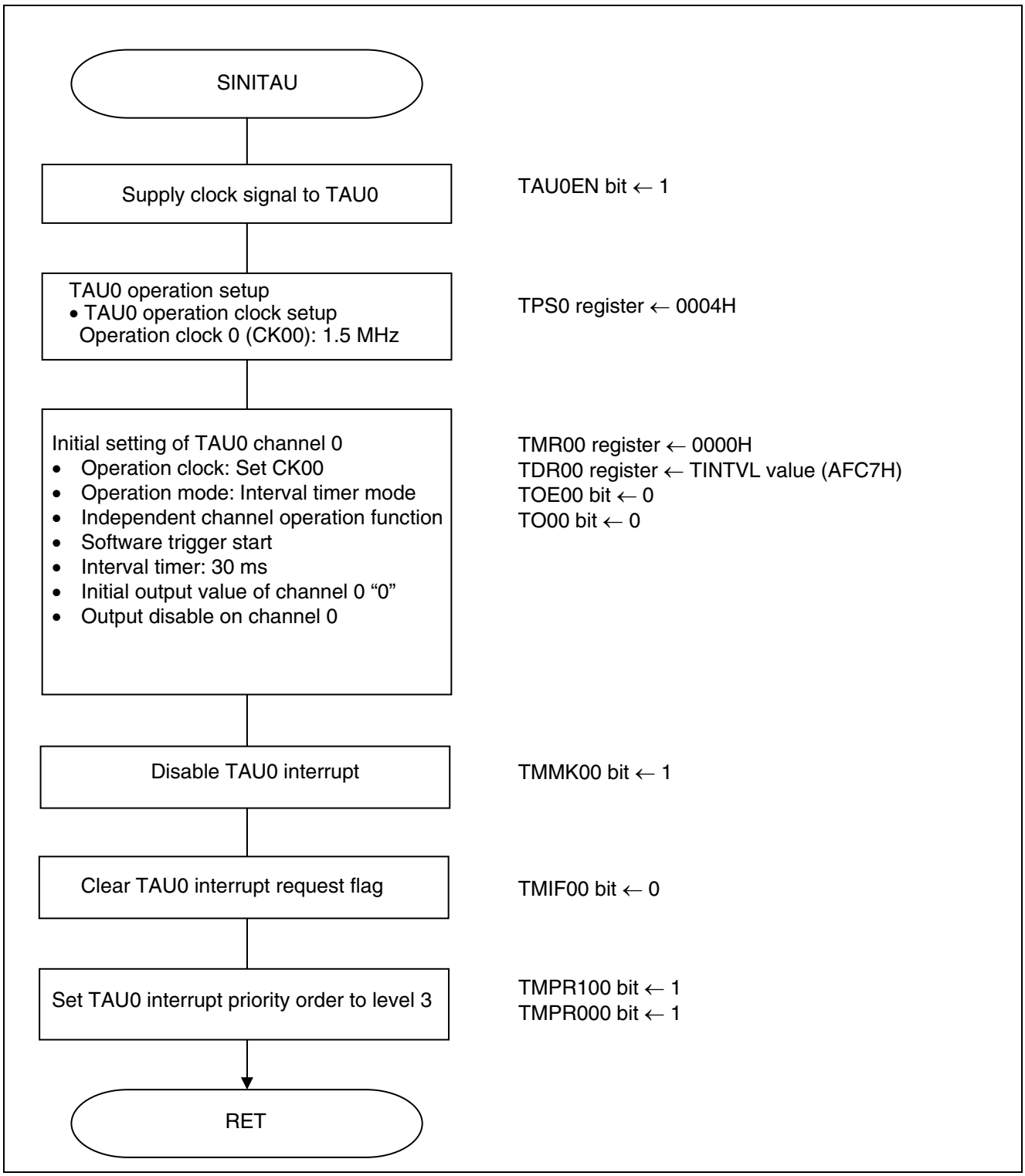

Figure 5.5 Timer Array Unit Setup

5.5.5 Key Interrupt Setup

Figure 5.6 shows the flowchart for setting up key interrupt.

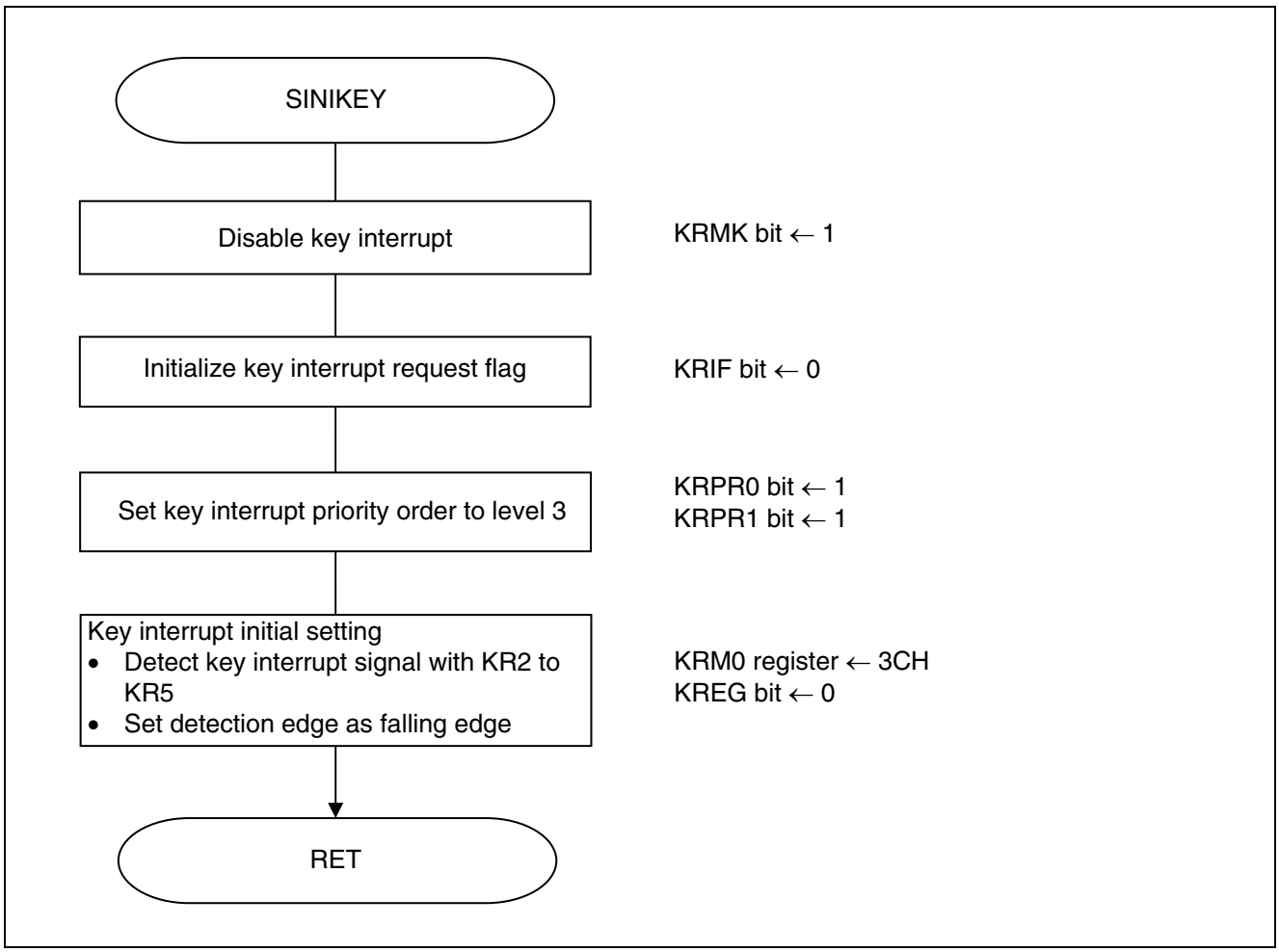

Figure 5.6 Key Interrupt Setup

Key Interrupt Setup

- Interrupt request flag register (IF1L)
  Clear interrupt request flag.
- Interrupt mask flag register (MK1L)
  Clear interrupt mask
- Priority specification flag registers (PR01L and PR11L)
  Select level 3 (low priority)
- Key return mode registers (KRM0 and KRM1)
  Detect key interrupt signal of the pins to be used.
- Key return control register (KRCTL)
  Set the usage of the key interrupt flags (KRF0 to KRF5) and the detection edge.

Symbol: IF1L

7	6	5	4	3	2	1	0
0	FLIL	MDIF	KRIF	TMKAIF	ADIF	TMIF03	TMIF02
0	x	x	**0**	x	x	x	x

Bit 4

KRIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK1L

7	6	5	4	3	2	1	0
1	FLMK	MDMK	KRMK	TMKAMK	ADMK	TMMK03	TMMK02
1	x	x	**1**	x	x	x	x

Bit 4

KRMK	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Caution For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Symbol: PR01L

7	6	5	4	3	2	1	0
1	FLPR0	MDPR0	KRPR0	TMKAPR0	ADPR0	TMPR003	TMPR002
x	x	x	**1**	x	x	x	x

Symbol: PR11L

7	6	5	4	3	2	1	0
1	FLPR1	MDPR1	KRPR1	TMKAPR1	ADPR1	TMPR103	TMPR102
x	x	x	**1**	x	x	x	x

Bit 4

KRPR1	KRPR0	Priority level selection
0	0	Specifying level 0 (high priority)
0	1	Specifying level 1
1	0	Specifying level 2
1	**1**	**Specifying level 3 (low priority)**

20-pin products

Symbol: KRM0

7	6	5	4	3	2	1	0
0	0	KRM05	KRM04	KRM03	KRM02	KRM01	KRM00
0	0	**1**	**1**	**1**	**1**	x	x

Bits 5 to 2

KRM0n	Key interrupt mode control (n = 2 to 5)
0	Does not detect key interrupt signal
1	**Detects key interrupt signal**

24-pin products

Symbol: KRM0

7	6	5	4	3	2	1	0
KRM07	KRM06	KRM05	KRM04	KRM03	KRM02	KRM01	KRM00
x	x	**1**	**1**	**1**	**1**	x	x

Bits 5 to 2

KRM0n	Key interrupt mode control (n = 2 to 5)
0	Does not detect key interrupt signal
1	**Detects key interrupt signal**

Symbol: KRM1

7	6	5	4	3	2	1	0
0	0	0	0	0	0	KRM09	KRM08
0	0	0	0	0	0	x	x

Symbol: KRCTL

7	6	5	4	3	2	1	0
KRMD	0	0	0	0	0	0	KREG
x	0	0	0	0	0	0	**0**

Bit 0

KREG	Selection of detection edge (KR0 to KR9)
0	**Falling edge**
1	Rising edge

Cautions 1 When setting the desired bits of the KRM00 to KRM09 bits to 1, pull up the relevant input pins to V_{DD} by an external resistor. Concerning KR1 and KR6 to KR9, the internal pull-up resistor can be used by setting the relevant bits to 1 in the key interrupt input pins PU125 and PU00 to PU03 (pull-up resistor registers 12 and 0 (the bit 5 of PU12 and bits 0 to 3 of PU0)).

2 For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

5.5.6 Main Processing

Figures 5.7 and 5.8 show the flowcharts for the main processing (1/2) and (2/2), respectively.

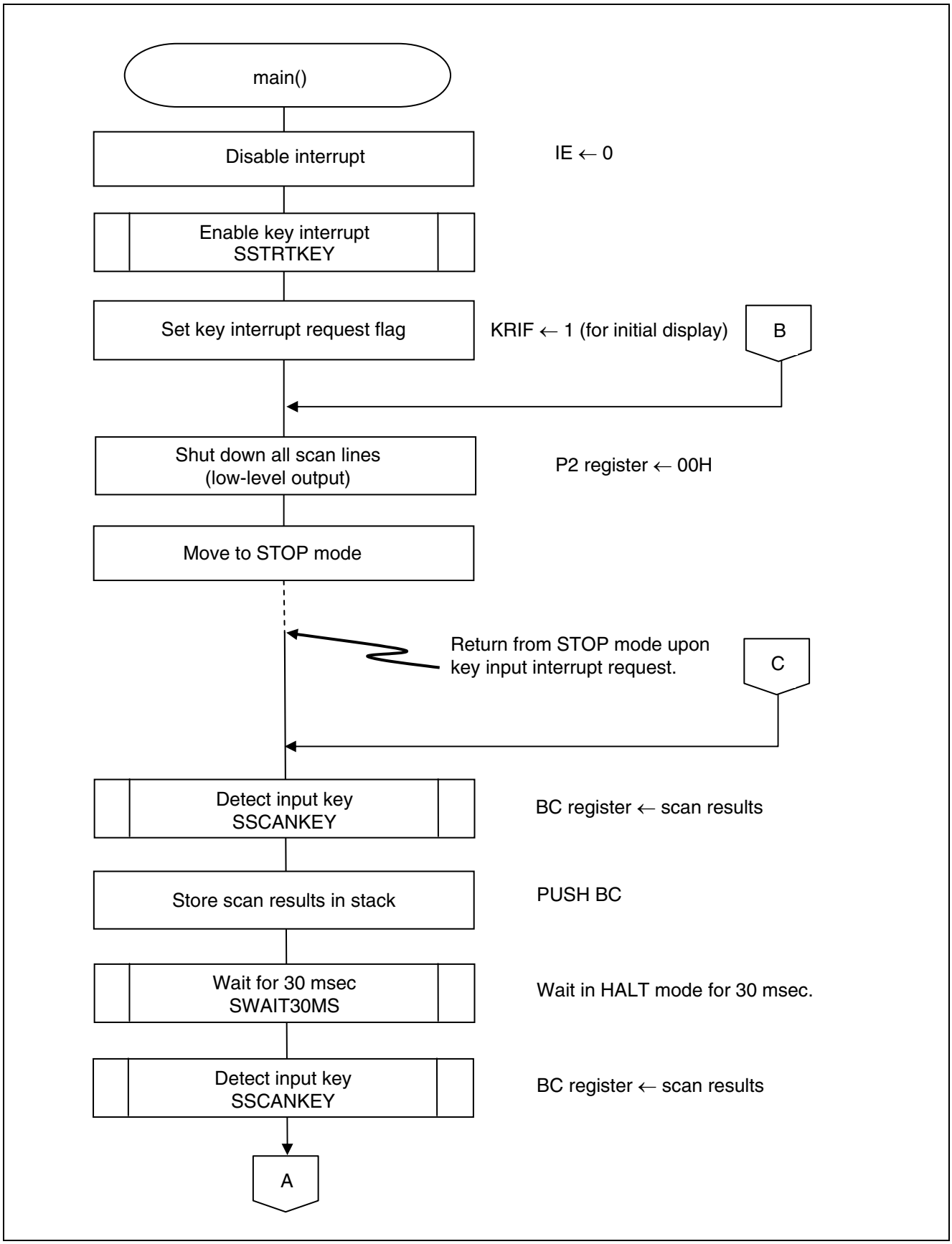

Figure 5.7 Main Processing (1/2)

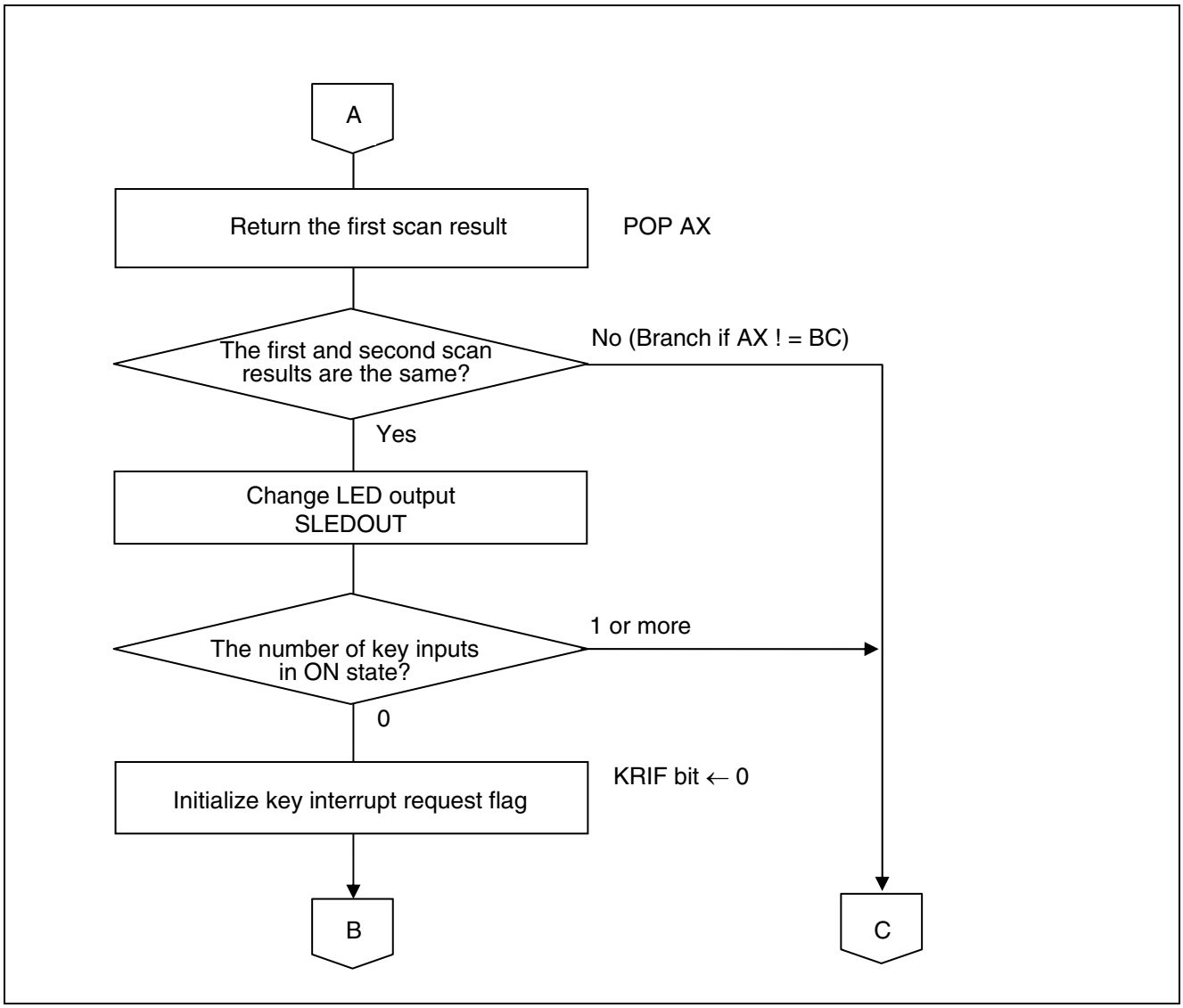

Figure 5.8 Main Processing (2/2)

5.5.7 30-msec Wait Processing

Figure 5.9 shows the flowchart for 30-msec wait processing.

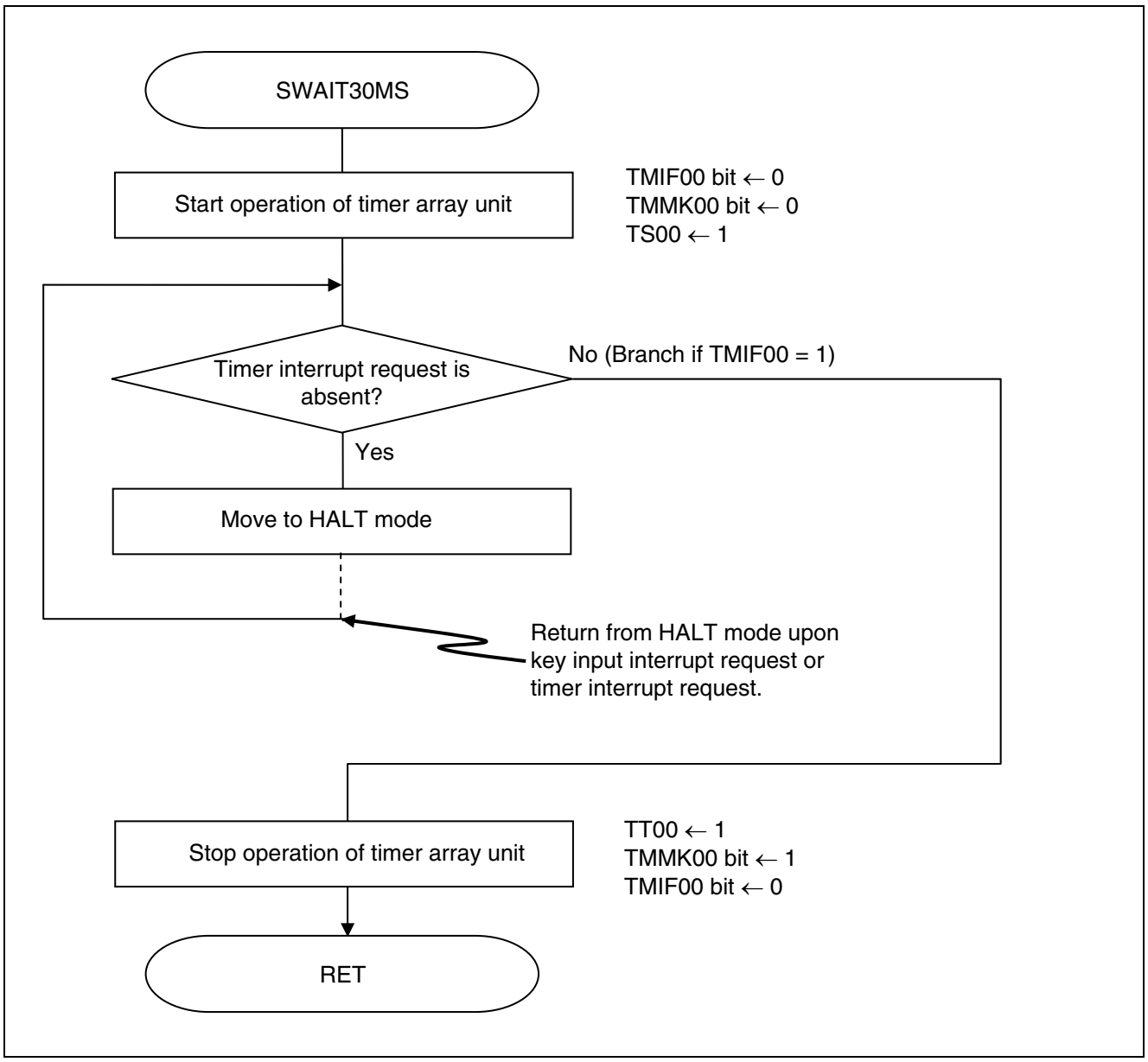

Figure 5.9 30-msec Wait Processing

5.5.8 Enabling Key Interrupt

Figure 5.10 shows the flowchart for enabling key interrupt.

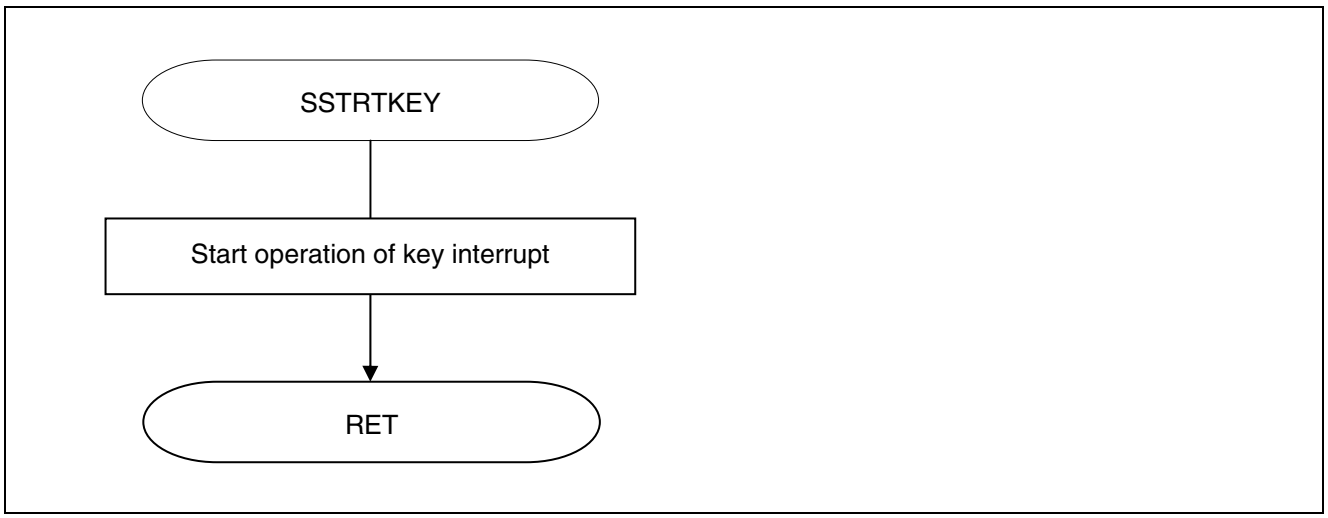

Figure 5.10 Enabling Key Interrupt

5.5.9 Detecting Input Key

Figures 5.11 and 5.12 show the flowcharts for detecting input key (1/2) and (2/2), respectively.

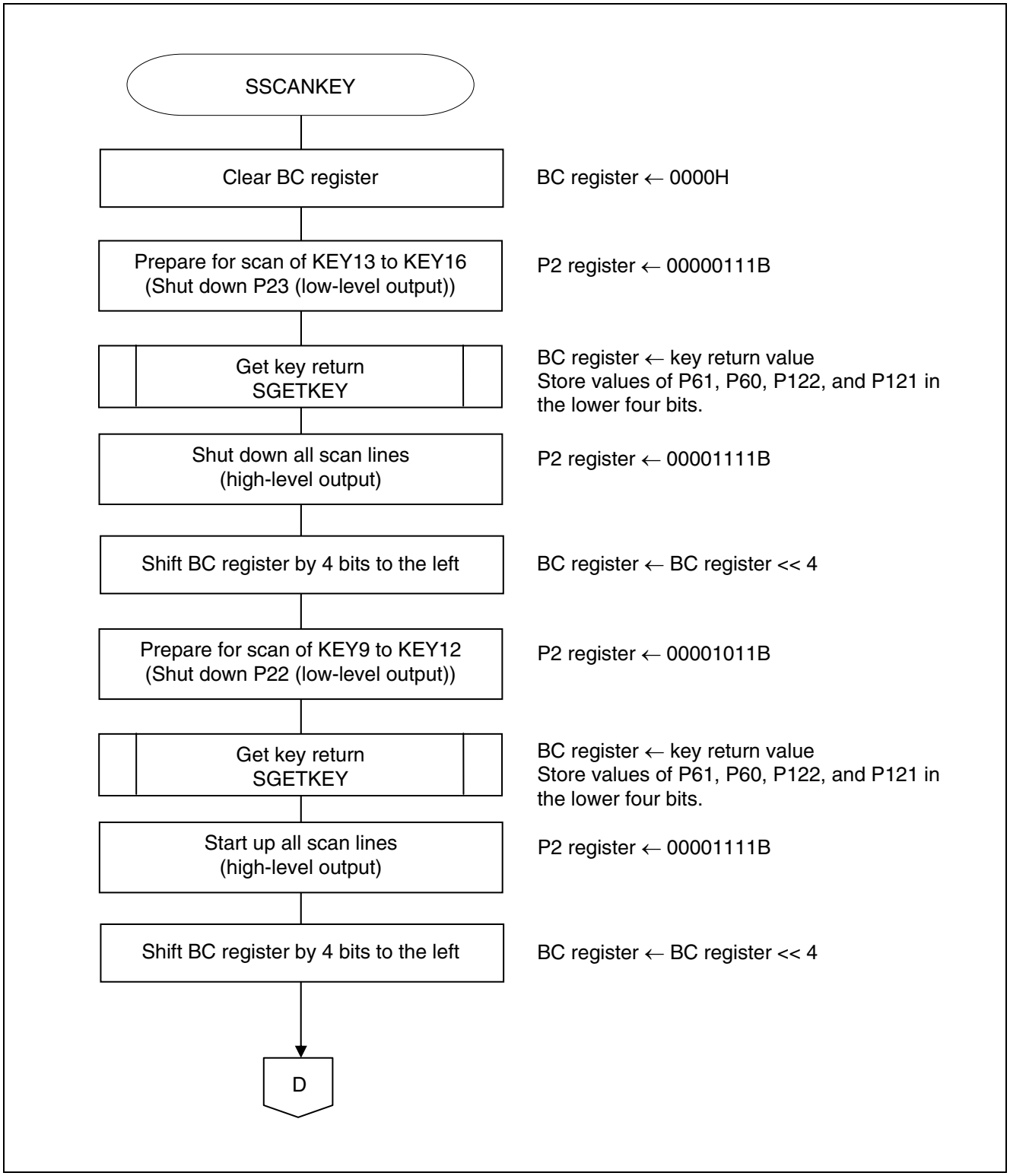

Figure 5.11 Detecting Input Key (1/2)

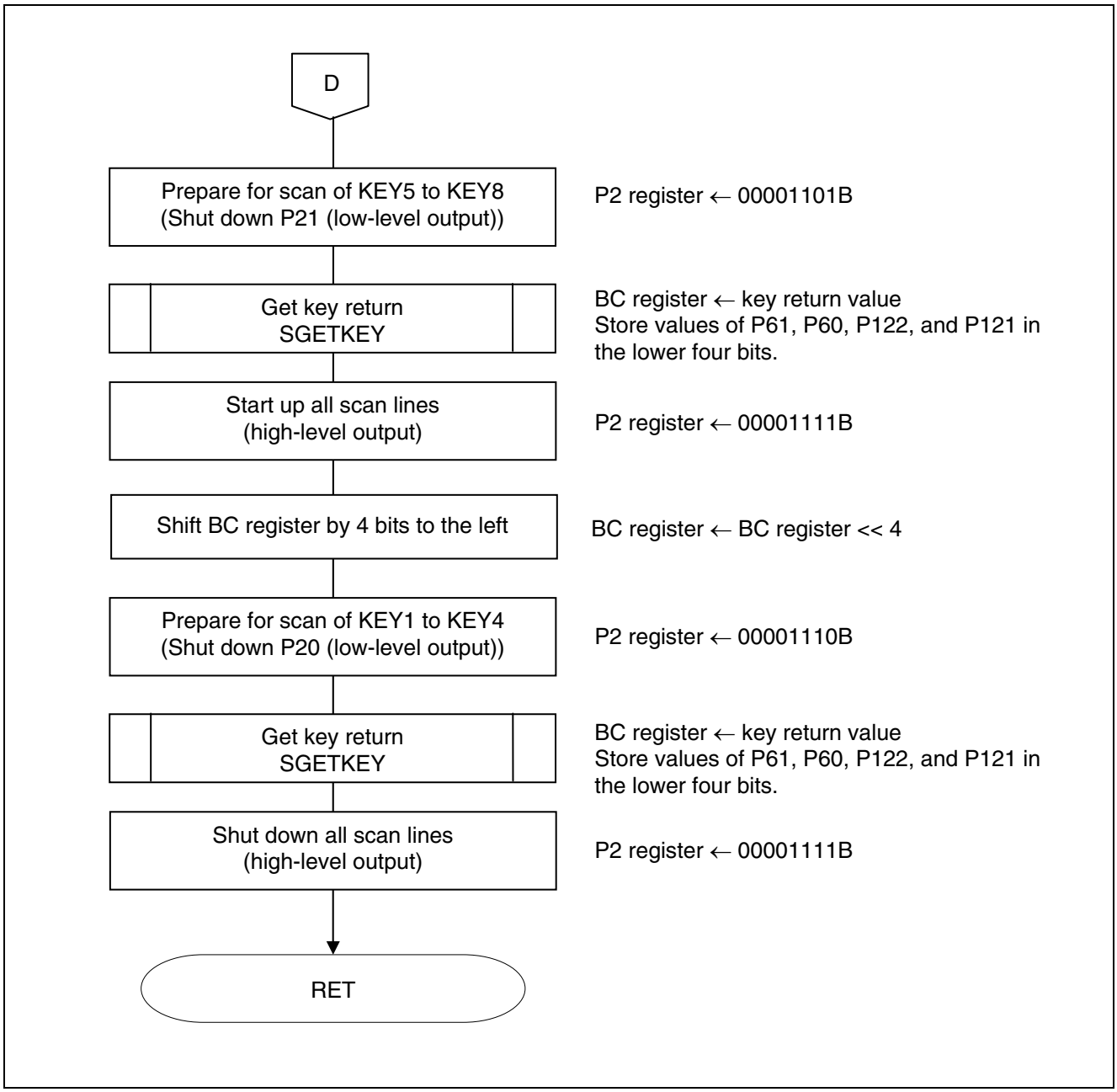

Figure 5.12 Detecting Input Key (2/2)

5.5.10 Getting Key Return

Figure 5.13 shows the flowchart for getting key return.

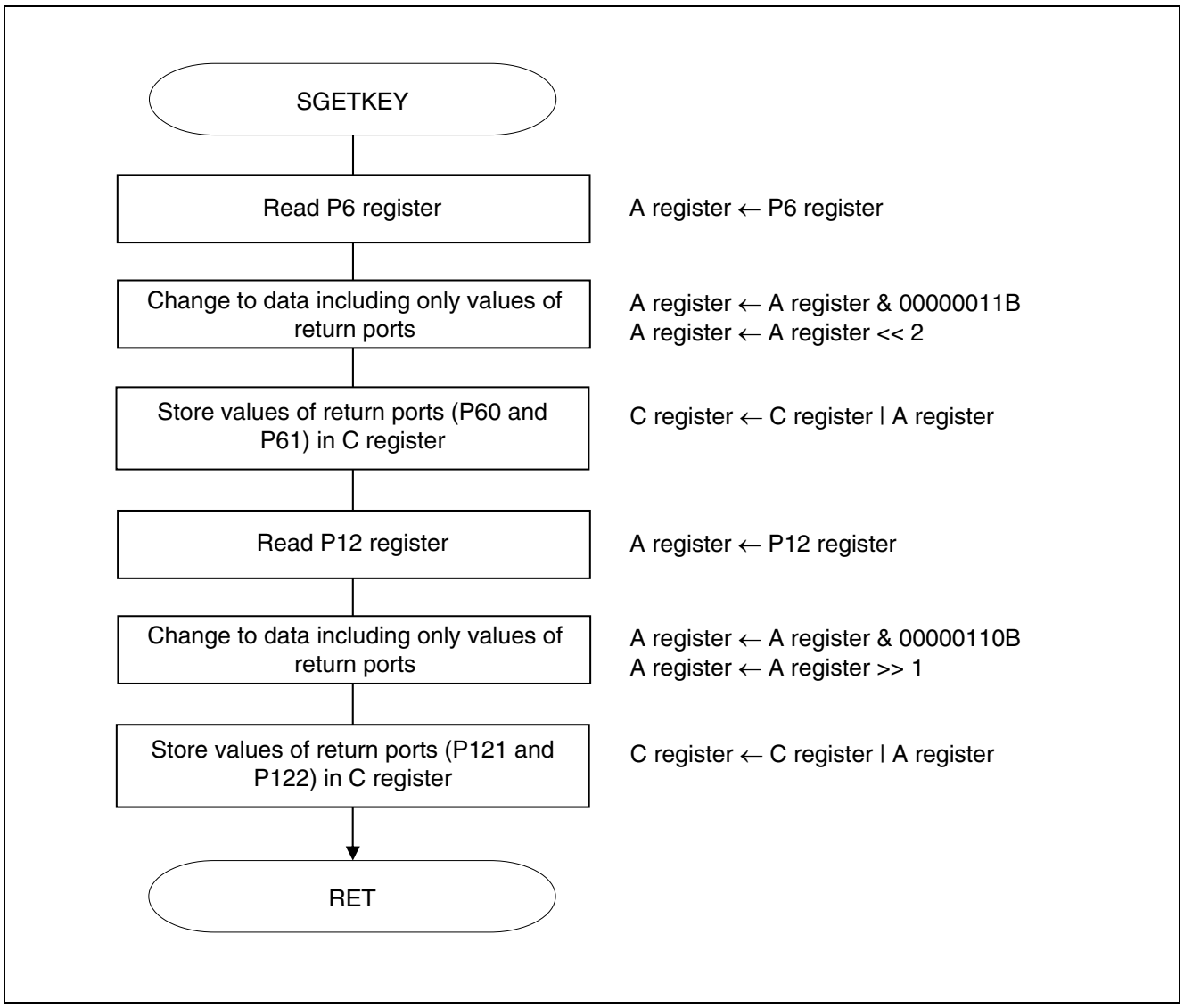

Figure 5.13 Getting Key Interrupt

5.5.11 Changing LED Output

Figures 5.14 and 5.15 show the flowcharts for changing LED output (1/2) and (2/2), respectively.

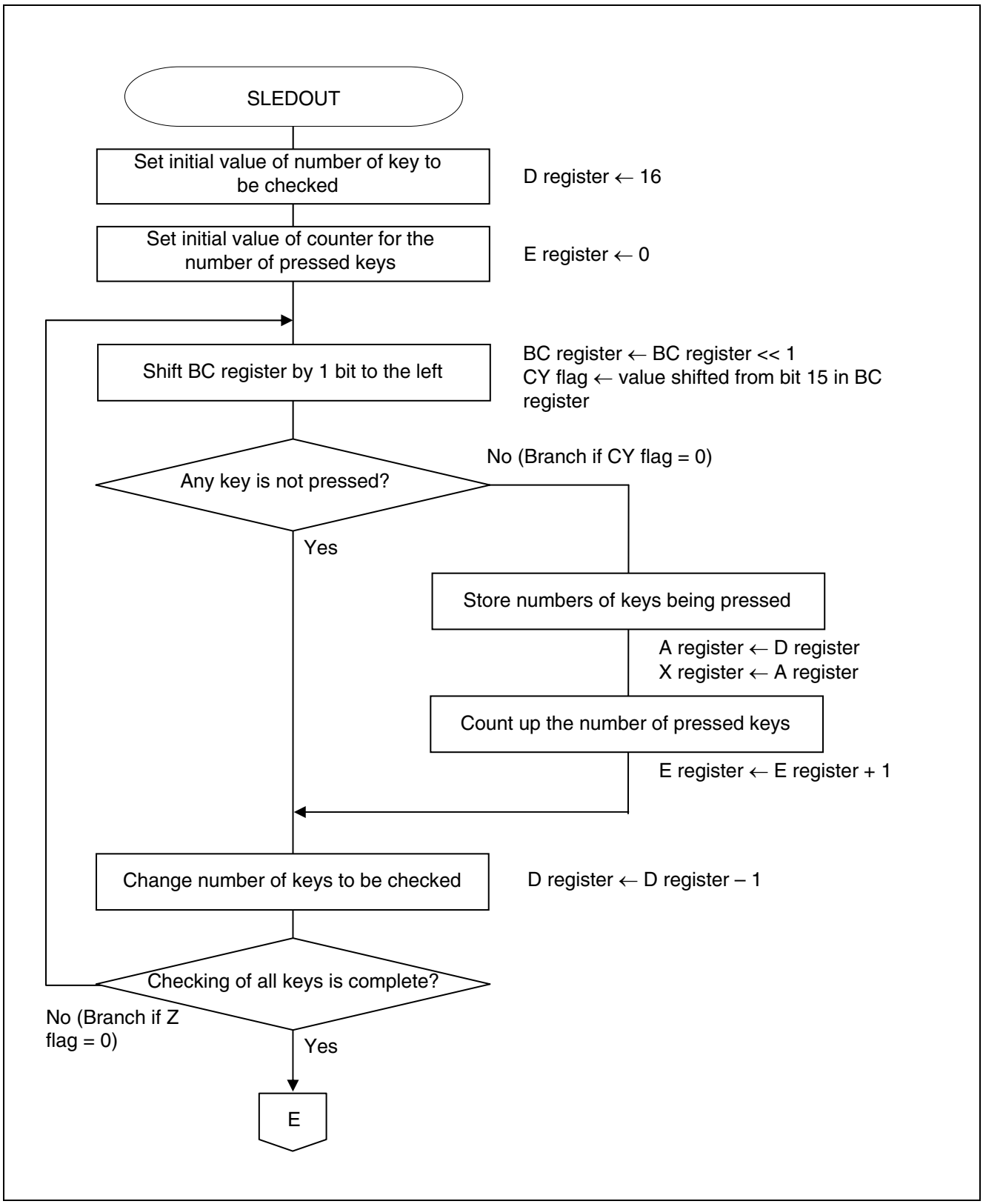

Figure 5.14 Changing LED Output (1/2)

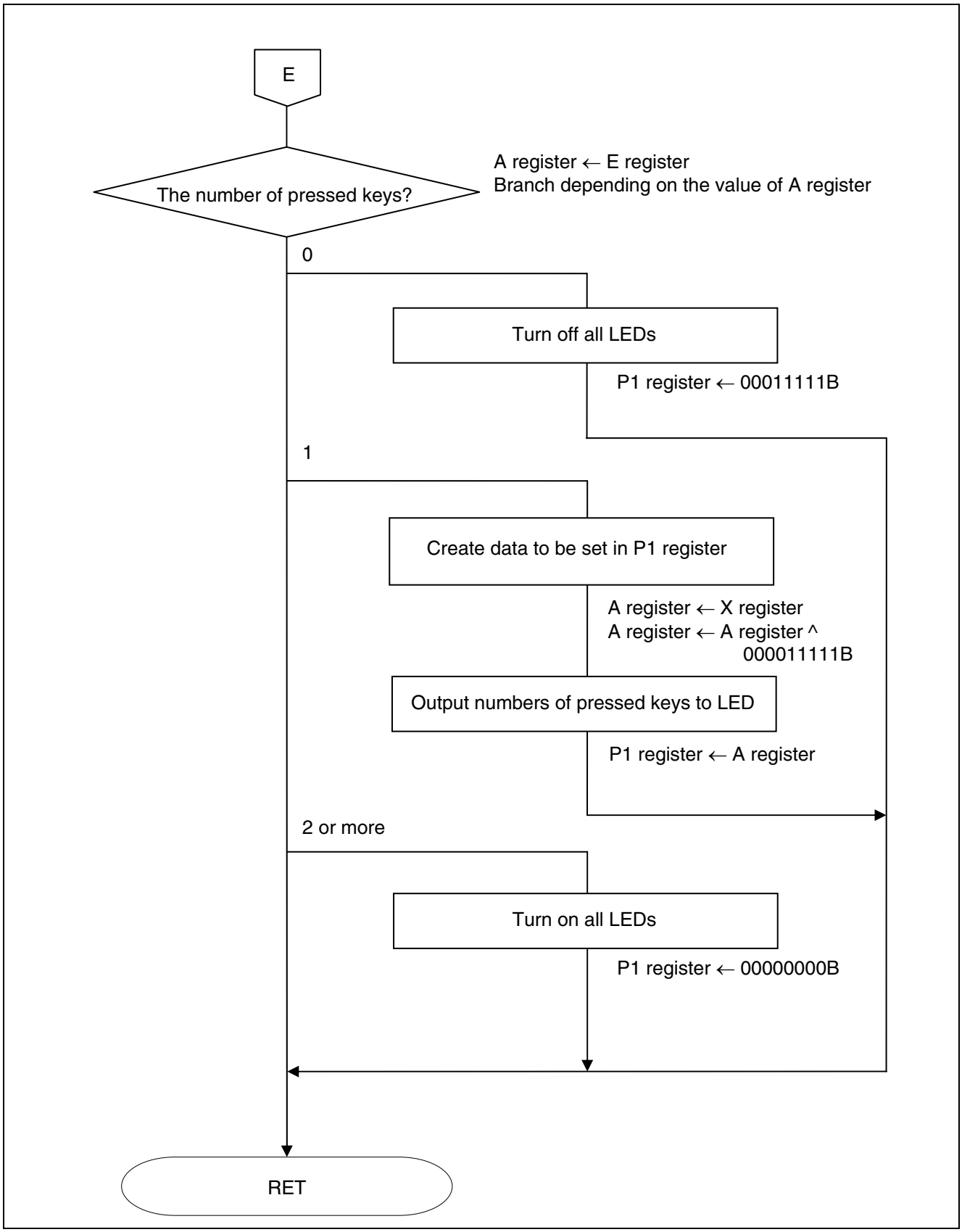

Figure 5.15 Changing LED Output (2/2)

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G12 User's Manual: Hardware (R01UH0200E)

RL78 Family User's Manual: Software (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

Website and Support

Renesas Electronics Website

- http://www.renesas.com/index.jsp

Inquiries

- http://www.renesas.com/contact/

Revision Record	RL78/G12 Key Interrupt Function

Rev.	Date	Description	
		Page	Summary
1.00	Aug 28, 2013	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to a product with a different type number, confirm that the change will not lead to problems.
   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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