R01AN3618EJ0100
Rev. 1.00
Feb. 03, 2017

RL78/G11

Forced Stop of PWM Output through Comparator and External Interrupts IAR

Introduction

This application note describes how to forcibly stop the PWM output from the timer KB0 without CPU intervention, by using the comparator feature and external interrupt requests.

Target Device

RL78/G11

When applying this application note to other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

1.1 Forced Stop of PWM Output through Comparator and External Interrupts

Upon detection of the over-current or over-voltage state, 16-bit timer KB0 output is fixed to the low level without CPU intervention.

Table 1.1 Peripheral Functions Used and their Usage

Peripheral Function	Usage
16-bit timer KB0 (hereinafter called KB0)	PWM output
External interrupt INTP11	Trigger for restart
External interrupt INTP10	Trigger for forced stop of PWM output
Programmable gain amplifier (hereinafter called PGA)	Amplifies input potential difference
Comparator 0 (hereinafter called CMP0)	Compares output stop voltages
TM00 in timer array unit (hereinafter called TAU)	Generates main period (10 ms)

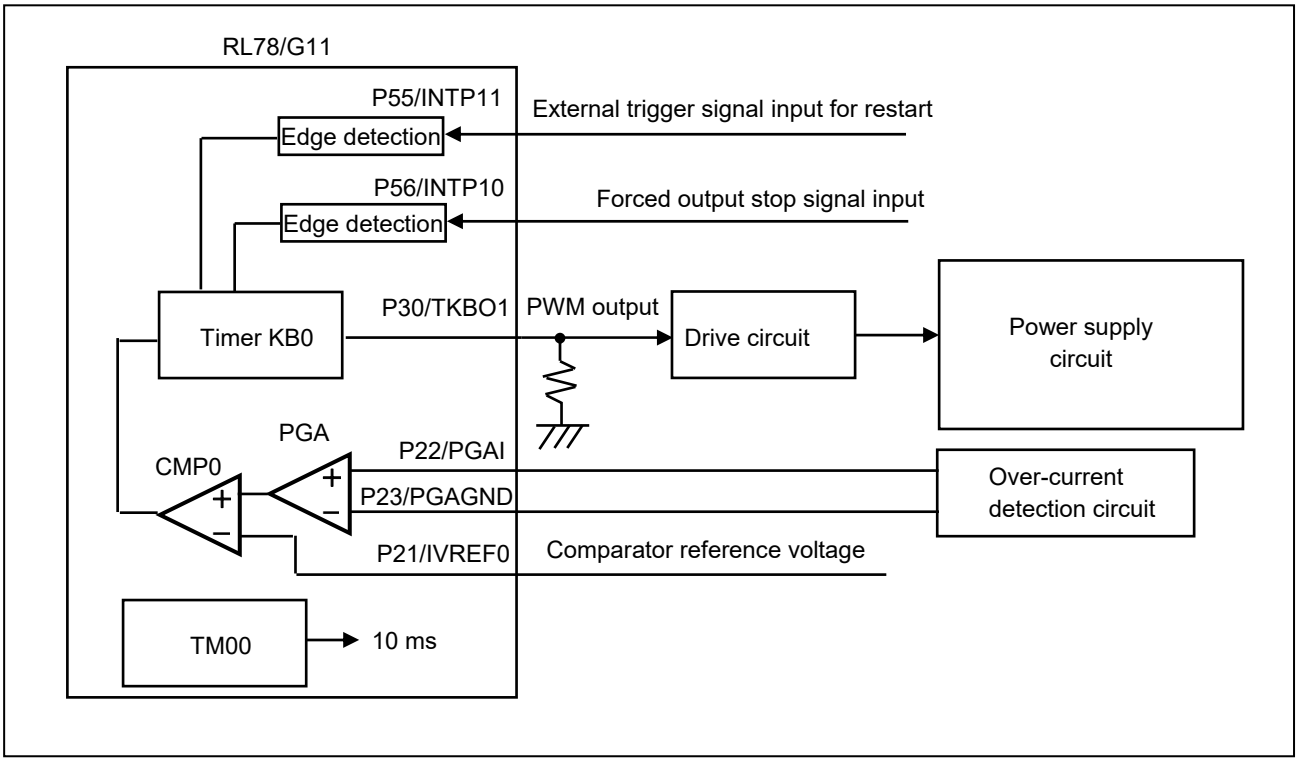

Figure 1.1 Basic Configuration

1.2 Over-Current/Over-Voltage Detection

The voltage output from the over-current detection circuit (circuit for converting current to voltage) is amplified eight times by the PGA. By comparing the resulting voltage with the comparator reference voltage, which is input to CMP0, the over-current is detected.

The over-current is specifically detected at the rising edge of the forced output stop signal, which is input to INTP10.

1.2.1 Over-Current Detection Method

Insert a resistor in series on the ground side of a load. By measuring the potential difference between the both ends of the resistor, a current flowing through the load can be measured.

Select the resistor with the minimum resistance value possible to reduce the influence on the load. However, since the resistor with a small resistance value can produce only a small potential difference, the potential difference is amplified by the PGA in this application note.

For example, with power source of 12-V output voltage and 350-mA output current, the over-current state is assumed when the output current exceeds 500 mA. To hold the resistor influence on the load to 1% or less, the resistance value of the resistor for measuring the current is set to 0.2 Ω to detect 500-mA output current. In this case, if the potential difference between the both ends of the resistor exceeds 0.1 V, the over-current state is determined.

The following summarizes the characteristics of the PGA incorporated into the RL78/G11.

- Input offset voltage: ±10 mA (MAX)
- Gain error: ±1% (for ×4 or ×8), ±1.5% (for ×16), ±2% (for ×12)
- Input voltage range: 0 V to 0.9 V_{DD}/gain

The input offset voltage refers to the input voltage error. This error is amplified by the PGA.

For example, when the input offset voltage ±10 mV is added to the input voltage 0.1 V, the resulting input voltage is 0.09 V to 0.11 V. Here, this input voltage is within the specified input voltage range of the PGA. (Since the lower limit of the power supply voltage is 2.7 V in this application note, 0.9 V_{DD} /gain = 0.9 × min. 2.7/8 = 0.3 V.)

Since the PGA gain is x8, the CMP0 input voltage range is from 0.72 V to 0.88 V.

The voltage to be input to the IVREF0 pin of the CMP0 is 0.72 V. Here, this input voltage is within the specified input voltage range of the IVREF0 pin.

In the above case, the influence caused by the PGA input offset voltage is approximately ±10% maximum. The detected current may include an error of ±10% maximum. If this error is not allowed in the application, add the corrective measures to hold down the input offset voltage influence.

For example, input the reference voltage to the PGA, and measure its PGA output (PGAOUT) by using the A/D converter incorporated in the RL78/G11. According to the result, adjust the input voltage to the minus pin of the CPM0 (comparator reference voltage) so that the input offset voltage influence be reduced. Note that with the RL78/G11, the on-chip D/A converter output can be used as the comparator reference voltage.

1.2.2 Over-Voltage Detection Method

In this application note, over-voltage is detected using the input signal to the INTP10 pin. When the INTP10 falling edge is detected, the TKBO1 output is fixed to the low level by using forced output stop function 2.

1.3 Conditions for Cancelling Forced Output Stop Function

In this application note, forced output stop functions 1 and 2 are used to detect over-current and over-voltage, respectively.

In over-current detection, the potential difference detected by the over-current detection circuit is multiplied eight times by the PGA and if the resulting voltage exceeds the comparator reference voltage (the input voltage to the IVREF0 pin), timer KB0 output (KBO1) is fixed to the low level through forced output stop function 1. Then, if 1 is written to the forced output stop function release trigger (TKBPAHTT01) while the above resulting voltage is lower than the comparator reference voltage (the input voltage to the IVREF0 pin), forced output stop function 1 is canceled at the next counter period.

If the INTP10 rising edge is detected, forced output stop function 2 is canceled at the next counter period.

2. Conditions for Confirming Operation

The sample code operations described in this application note are confirmed under the following conditions.

Table 2.1 Conditions for Confirming Operations

Item	Description
Microcontroller used	RL78/G11 (R5F1056A)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 24 MHz • CPU/peripheral hardware clock: 24 MHz
Operating voltage	3.3 V (can be operated from 2.7 V to 5.5 V) LVD operation (V_{LVD}): Reset mode; Voltage: 2.75 V
Integrated development environment (IAR)	IAR Embedded Workbench IDE V7.4.1.4268 from IAR Systems.
C compiler (IAR)	IAR C/C++ Compiler for Renesas RL78 V2.21.1.1833 from IAR Systems.

3. Related Application Notes

Refer to the following application notes as necessary, which are related to this application note.

RL78/G11 Forced Stop of PWM Output through Comparator and External Interrupts CC-RL (R01AN3477E) Application Note

4. Hardware Descriptions

4.1 Hardware Configuration Example

Figure 4.1 shows an example of hardware configuration described in this application note.

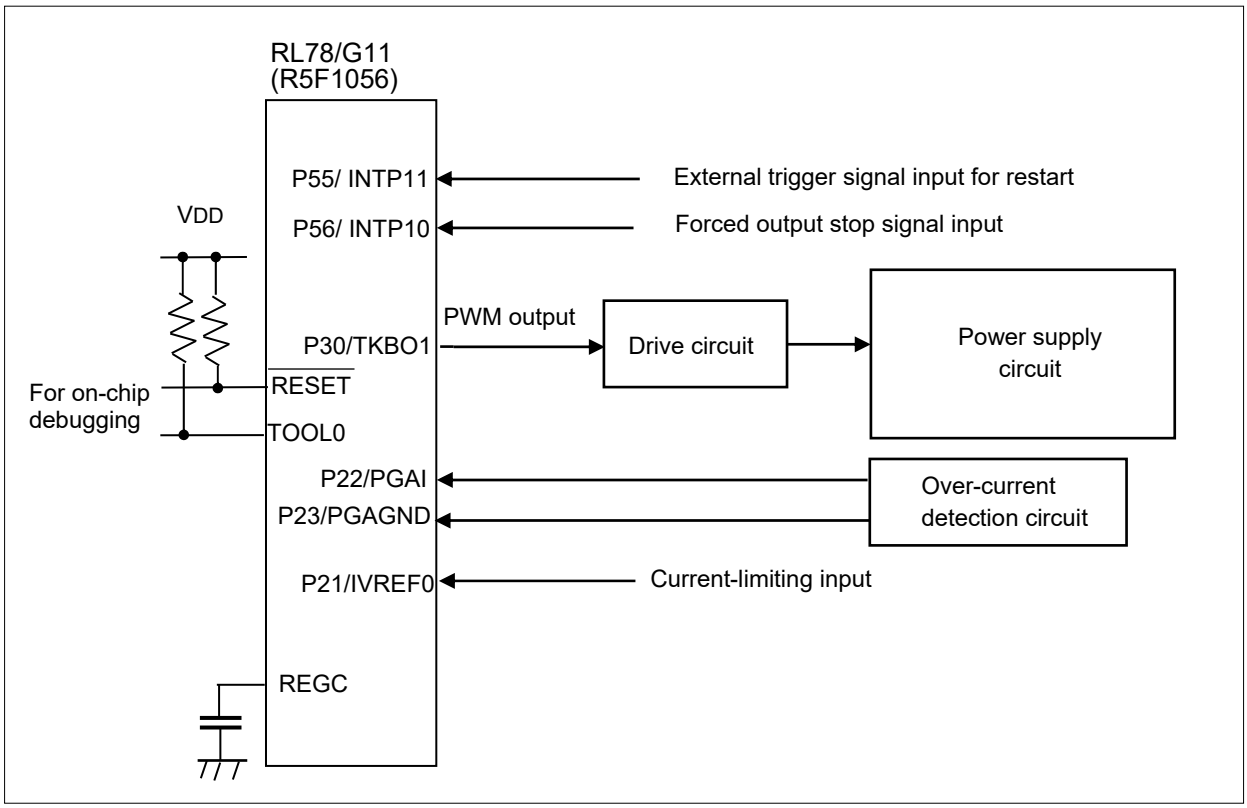

Figure 4.1 Hardware Configuration

Cautions 1 The above figure is a simplified circuit image for showing the outline of the connections. The actual circuit should be designed so that the pins are handled appropriately and that the electrical characteristics are satisfied (input-only ports should be each connected to V_{DD} or V_{SS} via a resistor).

2 Set V_{DD} to the reset-release voltage (V_{LVD}) specified by LVD or greater.

4.2 List of Pins Used

Table 4.1 lists the pins used and their functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
P30/ANI21/KR1/TI00/TO01/INTP3/SCK11/SCL11/ (TxD0)/PCLBUZ0/TKBO1/SDAA0	Output	PWM output
P55/KR3/SI00/RxD0/SDAA00/TOOLRXD/TI02/ TO02/INTP11/(VCOUT0)/SDAA1	Input	Triggers PWM waveform to be output again.
P56/ANI22/KR2/SCK00/SCL00/SO11/INTP10/ (TO03)/(INTFO)/SCLA1	Input	Forced output stop signal input
P22/ANI2/PGAI/IVCMP0	Input	Over-current detection (+)
P23/ANI3/ANO1/PGAGND	Input	Over-current detection (–)
P21/ANI1/AVEWFM/IVREF0	Input	Current–limiting input

5. Software Descriptions

5.1 Operation summary

This application note describes forced PWM output stop that uses the PGA, CMP0, TAU, timer KB0, and external interrupts.

As timer KB0 output, 100-kHz PWM is output by using TKBO1. The forced stop function is implemented using forced output stop functions 1 and 2.

Forced output stop function 1 is triggered by the rise of the CMP0 and sets TKBO1 output to the Hi-Z state; the function is cancelled by setting TKBPAHTT01 to 1 after the fall of the CMP0 and output can be enabled again at the next period.

Forced output stop function 2 is triggered by the detection of the INTP10 fall and fixes TKBO1 output to the low level; the function is cancelled at the period following the period in which the INTP10 input rises.

A 10-ms interval timer is provided for function extension using the TAU.

<TAU settings>

- Use channel 0 as an interval timer.
- Set the interval to 10 ms.

<PGA settings>

- Set GND of PGA to PGAGND.
- Set gain of PGA to x8.

<CMP0 settings>

- Set standard mode.
- Set the + pin input signal to PGA output, and - pin input signal to IVREF0.
- Select both-edge detection for edge detection setting.

<Timer KB0 settings>

- Set standalone mode.
- Set TKBO1 as an output pin, set the initial output level to the low level, and set the output level to active-high.
- Set the timer to be restarted by an external interrupt signal (INTP11) trigger.
- Set the PWM output period to 20 μs and duty to 50%.
- Set Hi-Z output for forced output stop function 1 and fixed low-level output for forced output stop function 2.
- Set CMP0 output and INTP10 output as the triggers of functions 1 and 2, respectively.
- Set type 4 as the operation mode of forced output stop function 1.
- Set type 2 as the operation mode of forced output stop function 2.

5.2 List of Option Byte Settings

Table 5.1 lists option byte settings.

Table 5.1 Option Byte Settings

Address	Setting	Address
000C0H	11101111B	Watchdog timer is stopped. (Counting stopped after a reset release)
000C1H	01111111B	LVD reset mode; 2.75 V (2.75 V to 2.81 V)
000C2H	11100000B	HS mode; high-speed on-chip oscillator: 24 MHz
000C3H	10000100B	On-chip debugging is enabled.

5.3 List of Functions

Table 5.2 lists the functions.

Table 5.2 Functions

Function Name	Summary
R_COMP0_Start	Process of starting CMP0 operation
R_PGA_Start	Process of starting PGA operation.
R_INTC10_Start	Process of starting external interrupt operation
R_TMR_KB0_Start	Process of starting timer KB0 operation
R_TAU0_Channel0_Start	Process of starting TAU0 channel 0 operation

5.4 Function Specifications

The following gives the specifications of the functions used in the sample code.

[Function name] R_ COMP0_Start

Summary	Process of starting CMP0 operation
Header	r_cg_comp.h, r_cg_userdefine.h
Declaration	void R_ COMP0_Start(void)
Description	Starts CMP0 operation.
Arguments	None
Return values	None
Remarks	None

[Function name] R_PGA_Start

Summary	Process of starting PGA operation
Header	r_cg_pga.h, r_cg_userdefine.h
Declaration	void R_ PGA_Start(void)
Description	Starts PGA operation.
Arguments	None
Return values	None
Remarks	None

[Function name] R_INTC10_Start

Summary	Process of starting external interrupt operation
Header	r_cg_intp.h, r_cg_userdefine.h
Declaration	void R_ INTC01_Stop(void)
Description	Starts external interrupt operation.
Arguments	None
Return values	None
Remarks	None

[Function name] R_TMR_KB0_Start

Summary	Process of starting timer KB operation
Header	r_cg_tmkb.h, r_cg_userdefine.h
Declaration	void R_TMR_KB0_Start (void)
Description	Starts timer KB operation.
Arguments	None
Return values	None
Remarks	None

[Function name] R_TAU0_Channel0_Start

Summary	Process of starting TAU0 channel 0 operation
Header	r_cg_tau.h, r_cg_userdefine.h
Declaration	void R_TAU0_Channel1_Start (void)
Description	Unmasks the interrupt mask of TAU0 channel 0.
Arguments	None
Return values	None
Remarks	None

5.5 Flowcharts

Figure 5.1 shows the overall flow of the process described in this application note.

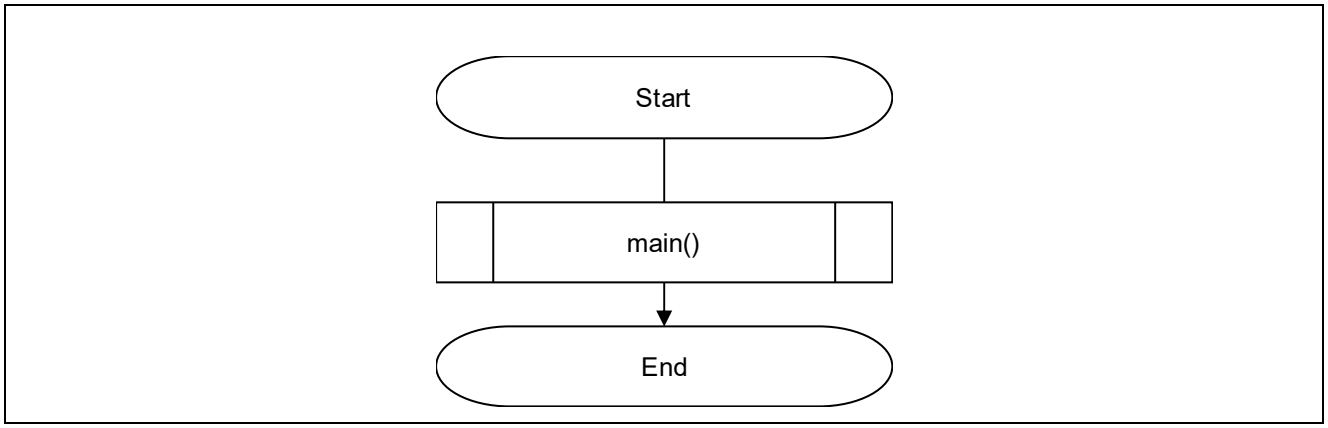

Figure 5.1 Overall Flow

Note: The start-up routine is executed before and after the initial setting function.

5.5.1 Initial Setting Function

Figure 5.2 shows the flowchart of the initial setting function.

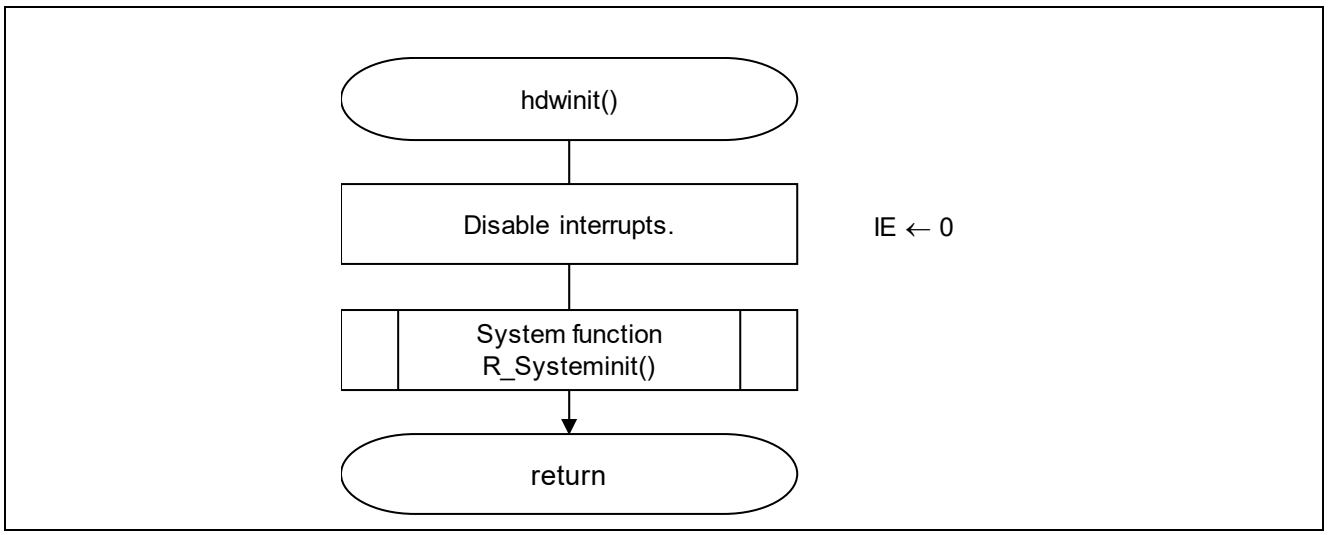

Figure 5.2 Initial Setting Function

5.5.2 System Function

Figure 5.3 shows the flowchart of the system function.

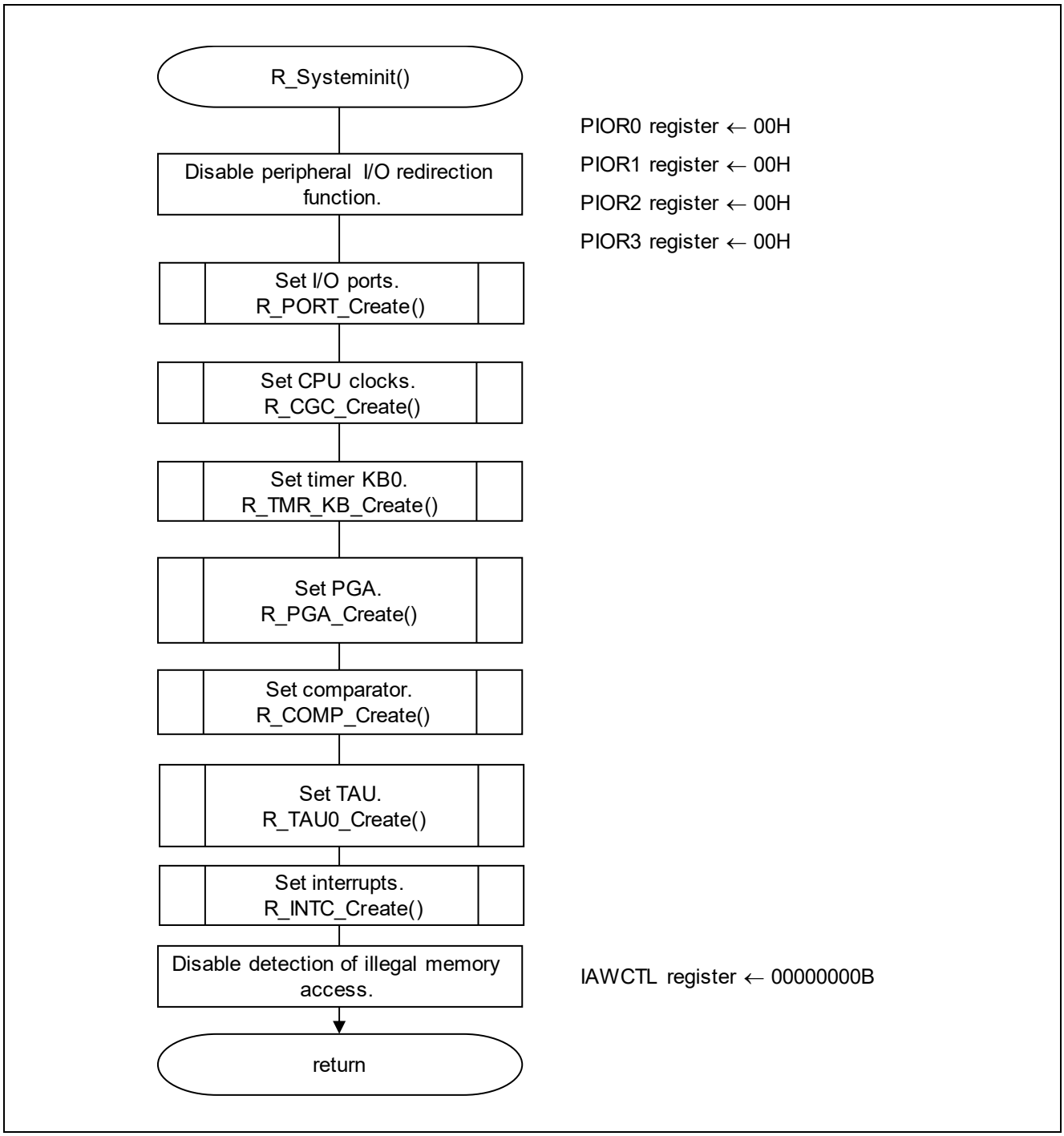

Figure 5.3 System Function

5.5.3 Setting I/O Ports

Figure 5.4 shows the flowchart for setting the I/O ports.

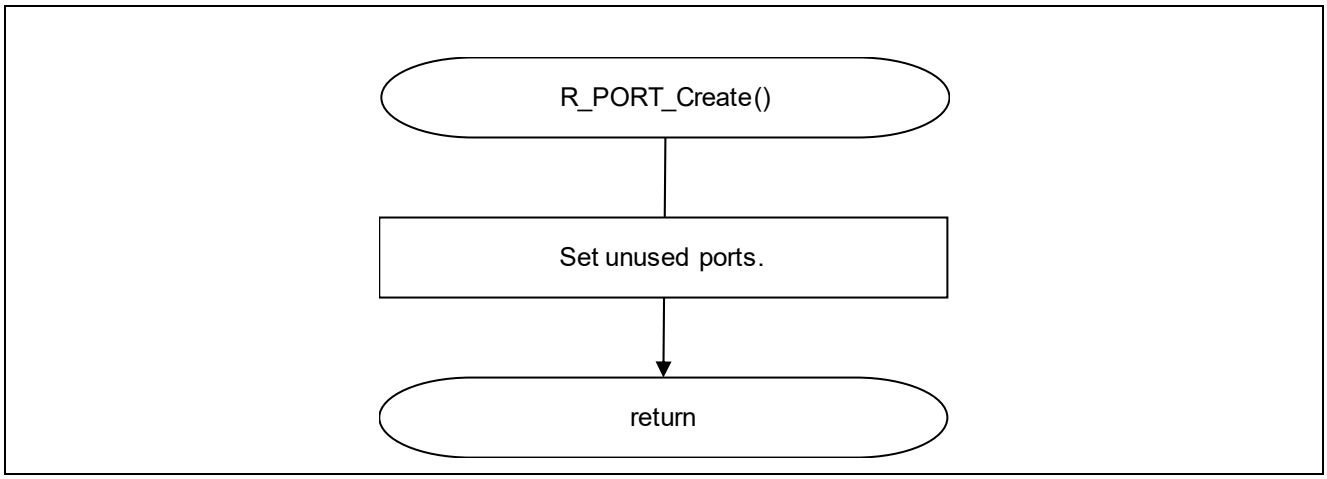

Figure 5.4 Setting I/O Ports

Note: For unused port settings, refer to the RL78/G11 User's Manual: Hardware.

Caution: Design unused ports so that the electrical characteristics are satisfied by appropriately treating the pertinent pins. Separately connect unused input-only ports to V_{DD} or V_{SS} via a resistor.

5.5.4 Setting CPU Clocks

Figure 5.5 shows the flowchart for setting the CPU clocks.

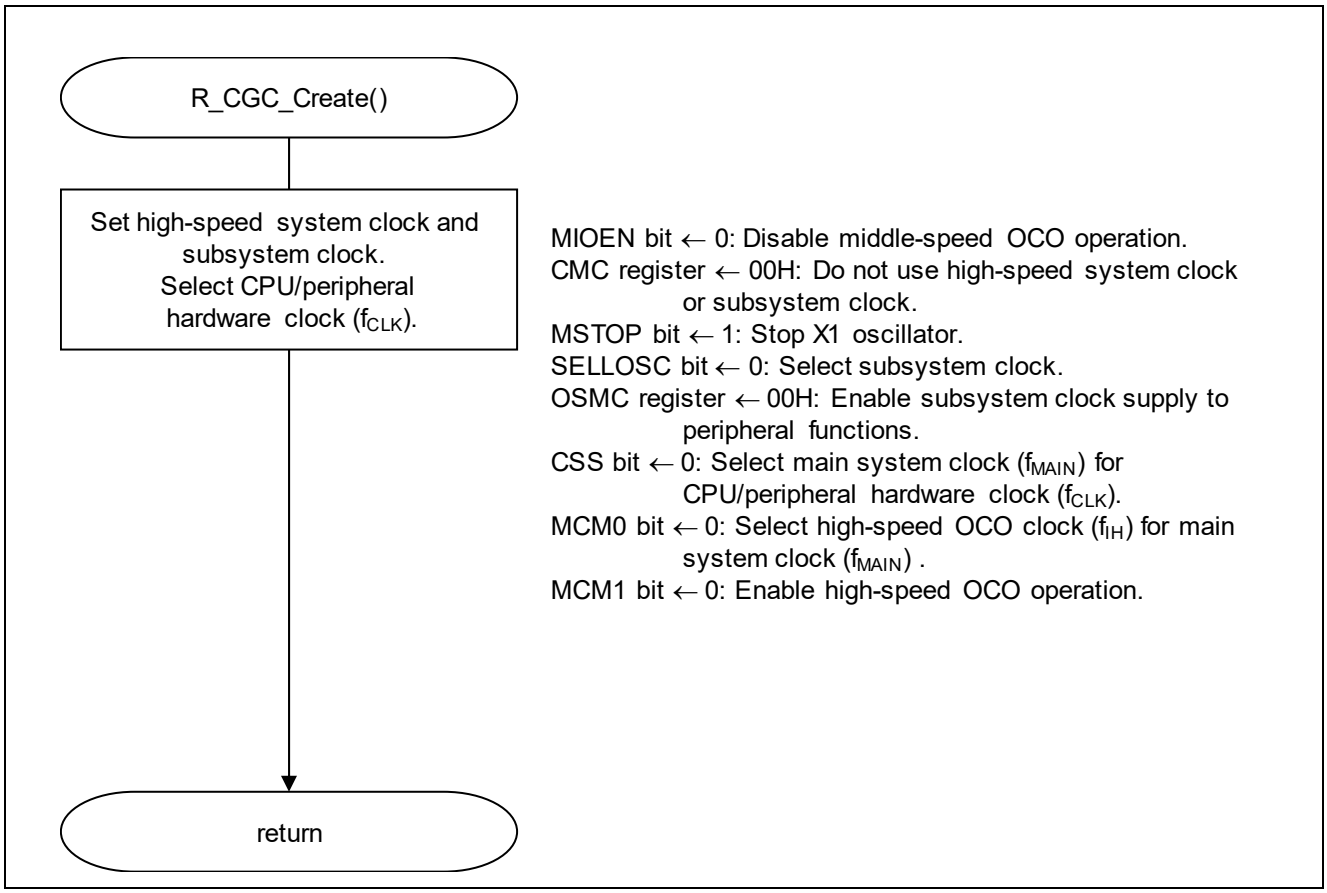

Figure 5.5 Setting CPU Clocks

5.5.5 Setting Timer KB0

Figure 5.6 shows the flowchart for setting timer KB0.

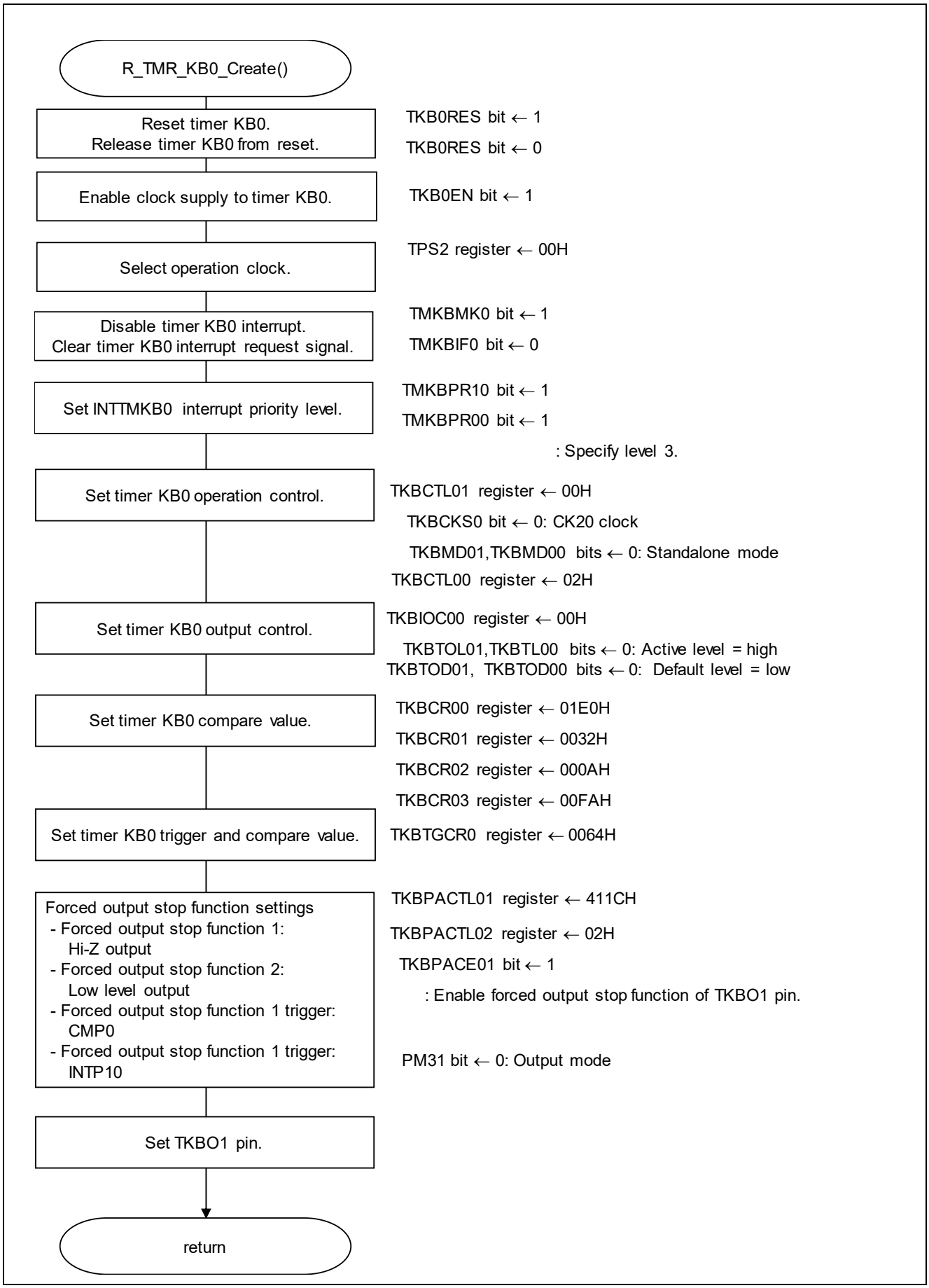

Figure 5.6 Setting Timer KB0

Controlling Timer KB0 Reset

- Peripheral reset control register 2 (PRR2)

Controls timer KB0 reset.

Symbol: PRR2

7	6	5	4	3	2	1	0
TMKARES	0	DOCRES	0	0	0	0	TKB0RES
x	0	x	0	0	0	0	**1/0**

Bit 0

TKB0RES	Reset control of timer KB0
0	**Timer KB0 reset release**
1	**Timer KB0 reset status**

Starting clock supply to timer KB0

- Peripheral enable register 2 (PER2)

Starts clock supply to timer KB0.

Symbol: PER2

7	6	5	4	3	2	1	0
TMKAEN	0	DOCEN	0	0	0	0	TKB0EN
x	0	x	0	0	0	0	**1**

Bit 0

TKB0EN	Control of timer KB0 input clock
0	Stops supply of input clock.
1	**Supplies input clock.**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting timer KB0 operation clock

- Timer clock select register 2 (TPS2)
  Selects the timer KB operation clock.

Symbol: TPS2

7	6	5	4	3	2	1	0
0	TPS212	TPS211	TPS210	0	TPS202	TPS201	TPS200
0	**0**	**0**	**0**	0	**0**	**0**	**0**

Bits 2-0

TPS202	TPS201	TPS200	Selection of operation clock (CK20)					
				f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz	f_{CLK} = 24 MHz
0	**0**	**0**	**f_{CLK}**	2 MHz	5 MHz	10 MHz	20 MHz	**24 MHz**
0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	12 MHz
0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	6 MHz
0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	3 MHz
1	0	0	$f_{CLK}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz	1.5 MHz
1	0	1	$f_{CLK}/2^5$	62.5 kHz	156.2 kHz	312.5 kHz	625 kHz	750 kHz
Other than the above			Setting prohibited					

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting timer KB0 interrupt

- Interrupt request flag register (IF2L)
  Clears interrupt request flags.
- Interrupt mask flag register (MK2L)
  Disables interrupt servicing.

Symbol: IF2L

7	6	5	4	3	2	1	0
FLIF	IICAIF1	TMKBIF0	ITIF01	ITIF00	DOCIF	CMPIF1	CMPIF0
x	x	**0**	x	x	x	x	x

Bit 5

TMKBIF0	Interrupt request flag
0	**No interrupt request signal is generated.**
1	Interrupt request is generated, interrupt request status

Symbol: MK2L

7	6	5	4	3	2	1	0
FLMK	IICAMK1	TMKBMK0	ITMK01	ITMK00	DOCMK	CMPMK1	CMPMK0
X	x	**1**	x	x	x	x	x

Bit 5

TMKBMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting timer KB operation control

- 16-bit timer KB operation control register 01 (TKBCTL01)
  Controls timer KB0 operation.
  Selects timer KB0 clock.
  Selects timer KB0 operation mode.

Symbol: TKBCTL01

7	6	5	4	3	2	1	0
TKBCE0	0	0	TKBCKS0	0	0	TKBMD01	TKBMD00
0	0	0	**0**	0	0	**0**	**0**

Bit 7

TKBCE0	Timer KB0 operation control
0	**Stops timer operation (counter is set to FFFF).**
1	Enables timer count operation.

Bit 4

TKBCKS0	Timer KB0 clock selection
0	**CK20 clock selected by TPS202 to TPS200 bits**
1	CK21 clock selected by TPS212 to TPS210 bits

Bits 1-0

TKBMD01	TKBMD00	Timer KB0 operation mode selection
0	**0**	**Standalone mode (uses master)**
1	1	Interleave PFC output mode
Other than the above		Setting prohibited

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting timer KB0 output control

- 16-bit timer KB output control register 00 (TKBIOC00)
  Sets the active level in timer output TKBO0.
  Sets the default level in timer output TKBO2.

Symbol: TKBIOC00

7	6	5	4	3	2	1	0
0	0	0	0	TKBTOL01	TKBTOL00	TKBTOD01	TKBTOD00
0	0	0	0	**0**	**0**	**0**	**0**

Bits 3, 2

TKBTOL0n	Active level setting of timer output TKBOn (n = 1,0)
0	**High level**
1	Low level

Bits 1, 0

TKBTOD0n	Default level setting of timer output TKBOn (n = 1,0)
0	**Low level**
1	High level

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting timer KB0 forced output stop function

- Forced output stop function control register 00 (TKBPACTL01)
  Selects the external interrupt trigger, comparator trigger, and operation mode for forced output stop function 2.
  Selects the comparator trigger, output status, and clear condition for forced output stop function 1.

- Forced output stop function control register 02 (TKBPACTL02)
  Controls trigger signal input.

Symbol: TKBPACTL01

15	14	13	12	11	10	9	8
TKBPAFXS013	TKBPAFXS012	TKBPAFXS011	TKBPAFXS010	0	0	0	TKBPAFCM01
0	**1**	**0**	**0**	0	0	0	**1**

7	6	5	4	3	2	1	0
0	0	TKBPAHZS011	TKBPAHZS010	KBPAHCM011	KBPAHCM010	TKBPAMD011	TKBPAMD010
0	0	**0**	**1**	**1**	**1**	**0**	**0**

Bit 15

TKBPAFXS013	External interruption trigger selection for forced output stop function 2
0	**INTP11 cannot be used as a trigger.**
1	INTP11 can be used as a trigger.

Bit 14

TKBPAFXS012	External interruption trigger selection for forced output stop function 2
0	INTP10 cannot be used as a trigger.
1	**INTP10 can be used as a trigger.**

Bit 13

TKBPAFXS011	Comparator trigger selection for forced output stop function 2
0	**CMP1 cannot be used as a trigger.**
1	CMP1 can be used as a trigger.

Bit 12

TKBPAFXS010	Comparator trigger selection for forced output stop function 2
0	**CMP0 cannot be used as a trigger.**
1	CMP0 can be used as a trigger.

Bit 8

TKBPAFCM01	Operation mode selection for forced output stop function 2
0	Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period.
1	**Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period following detection of the reverse edge of the trigger.**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Symbol: TKBPACTL01

15	14	13	12	11	10	9	8
TKBPAFXS013	TKBPAFXS012	TKBPAFXS011	TKBPAFXS010	0	0	0	TKBPAFCM01
0	**1**	**0**	**0**	0	0	0	**1**

7	6	5	4	3	2	1	0
0	0	TKBPAHZS011	TKBPAHZS010	KBPAHCM011	KBPAHCM010	TKBPAMD011	TKBPAMD010
0	0	**0**	**1**	**1**	**1**	**0**	**0**

Bit 5

TKBPAHZS011	Comparator trigger selection for forced output stop function 1
0	**CMP1 cannot be used as a trigger.**
1	CMP1 can be used as a trigger.

Bit 4

TKBPAHZS010	Comparator trigger selection for forced output stop function 1
0	CMP0 cannot be used as a trigger.
1	**COM0 can be used as a trigger.**

Bits 3, 2

TKBPAHCM011	TKBPAHCM010	Clear condition selection for forced output stop function 1
0	**0**	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT01) = 1 is written, regardless of the trigger signal level.
0	**1**	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing “forced output stop function release trigger (TKBPAHTT01) = 1” is invalid. Forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT01) = 1 is written while the trigger signal is in its inactive period.
1	**0**	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT01) = 1 is written, regardless of the trigger signal level. Note
1	**1**	**Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing “forced output stop function release trigger (TKBPAHTT01) = 1” is invalid. Forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT01) = 1 is written when the trigger signal is in its inactive period.** Note

Note: When timer KB is stopped (TKBCE0 = 0) without waiting for the next counter period, the forced output stop function is kept on until timer KB is restarted (TKBCE0 = 1).

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Symbol: TKBPACTL01

15	14	13	12	11	10	9	8
TKBPAFXS013	TKBPAFXS012	TKBPAFXS011	TKBPAFXS010	0	0	0	TKBPAFCM01
0	**1**	**0**	**0**	0	0	0	**1**

7	6	5	4	3	2	1	0
0	0	TKBPAHZS011	TKBPAHZS010	KBPAHCM011	KBPAHCM010	TKBPAMD011	TKBPAMD010
0	0	**0**	**1**	**1**	**1**	**0**	**0**

Bits 1, 0

TKBPAMD011	TKBPAMD010	Output status selection when executing forced output stop function	
		Forced output stop function 1	Forced output stop function 2
0	**0**	**Hi-Z output**	**Output fixed at low level**
0	1	Hi-Z output	Output fixed at high level
1	0	Output fixed at low level	Output fixed at low level
1	1	Output fixed at high level	Output fixed at high level

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Symbol: TKBPACTL02

7	6	5	4	3	2	1	0
0	0	0	0	0	0	TKBPACE01	TTKBPACE00
0	0	0	0	0	0	**1**	**0**

Bits 1, 0

TKBPACE0n	Input control of trigger signal used for forced output stop function of the TKBO0 pin
0	**Disable operation of forced output stop function**
1	**Enable operation of forced output stop function**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

5.5.6 Setting PGA

Figure 5.7 shows the flowchart for setting the PGA.

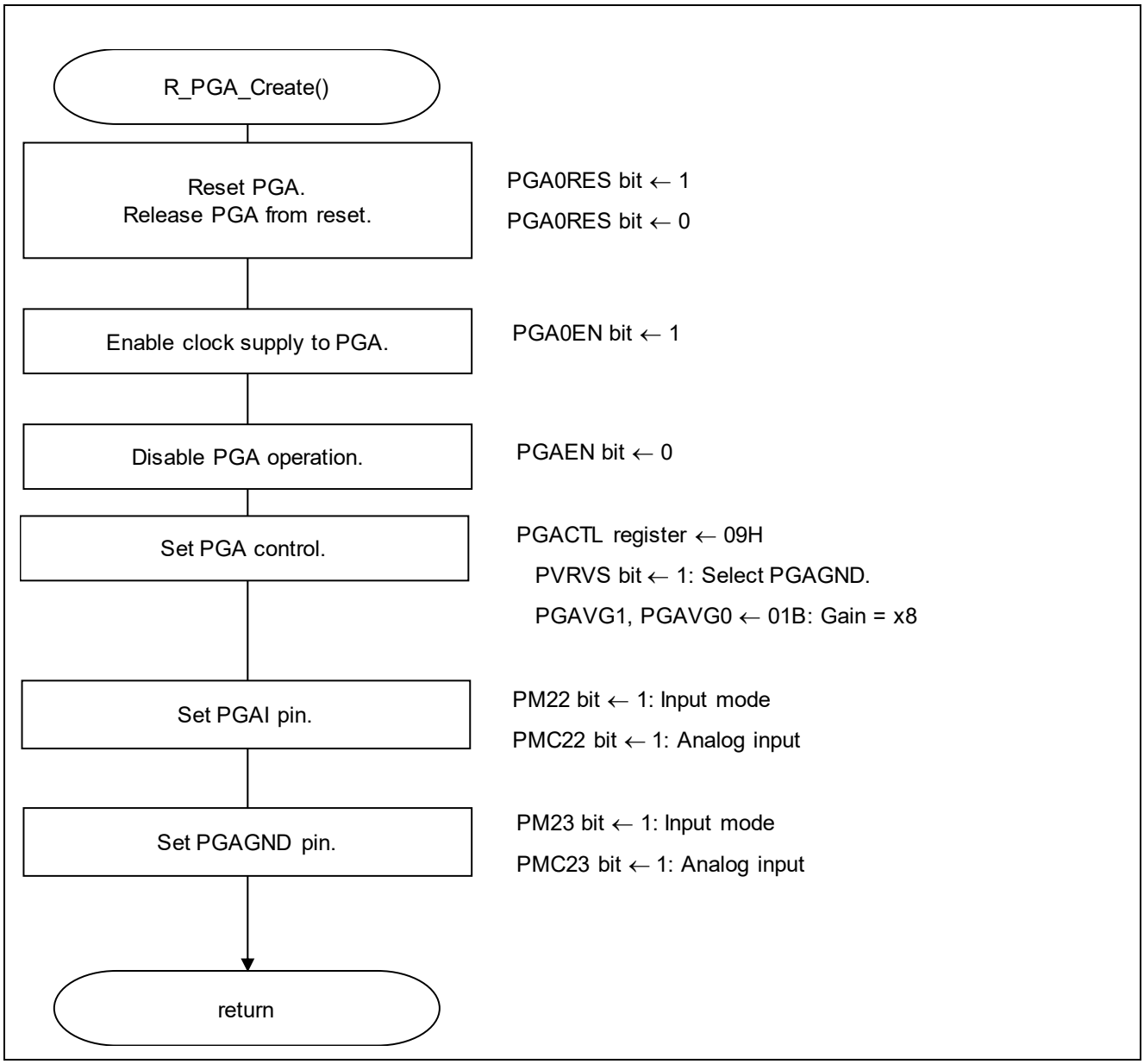

Figure 5.7 Setting PGA

Controlling PGA Reset

- Peripheral reset control register 1 (PRR1)

Controls PGA reset.

Symbol: PRR1

7	6	5	4	3	2	1	0
DACRES	0	CMPRES	0	0	PGA0RES	0	0
x	0	x	0	0	1/0	0	0

Bit 2

PGA0RES	Reset control of PGA
0	**PGA reset release**
1	**PGA reset state**

Starting clock supply to PGA

- Peripheral enable register 0 (PER0)

Starts clock supply to PGA.

Symbol: PER1

7	6	5	4	3	2	1	0
FACEN	0	CMPEN	0	DTCEN	PGA0EN	0	0
x	0	x	0	x	**1**	0	0

Bit 2

PGA0EN	PGA input clock control
0	SFR used by the PGA cannot be written. PGA is not initialized.
1	**SFR used by the PGA can be read/written.**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Controlling PGA operation

- PGA control register (PGACTL)

Enables/disables PGA operation and sets the amplification factor (gain).

Symbol: PGACTL

7	6	5	4	3	2	1	0
PGAEN	0	0	0	PVRVS	0	PGAVG1	PGAVG0
0	0	0	0	**1**	0	**0**	**1**

Bit 7

PGAEN	PGA operation control
0	**Stops operation of PGA.**
1	Enables operation of PGA.

Bit 3

PVRVS	GND selection of feedback resistance of the PGA
0	Selects V_{SS}.
1	**Selects PGAGND.**

Bits 1, 0

PGAVG1	PGAVG0	PGA amplification factor selection
0	0	x4
0	**1**	**x8**
1	0	x16
1	1	x32

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

5.5.7 Setting Comparator

Figure 5.8 shows the flowchart for setting the comparator.

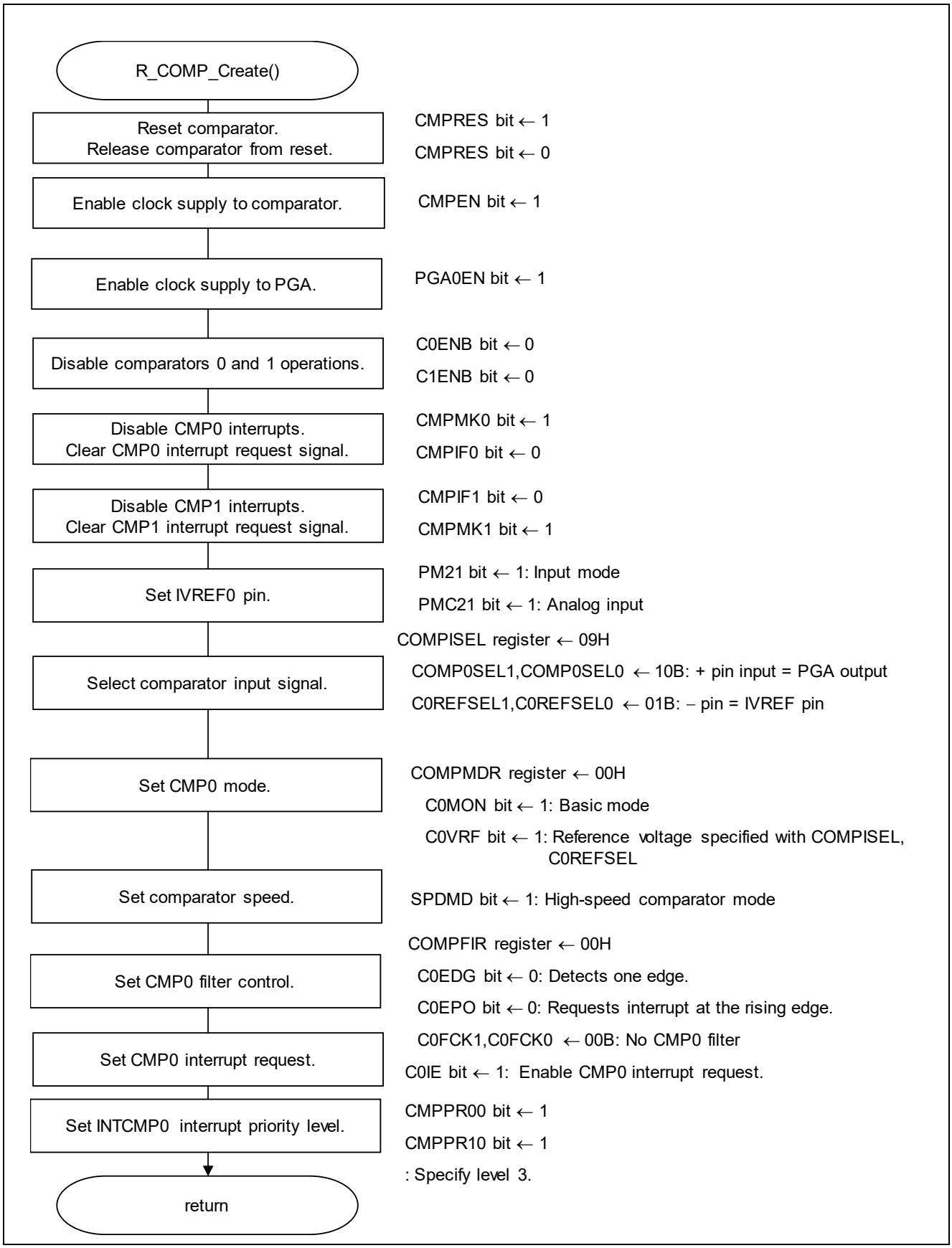

Figure 5.8 Setting Comparator

Controlling comparator reset

- Peripheral reset control register 1 (PRR1)
  Controls comparator reset.

Symbol: PRR1

7	6	5	4	3	2	1	0
DACRES	0	CMPRES	0	0	PGA0RES	0	0
x	0	**1/0**	0	0	x	0	0

Bit 5

CMPRES	Reset control of comparator
0	**Comparator reset release**
1	**Comparator reset state**

Starting clock supply to comparator

- Peripheral enable register 1 (PER1)
  Starts clock supply to comparator.

Symbol: PER1

7	6	5	4	3	2	1	0
DACEN	0	CMPEN	0	DTCEN	PGA0EN	0	0
x	0	**1**	0	x	x	0	0

Bit 5

CMPEN	Control of comparator input clock
0	Stops input clock supply.
1	**Supplies input clock.**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Controlling input signals

- Comparator input signal select control register (COMPISEL)

Selects the input signals on the + and – pins of CMP0.

Symbol: COMPISEL

7	6	5	4	3	2	1	0
0	0	0	0	COMP0SEL1	COMP9SEL0	C0REFSEL1	C0REFSEL0
0	0	0	0	**1**	**0**	**0**	**1**

Bits 3, 2

COMP0SEL1	COMP9SEL0	Selection of the input signal on ＋ pin of the CMP0
0	0	Nothing is selected.
0	1	IVCMP0 pin is selected.
1	**0**	**The output signal from the PGA is selected.**
1	1	Setting prohibited

Bits 1, 0

C0REFSEL1	C0REFSEL0	Selection of the input signal on － pin of the CMP00
0	0	Nothing is selected.
0	**1**	**IVREFP0 pin is selected.**
1	0	The output signal from channel 0 of the on-chip D/A converter is selected.
1	1	Setting prohibited

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting CMP0 mode

- Comparator mode setting register (COMPMDR)
  Enables/disables comparator operation.
  Selects the comparator reference voltage.
  Selects the comparator monitor flag.

Symbol: COMPMDR

7	6	5	4	3	2	1	0
C1MON	C1VRF	C1WDe	C1ENB	C0MON	C0VRF	C0WDE	C0ENB
x	x	X	x	**0**	**0**	**0**	**0**

Bit 3

C0MON	Comparator 0 monitor flag
0	**In standard mode:** **IVCMP0 < CMP0 reference voltage** **In window mode:** **IVCMP0 < Reference voltage specified in COMPISEL.C0REFSEL or IVCMP0 > IVREF1**
1	In standard mode: IVCMP0 > CMP0 reference voltage In window mode: Reference voltage specified in COMPISEL.C0REFSEL < IVCMP0 < IVREF1

Bit 2

C0VRF	CMP0 reference voltage selection
0	**The reference voltage for CMP0 is the voltage specified in COMPISEL.C0REFSEL.**
1	The reference voltage for CMP0 is the voltage on the BGRVREF pin.

Bit 1

C0WDE	CMP0 window mode selection
0	**CMP0 standard mode**
1	CMP0 window mode

Bit 0

C0ENB	CMP0 operation enable
0	**CMP0 operation disabled**
1	CMP0 operation enabled

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Controlling comparator filter

- Comparator filter control register (COMPFIR)

Selects edge detection, edge polarity, and filter for CMP0.

Symbol: COMPFIR

7	6	5	4	3	2	1	0
C1EDG	C1EPO	C1FCK1	C1FCK0	C0EDG	C0EPO	C0FCK1	C0FCK0
0	0	0	0	**0**	**0**	**0**	**0**

Bit 3

C0EDG	CMP0 edge detection selection
0	**Interrupt request by CMP0 one-edge detection**
1	Interrupt request by CMP0 both-edge detection

Bit 2

C0EPO	CMP0 edge polarity switching
0	**Interrupt request at CMP0 rising edge**
1	Interrupt request at CMP0 falling edge

Bits 1, 0

C0FCK1	C0FCK0	CMP0 filter selection
0	**0**	**No CMP0 filter**
0	1	CMP0 filter enabled, sampling at f_{CLK}
1	0	CMP0 filter enabled, sampling at $f_{CLK}/8$
1	1	CMP0 filter enabled, sampling at $f_{CLK}/32$

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

5.5.8 Setting Timer Array Unit

Figure 5.9 shows the flowchart for setting the TAU.

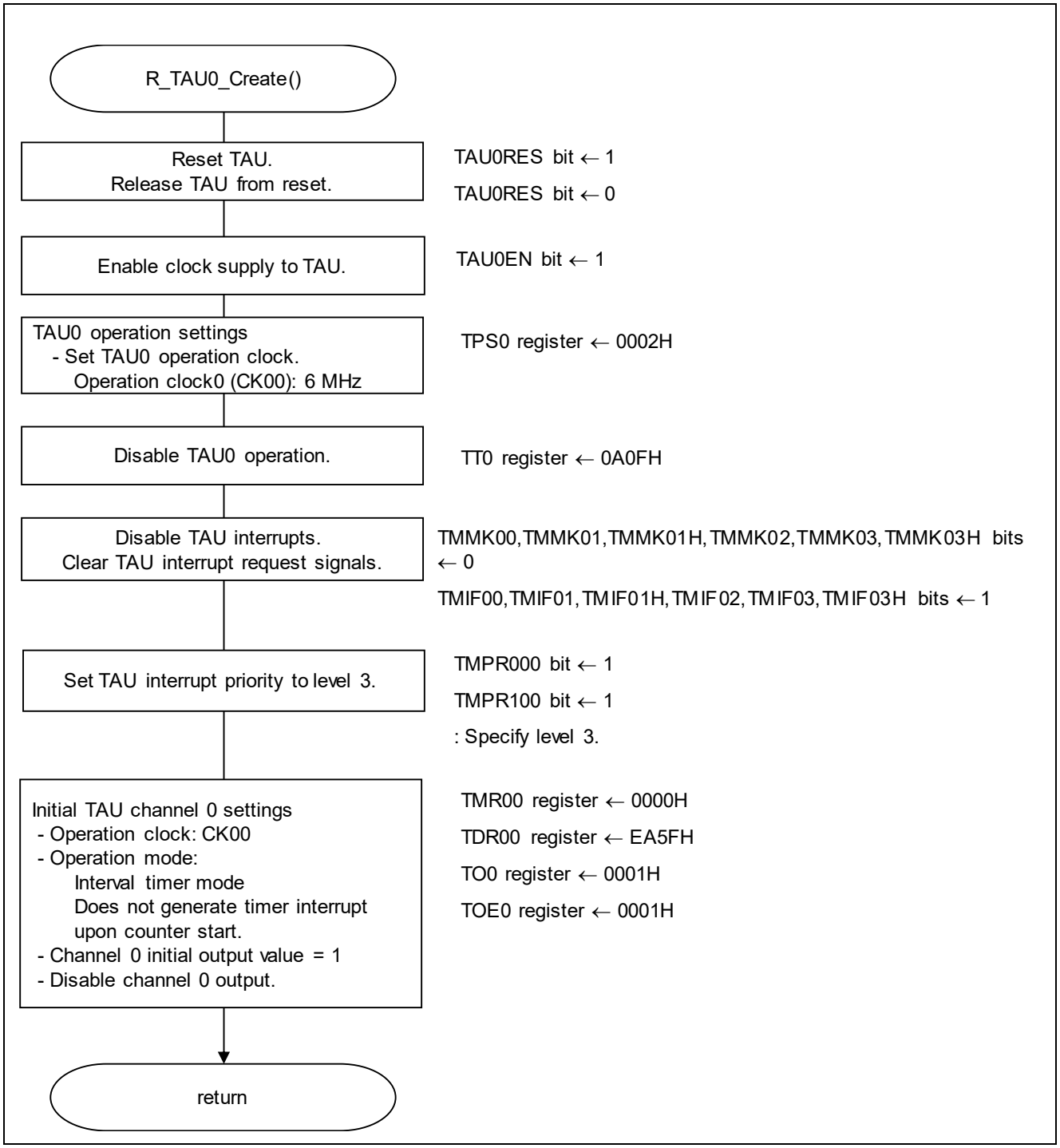

Figure 5.9 Setting TAU

Resetting TAU0

- Peripheral reset control register 0 (PRR0)

Resets TAU0.

Symbol: PRR0

7	6	5	4	3	2	1	0
0	IICA1RES	ADCRES	IICA0RES	0	SAU0RES	0	TAU0RES
0	x	x	x	0	x	0	**1/0**

Bit 0

TAU0RES	Reset control of TAU0
0	**Timer array unit reset release**
1	**Timer array unit reset state**

Starting clock supply to TAU0

- Peripheral enable register 0 (PER0)

Starts clock supply to TAU0.

Symbol: PER0

7	6	5	4	3	2	1	0
0	IICA1EN	ADCEN	IICA0EN	0	SAU0EN	0	TAU0EN
0	x	x	x	0	x	0	**1**

Bit 0

TAU0EN	Control of TAU0 input clock supply
0	Stops input clock supply.
1	**Supplies input clock.**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting timer clock frequency

- Timer clock select register 0 (TPS0)
  Select the operation clock for TAU0.

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS031	PRS030	0	0	PRS021	PRS020	PRS013	PRS012	PRS011	PRS010	PRS003	PRS002	PRS001	PRS000
0	0	x	x	0	0	x	x	x	x	x	x	**0**	**0**	**1**	**0**

Bits 3-0

PRS003	PRS002	PRS001	PRS000		Operation clock (CK00) selection				
					f_{CLK}= 2MHz	f_{CLK}= 5MHz	f_{CLK}= 10MHz	f_{CLK}= 20MHz	f_{CLK}= 24MHz
0	0	0	0	f_{CLK}	2 MHz	5 MHz	10 MHz	20 MHz	24 MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	12 MHz
0	**0**	**1**	**0**	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	**6 MHz**
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	3 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz	1.5 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156.2 kHz	313kHz	625 kHz	750 kHz
0	1	1	0	$f_{CLK}/2^6$	31.25 kHz	78.1 kHz	156 kHz	313 kHz	375 kHz
0	1	1	1	$f_{CLK}/2^7$	15.62 kHz	39.1 kHz	78.1 kHz	156 kHz	187.5 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	93.8 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.76 kHz	19.5 kHz	39.1 kHz	46.9 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.77 kHz	19.5 kHz	23.4 kHz
1	0	1	1	$f_{CLK}/2^{11}$	976 Hz	2.44 kHz	4.88 kHz	9.77 kHz	11.7 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	5.86 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	2.93 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.46 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	732 Hz

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting channel 0 operation mode

- Timer mode register 00 (TMR00)
  Selects the operation clock (f_{MCK}).
  Selects the count clock.
  Sets software trigger start.
  Sets the operation mode.

Symbol: TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**0**

Bits 15, 14

CKS001	CKS000	Selection of operation clock (f_{MCK}) of channel 0
0	**0**	**Operation clock CK00 set by the timer clock select register 0 (TPS0)**
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

CCS00	Selection of count clock (f_{TCLK}) of channel 0
0	**Operation clock (f_{MCK}) specified by the CKS000 and CKS001 bits**
1	Valid edge of input signal input from the TI00 pin

Bit 11

SPLIT00	Selection of 8 or 16-bit timer operation for channel 0
0	**Operates as 16-bit timer.** **(Operates in independent channel operation function or as slave channel in simultaneous channel operation function.)**
1	Operates as 8-bit timer.

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**0**

Bits 10-8

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 0
0	**0**	**0**	**Only software trigger start is valid (other trigger sources are unselected).**
0	0	1	Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Bits 7, 6

CIS001	CIS000	Selection of TI00 pin input valid edge
0	**0**	**Falling edge**
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**0**

Bits 3-0

MD 003	MD 002	MD 001	MD 000	Operation mode of channel 0	Corresponding function	Count operation of TCR
0	**0**	**0**	1/**0**	**Interval timer mode**	**Interval timer / Square wave output / Divider function / PWM output (master)**	**Counting down**
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The operation of each mode varies depending on MD000 bit (see table below).

Operation mode (Value set by the MD003 to MD001 bits (see table above))	MD000	Setting of starting counting and interrupt
- Interval timer mode (0, 0, 0) **- Capture mode (0, 1, 0)**	**0**	**Timer interrupt is not generated when counting is started (timer output does not change, either).**
	1	Timer interrupt is generated when counting is started (timer output also changes).
- Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
- One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	Start trigger is valid during counting operation At that time, interrupt is not generated.
- Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated.
Other than above		Setting prohibited

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware

Setting interval timer period

- Timer data register 00 (TDR00)
  Sets the interval timer compare value.

Symbol: TDR00

15	14		13	12	11	10	9	8	7	6	5	4	3	2	1	0

Timer interrupt (INTTM00) generation timing = (Set value of TDR00 + 1) x Count clock period

Setting timer output

- Timer output register 0 (TO0)
  Sets the timer output value.

Symbol: TO0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TO03	TO02	TO01	TO00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0

Bit 1

TO01	Timer output of channel 0
0	Timer output value is 0.
1	**Timer output value is 1.**

Enabling timer output

- Timer output enable register 0 (TOE0)
  Enables/disables timer output of each channel.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	TOE02	TOE01	TOE00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0

Bit 1

TOE01	Timer output enable/disable of channel 0
0	Timer output is disabled. Timer operation is not applied to the TO01 bit and the output is fixed. Writing to the TO01 bit is enabled and the level set in the TO01 bit is output from the TO01 pin.
1	**Timer output is enabled.** **Timer operation is applied to the TO01 bit and an output waveform is generated.** **Writing to the TO01 bit is ignored.**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

5.5.9 Setting Interrupts

Figure 5.10 shows the flowchart for initial setting of the interrupts.

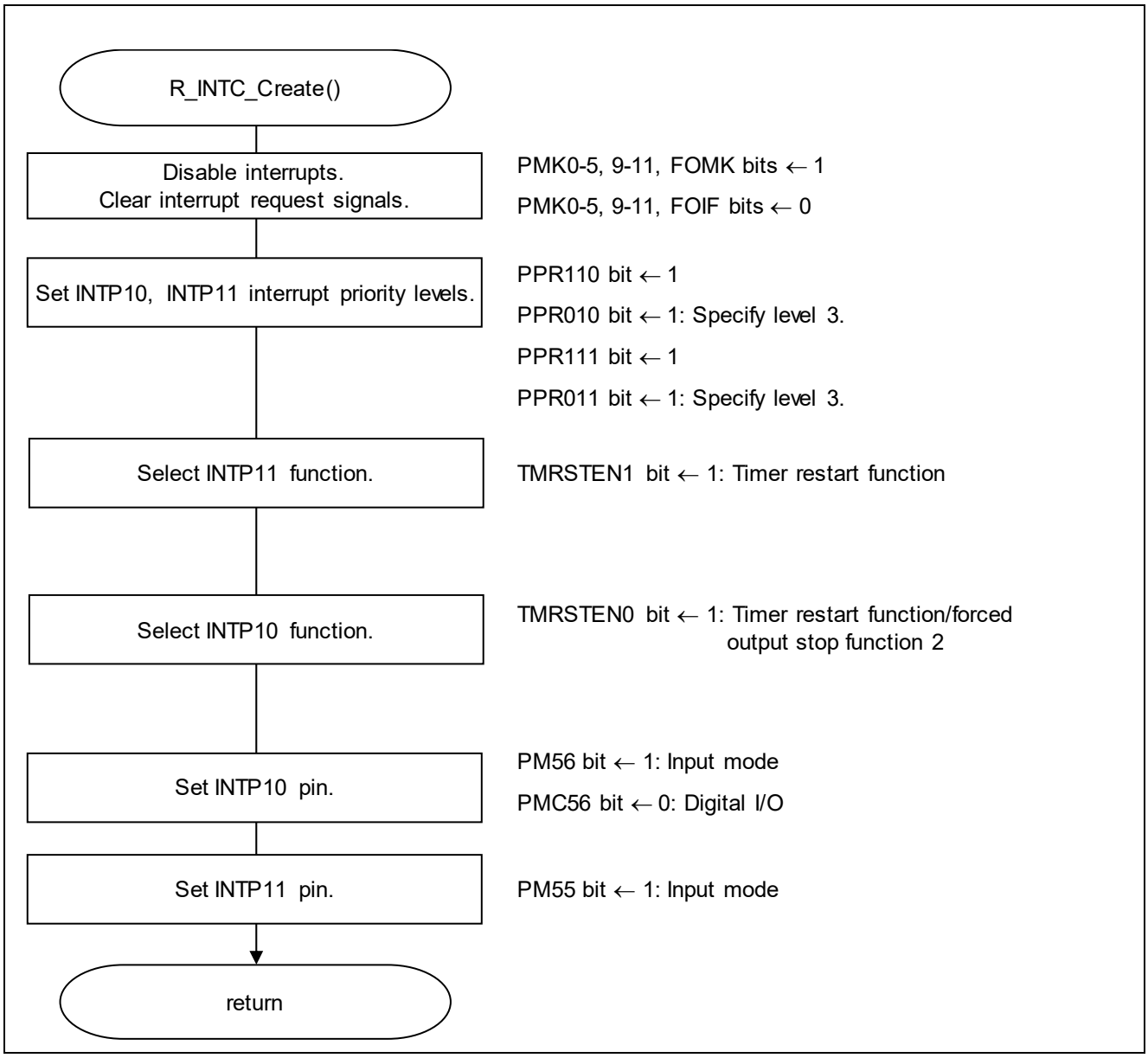

Figure 5.10 Setting Interrupts

Switching interrupt functions

- Peripheral function switch register 0 (PFSEL0)
  Selects I/O settings of peripheral functions.

Symbol: PFSEL0

7	6	5	4	3	2	1	0
CTRGSEL1	CTRGSEL0	INTPINV1	INTPINV0	PNFEN1	PNFEN0	TMRSTEN1	TMRSTEN0
0	0	0	**0**	**0**	**0**	**1**	**1**

Bits 5, 4

INTPINVn	Invert setting of INTP1n signal
0	**Do not invert INTP11 signal**
1	Invert INTP11 signal

Bits 3, 2

PNFENn	Noise filter setting of external interrupt INTP1n
0	**Noise filter enable**
1	Noise filter disable

Bit 1

TMRSTEN1	Switch of external interrupt INTP11
0	External interrupt function is selected (stop mode release enabled, timer restart disabled)
1	**Timer restart function is selected (stop mode release disabled, timer restart enabled).**

Bit 0

TMRSTEN0	Switch of external interrupt INTP10
0	External interrupt function is selected (stop mode release enabled, timer restart disabled)
1	**Timer restart function/forced output stop function 2 is selected (stop mode release disabled, timer restart enabled).**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

5.5.10 Main Function

Figure 5.11 shows the flowchart for the main function.

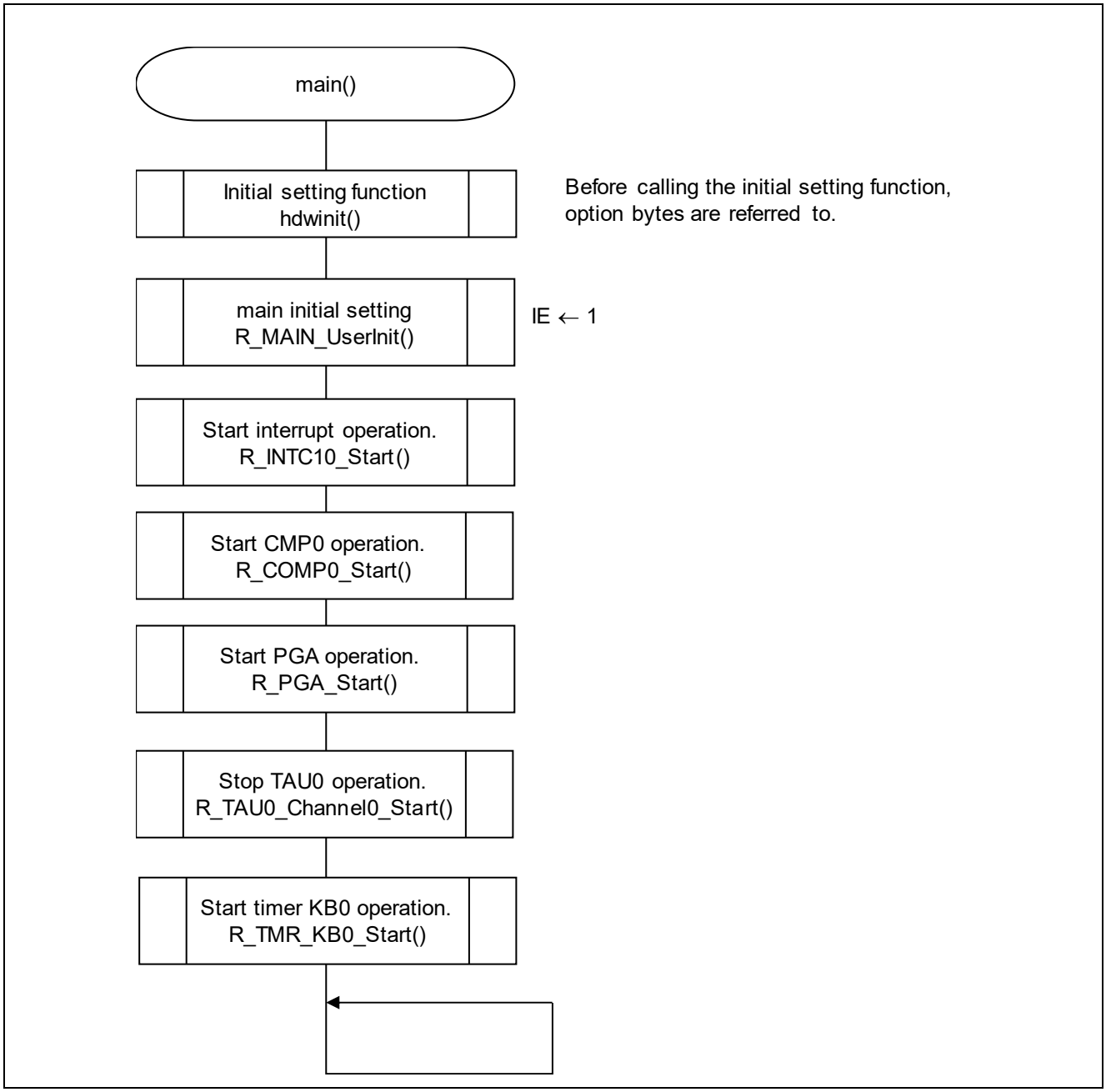

Figure 5.11 Main Function

5.5.11 Initial Setting of Main

Figure 5.12 shows the flowchart for initial setting of the main.

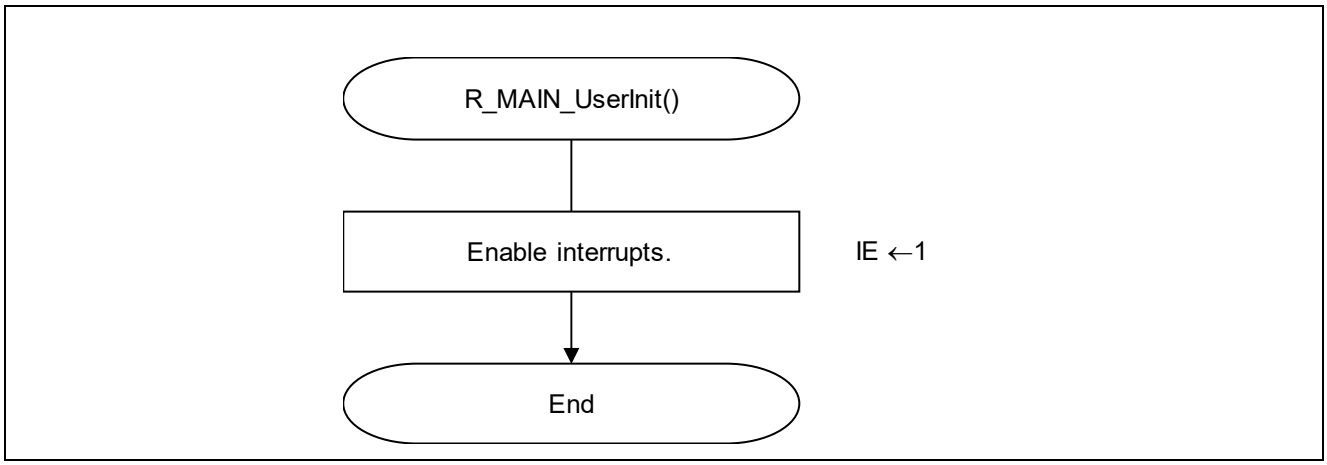

Figure 5.12 Initial Setting of Main

5.5.12 Comparator Operation Starting Function

Figure 5.13 shows the flowchart of the comparator operation starting function.

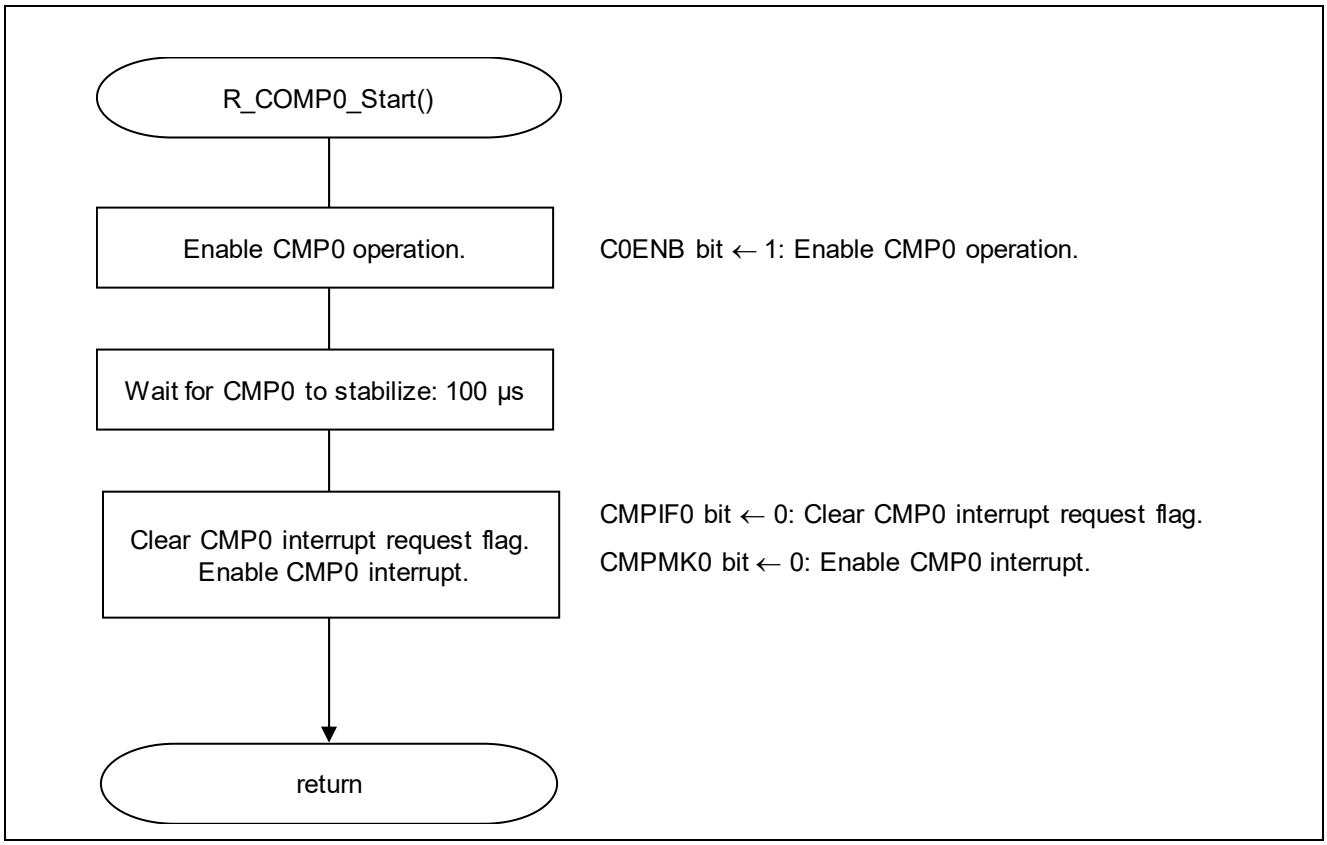

Figure 5.13 Comparator Operation Starting Function

5.5.13 Programmable Gain Amplifier Operation Starting Function

Figure 5.14 shows the flowchart of the PGA operation starting function.

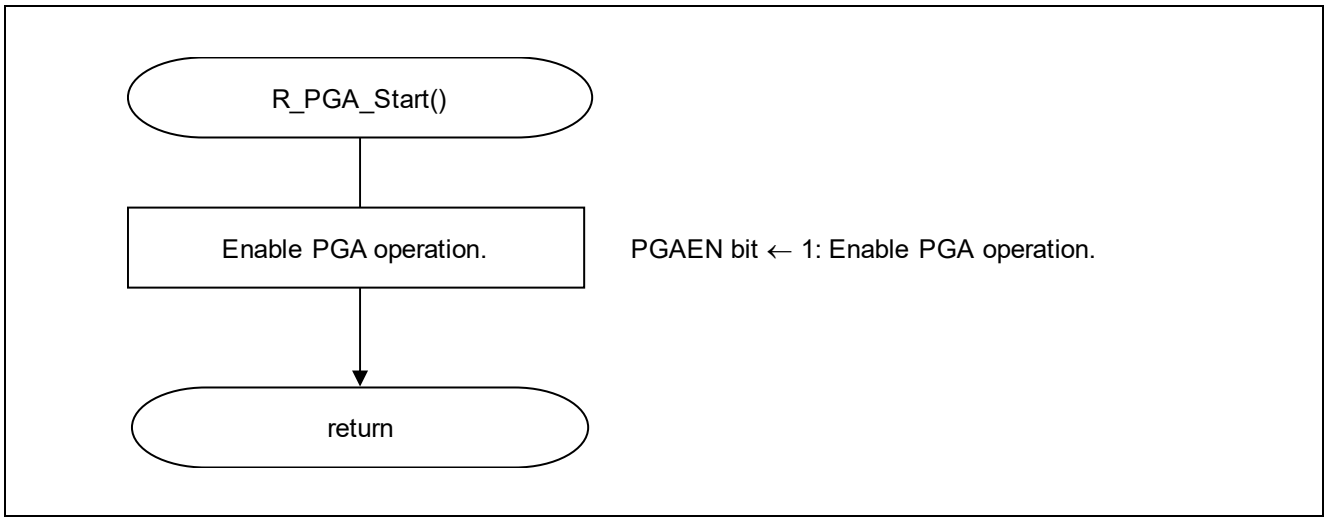

Figure 5.14 PGA Operation Starting Function

5.5.14 Timer Array Unit 0 Operation Starting Function

Figure 5.15 shows the flowchart of the TAU0 operation starting function.

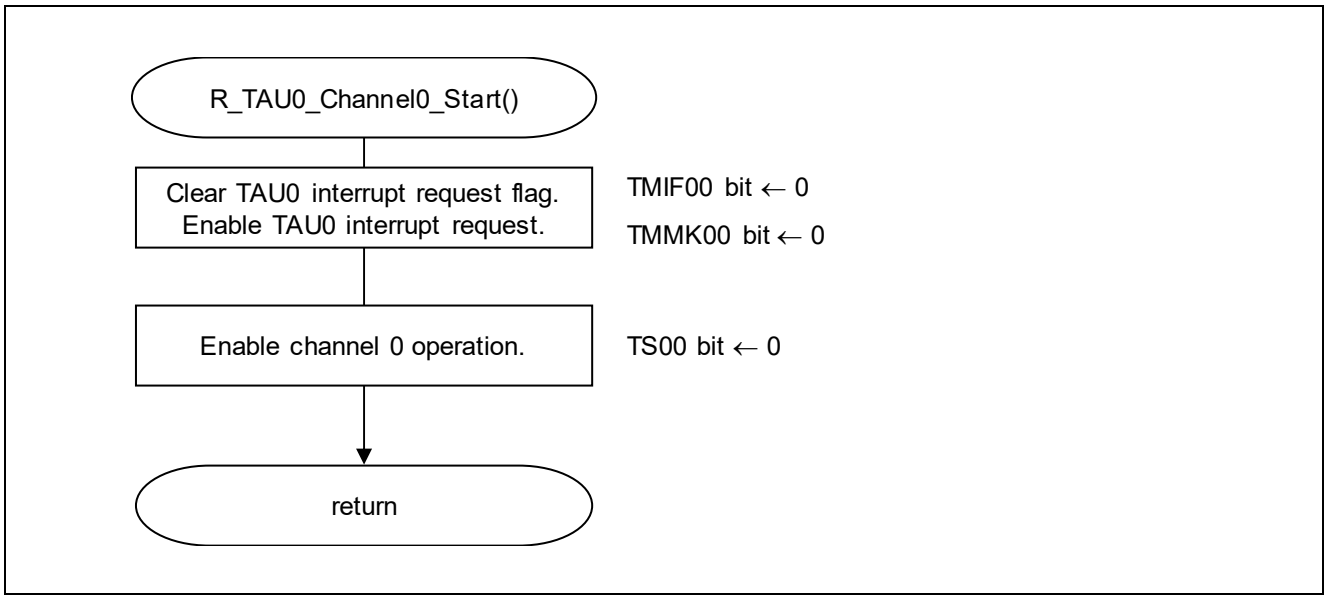

Figure 5.15 TAU0 Operation Starting Function

5.5.15 16-Bit Timer KB0 Operation Starting Function

Figure 5.16 shows the flowchart of the timer KB0 operation starting function.

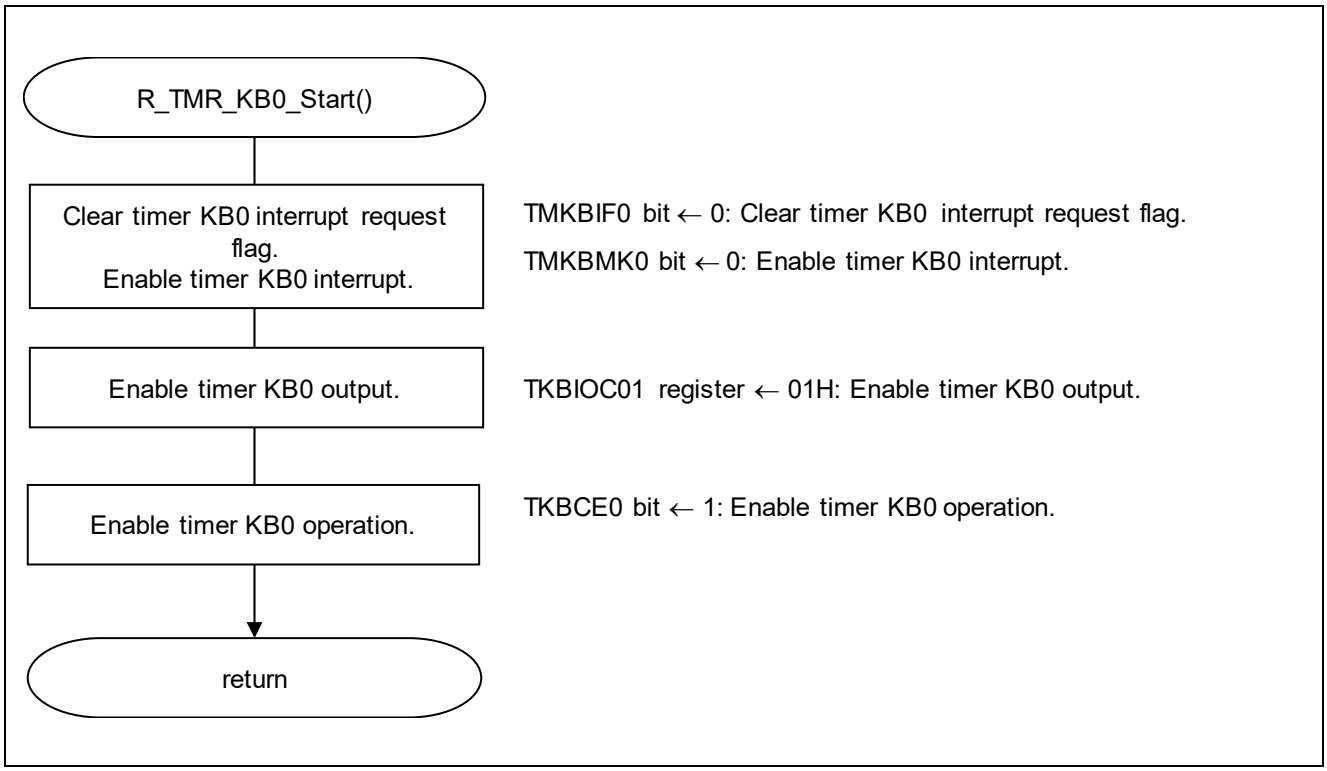

Figure 5.16 Timer KB0 Operation Starting Function

5.5.16 External Interrupt Operation Starting Function

Figure 5.17 shows the flowchart of the external interrupt operation starting function.

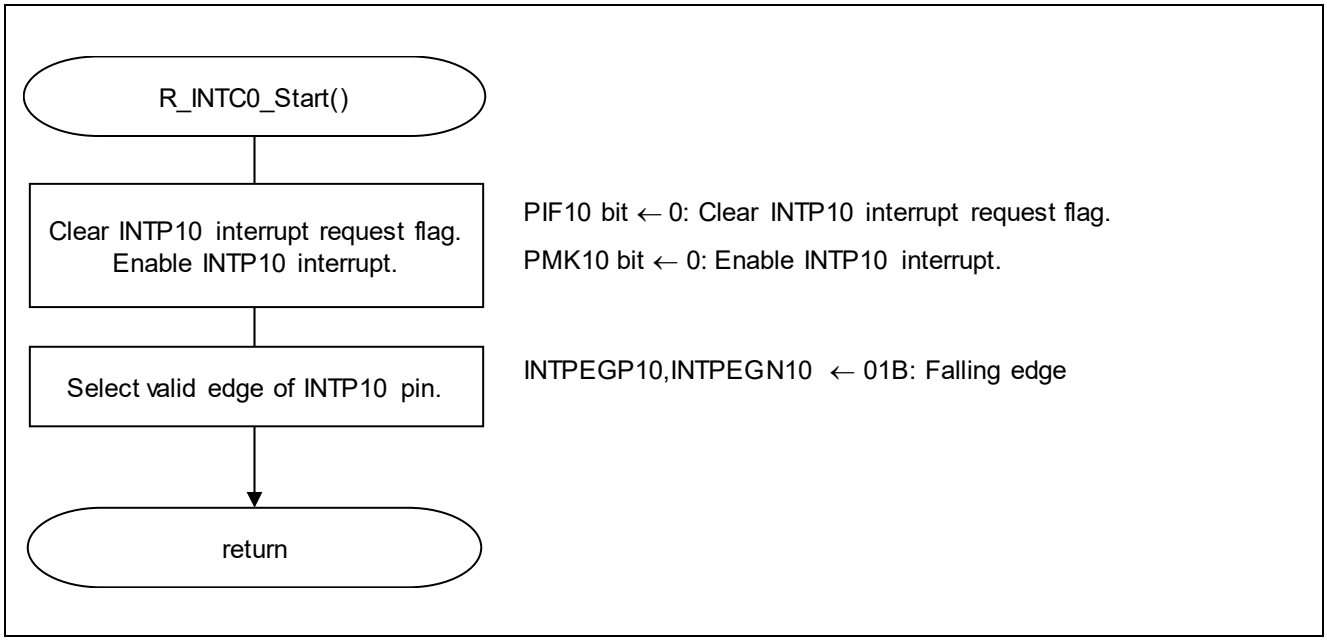

Figure 5.17 External Interrupt Operation Starting Function

6. Sample Code

The user can get the sample code from the Renesas Electronics website.

7. Reference Documents

RL78/G11 User's Manual: Hardware (R01UH0637E)

RL78 Family User's Manual: Software (R01US0015E)

(Get the latest version from the Renesas Electronics website.)

Technical Updates/Technical News

(Get the latest information from the Renesas Electronics website.)

Website and Support

Renesas Electronics Website

https://www.renesas.com/en-us/

Inquiries

http://www.renesas.com/inquiry

Revision History	RL78/G11 Forced Stop of PWM Output through Comparator and External Interrupts IAR

Rev.	Date	Revision Contents	
		Page	Description
1.00	Feb. 03, 2017	—	First edition issued.

すべての商標および登録商標は、それぞれの所有者に帰属します。

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other disputes involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawing, chart, program, algorithm, application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copy or otherwise misappropriation of Renesas Electronics products.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots etc.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Renesas Electronics products are neither intended nor authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems, surgical implantations etc.), or may cause serious property damages (space and undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for which the product is not intended by Renesas Electronics.
6. When using the Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat radiation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions or failure or accident arising out of the use of Renesas Electronics products beyond such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please ensure to implement safety measures to guard them against the possibility of bodily injury, injury or damage caused by fire, and social damage in the event of failure or malfunction of Renesas Electronics products, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures by your own responsibility as warranty for your products/system. Because the evaluation of microcomputer software alone is very difficult and not practical, please evaluate the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please investigate applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive carefully and sufficiently and use Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall not use Renesas Electronics products or technologies for (1) any purpose relating to the development, design, manufacture, use, stockpiling, etc., of weapons of mass destruction, such as nuclear weapons, chemical weapons, or biological weapons, or missiles (including unmanned aerial vehicles (UAVs)) for delivering such weapons, (2) any purpose relating to the development, design, manufacture, or use of conventional weapons, or (3) any other purpose of disturbing international peace and security, and you shall not sell, export, lease, transfer, or release Renesas Electronics products or technologies to any third party whether directly or indirectly with knowledge or reason to know that the third party or any other party will engage in the activities described above. When exporting, selling, transferring, etc., Renesas Electronics products or technologies, you shall comply with any applicable export control laws and regulations promulgated and administered by the governments of the countries asserting jurisdiction over the parties or transactions.
10. Please acknowledge and agree that you shall bear all the losses and damages which are incurred from the misuse or violation of the terms and conditions described in this document, including this notice, and hold Renesas Electronics harmless, if such misuse or violation results from your resale or making Renesas Electronics products available any third party.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.3.0-1 November 2016)

RENESAS

SALES OFFICES

Renesas Electronics Corporation

http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

© 2017 Renesas Electronics Corporation. All rights reserved.

Colophon 6.0