RL78/G11

Battery Voltage Monitoring CC-RL

R01AN3416EJ0100
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Introduction

This application note describes how to implement voltage monitoring during battery charging with a comparator function.

Target Device

RL78/G11

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

1.1 Approaches to Monitoring Battery Voltage in Hardware

The RL78/G11 contains a comparator that can be used to compare the externally input voltage against a reference input voltage and output the result as an INTFO signal.

As shown in the basic configuration of figure. 1.1, a signal that is the monitored input voltage approximately divided in half by resistance is connected to the non-inverted input of the comparator, while the reference voltage generated by the D/A converter is input to the inverted input of the comparator.

If the monitored input voltage is larger than the reference voltage, the comparator output becomes 1. When the INTFO function is used to perform external output with negative logic, the LED is lit.

Table 1.1 Peripheral Functions and Their Usage

Peripheral Function	Usage
A/D converter	Measures a power supply voltage (8-bit precision)
D/A converter	Generates a reference voltage (2 V) to be compared with a monitored voltage
IVCMP0	Provides analog signal input
INTFO	Used to drive the LED
TMKB0	Provides PWM output to control charging

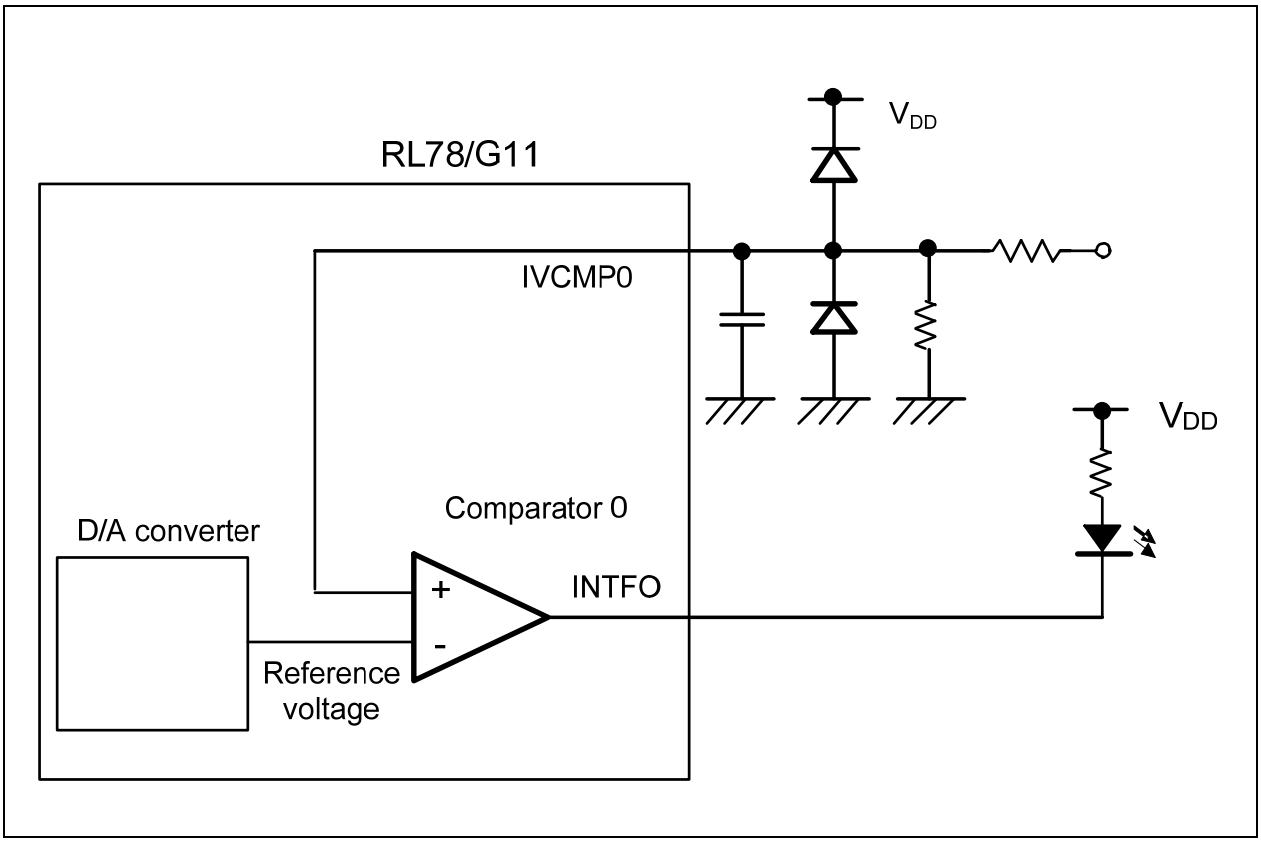

Figure 1.1 Basic Configuration

1.2 Generation of the Reference Voltage

The reference voltage (2V) is generated by the D/A converter. This application note can be used in a wide range of power source voltages (2.4V to 5.5V), and thus the setting of the D/A converter depends on the power source voltage.

A/D conversion is performed on an internal reference voltage (1.45V typ.), and the conversion result is used to obtain the V_{DD} voltage. Then, the D/A conversion value setting register 0 (DACS0) is set so that the output of the D/A converter is the reference voltage (2V).

The internal reference voltage has 8 bits of precision, and the result of the A/D conversion (SAR) is as follows:

$$SAR = (1.45 / V_{DD}) \times 256$$

The output voltage of the D/A converter (VANO0) is expressed by the following formula:

$$VANO0 = V_{DD} \times (DACS0 / 256)$$

The following is the setting for the D/A converter to output 2V:

$$DACS0 = 2 \times SAR / 1.45$$

1.3 Output of Comparison Result

The comparison result is output to the INTFO pin. In this application note, by connecting an LED to the INTFO pin, the LED is made to light when the voltage exceeds the monitored voltage.

2. Conditions for Confirming Operations

The sample code operations described in this application note are confirmed under the following conditions.

Table 2.1 Conditions for Confirming Operations

Item	Description
Microcontroller used	RL78/G11 (R5F1056A)
Operating frequency	- High-speed on-chip oscillator (HOCO) clock: 16 MHz - CPU/peripheral hardware clock: 16 MHz
Operating voltage	3.3 V (Operation is possible within 2.4 V to 5.5 V) LVD operation (V_{LVD}): Reset mode 2.45 V
Integrated development environment (CS+)	CS+ for CC V4.01.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.03.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V5.2.0.020 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.03.00 from Renesas Electronics Corp.

Note: The latest version should be downloaded and evaluated before usage.

3. Related Application Notes

The application notes related to this application note are listed below for reference.

4. Hardware Descriptions

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration described in this application note.

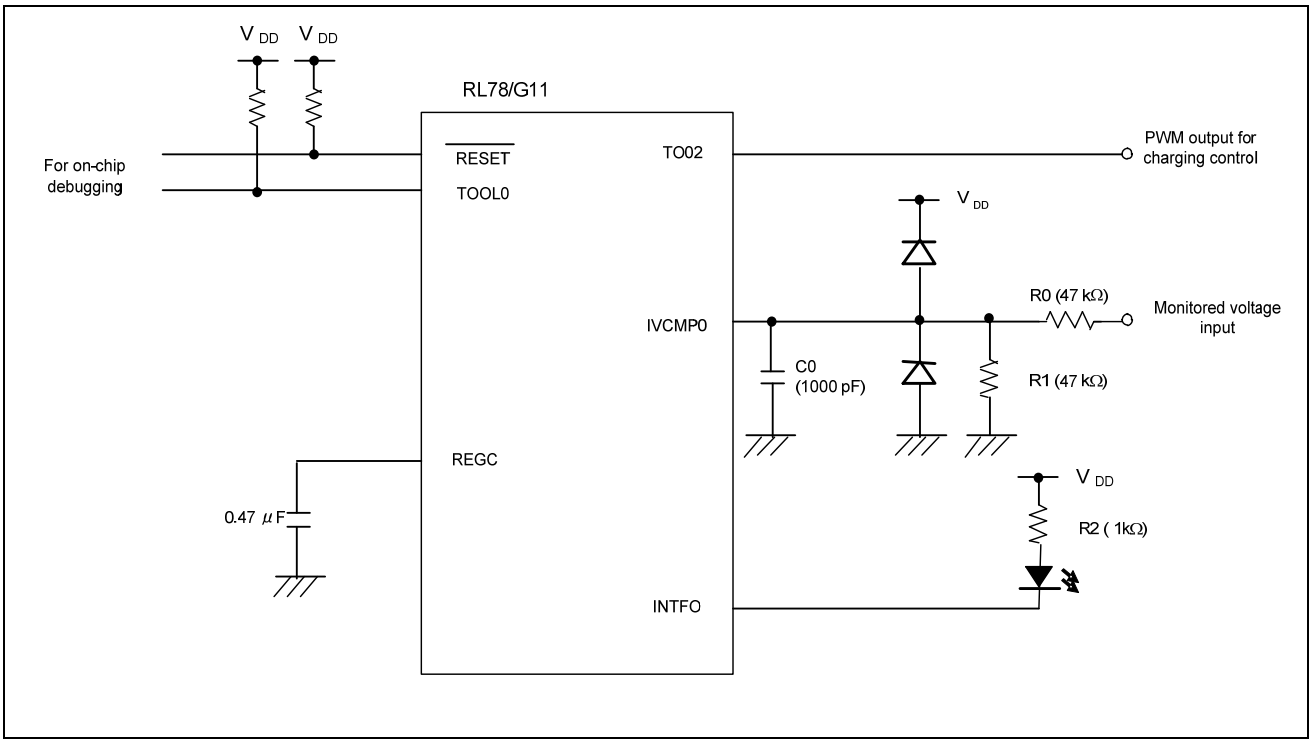

Figure 4.1 Hardware Configuration

Cautions: 1. This circuit diagram is simplified in order to show a summary of connections. When actually creating the circuit, pin processing and the like should be optimized and the circuit designed so as to satisfy the required electrical characteristics (input-only ports should be each connected to V_{DD} or V_{SS} via a resistor).

2. V_{DD} should be made equal to or higher than the reset release voltage (V_{LVD}) set using LVD.

4.2 List of Pins Used

Table 4.1 lists the pins used and their functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
P22/ANI2/PGAI/VCMP0	Input	Monitored voltage input
P56/ANI22/KR2/SCK00/SCL00/SO11/INTP10/(TO03) /(INTFO)/SCLA1	Output	Output for LED1 control
P30/ANI21?KR1/TI00/TO01/INTP3/SCK11/SCL11/(TxD0) /PCLBUZ0/TKB01/SDAA0	Output	PWM output for charging control

5. Software Descriptions

5.1 Operation Summary

In this application note a comparator is used to compare an externally input voltage against a reference input voltage and to output the result as an INTFO signal.

If the monitored input voltage exceeds the reference voltage, the comparator outputs 1, and when the INTFO function is used to perform external output with negative logic, the LED is lit.

(1) The comparator compares the reference voltage generated by the D/A converter and the external monitored voltage input IVCMP0, and the result is output as an INTFO signal.

(2) When IVCMP0 exceeds the reference voltage, the INTFO outputs 0 and the LED is lit.

(3) The TKBO1 provides PWM output for charging control.

5.2 List of Option Byte Settings

Table 5.1 shows the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Setting Value	Description
000C0H	11101111B	Watchdog timer is stopped. (Counting stopped after a reset release)
000C1H	00111111B	LVD reset mode; 2.45 V (2.4 V to 5.5 V)
000C2H	11101010B	HS mode; High-speed on-chip oscillator: 16 MHz
000C3H	10000100B	On-chip debugging is enabled.

5.3 List of Functions

Table 5.2 lists functions.

Table 5.2 Functions

Function Name	Summary
R_ADC_Set_OperationOn	Enables A/D voltage comparator operation
R_ADC_Start	Starts A/D conversion.
R_ADC_Stop	Stops A/D conversion.
R_COMP0_Start	Comparator 0 start processing
R_DAC0_Start	Starts D/A conversion
R_TMR_KB0_Start	Starts timer KB0 operation

5.4 Function Specifications

The following gives the specifications of the functions used in the sample code.

[Function name] R_ADC_Set_OperationOn

Summary	Enables A/D voltage comparator operation.
Header	r_cg_adc.h, r_cg_userdefine.h
Declaration	void R_ ADC_Set_OperationOn(void)
Description	Enables A/D voltage comparator operation.
Arguments	None
Return values	None
Remarks	None

[Function name]R_ADC_Start

Summary	Starts A/D conversion.
Header	r_cg_adc.h, r_cg_userdefine.h
Declaration	void R_ ADC_Start(void)
Description	Starts A/D conversion.
Arguments	None
Return values	None
Remarks	None

[Function name] R_ADC_Stop

Summary	Stops A/D conversion.
Header	r_cg_adc.h, r_cg_userdefine.h
Declaration	void R_ ADC_Stop(void)
Description	Stops A/D conversion.
Arguments	None
Return values	None
Remarks	None

[Function name] R_COMP1_Start

Summary	Starts comparator operation.
Header	r_cg_comp.h, r_cg_userdefine.h
Declaration	void R_ COMP1_Start(void)
Description	Starts comparator operation.
Arguments	None
Return values	None
Remarks	None

[Function name]R_DAC0_Start

Summary	Starts D/A conversion.
Header	r_cg_dac.h, r_cg_userdefine.h
Declaration	void R_ DAC0_Start(void)
Description	Starts D/A conversion.
Arguments	None
Return values	None
Remarks	None

[Function name]R_TMR_KB0_Start

Summary	Starts timer KB0 operation.
Header	r_cg_tmkb.h, r_cg_userdefine.h
Declaration	void R_ TMR_KB0_Start(void)
Description	Starts timer KB0 operation.
Arguments	None
Return values	None
Remarks	None

5.5 Flowcharts

Figure 5.1 shows the overall flow of the process described in this application note.

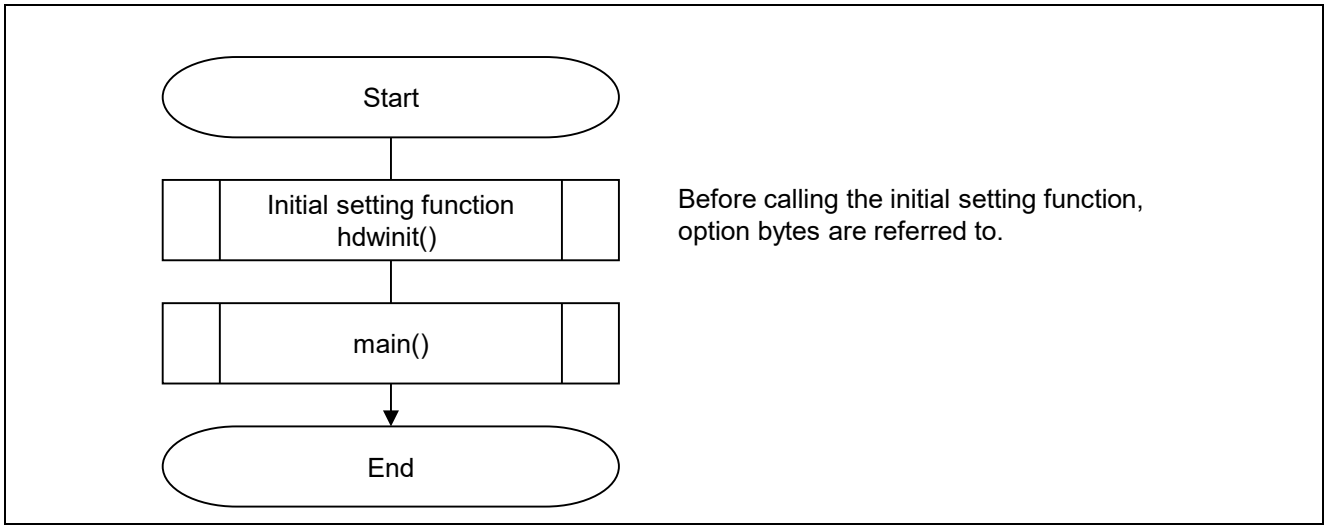

Figure 5.1 Overall Flow

Note: The start-up routine is executed before and after the initial setting function.

5.5.1 Initial Setting Function

Figure 5.2 shows the flowchart of the initial setting function.

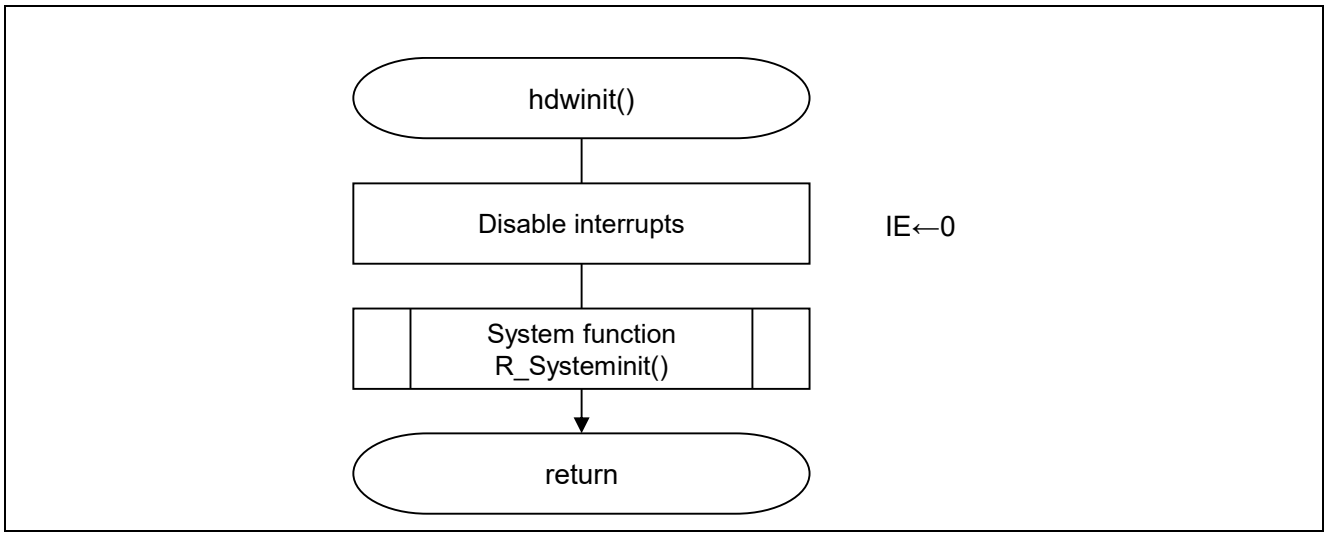

Figure 5.2 Initial Setting Function

5.5.2 System Function

Figure 5.3 shows the flowchart of the system function.

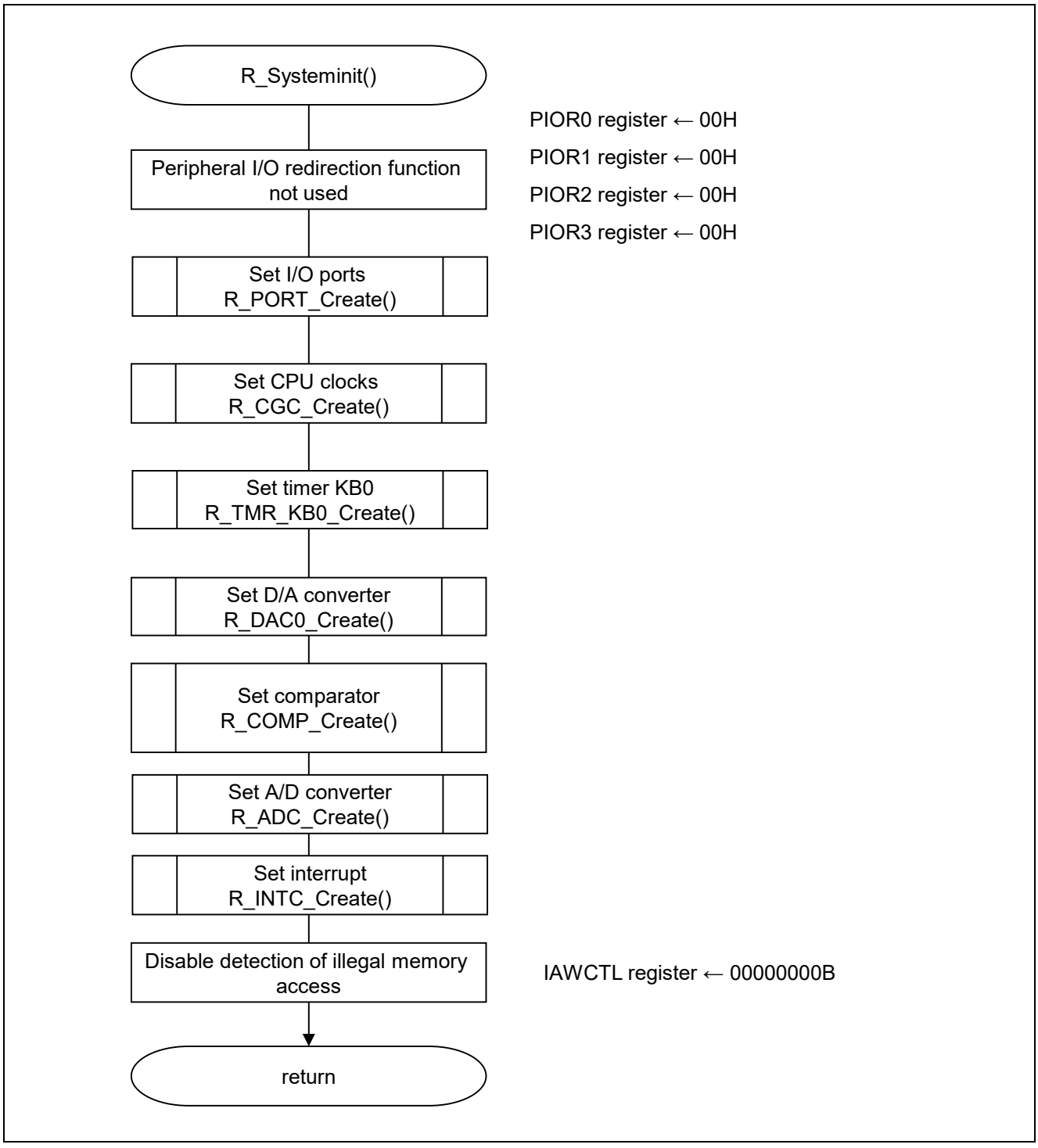

Figure 5.3 System Function

5.5.3 Setting I/O Ports

Figure 5.4 shows the flowchart for setting the I/O ports.

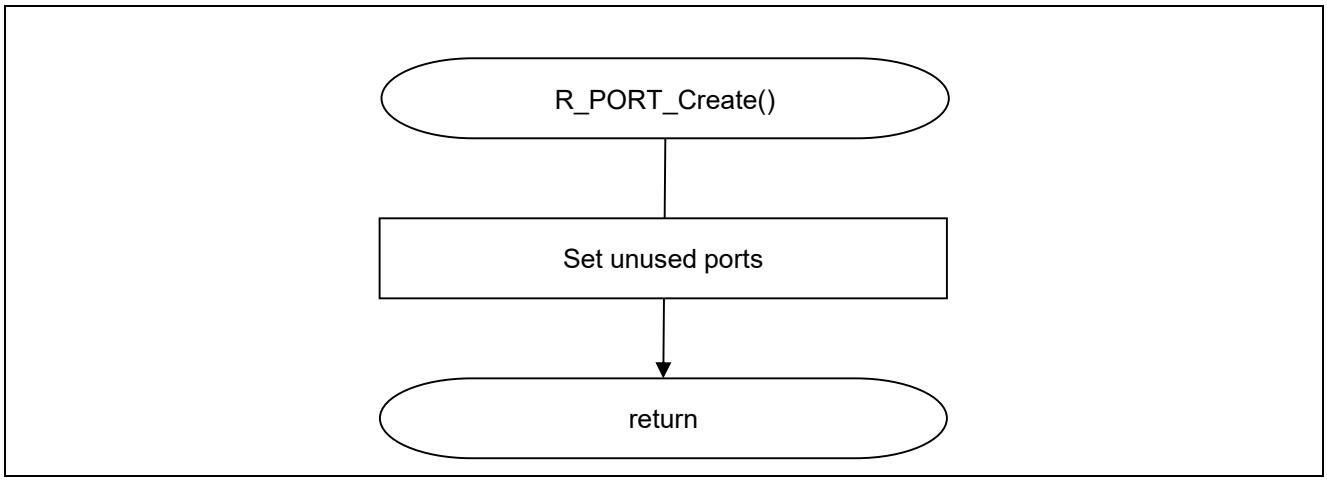

Figure 5.4 Setting I/O Ports

Note: For settings of unused ports, refer to the RL78/G11 User's Manual: Hardware.

Caution: Unused ports should be designed so that the electrical characteristics are satisfied by appropriately treating the pertinent pins. Separately connect unused input-only ports to V_{DD} or V_{SS} via a resistor.

5.5.4 Setting CPU Clocks

Figure 5.5 shows the flowchart for setting the CPU clocks.

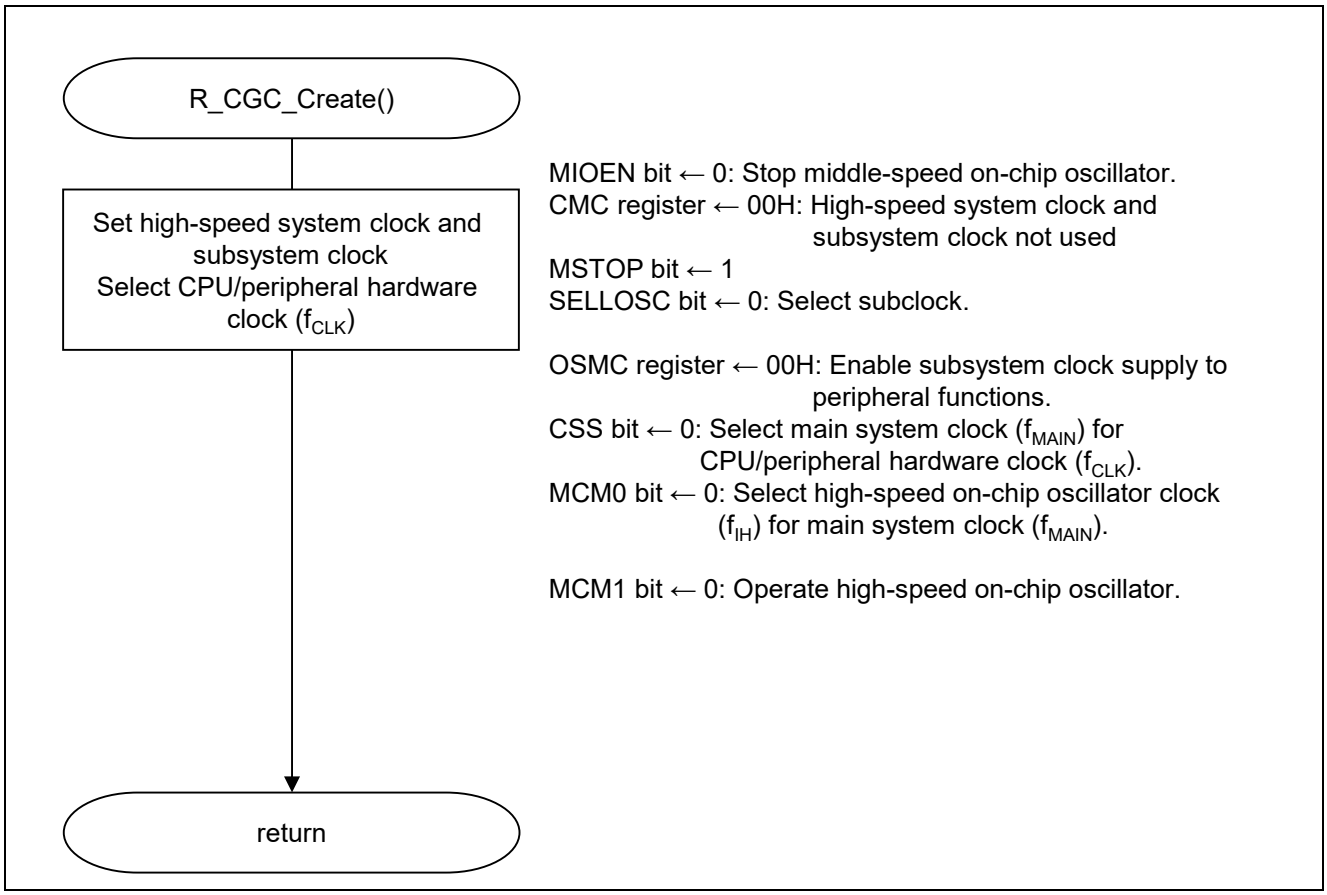

Figure 5.5 Setting CPU Clocks

5.5.5 Setting Comparator

Figure 5.6 shows the flowchart for setting the comparator.

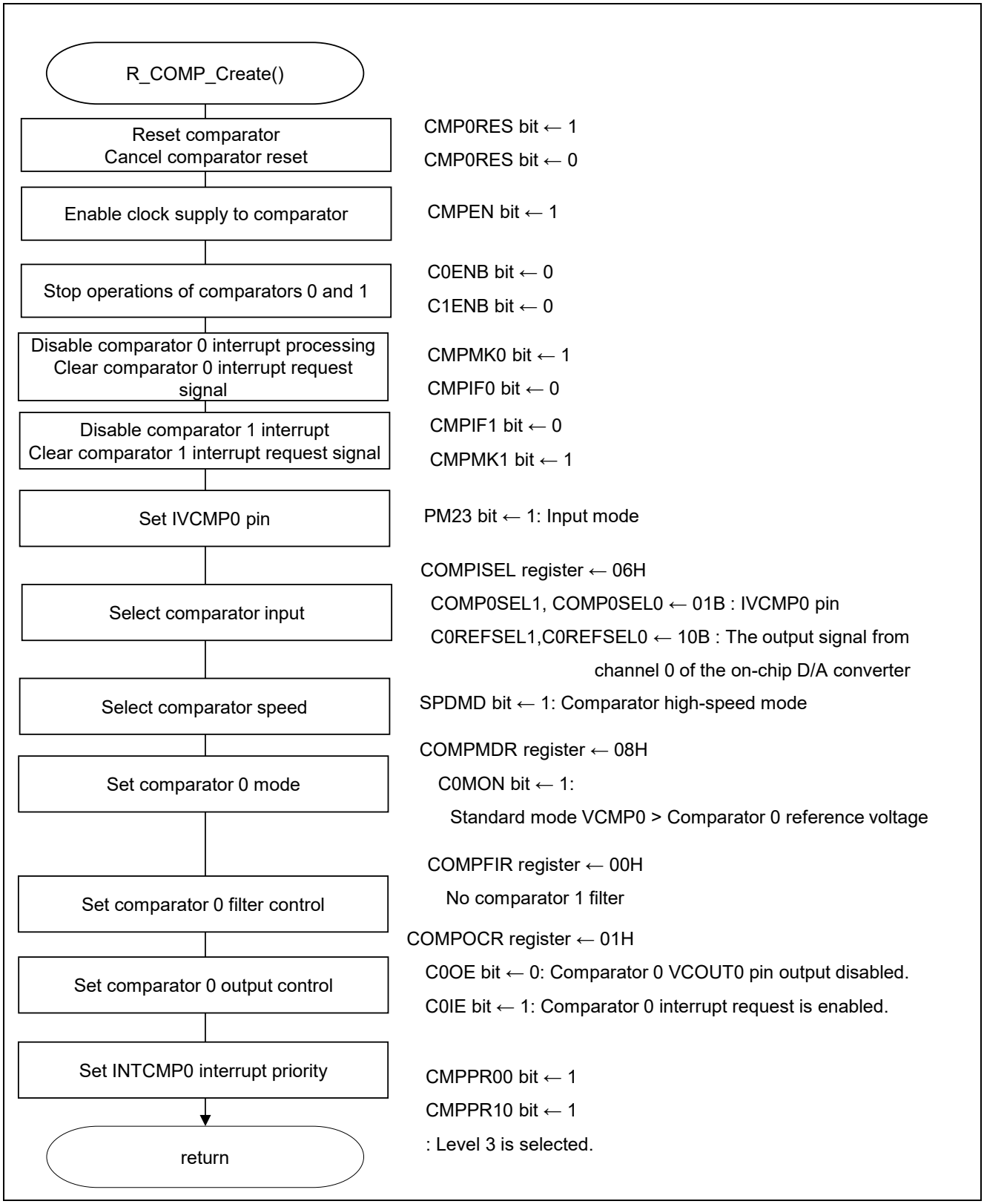

Figure 5.6 Setting Comparator

Starting clock supply to comparator

- Peripheral enable register 1 (PER1)
  Start supplying clock to the A/D converter.

Symbol: PER1

7	6	5	4	3	2	1	0
DACEN	0	CMPEN	0	DTCEN	PGA0EN	0	0
x	0	**1**	0	x	x	0	0

Bit 5

CMPEN	Control of comparator input clock
0	Stops input clock supply.
1	**Enables input clock supply.**

Setting comparator operation

- Comparator mode setting register (COMPMDR)
  Enable comparator operation.

Symbol: COMPMDR

7	6	5	4	3	2	1	0
C1MON	C1VRF	C1WDE	C1ENB	C0MON	C0VRF	C0WDE	C0ENB
x	x	x	**0**	x	x	x	**0**

Bit 4

C1ENB	Comparator 1 operation enable
0	**Comparator 1 operation disabled**
1	Comparator 1 operation enabled

Bit 0

C0ENB	Comparator 0 operation enable
0	**Comparator 0 operation disabled**
1	Comparator 0 operation enabled

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting comparator interrupt

- Interrupt request flag register (IF2L)
  Clear the interrupt request flag.
- Interrupt mask flag register (MK2L)
  Disable the interrupt processing.

Symbol: IF2L

7	6	5	4	3	2	1	0
FLIF	IICAIF1	TMKBIF0	ITIF01	ITIF00	DOCIF	CMPIF1	CMPIF0
x	x	x	x	x	x	**0**	**0**

Bits 0 and 1

CMPIF0,1	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK2L

7	6	5	4	3	2	1	0
FLMK	IICAMK1	TMKBMK0	ITMK01	ITMK00	DOCMK	CMPMK1	CMPMK0
x	x	x	x	x	x	**1**	**1**

Bits 0 and 1

CMPMK0,1	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Setting comparator peripheral reset

- Peripheral reset control register (PRR1)
  Control comparator peripheral resets.

Symbol: PRR1

7	6	5	4	3	2	1	0
DACRES	0	CMPRES	0	0	PGA0RES	0	0
x	0	**0/1**	0	0	x	0	0

Bit 5

CMPRES	Peripheral reset control on each peripheral hardware
0	**Peripheral reset release**
1	**Peripheral reset state**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

5.5.6 Setting D/A Converter

Figure 5.7 shows the flowchart for setting the D/A converter.

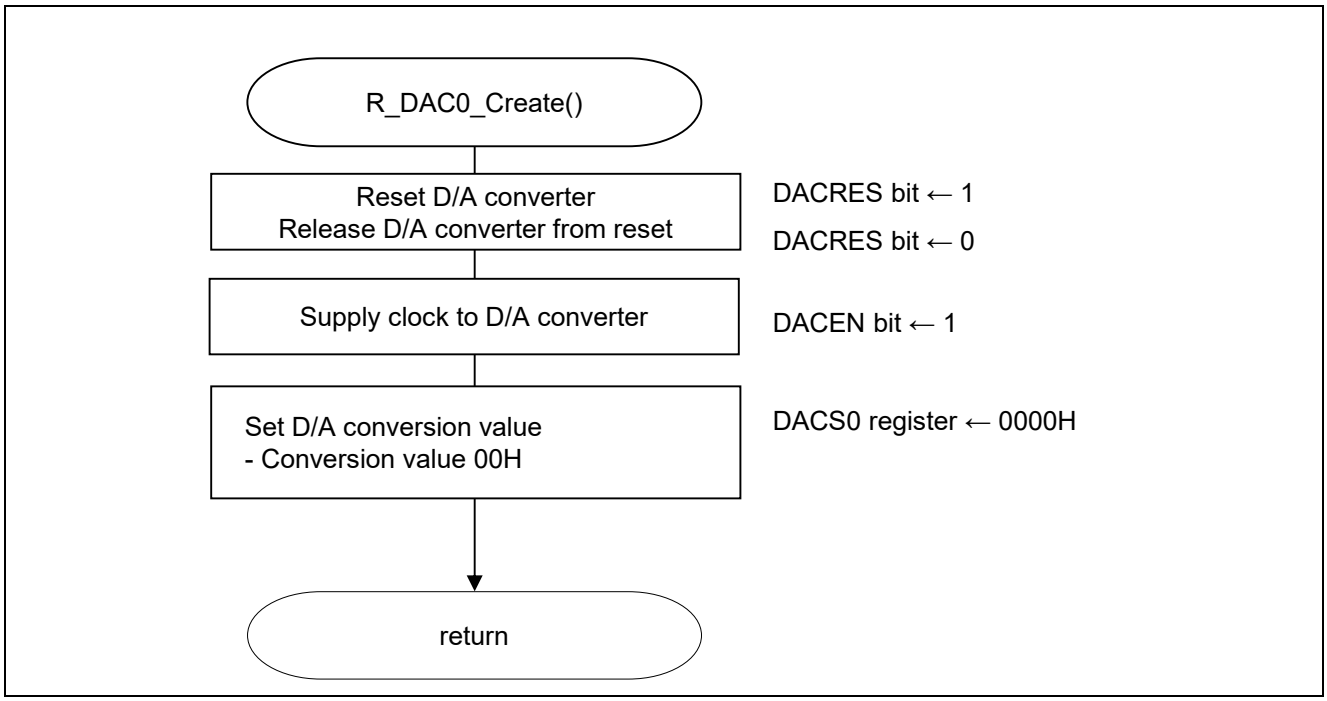

Figure 5.7 Setting D/A Converter

Setting peripheral reset of D/A converter

- Peripheral reset control register (PRR1)
  Control reset of the D/A converter.

Symbol: PRR1

7	6	5	4	3	2	1	0
DACRES	0	CMPRES	0	0	PGA0RES	0	0
0/1	0	x	0	0	x	0	0

Bit 7

DACRES	Reset control of D/A converter
0	**D/A converter reset release**
1	**D/A converter reset state**

Starting clock supply to D/A converter

- Peripheral enable register 1 (PER1)
  Start supplying clock to the D/A converter.

Symbol: PER1

7		6	5	4	3	2	1	0
DACEN		0	CMPEN	0	DTCEN	PGA0EN	0	0
1		0	x	0	x	x	0	0

Bit 0

DACEN	Control of D/A converter input clock
0	Stops input clock supply.
1	**Supplies input clock.**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting D/A conversion value

- D/A conversion value setting register 0 (DACS0)
  Set the analog voltage value to be output to the D/A converter pins.

Symbol: DACS0

7	6	5	4	3	2	1	0
DACS07	DACS06	DACS05	DACS04	DACA03	DACS02	DACS01	DACS00
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

5.5.7 Setting A/D Converter

Figure 5.8 shows the flowchart for setting the A/D converter.

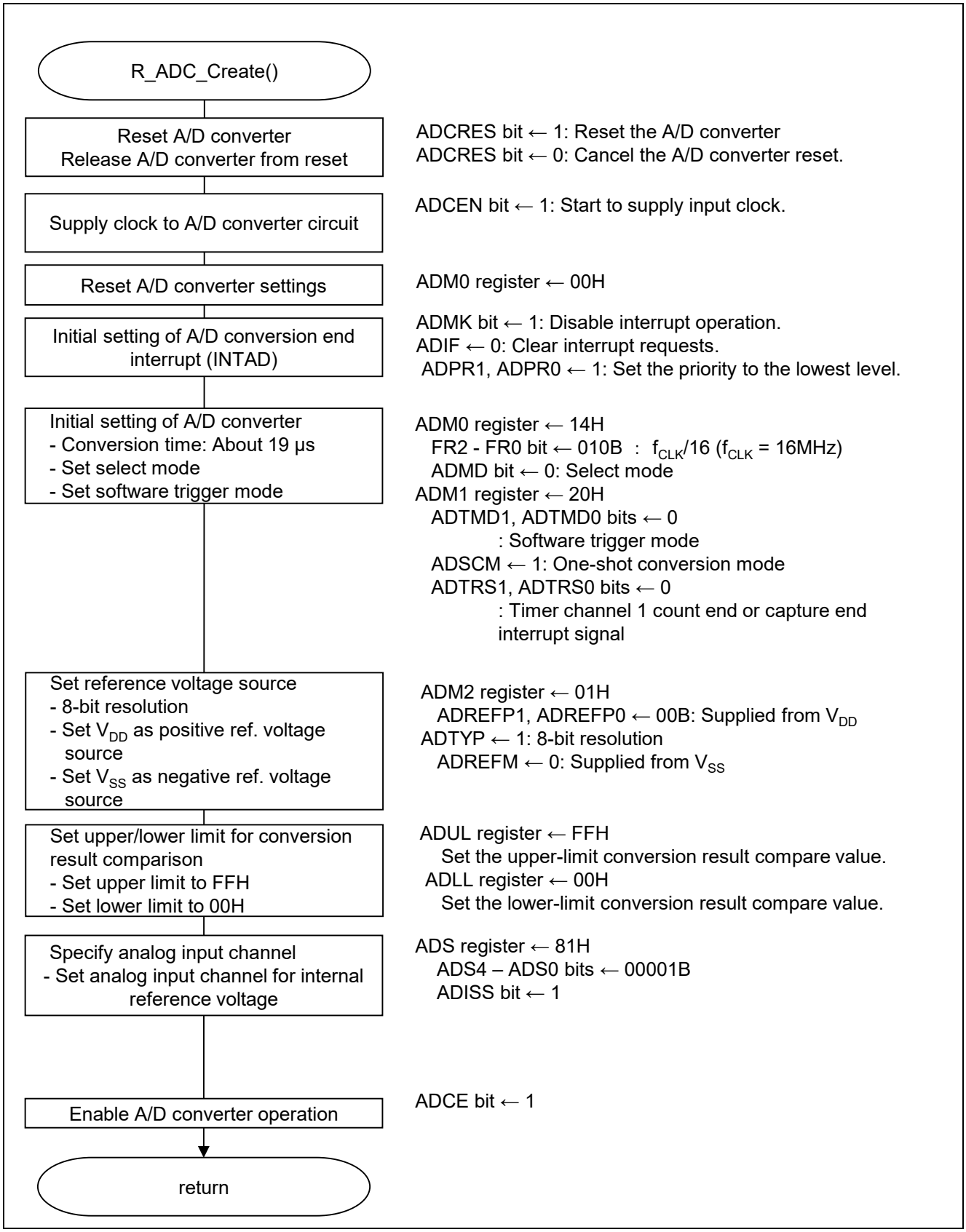

Figure 5.8 Setting A/D Converter

Controlling reset of A/D converter

- Peripheral reset control register 0 (PRR0)

Control reset of the A/D converter.

Symbol: PRR0

7	6	5	4	3	2	1	0
0	IICA1RES	ADCRES	IICA0RES	0	SAU0RES	0	TAU0RES
0	x	**1/0**	x	0	x	0	x

Bit 5

ADCRES	Reset control of A/D converter
0	**A/D converter reset release**
1	**A/D converter reset state**

Starting clock supply to A/D

- Peripheral enable register 0 (PER0)

Start supplying clock to the A/D converter.

Symbol: PER0

7	6	5	4	3	2	1	0
0	IICA1EN	ADCEN	IICA0EN	0	SAU0EN	0	TAU0EN
0	x	**1**	x	0	x	0	x

Bit 5

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Setting A/D conversion time and operation mode

- A/D converter mode register 0 (ADM0)

Control the A/D conversion operation.

Set the A/D conversion channel select mode.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
x	**0**	**0**	**1**	**0**	**1**	**0**	x

Bit 6

ADMD	Specification of A/D conversion channel selection mode
0	**Select mode**
1	Scan mode

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
x	**0**	**0**	**1**	**0**	**1**	**0**	x

Bits 5 to 1

ADM0					Mode	Conv clock (f_{AD})	No. of conv clock (Sampling clock)	Conv time	Conversion time selection				
FR2	FR1	FR0	LV1	LV0					f_{CLK}= 1MHz	f_{CLK}= 4MHz	f_{CLK}= 8MHz	f_{CLK}= 16MHz	f_{CLK}= 24MHz
0	0	0	1	0	Low-voltage 1	$f_{CLK}/64$	19 f_{AD} (No. of Sampling clock : 7 f_{AD})	$1216/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	76µs	50.667µs
0	0	1				$f_{CLK}/32$		$608/f_{CLK}$			76µs	38µs	25.333µs
0	1	0				$f_{CLK}/16$		$304f_{CLK}$		76µs	38µs	19µs	12.667µs
0	1	1				$f_{CLK}/8$		$152/f_{CLK}$		38µs	19µs	9.5µs	6.333µs
1	0	0				$f_{CLK}/6$		$114/f_{CLK}$		28.5µs	14.25µs	7.125µs	4.75µs
1	0	1				$f_{CLK}/5$		$76/f_{CLK}$	95µs	23.75µs	11.875µs	5.938µs	3.958µs
1	1	0				$f_{CLK}/4$		$86/f_{CLK}$	76µs	19µs	9.5µs	4.75µs	3.167µs
1	1	1				$f_{CLK}/2$		$38/f_{CLK}$	38µs	9.5µs	4.75µs	2.375µs	Setting prohibited
0	0	0	**1**	**1**	**Low-voltage 2**	$f_{CLK}/64$	**17 f_{AD} (No. of Sampling clock : 5 f_{AD})**	$1088/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	68µs	45.333µs
0	0	1				$f_{CLK}/32$		$544/f_{CLK}$			68µs	34µs	22.667µs
0	**1**	**0**				**$f_{CLK}/16$**		$272/f_{CLK}$		68µs	34µs	**17µs**	11.333µs
0	1	1				$f_{CLK}/8$		$136/f_{CLK}$		34µs	17µs	8.5µs	5.667µs
1	0	0				$f_{CLK}/6$		$102/f_{CLK}$		25.5µs	12.75µs	6.375µs	4.25µs
1	0	1				$f_{CLK}/5$		$85/f_{CLK}$	85µs	21.25µs	10.625µs	5.3125µs	3.542µs
1	1	0				$f_{CLK}/4$		$68/f_{CLK}$	68µs	17µs	8.5µs	4.25µs	2.833µs
1	1	1				$f_{CLK}/2$		$34/f_{CLK}$	34µs	8.5µs	4.25µs	2.125µs	Setting prohibited

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting A/D conversion trigger mode

- A/D converter mode register 1 (ADM1)
  Select the A/D conversion trigger mode.
  Specify the A/D conversion operation mode
  Select the hardware trigger signal.

Symbol: ADM1

7	6	5	4	3	2	1	0
ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0
0	**0**	**1**	0	0	0	**0**	**0**

Bits 7 and 6

ADTMD1	ADTMD0	Selection of A/D conversion trigger mode
0	**x**	**Software trigger mode**
1	0	Hardware trigger no-wait mode
1	1	Hardware trigger wait mode

Bit 5

ADSCM	Specification of A/D conversion mode
0	Sequential conversion mode
1	**One-shot conversion mode**

Bits 1 and 0

ADTRS1	ADTRS0	Selection of hardware trigger signal
0	**0**	**End of timer channel 1 count or capture interrupt signal (INTTM01)**
0	1	Event signal selected by ELC
1	0	Real-time clock 2 interrupt signal (INTRTC)
1	1	12-bit interval timer interrupt signal (INTIT)

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting reference voltage source

- A/D converter mode register 2 (ADM2)

Select the A/D converter positive-side reference voltage source.
Select the A/D converter negative-side reference voltage source.
Check the conversion result upper-limit/lower-limit value
Set SNOOZE mode.
Select A/D conversion resolution.

Symbol: ADM2

7	6	5	4	3	2	1	0
ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADTYP
0	**0**	**0**	0	**0**	**0**	0	**1**

Bits 7 and 6

ADREFP1	ADREFP0	Selection of + side reference voltage source of A/D converter
0	**0**	**Supplied from V_{DD}**
0	1	Supplied from AV_{REFP}/ANI
1	0	Supplied from internal reference voltage（1.45 V）
1	1	Setting prohibited

Bit 5

ADREFM	Selection of – side reference voltage source of A/D converter
0	**Supplied from V_{SS}**
1	Supplied from AV_{REFM}/ANI1

Bit 3

ADRCK	Checking upper limit and lower limit conversion result values
0	**Interrupt signal (INTAD) is generated when the ADLL register ≤ the ADCR register ≤ the ADUL register.**
1	Interrupt signal (INTAD) is generated when ADCR register < ADLL register, ADUL register < ADCR register.

Bit 2

AWC	Specification of SNOOZE mode
0	**Do not use the SNOOZE mode function.**
1	Use the SNOOZE mode function.

Bit 0

ADTYP	Selection of A/D conversion resolution
0	10-bit resolution
1	**8-bit resolution**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting upper limit and lower limit values for conversion result comparison

- Conversion result comparison upper limit setting register (ADUL)
- Conversion result comparison lower limit setting register (ADLL)

Set the upper limit and lower limit conversion result compare values.

Symbol: ADUL

7	6	5	4	3	2	1	0
ADUL7	ADUL6	ADUL5	ADUL4	ADUL3	ADUL2	ADUL1	ADUL0
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Symbol: ADLL

7	6	5	4	3	2	1	0
ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting input channel

- Analog input channel specification register (ADS)
  Specify the input channel of analog voltage to be converted.

Symbol: ADS

7	6	5	4	3	2	1	0
ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0
0	0	0	**0**	**0**	**0**	**0**	**0**

Bits 7, 4 to 0

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	0	0	0	0	0	ANI0	P20/ANI0/AV_{REFP} pin
0	0	0	0	0	1	ANI1	P21/ANI1/AV_{REFM} pin
0	0	0	0	1	0	ANI2	P22/ANI2 pin
0	0	0	0	1	1	ANI3	P23/ANI3 pin
0	1	0	0	0	0	ANI16	P01/ANI16 pin
0	1	0	0	0	1	ANI17	P00/ANI17 pin
0	1	0	0	1	0	ANI18	P33/ANI18 pin
0	1	0	0	1	1	ANI19	P32/ANI19 pin
0	1	0	1	0	0	ANI20	P31/ANI20 pin
0	1	0	1	0	1	ANI21	P30/ANI21 pin
0	1	0	1	1	0	ANI22	P56/ANI22 pin
0	1	0	1	1	1	—	PGAOUT(PGA output)
1	0	0	0	0	0	—	Temperature sensor output voltage note1
1	**0**	**0**	**0**	**0**	**1**	**—**	**Internal reference voltage (1.45V) note1**
上記以外						設定禁止	

Note1: Operation is possible only in HS (high-speed main) mode.

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting A/D conversion end interrupt

- Interrupt request flag register (IF1H)
  Clear interrupt request flags.
- Interrupt mask flag register (MK1H)
  Disable interrupt processing.

Symbol: IF1H

7	6	5	4	3	2	1	0
PIF11	PIF00	PIF9	PIF8	PIF7	KRIF	ITIF	ADIF
x	x	x	x	x	x	x	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK1H

7	6	5	4	3	2	1	0
PMK11	PMK10	PMK9	PMK8	PMK7	KRMK	TMKAMK	ADMK
x	x	x	x	x	x	x	**1**

Bit 0

ADMK	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

5.5.8 Setting 16-Bit Timer KB0

Figure 5.9 shows the flowchart for setting the 16-bit timer KB0.

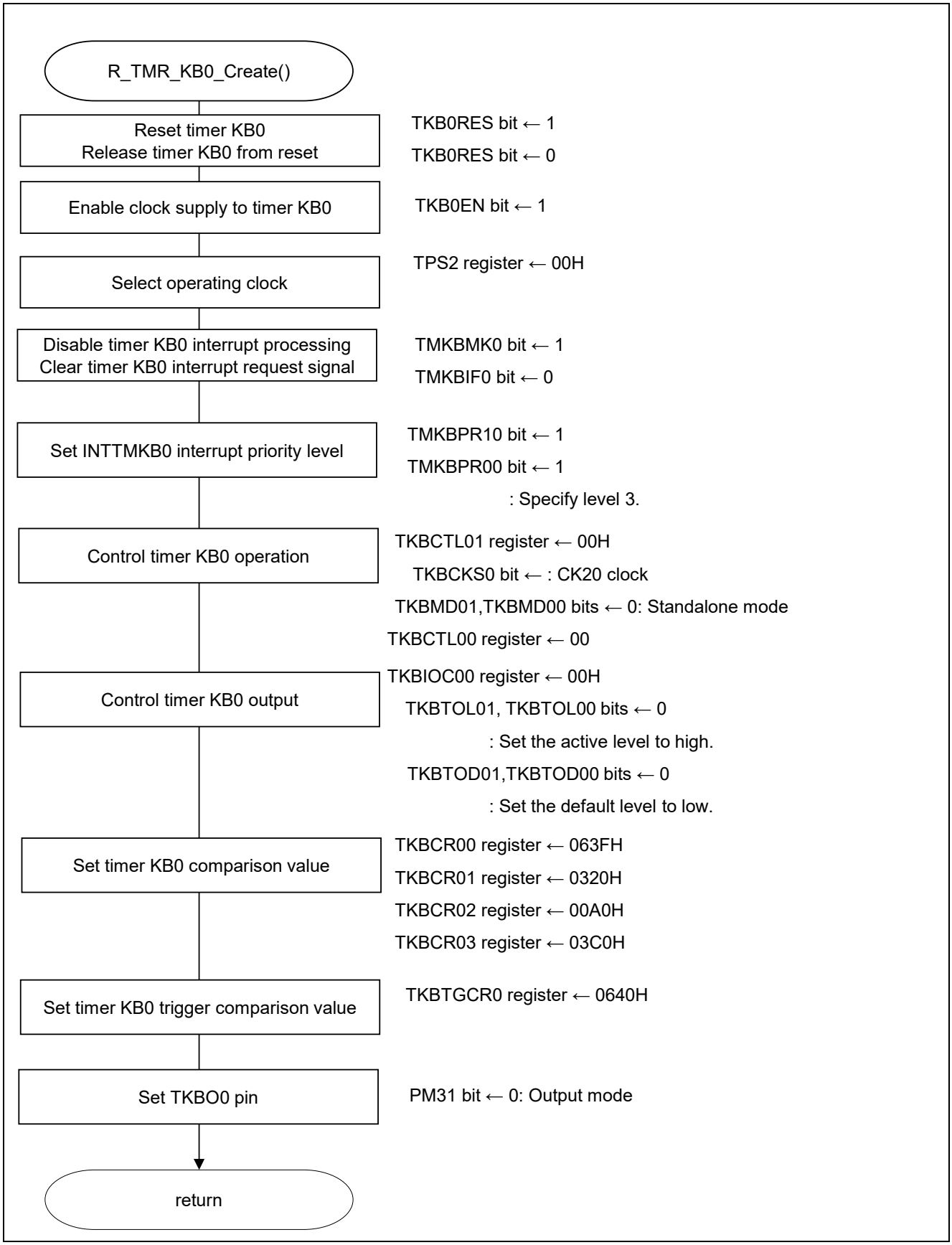

Figure 5.9 Setting 16-Bit Timer KB0

Controlling reset of timer KB0

- Peripheral reset control register 2 (PRR2)

Control reset of the timer KB0.

Symbol: PRR2

7	6	5	4	3	2	1	0
TMKARES	0	DOCRES	0	0	0	0	TKB0RES
x	0	x	0	0	0	0	**0/1**

Bit 0

TKB0RES	Reset control of timer KB0
0	**Timer KB0 reset release**
1	**Timer KB0 reset state**

Starting clock supply to timer KB0

- Peripheral enable register 2 (PER2)

Start supplying clock to the timer KB0.

Symbol: PER2

7	6	5	4	3	2	1	0
TMKAEN	0	DOCEN	0	0	0	0	TKB0EN
x	x	x	0	0	0	0	**1**

Bit 0

TKB0EN	Control of timer KB0 input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting timer KB end interrupt

- Interrupt request flag register (IF2L)
  Clear interrupt request flags.
- Interrupt mask flag register (MK2L)
  Disable interrupt processing.

Symbol: IF2L

7	6	5	4	3	2	1	0
FLIF	IICAIF1	TMKBIF0	ITIF01	ITIF00	DOCIF	CMPIF1	CMPIF0
x	x	**0**	x	x	x	x	x

Bit 5

TMKBIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK2L

7	6	5	4	3	2	1	0
FLMK	IICAMK1	TMKBMK0	ITMK01	ITMK00	DOCMK	CMPMK1	CMPMK0
x	x	**1**	x	x	x	x	x

Bit 5

TMKBMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

5.5.9 Setting Interrupt

Figure 5.10 shows the flowchart for setting the Interrupt.

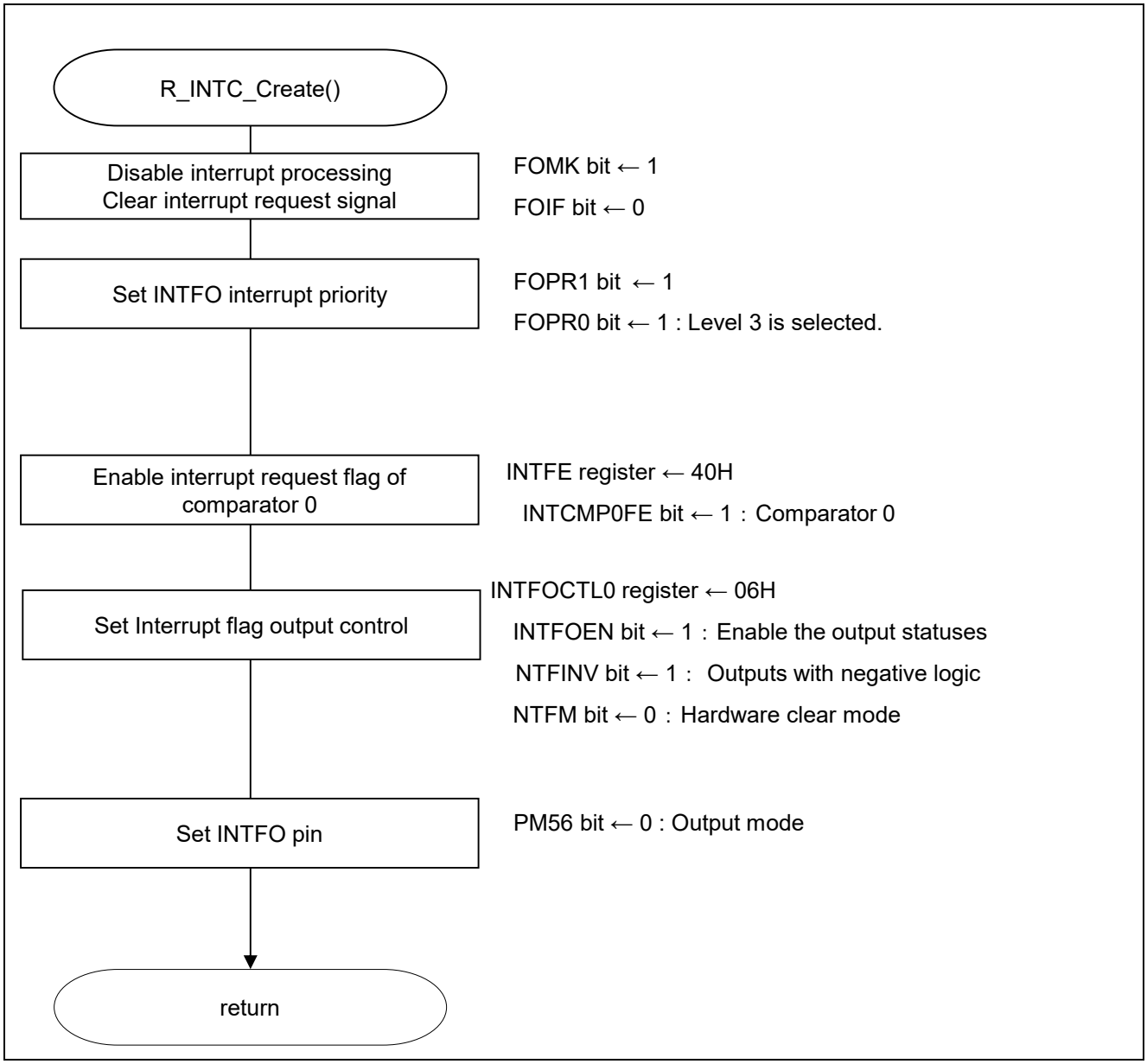

Fig 5.10 Setting Interrupt

Setting INTFO interrupt

- Interrupt request flag register (IF2H)
  Clear the interrupt request flag.
- Interrupt mask flag register (MK2H)
  Disable the interrupt processing.

Symbol: IF2H

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	FOIF
0	0	0	0	0	0	0	**0**

Bit 0

FOIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK2H

7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	FOMK
1	1	1	1	1	1	1	**1**

Bit 0

FOMK	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting Interrupt flag control

- Interrupt flag enable register (INTFE)
  Set enable/disable of changing interrupt request flags.
- Interrupt flag output control register 0 (INTFOCTL0)
  Control output statuses of interrupt request flags.

Symbol: INTFE

7	6	5	4	3	2	1	0
INTCMP1FE	INTCMP0FE	INTDOCFE	INTTMKB0FE	INTIT01FE	INTIT00FE	INTITFE	INTADFE
0	**1**	0	0	0	0	0	0

Bit 6

INTCMO0FE	Selection of whether to enable or disable the changing interrupt request flag of comparator 0
0	Disable the changing interrupt request flag
1	**Enable the changing interrupt request flag**

Symbol: INTFOCTL0

7	6	5	4	3	2	1	0
0	0	0	0	0	INTFOEN	INTFINV	INTFM
0	0	0	0	0	**1**	**1**	**0**

Bit 2

INTFOEN	Selection of whether enable or disable the output of statuses of interrupt request flags
0	Disable the output statuses
1	**Enable the output statuses**

Bit 1

INTFINV	Select the logic of output status of interrupt request flags
0	Outputs with positive logic (non-inverted)
1	**Outputs with negative logic (inverted)**

Bit 0

INTFM	Select the output mode of status of interrupt request flags
0	**Hardware clear mode** **The output is same as interrupt request signal and is not to be cleared by software**
1	Software clear mode The output is only able to be cleared by software The output is not able to be cleared by hardware

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

5.5.10 Main Function

Figure 5.11 shows the flowchart for the main function.

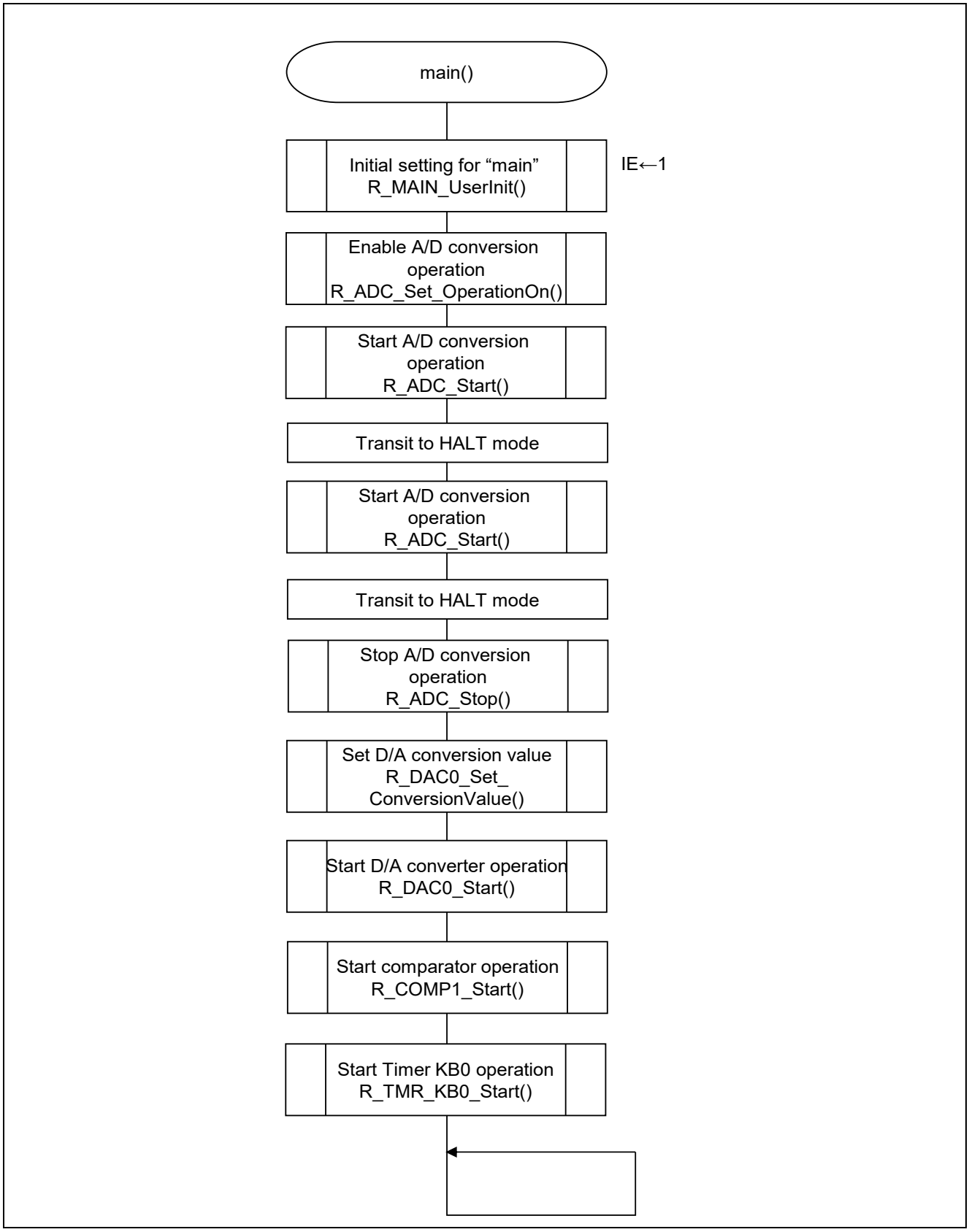

Figure 5.11 Main Function

5.5.11 Initial Setting for “main”

Figure 5.12 shows the flowchart of the initial setting for “main”.

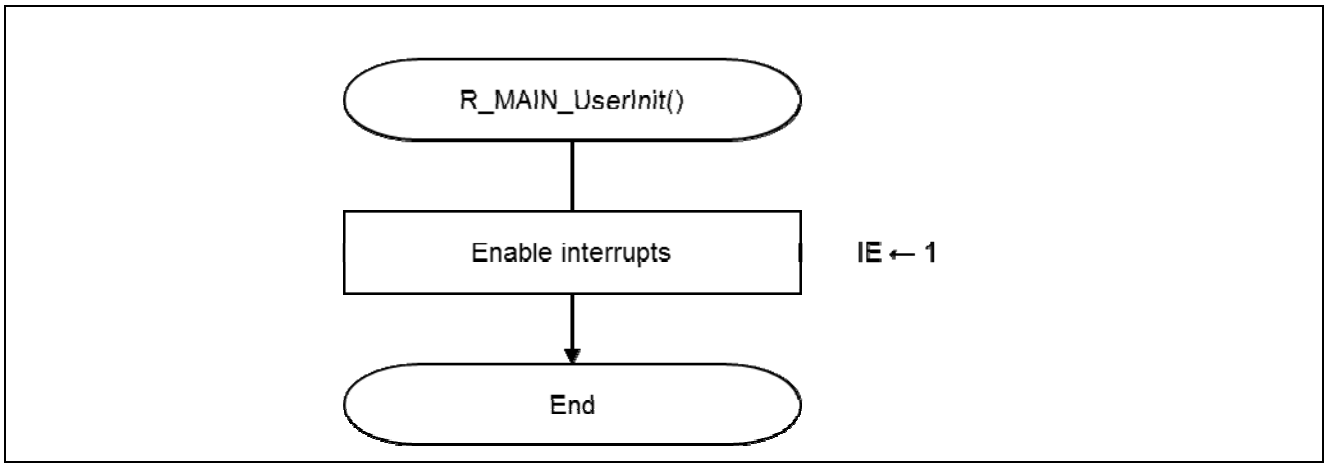

Figure 5.12 Initial Setting for “main”

5.5.12 A/D Converter Operation Start Function

Figure 5.13 shows the flowchart of the A/D converter operation start function.

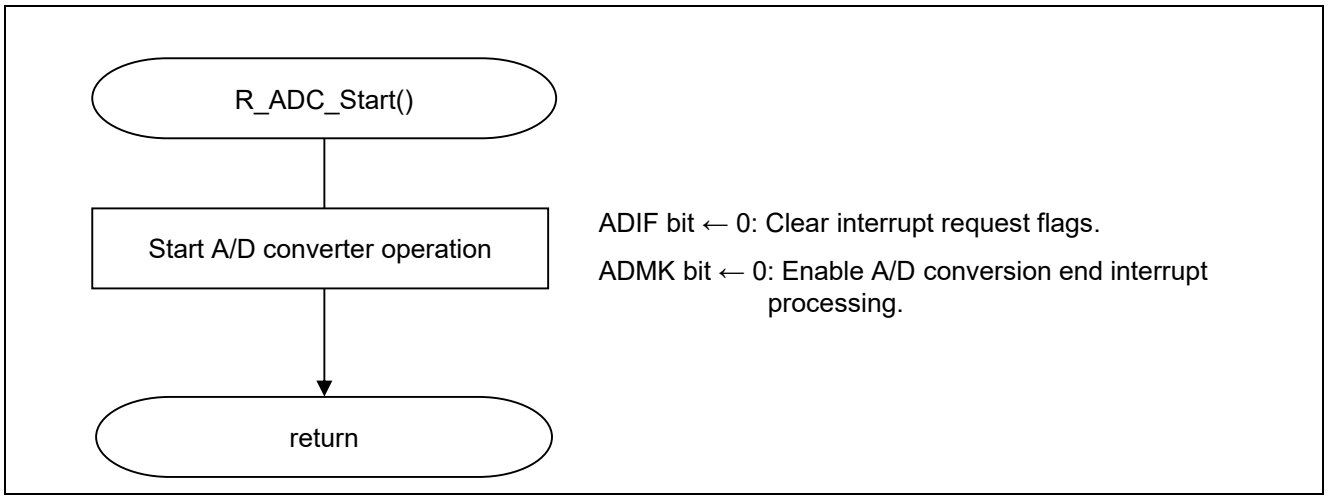

Figure 5.13 A/D Converter Operation Start Function

5.5.13 A/D Converter Operation Stop Function

Figure 5.14 shows the flowchart of the A/D converter operation stop function.

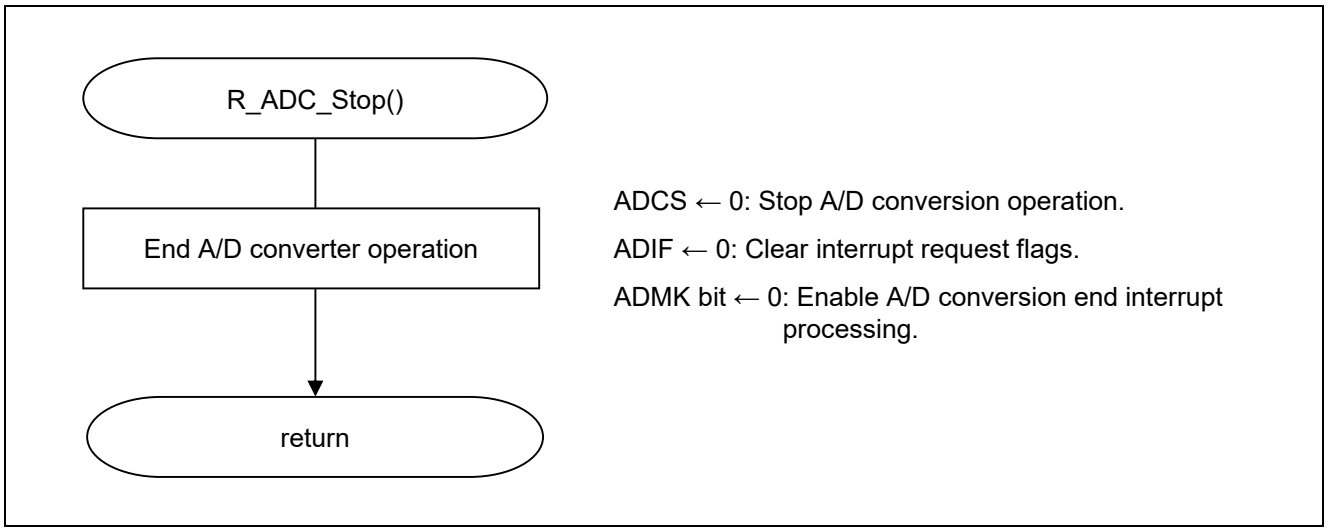

Figure 5.14 A/D Converter Operation Stop Function

5.5.14 A/D Converter Operation Enable Function

Figure 5.15 shows the flowchart of the A/D converter operation enable function.

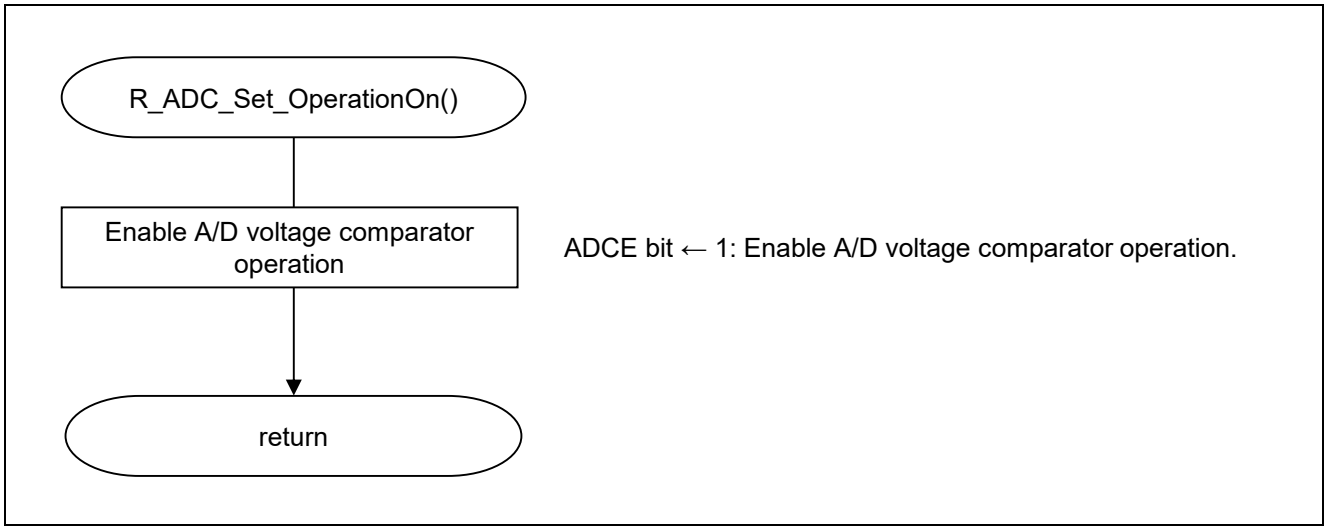

Figure 5.15 A/D Converter Operation Enable Function

5.5.15 D/A Converter Operation Start Function

Figure 5.16 shows the flowchart of the D/A conversion start function.

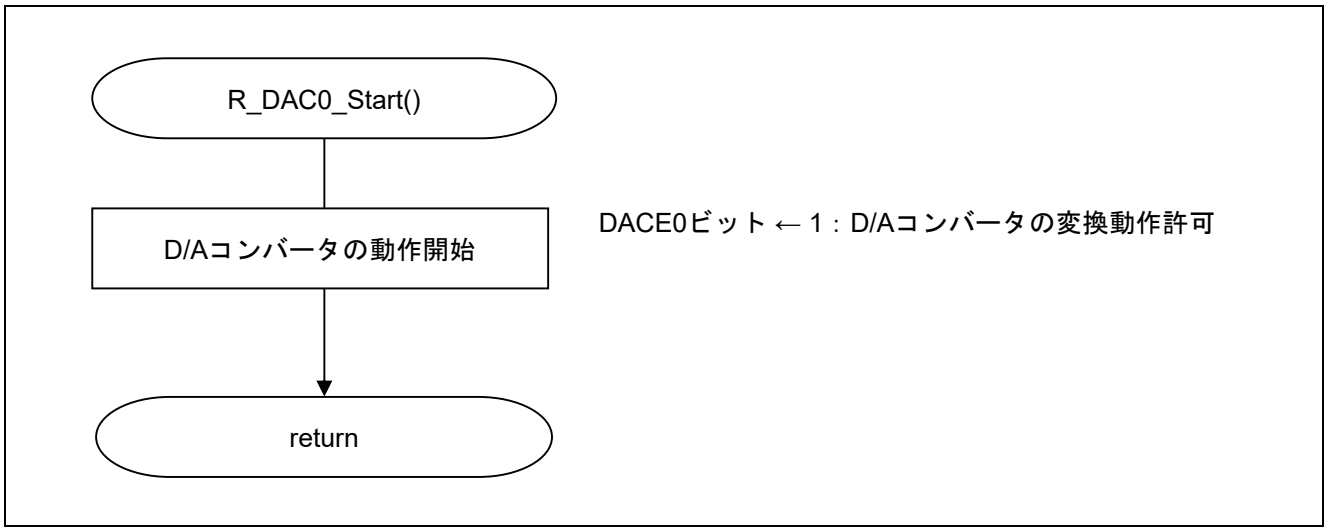

Figure 5.16 D/A Converter Operation Start Function

5.5.16 Comparator 0 Operation Start Function

Figure 5.17 shows the flowchart for the comparator 0 operation start function.

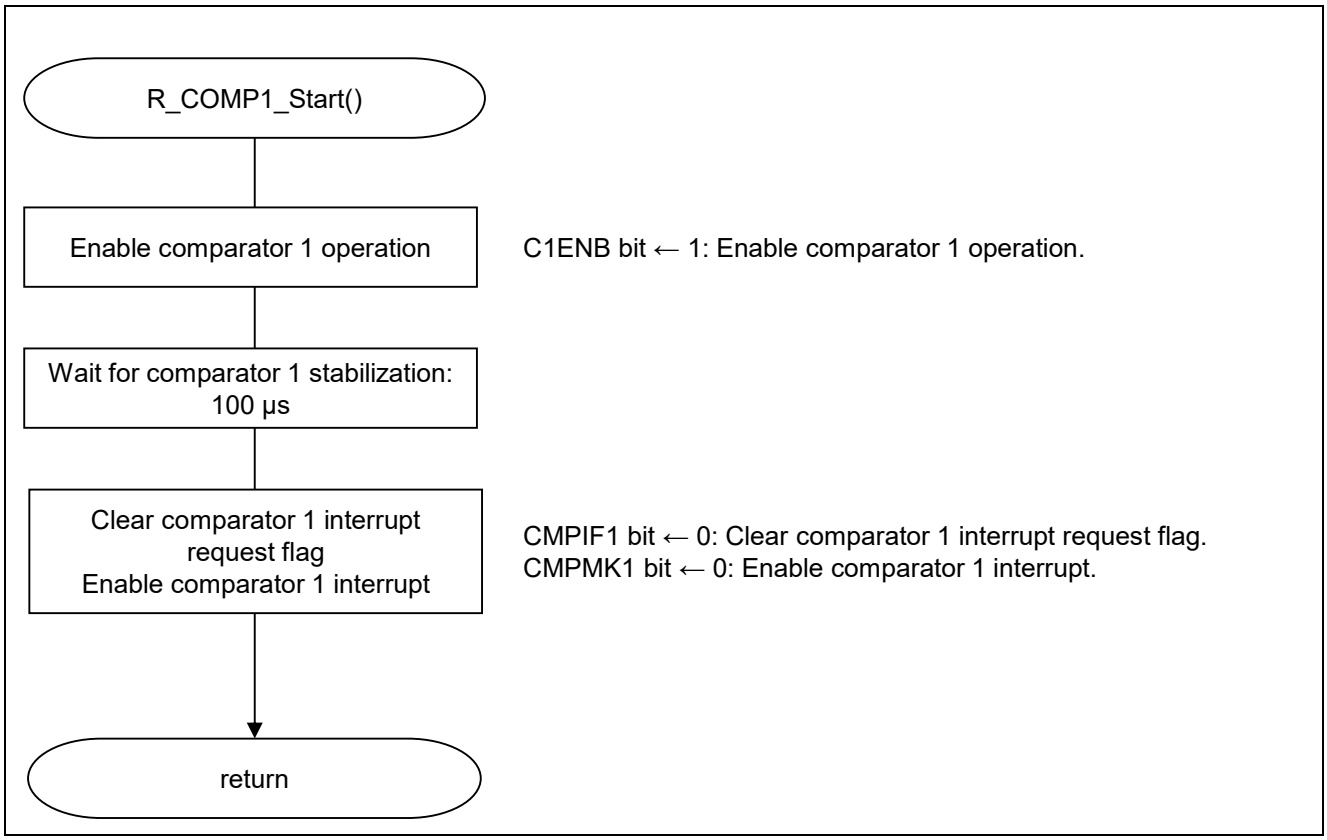

Figure 5.17 Comparator 0 Operation Start Function

5.5.17 Timer KB0 Operation Start Function

Figure 5.18 shows the flowchart of the Timer KB0 operation start function.

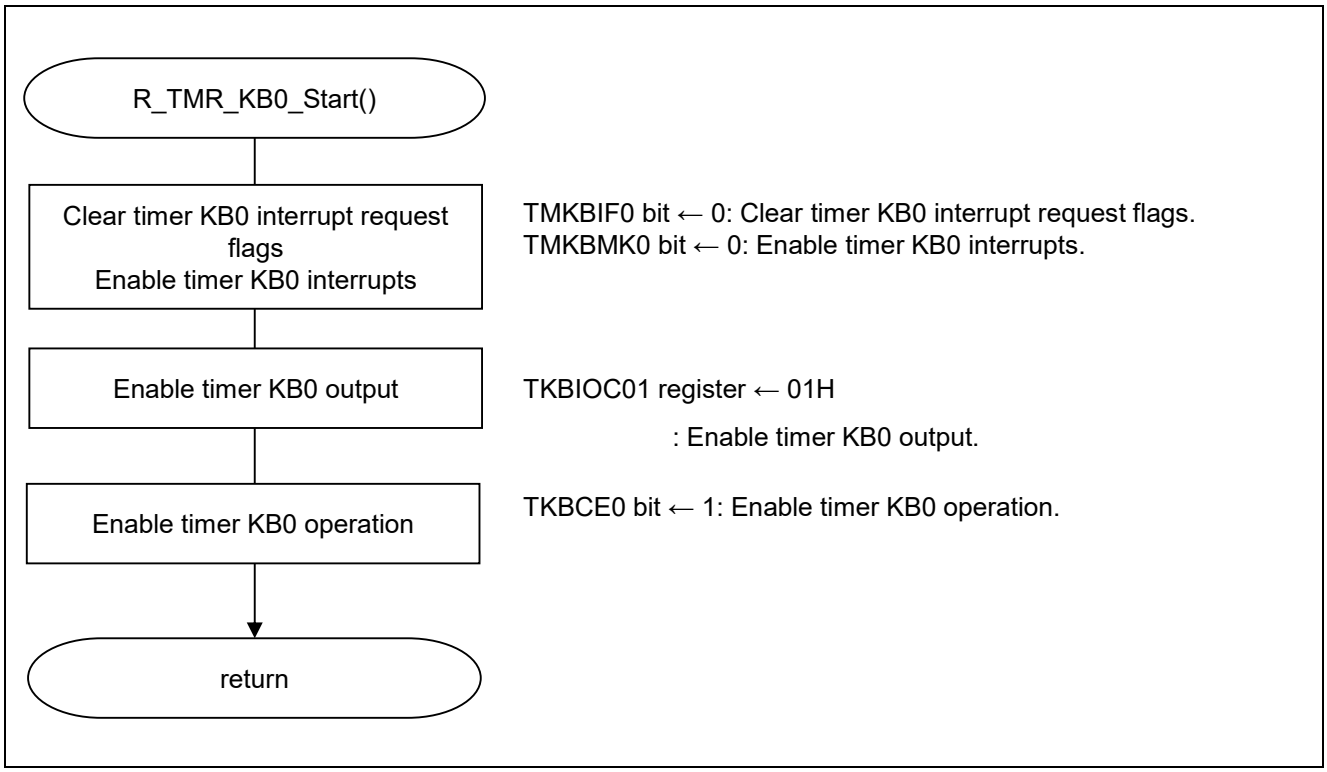

Figure 5.18 Timer KB0 Operation Start Function

5.5.18 D/A Conversion value set Function

Figure 5.19 shows the flowchart of the D/A conversion value set function.

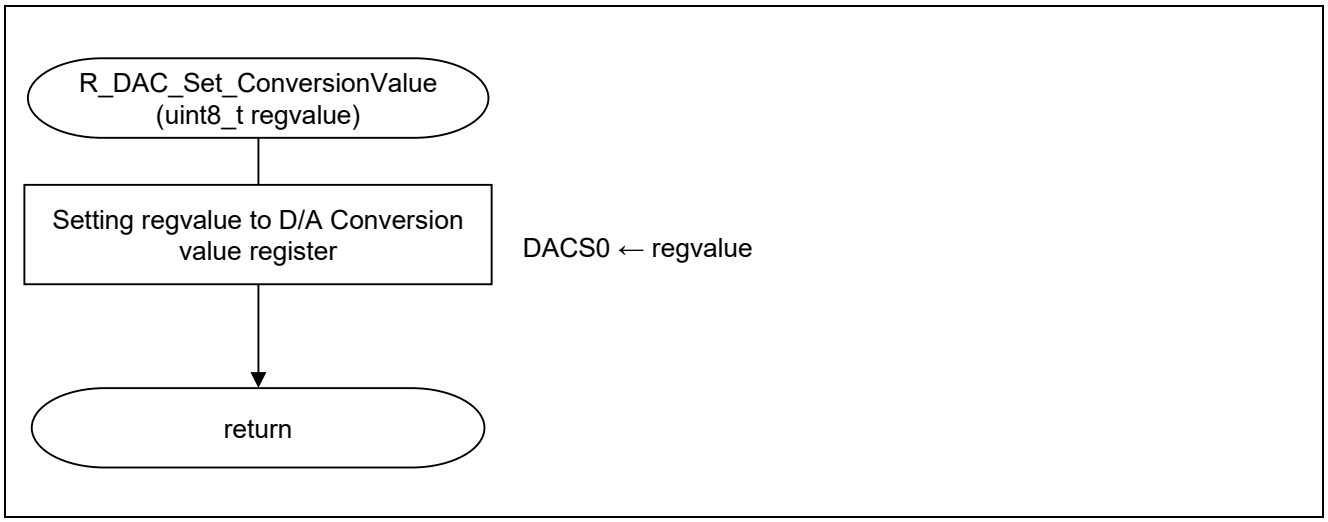

Figure 5.19 D/A Conversion value set Function

6. Sample Code

The user can get the sample code from the Renesas Electronics website.

7. Reference Documents

RL78/G11 User's Manual: Hardware (R01UH0637E)

RL78 Family User's Manual: Software (R01US0015E)

(Get the latest version from the Renesas Electronics website.)

Technical Updates/Technical News

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Revision History	RL78/G11 Battery Voltage Monitoring CC-RL

Rev.	Date	Revision Contents	
		Page	Description
1.00	Dec. 19, 2016	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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