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# RL78/G10

## Single-Wire UART Communication

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### Introduction

Making a single pin serve for a double purpose, transmission and reception, saves the number of pins used for communication. This application note explains how to perform the single-wire UART communication that a pin used for the UART reception by the serial array unit (SAU) and the UART transmission by the timer array unit (TAU) of RL78/G10. Data which is same as ASCII characters transmitted from the device on the opposite side is transmitted to the device on the opposite side.

### Target Device

RL78/G10

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

## Contents

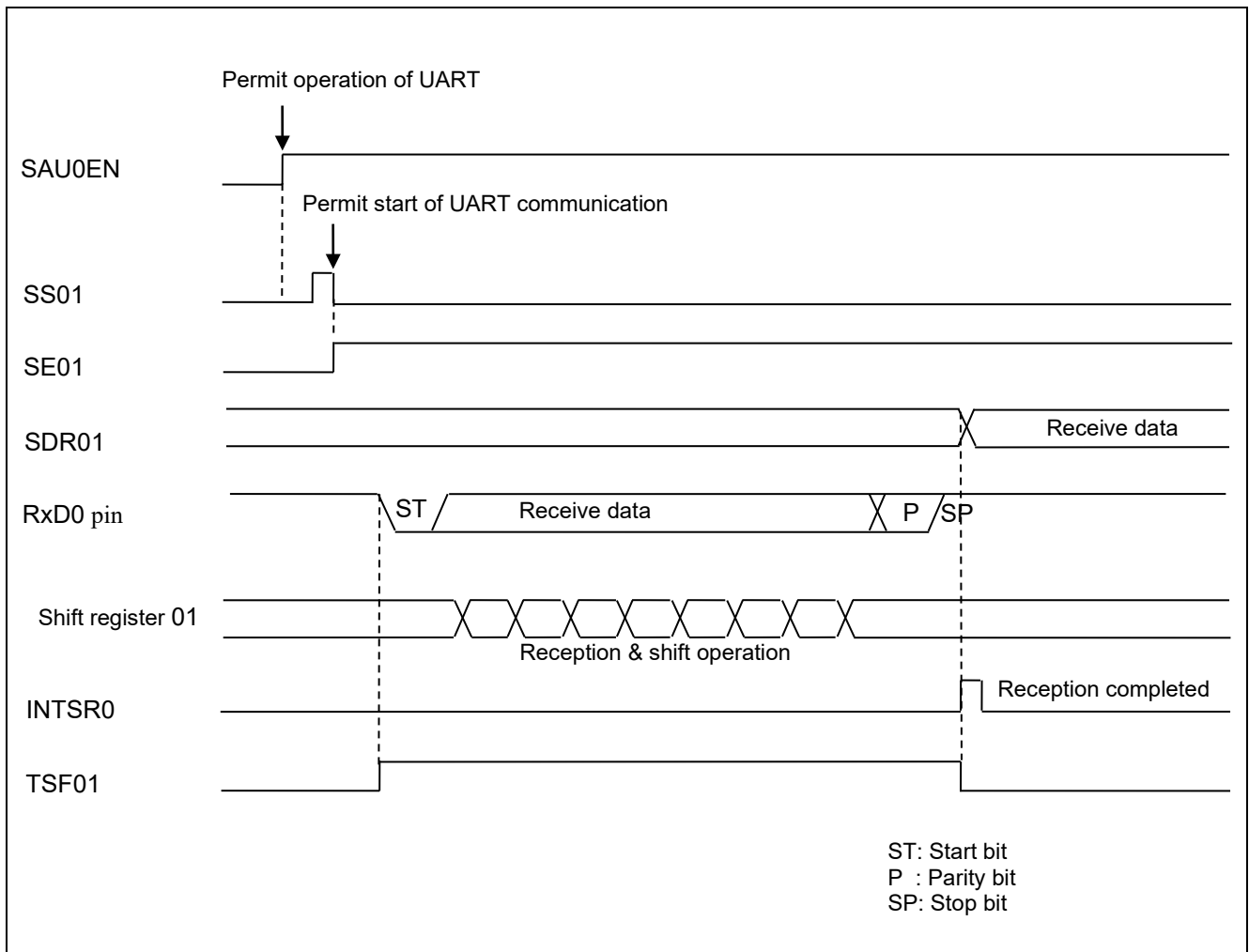
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### 1. Specifications

Table 1.1 shows the peripheral function to be used and its use. Figure 1.1 shows the UART reception timing, and Figure 1.2 shows the UART transmission timing.

**Table 1.1 Peripheral Function to be Used and its Use**

Peripheral Function	Use
Serial array unit	UART reception
Timer array unit	UART transmission timing generation
Port function	UART transmission



**Figure 1.1 UART Reception Timing Chart**

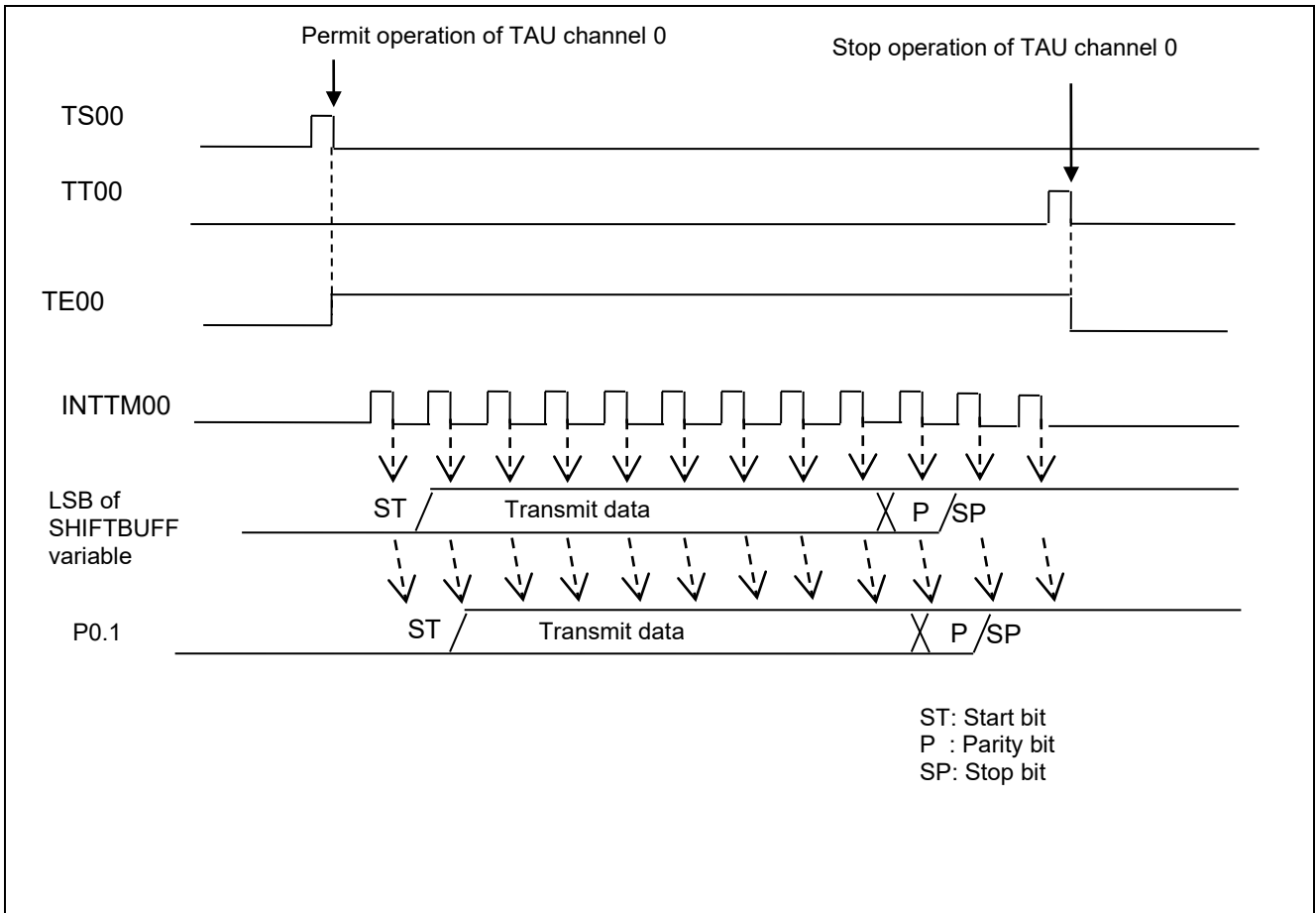


Figure 1.2 UART Transmission Timing Chart

## 2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

**Table 2.1 Operation Check Conditions**

Item	Description
Microcontroller used	RL78/G10 (R5F10Y16ASP)
Operating frequency	<ul style="list-style-type: none"> <li>· High-speed on-chip oscillator (HOCO) clock: 20MHz</li> <li>· CPU/peripheral hardware clock: 20MHz</li> </ul>
Operating voltage	5.0V (can run at a voltage range of 2.9 V to 5.5 V.) SPOR operation: VSPOR = 2.90V (TYP.), VSPDR = 2.84V (TYP.) (reset occurrence: $VDD < 2.84V$ , reset release: $VDD \geq 2.90V$ )
Integrated development environment (CS+)	CS+ for CA, CX V3.00.00 from Renesas Electronics Corp.
Assembler (CS+)	RA78K0R V1.70 from Renesas Electronics Corp.
Integrated development environment (e2studio)	e2studio V3.1.2.10 from Renesas Electronics Corp.
Assembler (e2studio)	KPIT GNURL78-ELF Toolchain V14.03 from Renesas Electronics Corp.
Board to be used	RL78/G10 target board (QB-R5F10Y16-TB)

## 3. Related Application Note

The application note that is related to this application note is listed below for reference.

- RL78/G10 Initialization (R01AN1454E) Application Note

## 4. Description of the Hardware

### 4.1 Hardware Configuration Example

Figure 4.1 shows a connection example.

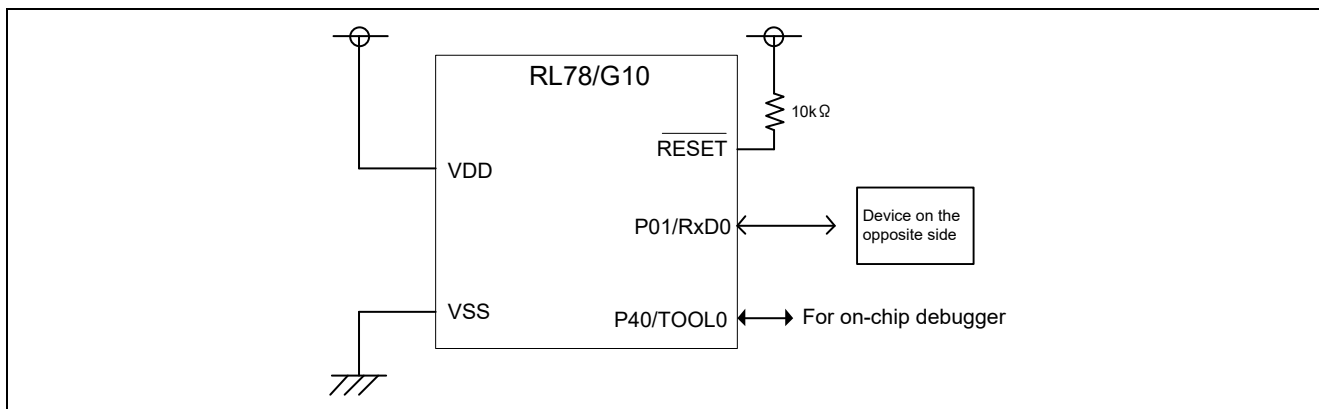


Figure 4.1 Connection Example

### 4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their function.

Table 4.1 Pins to be Used and their Functions

Pin Name	I/O	Description
P01/RxD0	I/O	UART transmission/reception

## 5. Description of the Software

### 5.1 Operation Outline

In this sample code, the same data as the data received from the device on the opposite side is transmitted to the device on the opposite side.

(1) Performs initial setting of UART.

<UART Setting Conditions>

- Uses SAU0 channel 1 as UART (reception function).
- Uses the P01/RxD0 pin for data input.
- The data length is 8 bits or 7 bits.
- The order of data transfer is set with LSB first.
- For the parity setting, one is chosen from even parity, odd parity and no parity by DEV&TM\_CH.inc. In default configuration, it is set to even parity.
- Sets the receive data level to standard (non-inverted).
- The transfer rate is selectable by DEV&TM\_CH.inc. A default value is 76800 bps.
- Uses reception end interrupt (INTSR0).
- Selects interrupt priority level 3 (low interrupt priority level) for INTSR0.

(2) Performs initial setting of TAU.

When carrying out UART transmission using a port function, TAU is used to generate the transmitting timing which is a baud rate. A default setup is as follows: the operation of a high-speed on-chip oscillator is performed at 20 MHz and a target baud rate is 76800 bps.

<TAU Setting Conditions>

- Uses channel 0 (uses INTTM00 interrupt).
- Sets count clock  $f_{\text{TCLK}} = \text{CK00} = f_{\text{CLK}}$  (20MHz).
- Only a software trigger is enabled.
- Interval timer mode
- Because 76800bps is generated at 20MHz, the count value will be 260 (0x104):  $20\text{M} \div 76800 = 260$  (0x104). Therefore, the setup value to TDR00 register is 259 (0x103):  $260 - 1 = 259$  (0x103): TDR00H = 01H and TDR00L = 03H.
- Since a timer output pin is not used, the output to TO00 pin by timer operation is set as disabled.

(3) After the system is made to enter a UART communication wait state by using the serial array unit channel 1 start bit, it stands by in the loop processing in a main function. When the reception end interrupt (INTSR0) is generated, it takes received data and enters into a transmitting processing TxDATA function continuously.

(4) A bit string for transmission is created in LSB-first format in the TxDATA function. Received data is arranged to the lower bits of 16-bit variable and 0xFF is set to the upper bit to use as STOP bit or a parity bit (when a value is 1). If this 16-bit variable is shifted 1-bit to the left, 0 will be written in the least significant bit and this will be used as a START bit. When a parity bit is required, it is added after computing a parity value. Now, the bit string of transmission data is completed. Finally, in order to switch from UART reception to UART transmission, SAU channel 1 (UART reception) is stopped, P01 pin is switched to output mode, and the TAU channel 0 is set to starting of operation for data transmission timing generation.

- (5) A TAU channel 0 interrupt function is performed periodically. Whenever this interruption function is performed, UART transmission for 1 bit is performed. Executing frequency is 76923bps:  $20\text{MHz} / (0x103+1) = 76923\text{bps}$ . In this interrupt function, UART transmission is realized by shifting the bit string of the UART transmission data created in the preceding paragraph to 1-bit right for moving a LSB to CY flag and setting the contents of this CY flag to a port. After this interrupt function is performed by the predetermined number of times, in order to finish UART transmission and to return to UART reception standby, operation of TAU channel 0 is stopped and the SAU channel 1 (UART reception) is set to starting operation.

In addition, in order to raise the accuracy of the cycle of UART transmission, this interruption is always set as the priority level 0 (high priority). When other interrupt functions are added to this sample program, EI command is executed by processing of the beginning of that interrupt function, multi-interrupt operation is enabled as promptly as possible, and designing to shift to this TAU channel 0 interrupt function is required.



## 5.2 List of Option Byte Settings

Table 5.1 lists the option byte settings.

Table 5.1 Option Byte Settings Used in the Sample Code

Address	Value	Description
000C0H	1110 1110B	Disables the watchdog timer.
000C1H	1111 0111B	P12.5 pin is used as RESET pin. When reset occurs: 2.84 V (TYP.) When reset is released: 2.90 V (TYP.)
000C2H	1111 1001B	HOCO: 20 MHz
000C3H	1000 0101B	Enables the on-chip debugging.

## 5.3 List of variables

Table 5.2 lists the global variables.

Table 5.2 Global Variables

Type	Variable Name	Contents	Function Used
1-byte are	Rxstate	Reception status of data	SINITAU, RxDATA, RxSTATUS, IINTSR0
1-byte are	RxDtbuf	Storing of received data	(It is accessed by the 2-byte access command to Rxstate.)
2-byte are	SHIFTBUF	Storing of transmission data (9 – 11 bits)	TxDATA, IINTTM0n
1-byte are	BITCOUNT	Remaining number of times of the transmission	TxSTATUS, WAIT_TxEND, TxDATA, IINTTM0n
1-byte are	BITMASK	8-bit data: 0x00 7-bit data: 0x80	TxDATA
1-byte are	WORK	The work area used in the process in which a parity bit is generated.	TxDATA

## 5.4 List of Functions

Table 5.3 shows functions.

**Table 5.3 Functions**

Function Name	Outline
RESET_START	Overall flow
main	Main function
RxSTATUS	UART reception status check function
RxDATA	UART receiving data extract function
TxDATA	UART data transmission preparation function
WAIT_TxEND	UART transmission end wait function
SINIPOINT	I/O initialization
SINICLK	CPU clock initialization
SINITAU	Timer array unit initialization
SINISAU	Serial array unit initialization
IINTSR0	UART reception end interrupt
IINTTM0n	TAU channel 0 interrupt

## 5.5 Function Specifications

This section describes the specifications for the functions that are used in the sample code.

[Function Name] RESET_START	
<b>Synopsis</b>	Overall flow
<b>Header</b>	DEV&TM_CH.inc
<b>Explanation</b>	Initializes Stack pointer, port function, CPU clock, timer array unit (TAU), and serial array unit (SAU), and executes main function.
<b>Argument</b>	None : [Explanation]
<b>Return value</b>	None
[Function Name] main	
<b>Synopsis</b>	Main function
<b>Header</b>	DEV&TM_CH.inc
<b>Explanation</b>	Waits for UART reception by serial array unit (SAU). When a reception is detected, starts timer array unit (TAU), and performs UART transmission by the port.
<b>Argument</b>	None
<b>Return value</b>	None
[Function Name] RxSTATUS	
<b>Synopsis</b>	UART reception status check function
<b>Header</b>	DEV&TM_CH.inc
<b>Explanation</b>	The existence of UART received data is reflected on CY flag.
<b>Argument</b>	None
<b>Return value</b>	CY
[Function Name] RxDATA	
<b>Synopsis</b>	UART receiving data extract function
<b>Header</b>	DEV&TM_CH.inc
<b>Explanation</b>	Reads received data (variable RxDTbuff) into A register and reception status information (variable Rxstatus) into X register, and clears Variable Rxstatus to 0.
<b>Argument</b>	None
<b>Return value</b>	AX
[Function Name] TxDATA	
<b>Synopsis</b>	UART data transmission preparation function
<b>Header</b>	DEV&TM_CH.inc
<b>Explanation</b>	Arranges the data for UART transmission to Variable SHIFTBUFF by LSB first. The length and the contents of data change with data bit length and the existence of parity bits.
<b>Argument</b>	AX
<b>Return value</b>	None

---

**[Function Name]** WAIT\_TxEND

---

<b>Synopsis</b>	UART transmission end wait function
<b>Header</b>	DEV&TM_CH.inc
<b>Explanation</b>	Waits until UART data transmission is completed.
<b>Argument</b>	None
<b>Return value</b>	None

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**[Function Name]** SINIPORT

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<b>Synopsis</b>	I/O initialization
<b>Header</b>	DEV&TM_CH.inc
<b>Explanation</b>	Initializes the port function.
<b>Argument</b>	None
<b>Return value</b>	None

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**[Function Name]** SINICLK

---

<b>Synopsis</b>	CPU clock initialization
<b>Header</b>	DEV&TM_CH.inc
<b>Explanation</b>	Initializes the CPU clock.
<b>Argument</b>	None
<b>Return value</b>	None

---

**[Function Name]** SINITAU

---

<b>Synopsis</b>	Timer array unit initialization
<b>Header</b>	DEV&TM_CH.inc
<b>Explanation</b>	Initializes the timer array unit (TAU).
<b>Argument</b>	None
<b>Return value</b>	None

---

**[Function Name]** SINISAU

---

<b>Synopsis</b>	Serial array unit initialization
<b>Header</b>	DEV&TM_CH.inc
<b>Explanation</b>	Initializes the serial array unit (SAU).
<b>Argument</b>	None
<b>Return value</b>	None

---

**[Function Name]** IINTSR0

---

<b>Synopsis</b>	UART reception end interrupt
<b>Header</b>	DEV&TM_CH.inc
<b>Explanation</b>	Stores the reception data into Variable RxDTbuff and the reception status information into Variable Rxstatus.
<b>Argument</b>	None
<b>Return value</b>	None

---

[Function Name] IINTTM0n

---

<b>Synopsis</b>	TAU channel 0 interrupt
<b>Header</b>	DEV&TM_CH.inc
<b>Explanation</b>	Outputs the LSB of Variable SHIFTBUFF to P0.1, and performs UART transmission. After that, shifts 1 bit to the right of SHIFTBUFF, saves it, and prepares for transmission of the following bit.
<b>Argument</b>	None
<b>Return value</b>	None

### 5.6 Flowcharts

Figure 5.1 shows the overall flowchart.

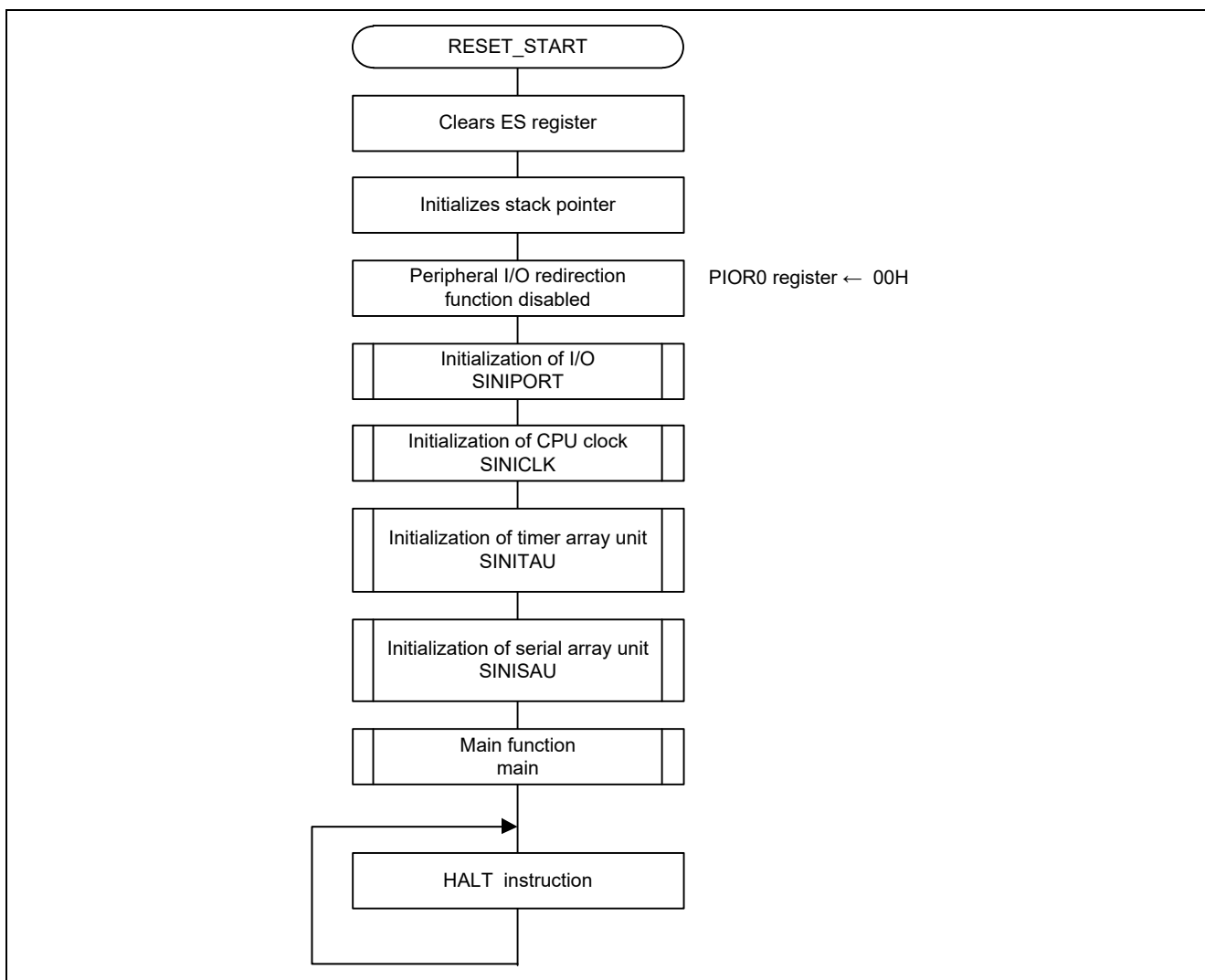
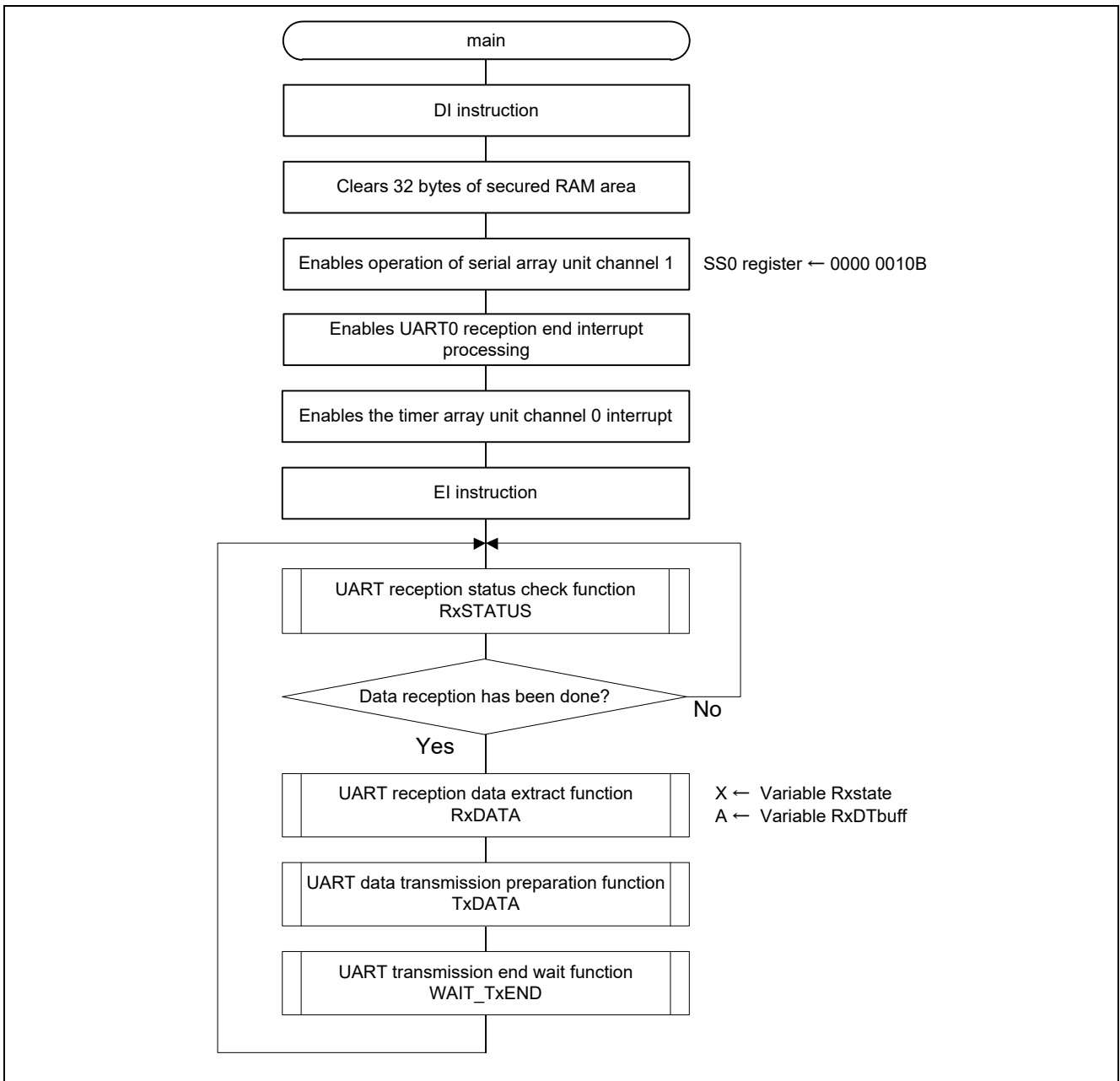


Figure 5.1 Overall Flow

**5.6.1 Main Function**

Figure 5.2 shows the flowchart for main function.



**Figure 5.2 Main Function**

### 5.6.2 UART Reception Status Check Function

Figure 5.3 shows the UART reception status check function.

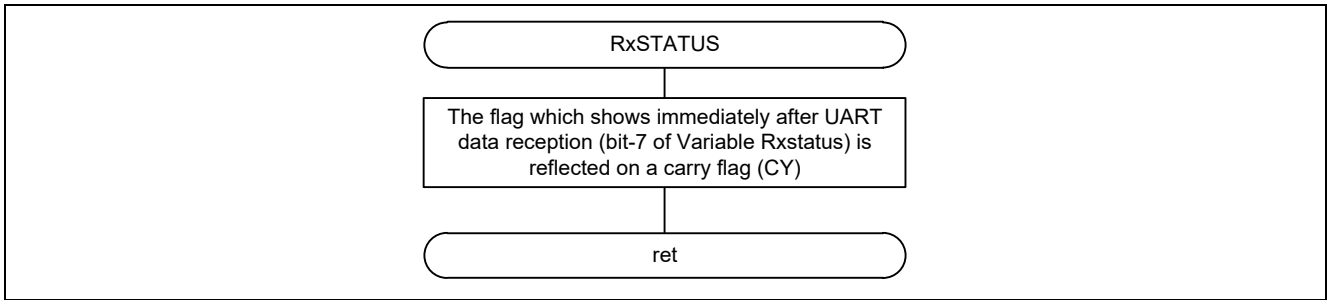


Figure 5.3 UART Reception Status Check Function

### 5.6.3 UART Receiving Data Extract Function

Figure 5.4 shows the UART receiving data extract function.

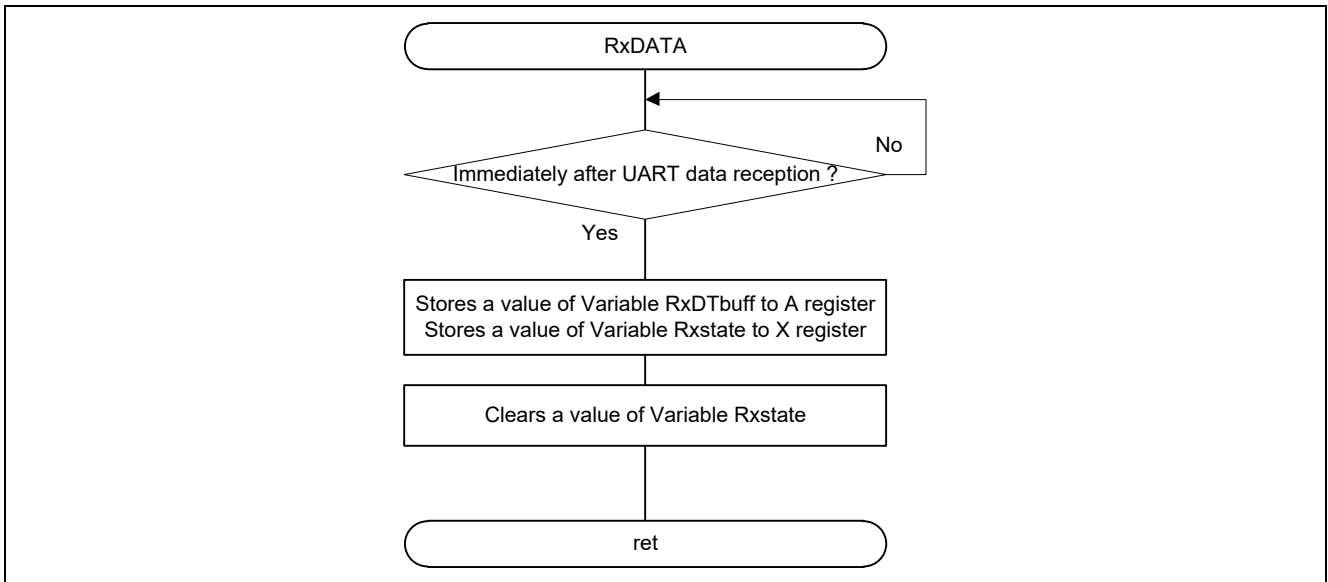
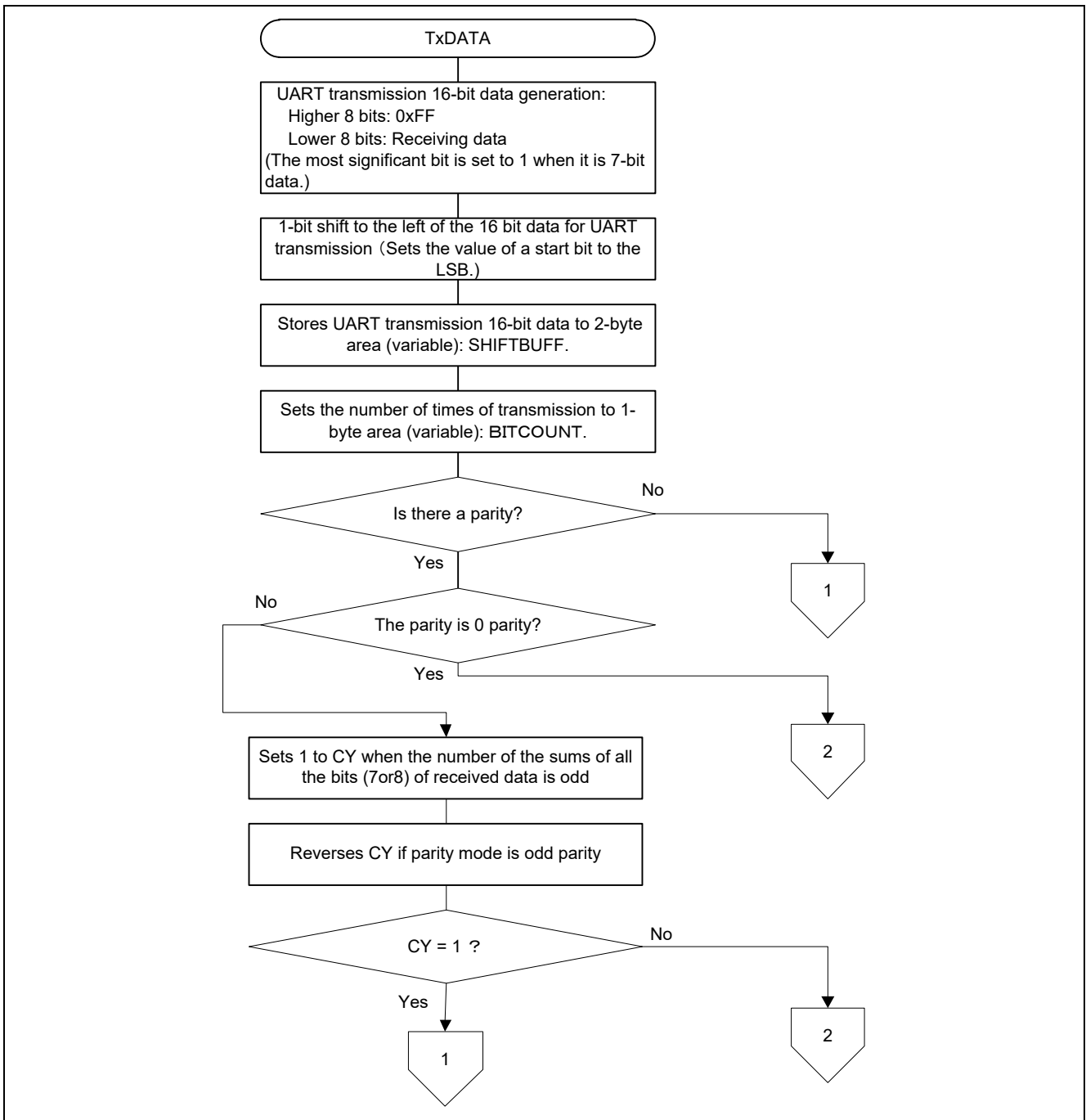


Figure 5.4 UART Receiving Data Extract Function



**5.6.4 UART Data Transmission Preparation Function**

Figure 5.5 and Figure 5.6 shows the UART data transmission preparation function.



**Figure 5.5 UART Data Transmission Preparation Function (1/2)**

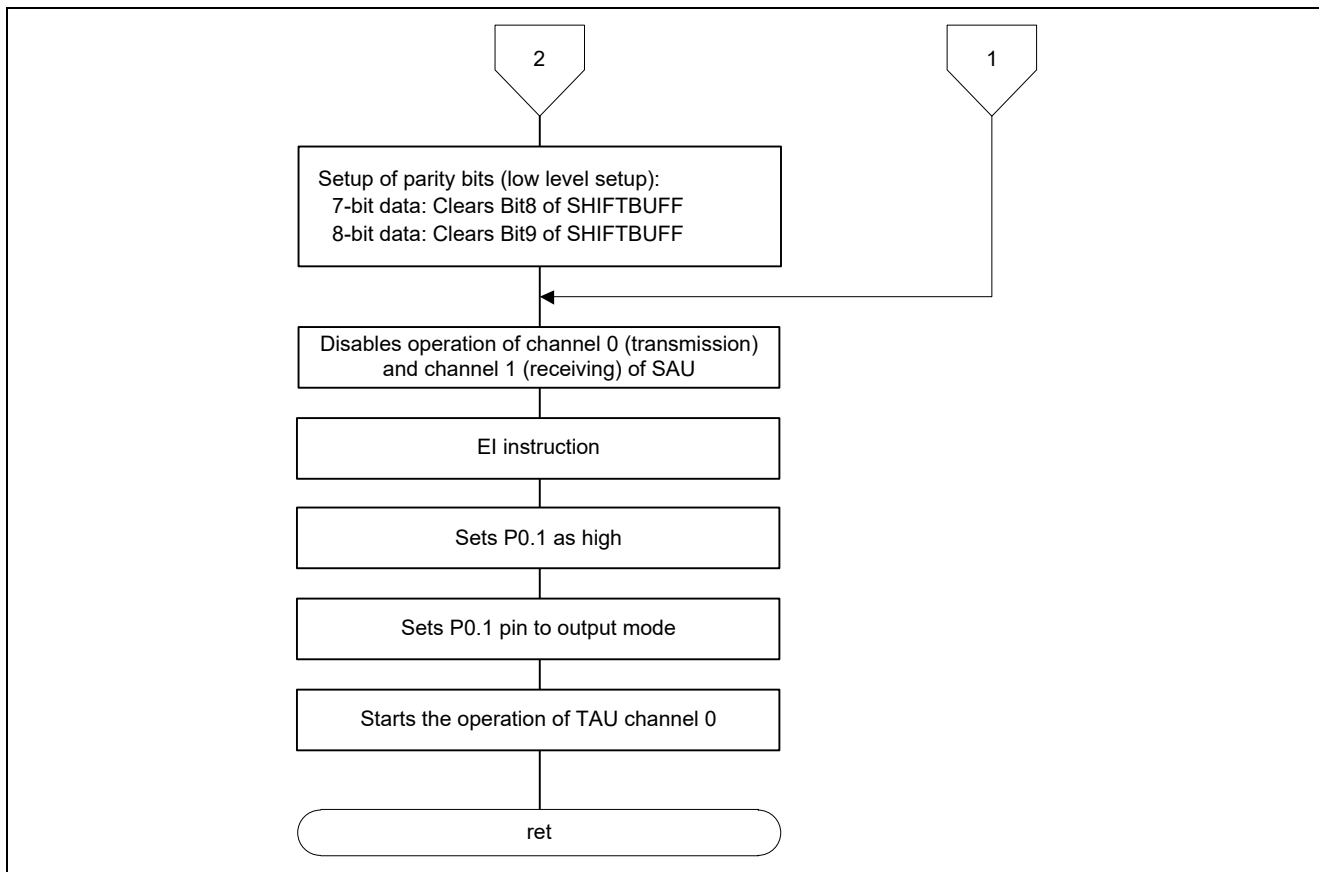
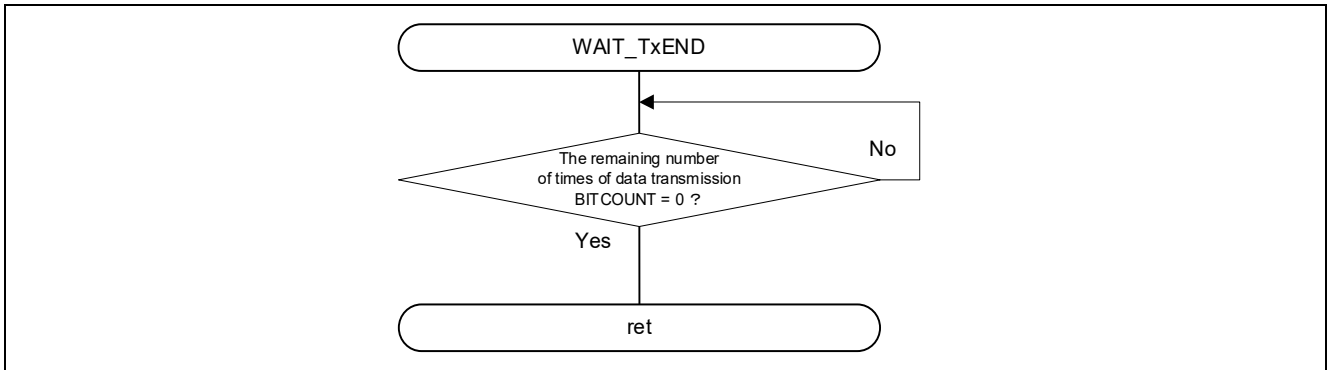


Figure 5.6 UART Data Transmission Preparation Function (2/2)

**5.6.5 UART Transmission End Wait Function**

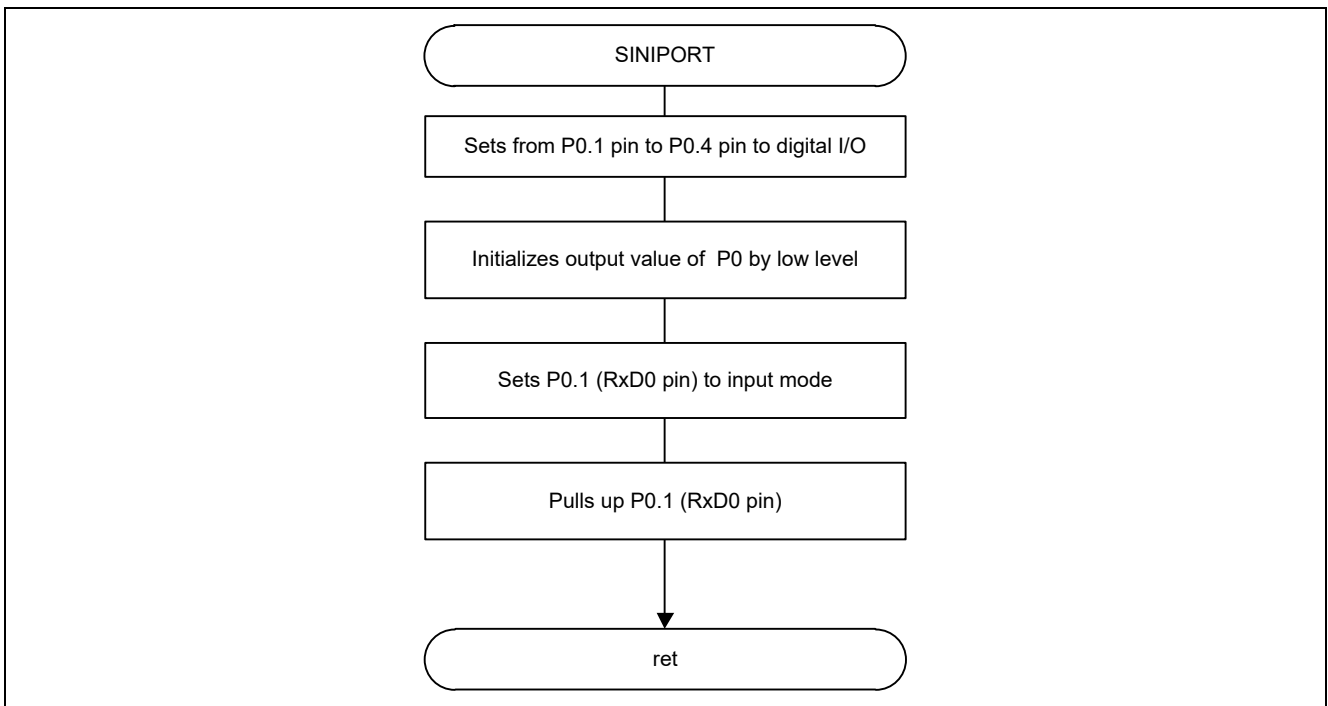
Figure 5.7 shows the UART transmission end wait function.



**Figure 5.7 UART Transmission End Wait Function**

**5.6.6 I/O Initialization**

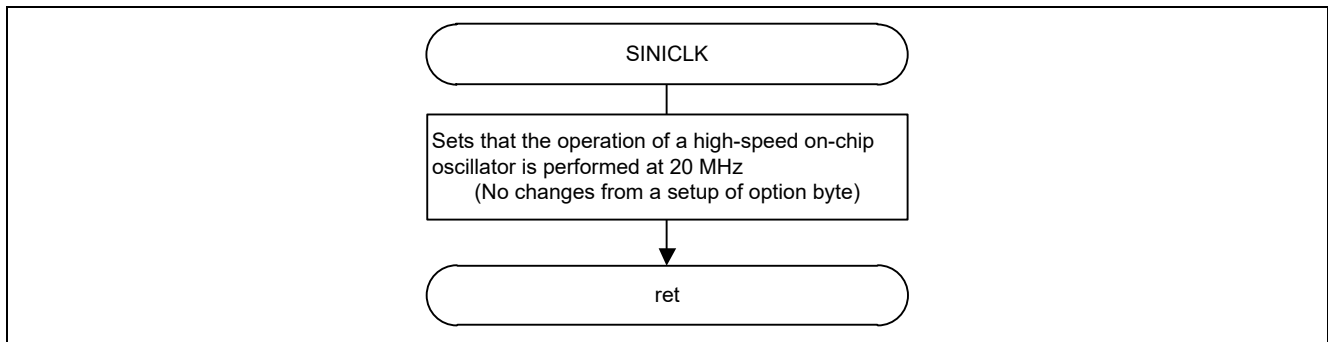
Figure 5.8 shows the I/O initialization.



**Figure 5.8 I/O Initialization**

### 5.6.7 CPU Clock Initialization

Figure 5.9 shows the CPU clock initialization.



**Figure 5.9 CPU Clock Initialization**

### 5.6.8 Timer Array Unit Initialization

Figure 5.10 shows the timer array unit initialization.

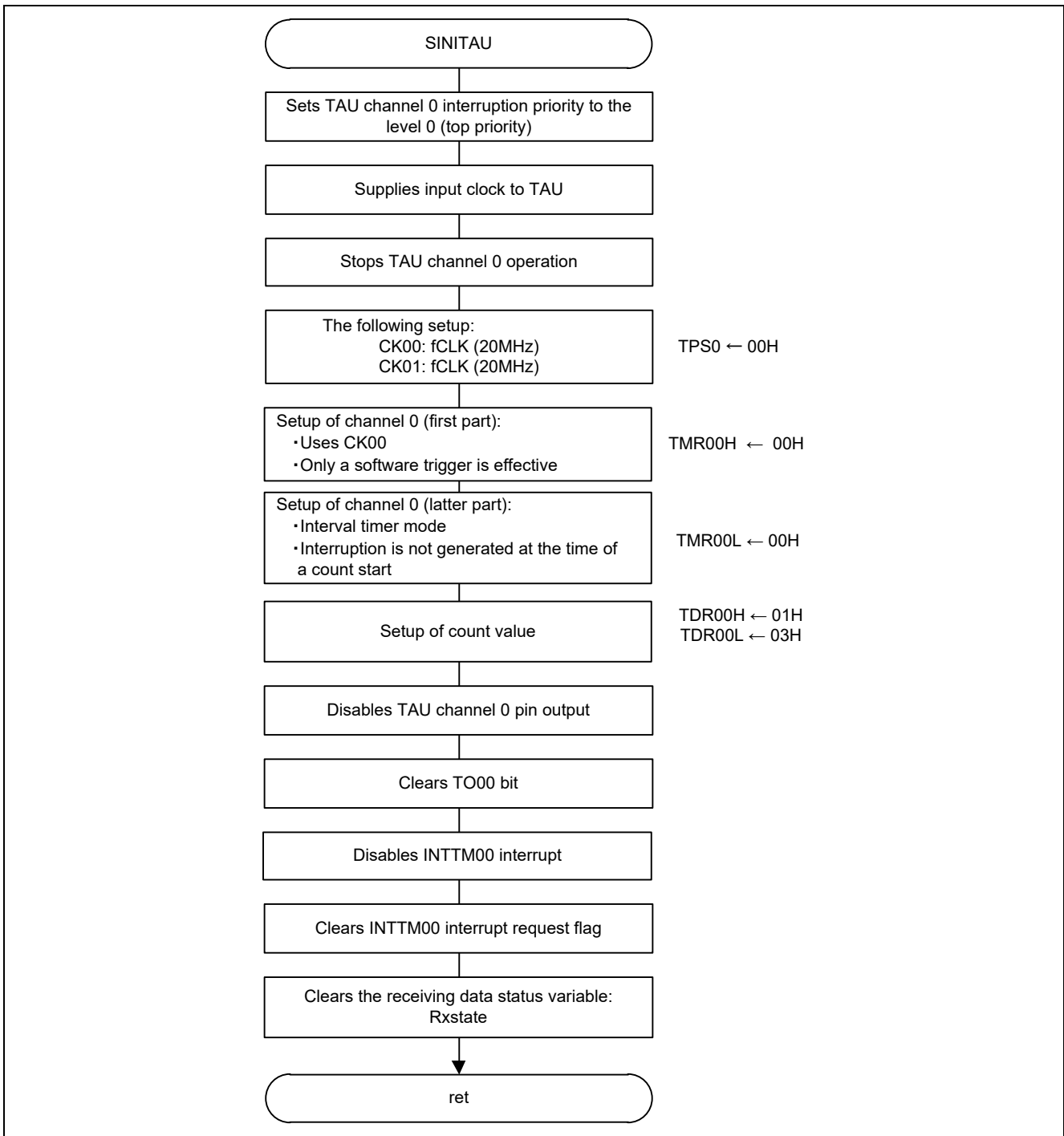
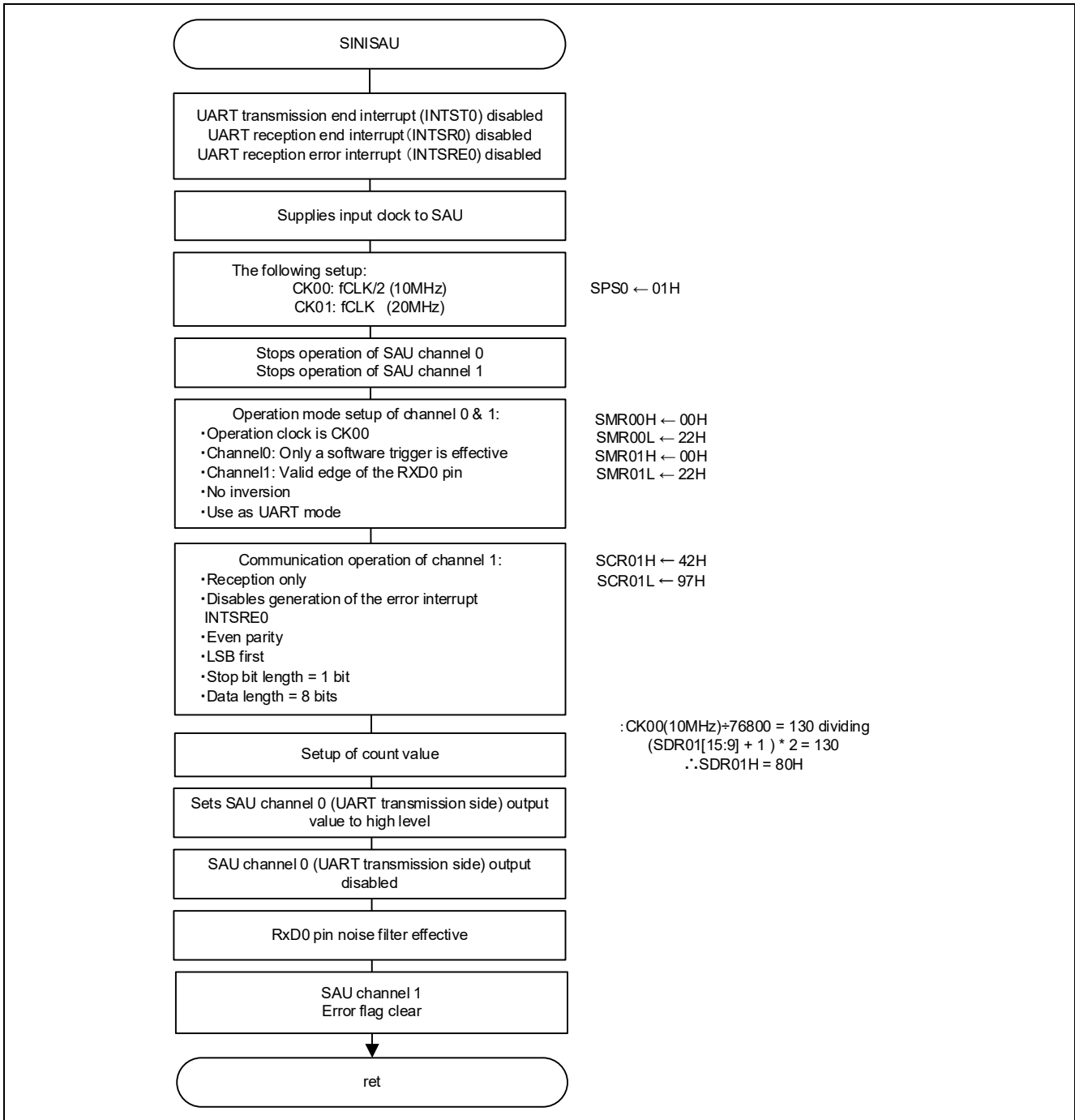


Figure 5.10 Timer Array Unit Initialization

**5.6.9 Serial Array Unit Initialization**

Figure 5.11 shows the serial array unit initialization.



**Figure 5.11 Serial Array Unit Initialization**

### 5.6.10 UART Reception End Interrupt

Figure 5.12 shows the UART reception end interrupt.

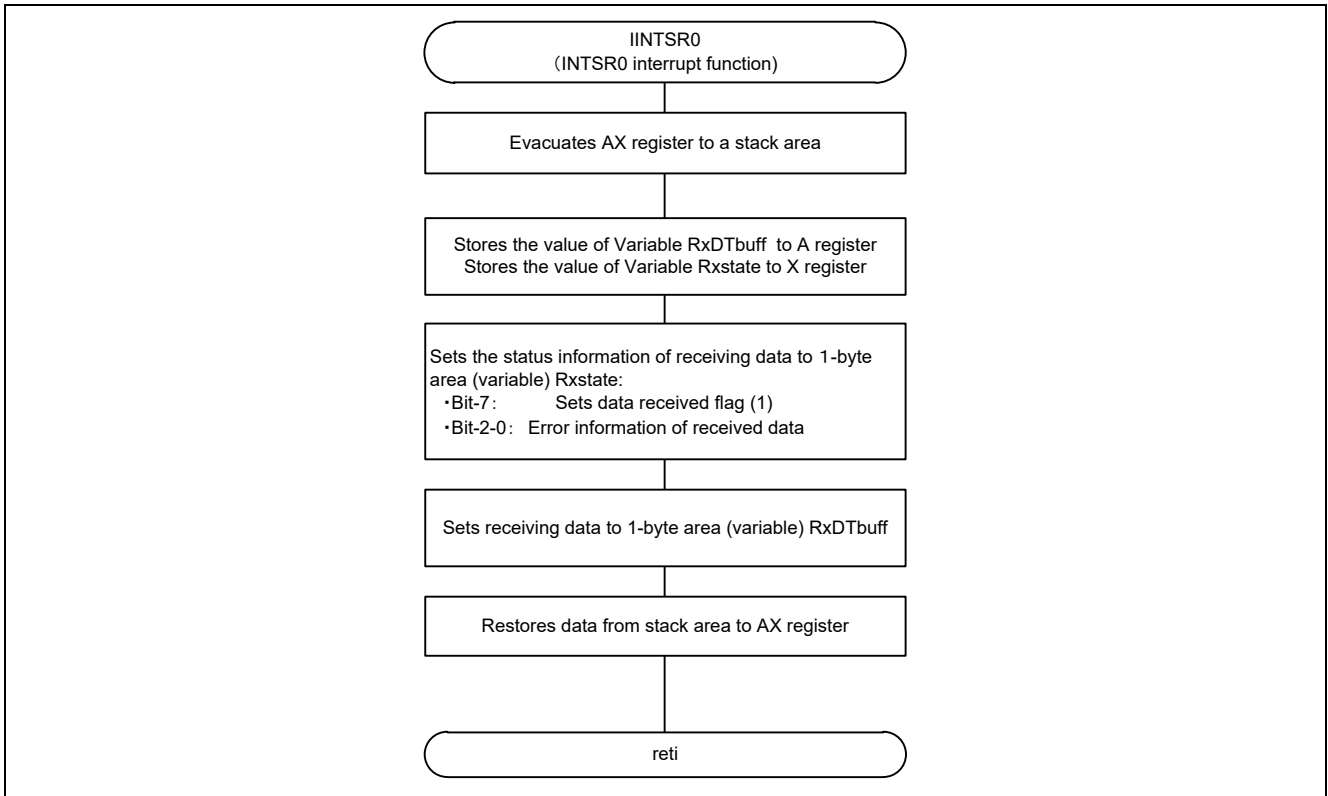


Figure 5.12 UART Reception End Interrupt

5.6.11 TAU Channel 0 Interrupt

Figure 5.13 shows the TAU channel 0 interrupt.

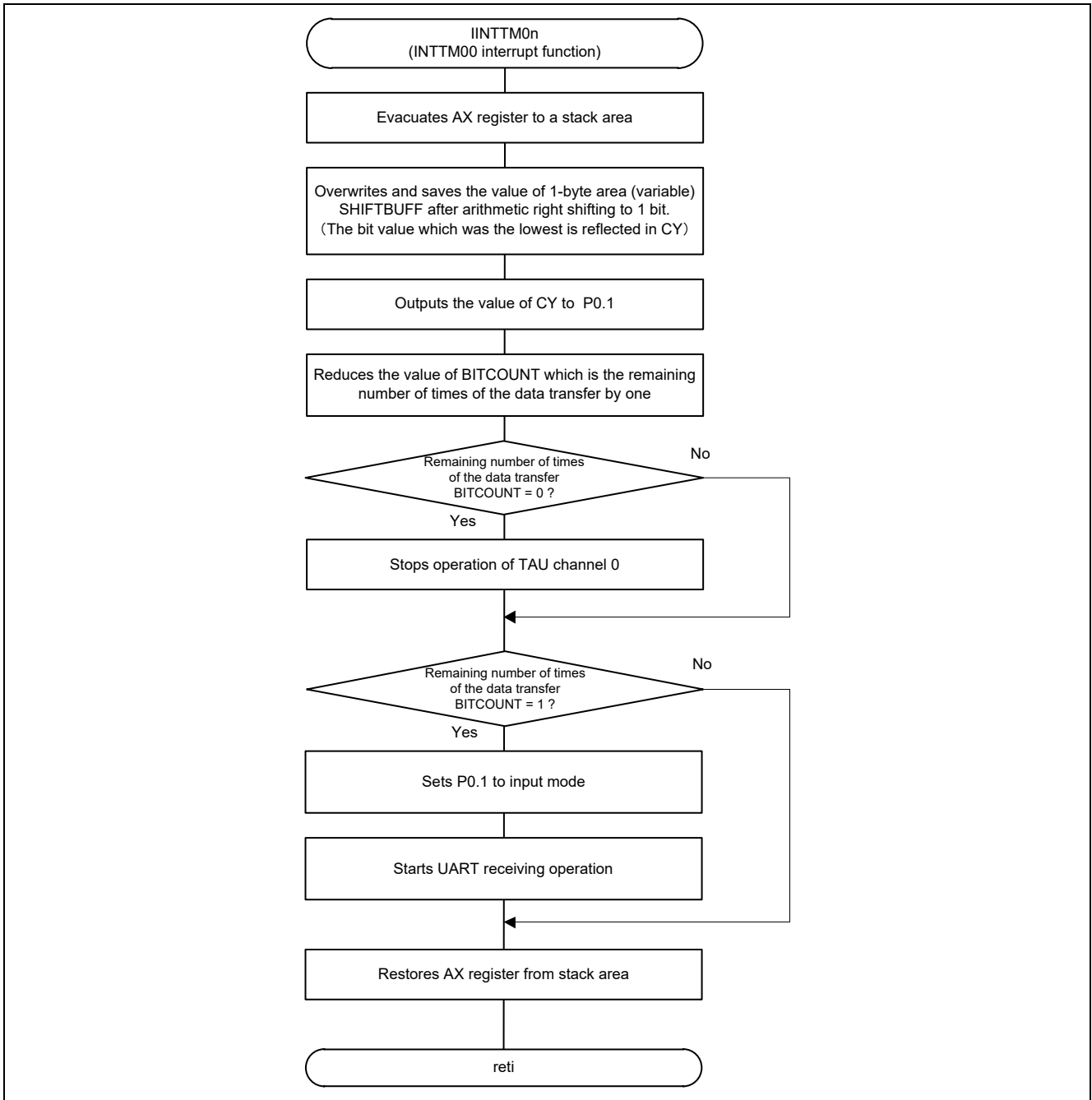


Figure 5.13 TAU Channel 0 Interrupt



## 6. Sample Code

The sample code is available on the Renesas Electronics Website.

## 7. Documents for Reference

RL78/G10 User's Manual: Hardware (R01UH0384E)

RL78 Family User's Manual: Software (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

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## Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2014.11.25	-	First Edition
2.00	2015.03.31	5	e2studio and IAR information added in Table 2.1
		9	Modification of description in Table 5.2
		19	Modification of description in Figure 5.7
		22	Modification of description in Figure 5.11
2.10	2022.09.30	5	Delete IAR information from Table 2.1

# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

## 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

## 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

## 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

## 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

## 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

## 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

## 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

## 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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