RL78/F24

Event Link Controller (ELC) Operations

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Introduction

This document describes about operations of Event Link Controller (ELC) of RL78/F24.

Target Device

- RL78/F24

Contents

1. Operation of ELC

The interrupt request (event signal) output from each peripheral function has a route to the interrupt control circuit and a route to ELC as an event, each of which is independent (See Figure 1-1). Therefore, ELC event signals can be used regardless of the interrupt control circuit. In addition, Event Link operations can be performed by linked peripheral functions without CPU.

Figure 1-1 shows the relationship between the interrupt control circuit and Event Link operation. The figure shows an example of a peripheral function with a status flag and an interrupt enable control function.

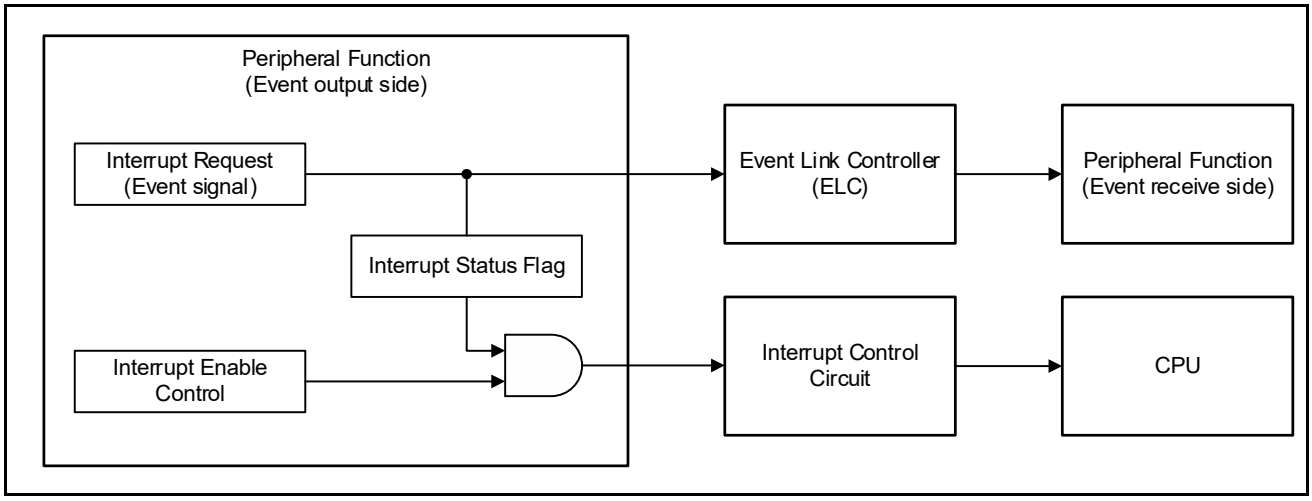


Figure 1-1. Block Diagram between Event Link Operation and Interrupt Control Circuit

2. Event Signal and Event Link Operations

2.1 Event Signal

Table 2-1 shows the event signal (peripheral function event output side) used in ELC.

Table 2-1. Event Output Signals of each Peripheral Functions

Event Generator	Event Signal	Event Output Destination Select Register
External interrupt edge detection 0	INTP0	ELSELR00
External interrupt edge detection 1	INTP1	ELSELR01
External interrupt edge detection 2	INTP2	ELSELR02
External interrupt edge detection 3	INTP3	ELSELR03
External interrupt edge detection 4	INTP4	ELSELR04
External interrupt edge detection 5	INTP5	ELSELR05
Key return signal detection	INTKR	ELSELR06
RTC fixed-cycle signal / Alarm match detection	INTRTC	ELSELR07
TRD0 input capture A / Compare match A	INTTRD0_IFA	ELSELR08
TRD0 input capture B / Compare match B	INTTRD0_IFB	ELSELR09
TRD1 input capture A / Compare match A	INTTRD1_IFA	ELSELR10
TRD1 input capture B / Compare match B	INTTRD1_IFB	ELSELR11
RD1 underflow	INTTRD1_UDF	ELSELR12
Timer RJ0	INTTRJ0	ELSELR13
TAU0 channel 0 count end / Capture end	INTTM00	ELSELR14
TAU0 channel 1 count end / Capture end	INTTM01	ELSELR15
TAU0 channel 2 count end / Capture end	INTTM02	ELSELR16
TAU0 channel 3 count end / Capture end	INTTM03	ELSELR17
TAU0 channel 4 count end / Capture end	INTTM04	ELSELR18
Comparator detection 0	INTCMP0	ELSELR19
TAU0 channel 5 count end / Capture end	INTTM05	ELSELR20
TAU0 channel 6 count end / Capture end	INTTM06	ELSELR21
TAU0 channel 7 count end / Capture end	INTTM07	ELSELR22
TAU1 channel 0 count end / Capture end	INTTM10	ELSELR23
TAU1 channel 1 count end / Capture end	INTTM11	ELSELR24
TAU1 channel 2 count end / Capture end	INTTM12	ELSELR25

2.2 Event Link Operations

Table 2-2 shows the peripheral functions of the Event Link destination and the operation when an event is received.

Table 2-2. Event Link Destination Peripheral Functions and the Operations

Link Destination Peripheral Function	Operation When Receiving Event
A/D converter	A/D conversion starts
D/A converter	Real-time output
TAU0 channel 0	Delay counter, input pulse interval measurement, external event counter
TAU0 channel 1	
TAU0 channel 2	
TAU0 channel 3	
Timer RJ0	Count source
Timer RDe (Timer RD0)	TRDIOD0 input capture, pulse output cutoff
Timer RDe (Timer RD1)	TRDIOD1 input capture, pulse output cutoff
PWMOPA	Pulse output forced cutoff

3. Control Register for ELC

ELC control uses the event output destination select register n (ELSELRn). The ELSELRn register sets which peripheral function the event signal of the peripheral function assigned to each register should be linked to. The specifications of the ELSELRn register are explained in Figure 3-1.

Address: F0780H to F0799H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ELSELRn	0	0	0	0	ELSELRn [3:0]			

ELSELRn [3:0] Note	Event Link Selection
0000B	Event link disabled
0001B	A/D converter
0010B	TAU0 channel 0
0011B	TAU0 channel 1
0100B	Timer RJ0
0101B	Timer RDe (Timer RD0)
0110B	Timer RDe (Timer RD1)
0111B	D/A converter
1000B	TAU0 channel 2
1001B	TAU0 channel 3
1010B	PWMOPA
Other than above	Setting prohibited

Note See **Table 2-1** Event Link Destination Peripheral for ELSELRn register.

Figure 3-1. ELSELRn Register (n = 00 to 25)

4. ELC Usage Examples

4.1 32-bit Timer using TAU0 Channel 0 and Channel 1

An example of using ELC to link the event signal of TAU0 channel 0 to TAU0 channel 1 and using it as a 32-bit timer is shown. Table 4-1 shows the peripheral functions and settings used in this example, and Figure 4-1 shows the event link connection block diagram of this example.

Table 4-1. Peripheral Functions for the 32-bit Timer

Peripheral Function	Description
ELC	Link TAU0 channel 0 count end (INTTM00) to TAU0 channel 1
TAU0 channel 0	Interval timer mode
TAU0 channel 1	External event counter mode

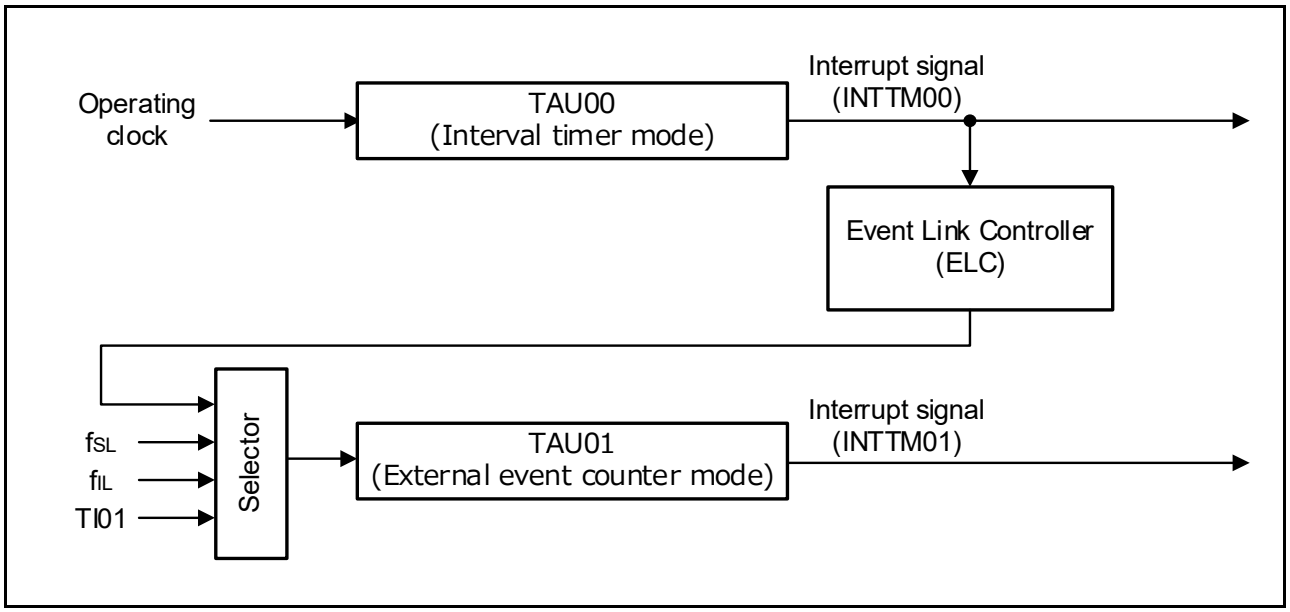
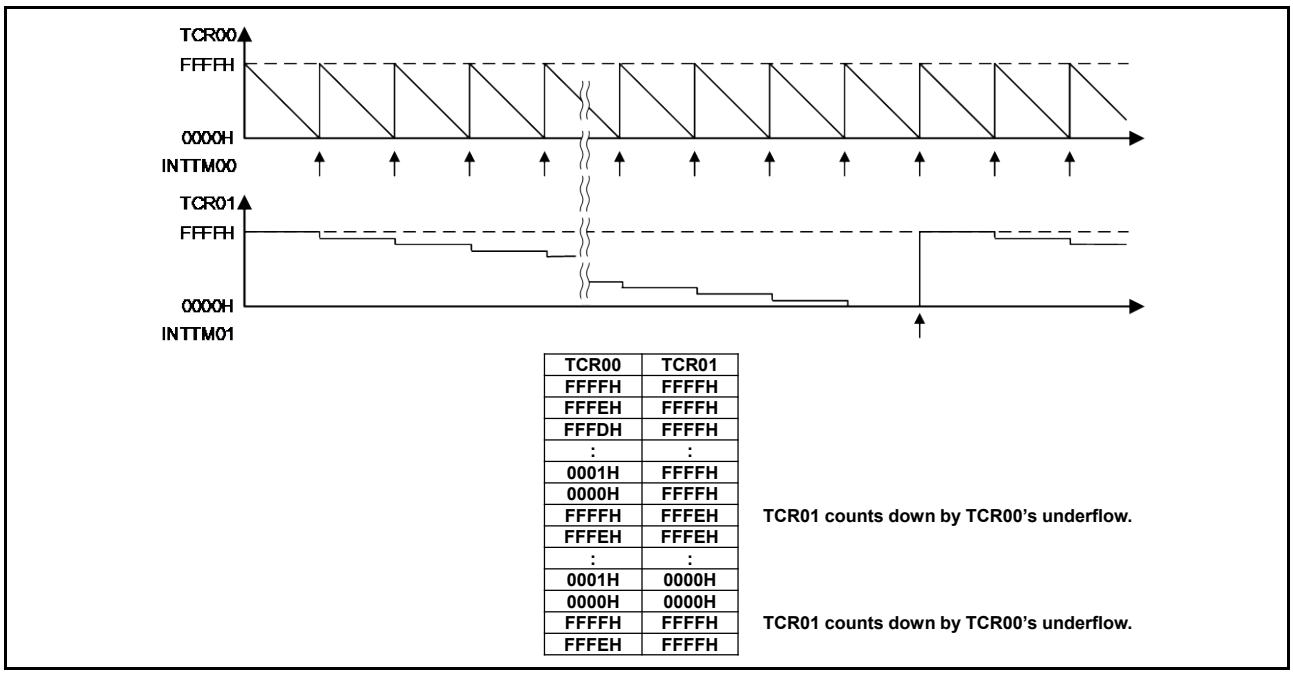


Figure 4-1. Event Link Connection Block Diagram TAU00 and TAU01 for the 32-bit Timer

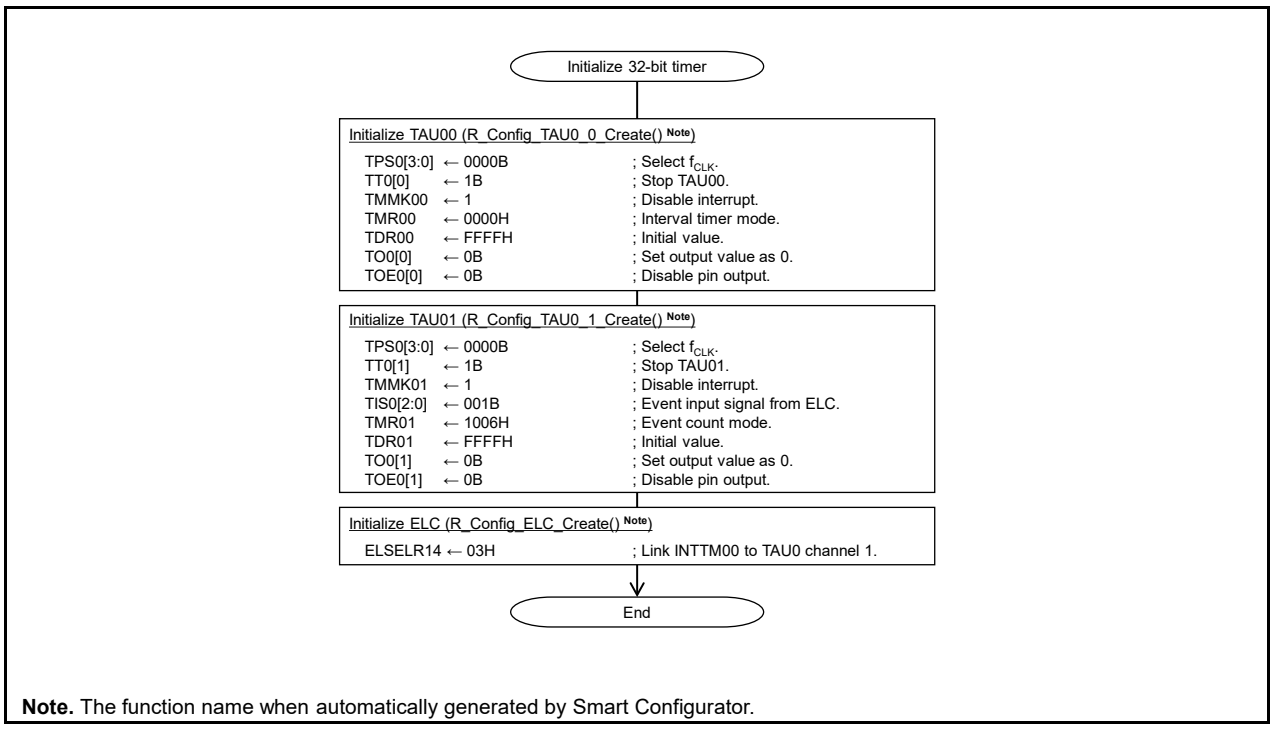
Figure 4-2 shows the operation when TAU00 and TAU01 are connected to implement a 32-bit timer. With TAU00 as the lower 16 bits and TAU01 as the upper 16 bits, when TAU00 underflows, it counts down to TAU01.



TCR00	TCR01	
FFFFH	FFFFH	
FFFEH	FFFFH	
FFFDH	FFFFH	
:	:	
0001H	FFFFH	
0000H	FFFFH	
FFFFH	FFFEH	TCR01 counts down by TCR00's underflow.
FFFEH	FFFEH	
:	:	
0001H	0000H	
0000H	0000H	
FFFFH	FFFFH	TCR01 counts down by TCR00's underflow.
FFFEH	FFFFH	

Figure 4-2. Timer Count Operation by TAU00 and TAU01 for the 32-bit Timer

Figure 4-3 shows an example of the initial setting flow for this example. TAU00, TAU01 and ELC are initialized to the function indicated by Table 4-1. Using the Smart Configurator tool automatically generates the same code with the function names in the figure.

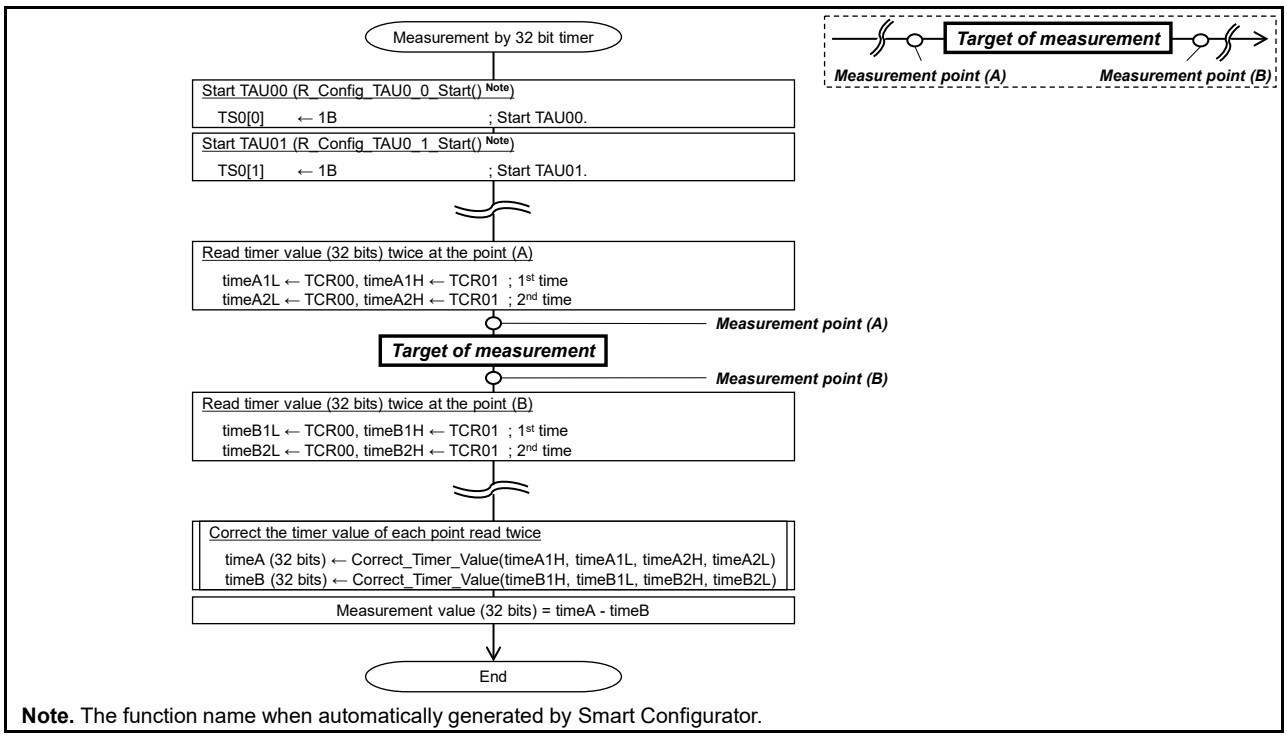


Note. The function name when automatically generated by Smart Configurator.

Figure 4-3. Example Software Flow of 32-bit Timer by TAU00 and TAU01 (1/3) – Initialization

Figure 4-4 shows an example flow for measuring the execution time of the process to be measured using this timer function.

In this example, an underflow may occur in parallel when reading the upper 16-bit timer value followed by the lower 16-bit timer value continuously, and countermeasures are also shown. In Figure 4-4, the timer value reading is performed twice each, and the correction processing shown in Figure 4-5 is performed.



Note. The function name when automatically generated by Smart Configurator.

Figure 4-4. Example Software Flow of 32-bit Timer by TAU00 and TAU01 (2/3) – Measurement

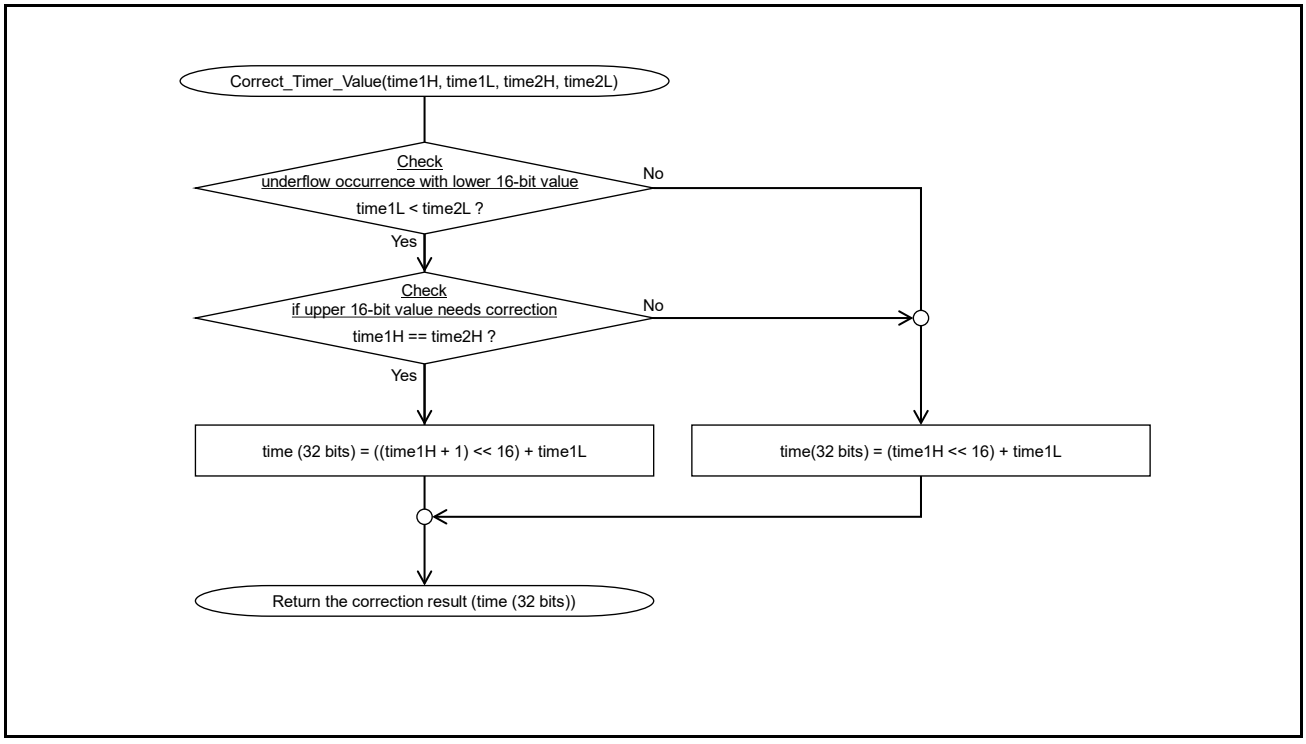


Figure 4-5. Example Software Flow of 32-bit Timer by TAU00 and TAU01 (3/3) – Timer Value Correction

4.2 INTP0 Event Down-Counting Operation by TAU00

When performing one-time processing when a fixed number of external interrupts occur, software processing can be reduced by using a hardware timer down-count. In this example, instead of activating the software interrupt processing directly with the external interrupt INTP0, ELC is used to input the event counter source of TAU0 channel 0, and then count down the number of times set in the TAU00. Then, the timer interrupt is generated once and processed by the software.

Table 4-2 shows the peripheral functions and settings used in this example, and Figure 4-6 shows the event link connection block diagram of this example.

Table 4-2. Peripheral Functions for the INTP0 Down-Counting by TAU00

Peripheral Function	Description
ELC	Link external interrupt edge detection 0 (INTP0) to TAU0 channel 0
INTP0	External interrupt
TAU0 channel 0	External event counter mode

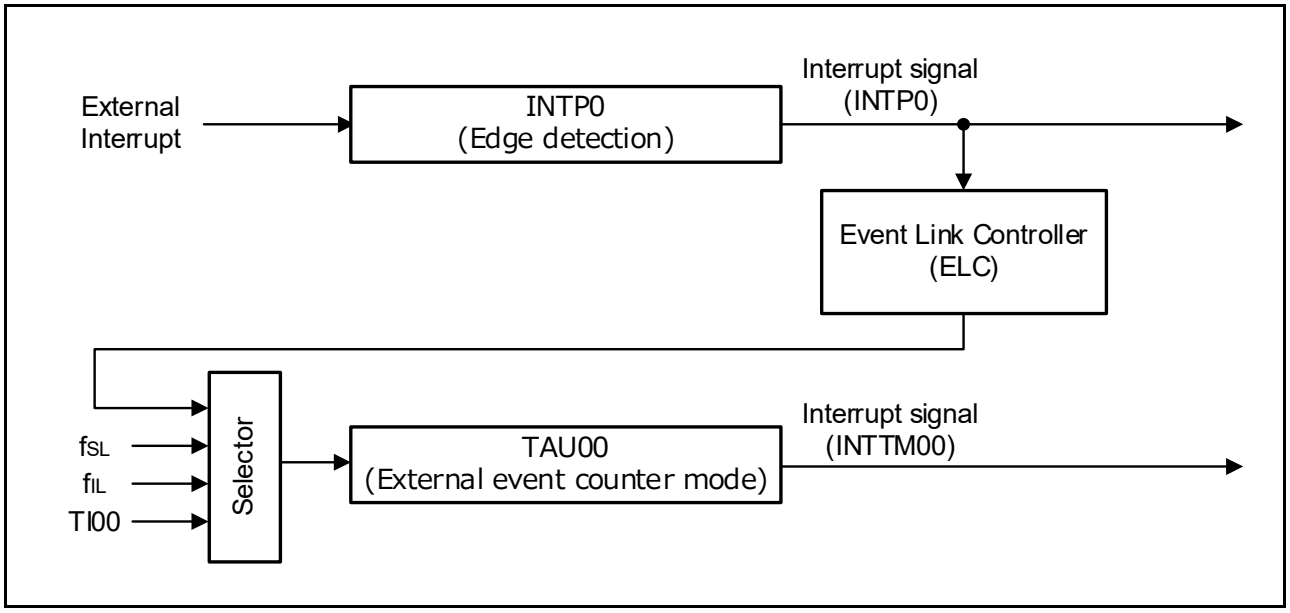


Figure 4-6. Event Link Connection Block Diagram INTP0 and TAU00 for the Interrupt Event Down-Counting

The following shows the operation when INTP0 and TAU00 are connected to Figure 4-7 to realize down-counting of an external event. "Normal INTP0 Process" in the figure is an example of normal processing in which a countdown is implemented by software. On the other hand, in the "INTP0 process using TAU00 via ELC" in the figure, the frequency of interrupt processing is reduced by down-counting with the hardware timer TAU00.

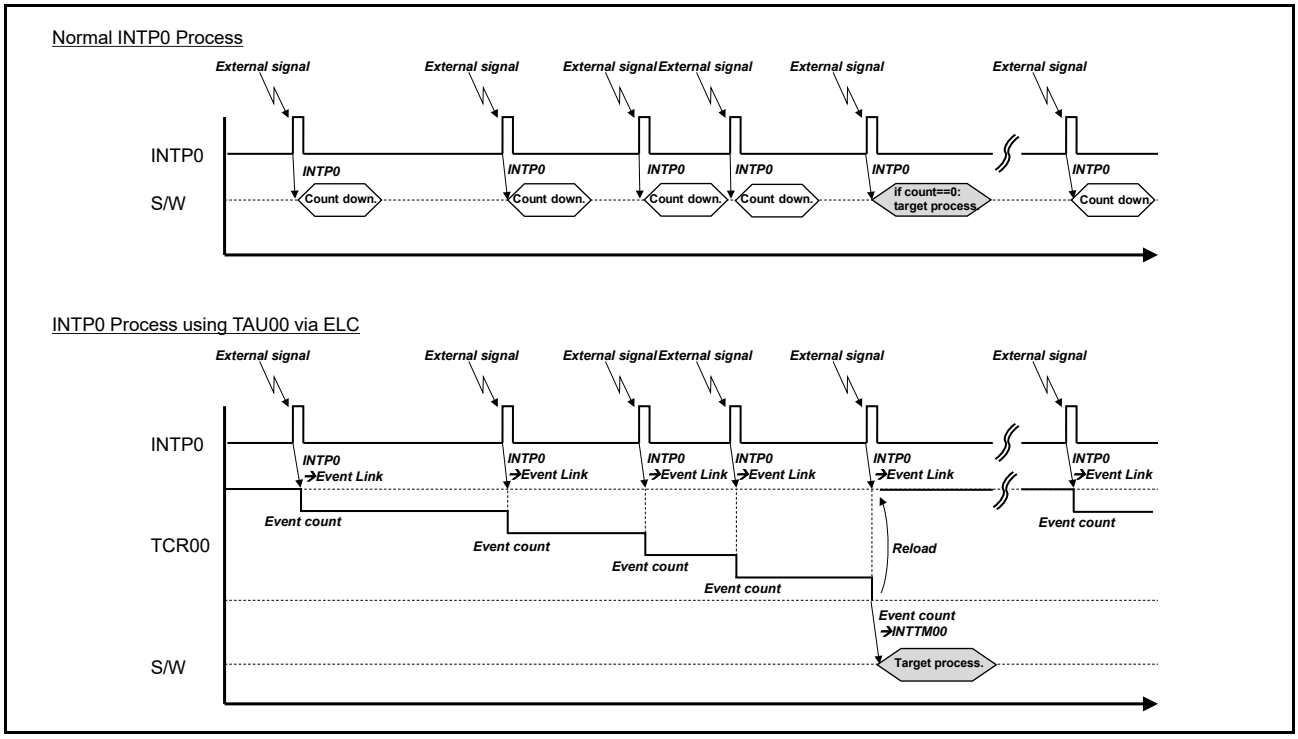
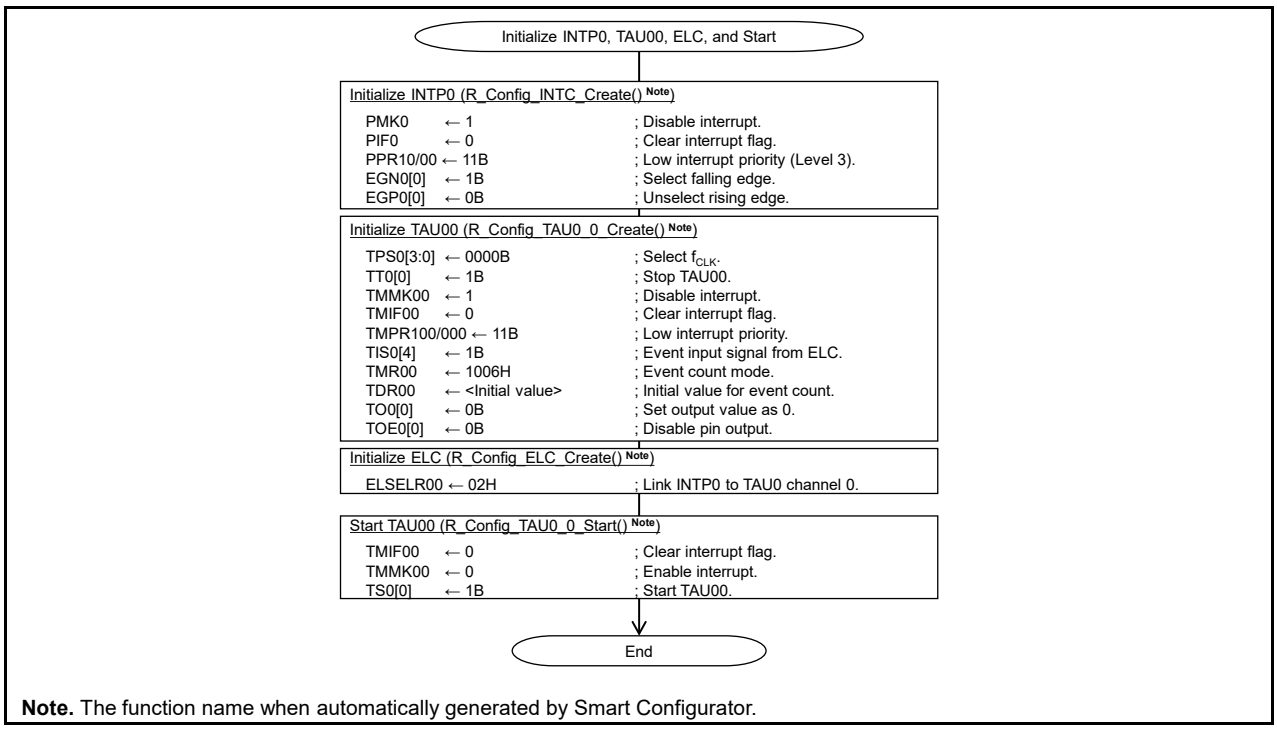


Figure 4-7. INTP0 Event Down-Counting Operation by TAU00

Figure 4-8 shows an example of the initial setting flow for this example. Initialize INTP0, TAU00, and ELC to the functions in Table 4-2.



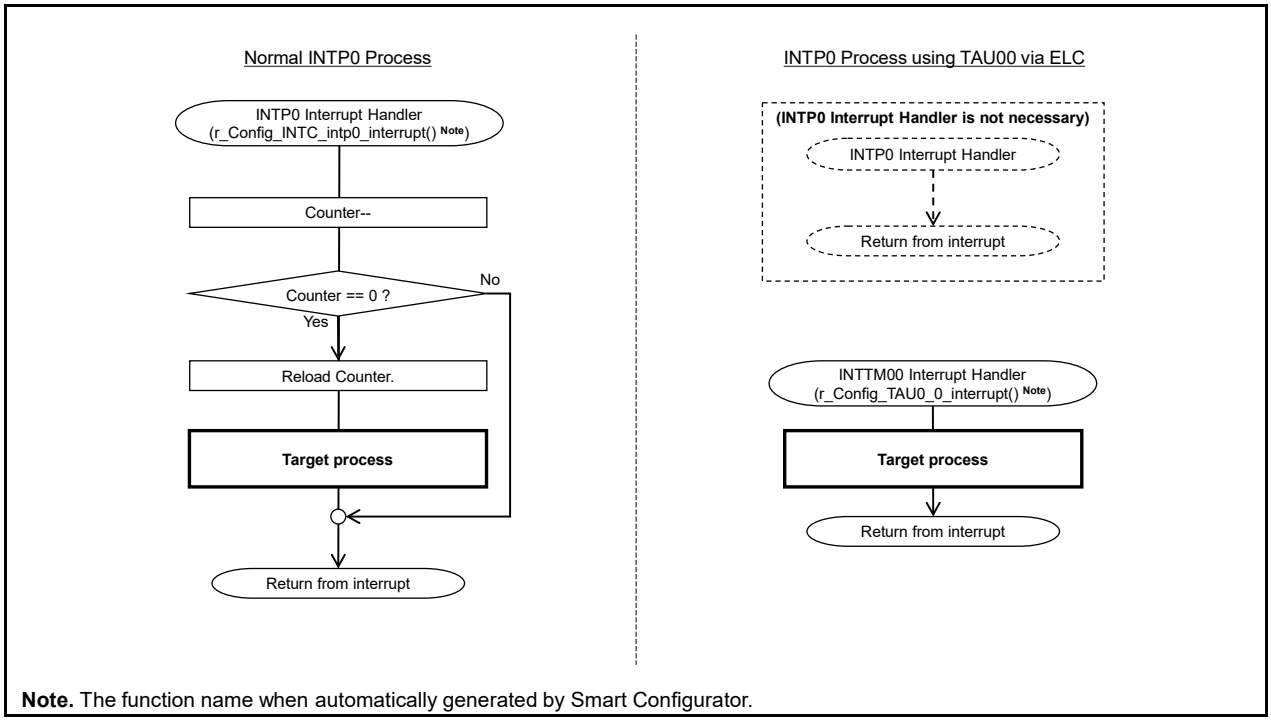
Note. The function name when automatically generated by Smart Configurator.

Figure 4-8. Example Software Flow of INTP0 Event Down-Counting Operation by TAU00 (1/2) – Initialization

Figure 4-9 shows the difference in the interrupt processing flow in this example.

In the "Normal INTP0 Processing" in the figure, the software interrupt processing is activated each time an external interrupt INTP0 event occurs. This is determined by software and the target interrupt is handled.

On the other hand, in the "INTP0 Process using TAU00 via ELC" in the figure, the hardware timer TAU00 counts down, and the hardware judges the event occurrence for the predetermined number of times, so software processing is performed only once. It can be simplified. In this case, the INTP0 interrupt handler is not necessary, and the "Target process" is executed by the INTTM00 interrupt handler.



Note. The function name when automatically generated by Smart Configurator.

Figure 4-9. Example Software Flow of INTP0 Event Down-Counting Operation by TAU00 (2/2) – Interrupt Handlers

5. ELC Overheads for Link Destination Peripheral Functions

Table 5-1 shows ELC overheads for each link destination peripheral functions, from the ELC event to the peripheral input.

Table 5-1. ELC Overheads for each Link Destination Peripheral Functions

Link Destination Peripheral Function	ELC Overhead
A/D converter	ELC event is direct hardware trigger for A/D converter (no overhead).
TAU0 channel 0 to 3	4 f_{CLK} cycles overhead (maximum) from ELC event to the detection.
Timer RJ0	ELC event is direct source of Timer RJ0 count (no overhead).
Timer RDe (TRD0, TRD1)	3 f_{TRD} cycles overhead (maximum) from ELC event to the detection.
D/A converter	2 f_{CLK} cycles overhead (maximum) from ELC event to the detection, and the D/A converter operation starts in the next cycle.
PWMOPA	2 f_{CLK} cycles overhead (maximum) from ELC event to the detection, and the pulse output forced cutoff state starts in the next cycle.

6. References

Documents referenced in this application note are shown below. When referring to these documents, make sure to obtain the latest version of each document from Renesas Electronics website.

- RL78/ F23, F24 User's Manual: Hardware Rev. 1.00
- RL78/ F13, F14 User’s Manual: Hardware Rev. 2.10
- RL78 Smart Configurator User's Guide: CS+ Rev. 1.01

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2023. 7.30	-	First edition issued.

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