

RL78/F15

R01AN6059EJ0100

Rev.1.00

Interrupt Source Determination Procedure

2021.09.30

Introduction

In the target devices (RL78/F15), multiple interrupt sources are shared in one interrupt vector table address as shown in the following **Table 1-1**. When using multiple interrupt sources together, software processing must determine which interrupt occurred in the interrupt processing or both interrupts occurred.

This application note describes how to determine the interrupt source when using both interrupt sources simultaneously.

Table 1-1 List of Multiple Interrupt Sources that are Shared in One Interrupt Vector Table (1/2)

Vector Table Address	Interrupt Source ^{Note}		Reference Section	
	Name	Trigger		
0010H	INTP4	Pin input edge detection 4	Section 1.1	
	INTSPM	Stack pointer overflow/underflow detection		
0012H	INTP5	Pin input edge detection 5	Section 1.2	
	INTCMP0	Comparator detection 0		
0014H	INTP13	Pin input edge detection 13	Section 1.3	
	INTCLM	Main clock or PLL clock stopn detection		
002AH	INTP8	Pin input edge detection 8	Section 1.4	
	INTRTC	RTC pretimed signal or alarm match detection		
002EH	INTTM01	End of TAU0 channel 1 count/capture	Section 1.5	
	INTLIN2TRM	LIN2 transmission		
0030H	INTTM02	End of TAU0 channel 2 count/capture		
	INTLIN2RVC	LIN2 reception end		
0032H	INTTM03	End of TAU0 channel 3 count/capture		
	INTLIN2STA/INTLIN2	LIN2 reception status/ LIN2 interrupt		
0036H	INTP6	Pin input edge detection 6		Cannot identify both interrupt sources.
	INTTM11H	Upper 8-bit interval timer interrupt of TAU1 channel 1		
0038H	INTP7	Pin input edge detection 7		
	INTTM13H	Upper 8-bit interval timer interrupt of TAU1 channel 3		
003AH	INTP9	Pin input edge detection 9		
	INTTM01H	Upper 8-bit interval timer interrupt of TAU0 channel 1		
003CH	INTP10	Pin input edge detection 10		
	INTTM03H	Upper 8-bit interval timer interrupt of TAU0 channel 3		
003EH	INTST1/INTCSI10/INTIIC10	UART1 transmission/ CSI10/ IIC10 trasmission end	Section 1.6	
	INTIEBBTD	IEBus data interrupt		
0040H	INTSR1/INTCSI11/INTIIC11	UART1 reception/ CSI11/ IIC11 transmission end	Section 1.7	
	INTIEBBTV	IEBus vectored interrupt		
0042H	INTTM04	End of TAU0 channel 4 count/capture	Section 1.8	
	INTST2/INTCSI20	UART2 transmission/ CSI20 transmission end		
0044H	INTTM05	End of TAU0 channel 5 count/capture		
	INTSR2/INTCSI21	UART2 reception/ CSI20 transmission end		
0046H	INTTM06	End of TAU0 channel 6 count/capture		
	INTSRE2	UART2 reception error occur		
0048H	INTP15	Pin input edge detection 15	Section 1.8	
	INTTM07	End of TAU0 channel 7 count/capture		
004AH	INTP11	Pin input edge detection 11	Cannot use both simultaneously.	
	INTLIN0WUP	LIN0 reception pin input detection		

Note: It depends on the product. For details, show the user's manual: hardware.

Table 1-1 List of Multiple Interrupt Sources that are Shared in One Interrupt Vector Table (2/2)

Vector Table Address	Interrupt Source ^{Note}		Reference Section	
	Name	Trigger		
005AH	INTTM10	End of TAU1 channel 0 count/capture	Section 1.9	
	INTTM20	End of TAU2 channel 0 count/capture		
005CH	INTTM11	End of TAU1 channel 1 count/capture		
	INTTM21	End of TAU2 channel 1 count/capture		
005EH	INTTM12	End of TAU1 channel 2 count/capture		
	INTTM22	End of TAU2 channel 2 count/capture		
0060H	INTTM13	End of TAU1 channel 3 count/capture		
	INTTM23	End of TAU2 channel 3 count/capture		
0064H	INTP12	Pin input edge detection 12		Cannot use both simultaneously.
	INTLIN1WUP	LIN1 reception pin input detection		
006CH	INTTM14	End of TAU1 channel 4 count/capture		Section 1.9
	INTTM24	End of TAU2 channel 4 count/capture		
006EH	INTTM15	End of TAU1 channel 5 count/capture		
	INTTM25	End of TAU2 channel 5 count/capture		
0070H	INTTM16	End of TAU1 channel 6 count/capture		
	INTTM26	End of TAU2 channel 6 count/capture		
0072H	INTTM17	End of TAU1 channel 7 count/capture		
	INTTM27	End of TAU2 channel 7 count/capture		
007CH	INTP14	Pin input edge detection 14	Cannot use both simultaneously.	
	INTLIN2WUP	LIN2 reception pin input detection		

Note: It depends on the product. For details, show the user's manual: hardware.

Contents

1. Interrupt Source Determination Procedure	4
1.1 Determination between INTP4 and INTSPM	4
1.2 Determination between INTP5 and INTCMP0	5
1.3 Determination between INTP13 and INTCLM	6
1.4 Determination between INTP8 and INTRTC	7
1.5 Determination between INTTM0n and INTLIN2x	8
1.6 Determination between INTSAU1x and INTIEBBy	9
1.7 Determination between INTTM0x and INTSAU2y	10
1.8 Determination between INTP15 and INTTM07	11
1.9 Determination between INTTM1x and INTTM2x	12
2. Notes on Interrupt Source Determination	13
2.1 Notes when Clearing bit of INTFLGn Register	13
2.2 Notes when Using INTSPM and INTCLM	13
3. References	14
Revision History	15

1. Interrupt Source Determination Procedure

In the target devices (RL78/F15), multiple interrupt sources are shared in one interrupt vector table address. When using multiple interrupt sources together, software processing must determine which interrupt occurred in the interrupt processing or both interrupts occurred. The following describes how to determine the interrupt source when using both interrupt sources simultaneously.

1.1 Determination between INTP4 and INTSPM

Figure 1-1 shows an interrupt processing example in case of both INTP4 (Pin input edge detection 4) and INTSPM (Stack pointer overflow/underflow) are enabled.

Interrupt by INTP4 can be determined from INTFLG00 bit of INTFLG0 (Interrupt source determination flag register 0). And interrupt by INTSPM can be determined by reading stack pointer from user software.

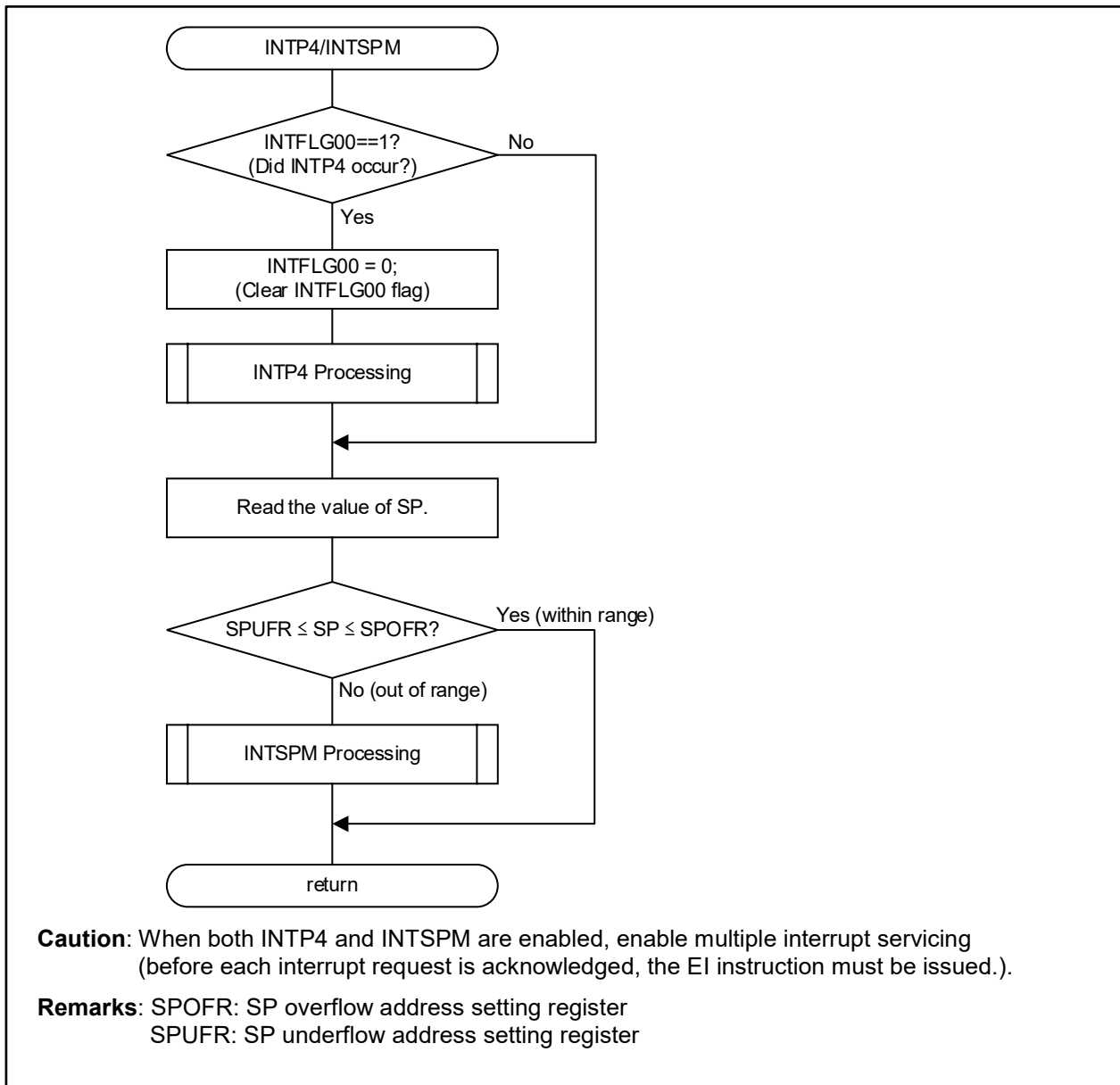


Figure 1-1 INTP4/INTSPM Interrupt Judgement Example

1.2 Determination between INTP5 and INTCMP0

Figure 1-2 shows an interrupt processing example in case of both INTP5 (Pin input edge detection 5) and INTCMP0 (Comparator detection 0) are enabled.

Interrupt by INTP5 can be determined from INTFLG01 bit of INTFLG0 (Interrupt source determination flag register 0). And interrupt by INTCMP0 can be determined from INTFLG06 bit of INTFLG0 (Interrupt source determination flag register 0).

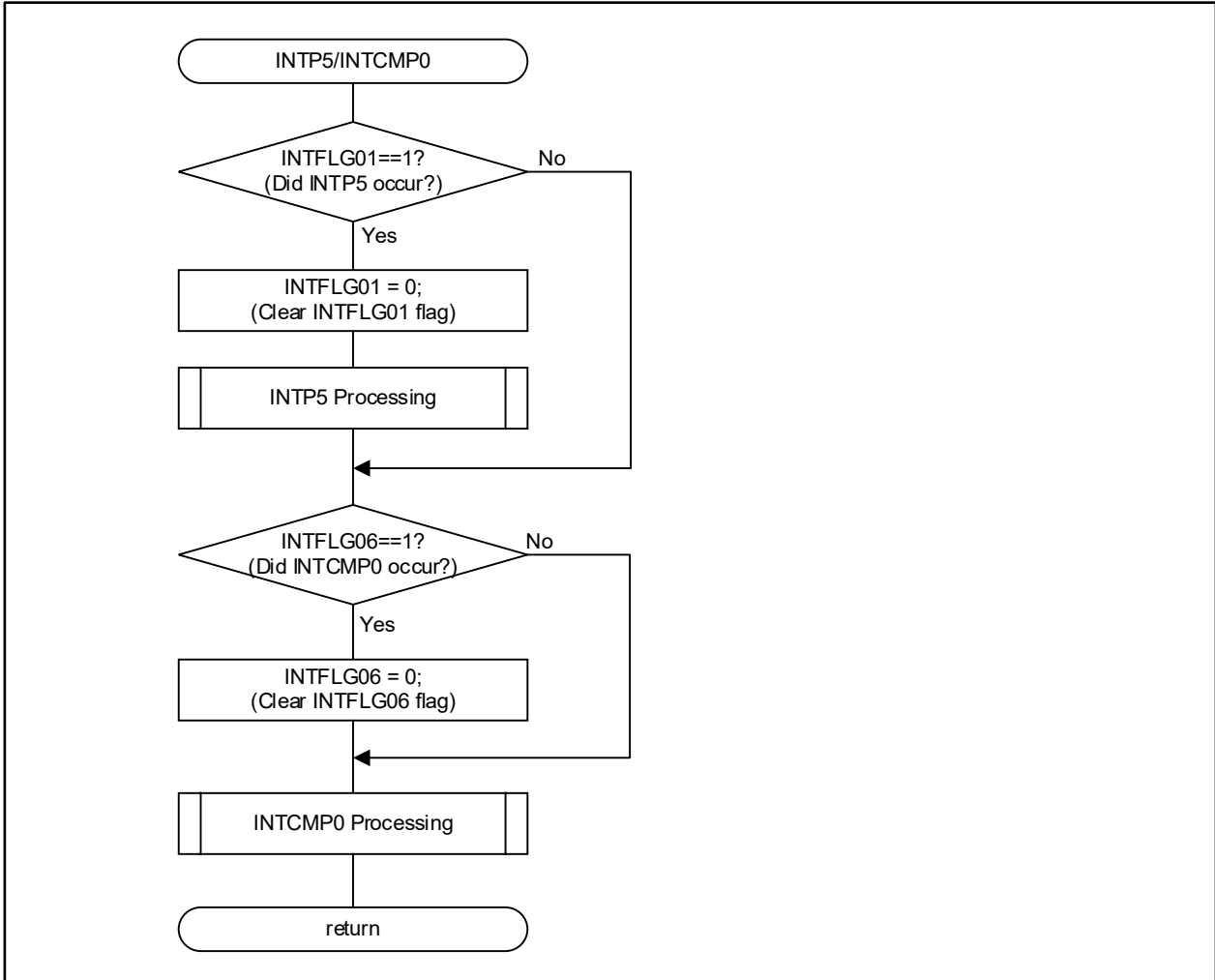


Figure 1-2 INTP5/INTCMP0 Interrupt Judgement Example

1.3 Determination between INTP13 and INTCLM

Figure 1-3 shows an interrupt processing example in case of both INTP13 (Pin input edge detection 13) and INTCLM (Main clock or PLL clock stop) are enabled.

Interrupt by INTP13 can be determined from INTFLG07 bit of INTFLG0 (Interrupt source determination flag register 0). And interrupt by INTCLM can be determined from SELPLLS bit of PLLSTS (PLL status register) and SELPLL bit of PLLCTL (PLL control register).

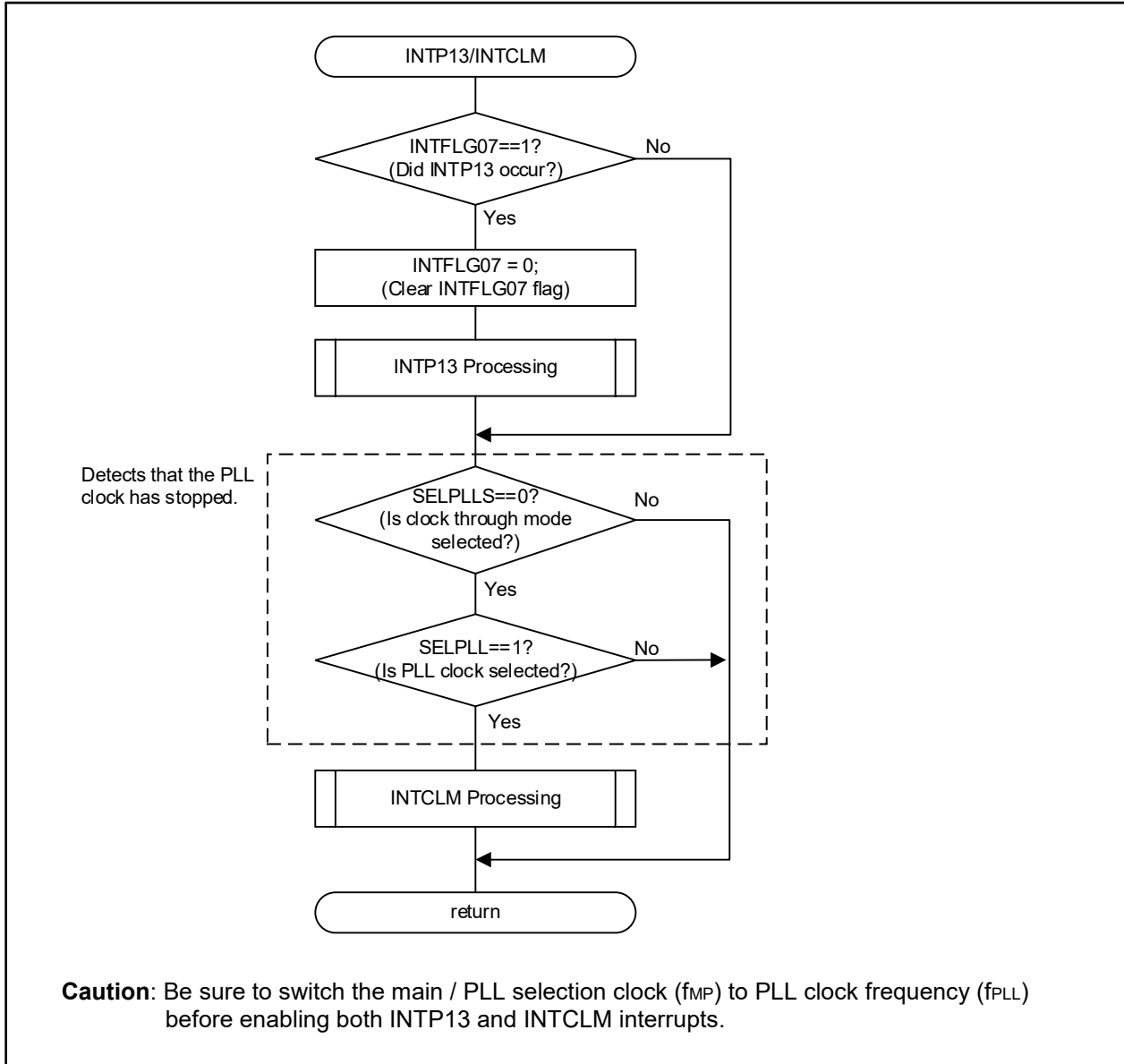


Figure 1-3 INTP13/INTCLM Interrupt Judgement Example

1.4 Determination between INTP8 and INTRTC

Figure 1-4 shows an interrupt processing example in case of both INTP8 (Pin input edge detection 8) and INTRTC (RTC pretimed signal or alarm match detection) are enabled.

Interrupt by INTP8 can be determined from INTFLG02 bit of INTFLG0 (Interrupt source determination flag register 0). And interrupt by INTRTC can be determined from WAFG bit and RIFG bit of RTCC1 (Real-time clock control register 1).

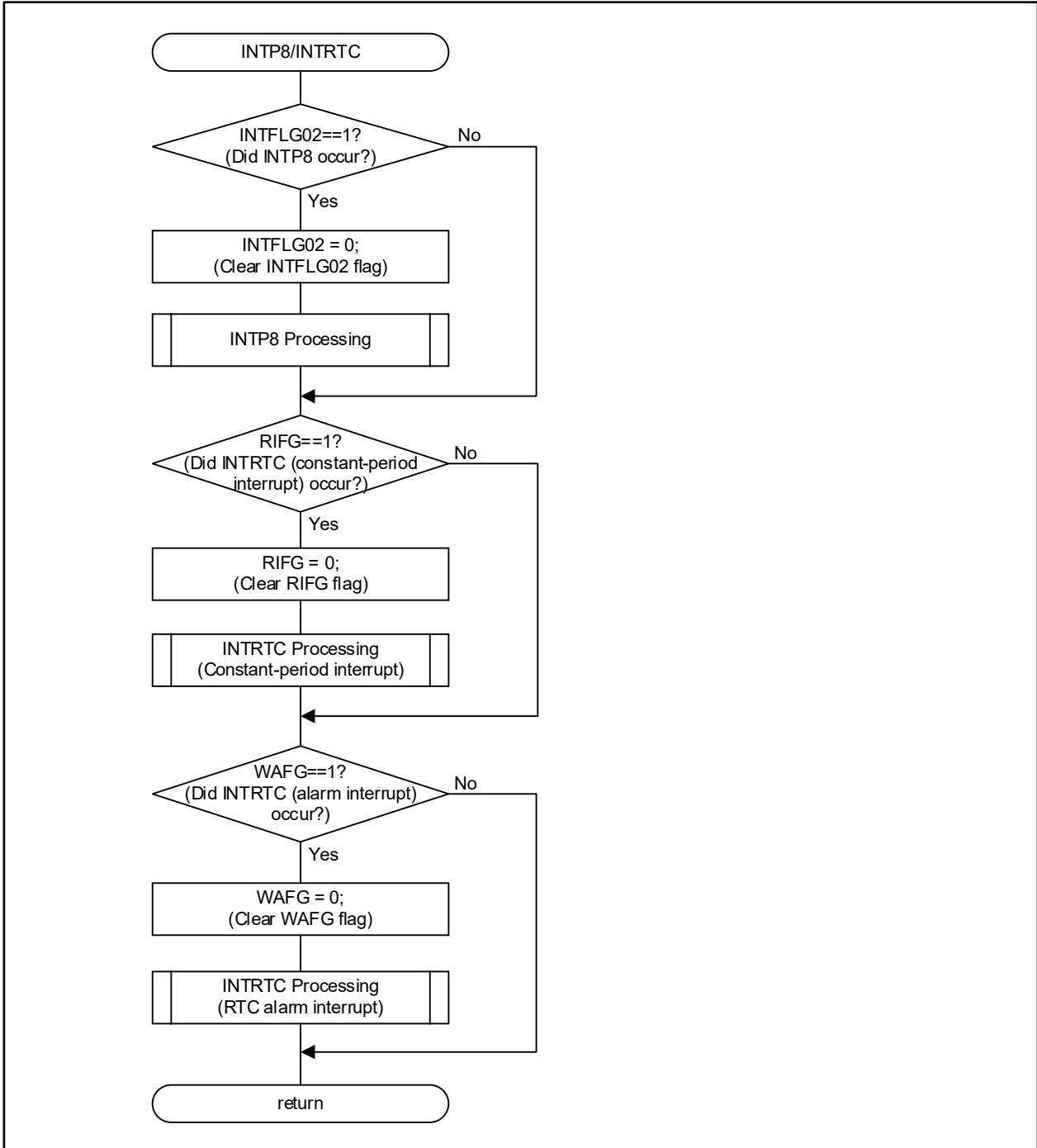


Figure 1-4 INTP8/INTRTC Interrupt Judgement Example

1.5 Determination between INTTM0n and INTLIN2x

Figure 1-5 shows an interrupt processing example in case of both INTTM0n (End of TAU0 channel n count/capture) and INTLIN2x (LIN2 transmission/reception end/reception status interrupt) are enabled.

Interrupt by INTTM0n can be determined from INTFLG1n bit of INTFLG1 (Interrupt source determination flag register 1). And interrupt by INTLIN2x can be determined from the interrupt request flag inside of the LIN2 module. On the other hand, if INTLIN2RVC is used as UART mode, it is impossible to identify both interrupt source. In that case, disable INTTM02 interrupts before using INTLIN2RVC.

Remarks: n = 1 to 3
x = TRM, RVC, STA

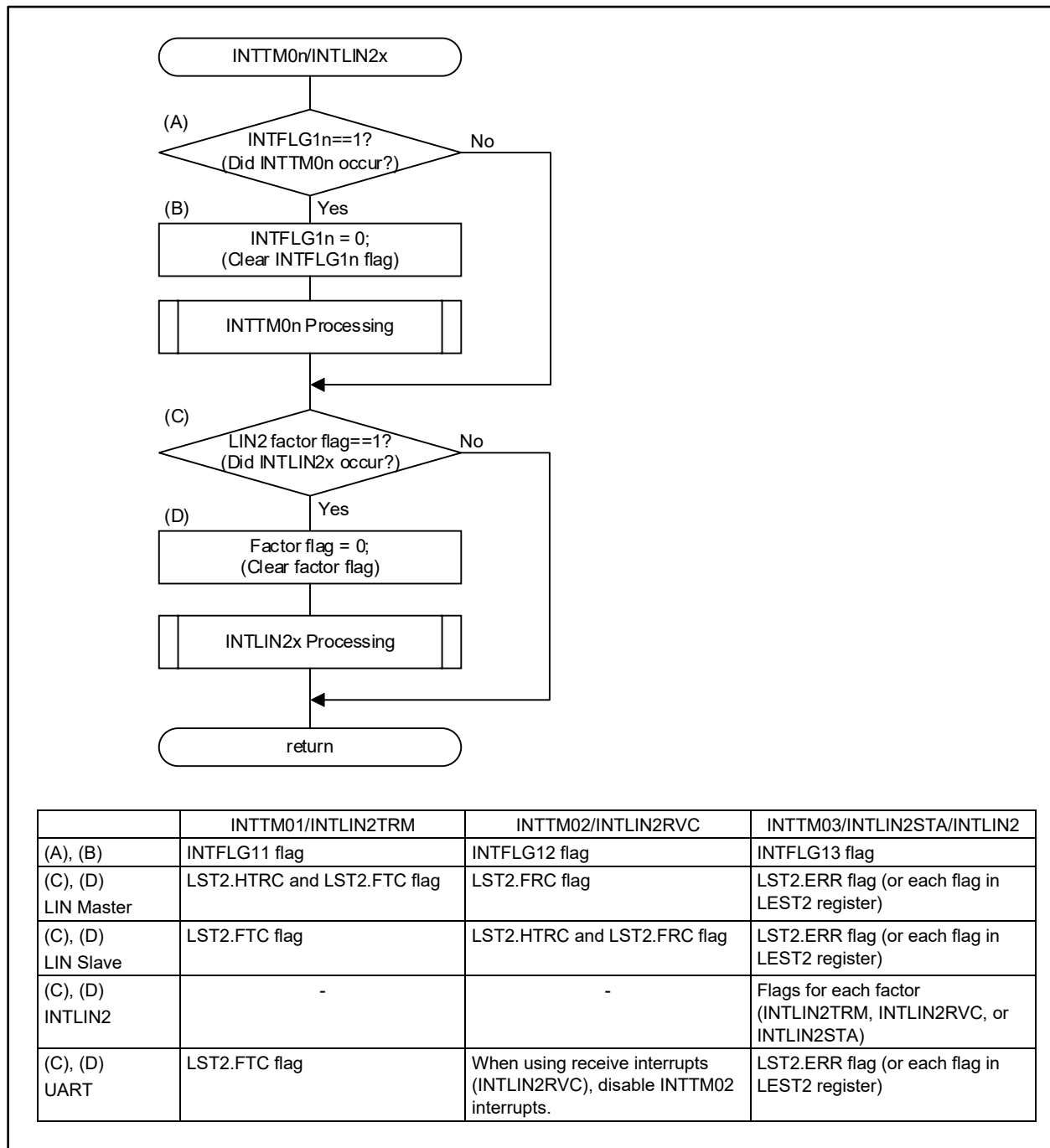


Figure 1-5 INTM0n/INTLIN2x Interrupt Judgement Example

1.6 Determination between INTSAU1x and INTIEBBy

Figure 1-6 shows an interrupt processing example in case of both INTSAU1 (UART1 transmission and reception, CSI10/CSI11/IIC10/IIC11 transfer end) and INTIEBBy (IEBus data/vector interrupt) are enabled.

Interrupt by INTSAU1 can be determined from INTFLG41 and INTFLG42 bit of INTFLG4 (Interrupt source determination flag register 4). And interrupt by INTIEBBy can be determined from from INTFLG46 and INTFLG47 bit of INTFLG4 (Interrupt source determination flag register 4).

Remarks: x = ST1/CSI10/IIC10, SR1/CSI11/IIC11
y = TD, TV

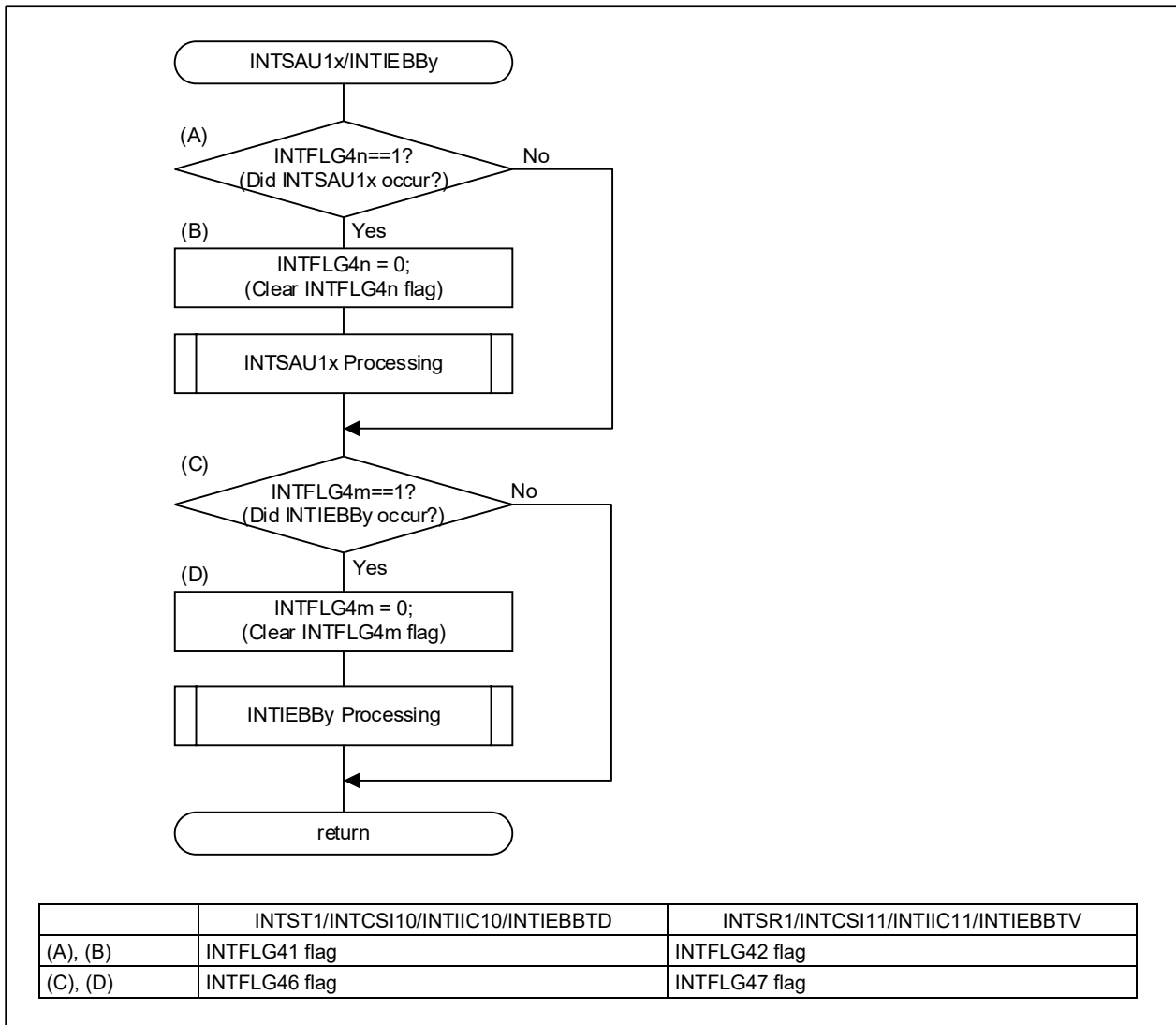


Figure 1-6 INTSAU1x/INTIEBBy Interrupt Judgement Example

1.7 Determination between INTTM0x and INTSAU2y

Figure 1-7 shows an interrupt processing example in case of both INTTM0n (End of TAU0 channel x count/capture) and INTSAU2y (UART2 transmission/reception, CSI20/CSI2 transfer end, UART2 reception error occur) are enabled.

Interrupt by INTTM0x can be determined from INTFLG1x bit of INTFLG1 (Interrupt source determination flag register 1). And interrupt by INTSAU2y can be determined from INTFLG43 and INTFLG44 bit of INTFLG4 (Interrupt source determination flag register 4).

Remarks: x = 4, 5, 6
y = ST2/CSI20, SR2/CSI21, SRE2

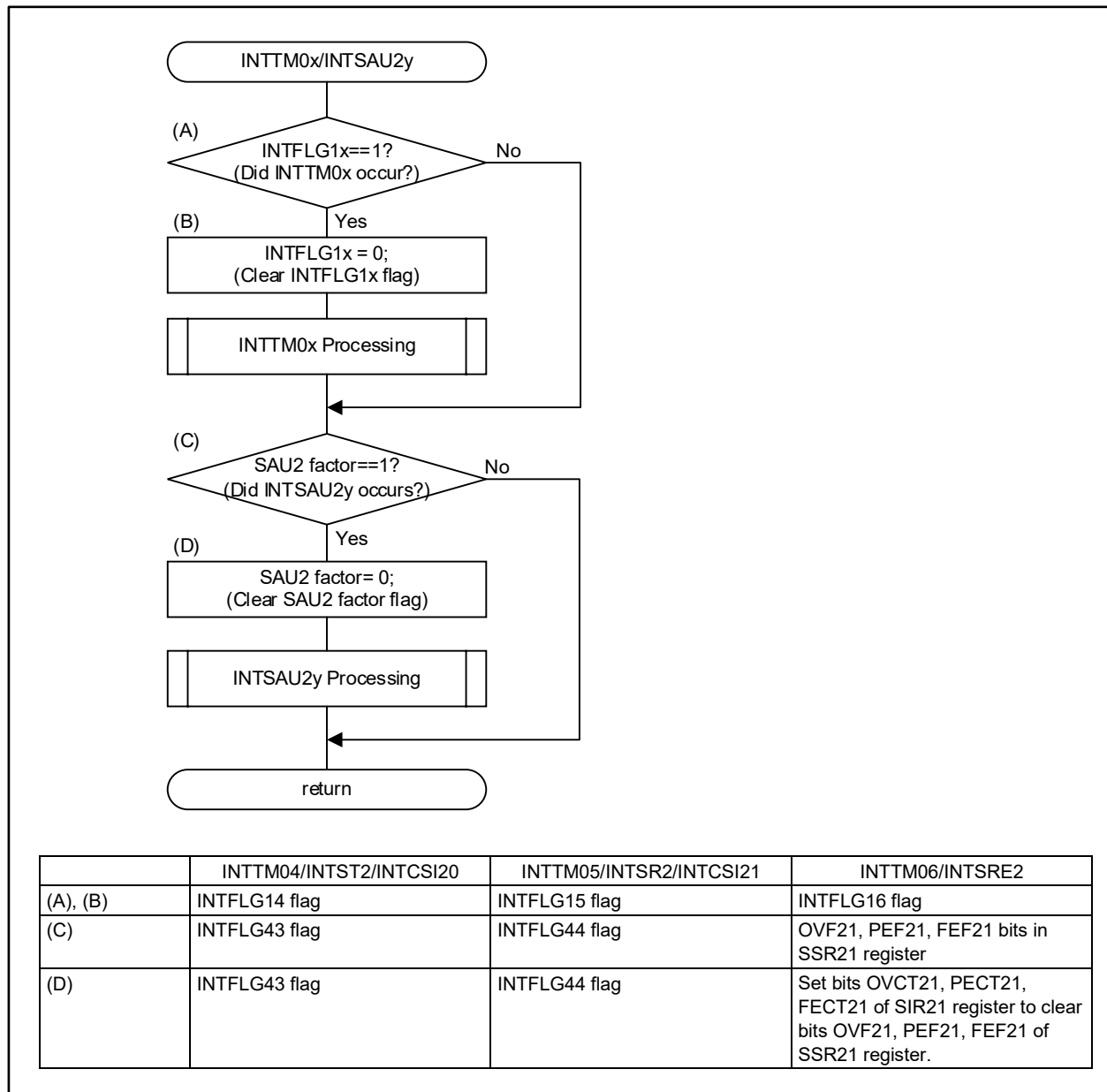


Figure 1-7 INTTM0x/INTSAU2y Interrupt Judgement Example

1.8 Determination between INTP15 and INTTM07

Figure 1-8 shows an interrupt processing example in case of both INTP15 (Pin input edge detection 15) and INTTM07 (End of TAU0 channe 7 count/capture) are enabled.

Interrupt by INTP15 can be determined from INTFLG40 bit of INTFLG4 (Interrupt source determination flag register 4). And interrupt by INTTM07 can be determined from INTFLG17 bit of INTFLG1 (Interrupt source determination flag register 1).

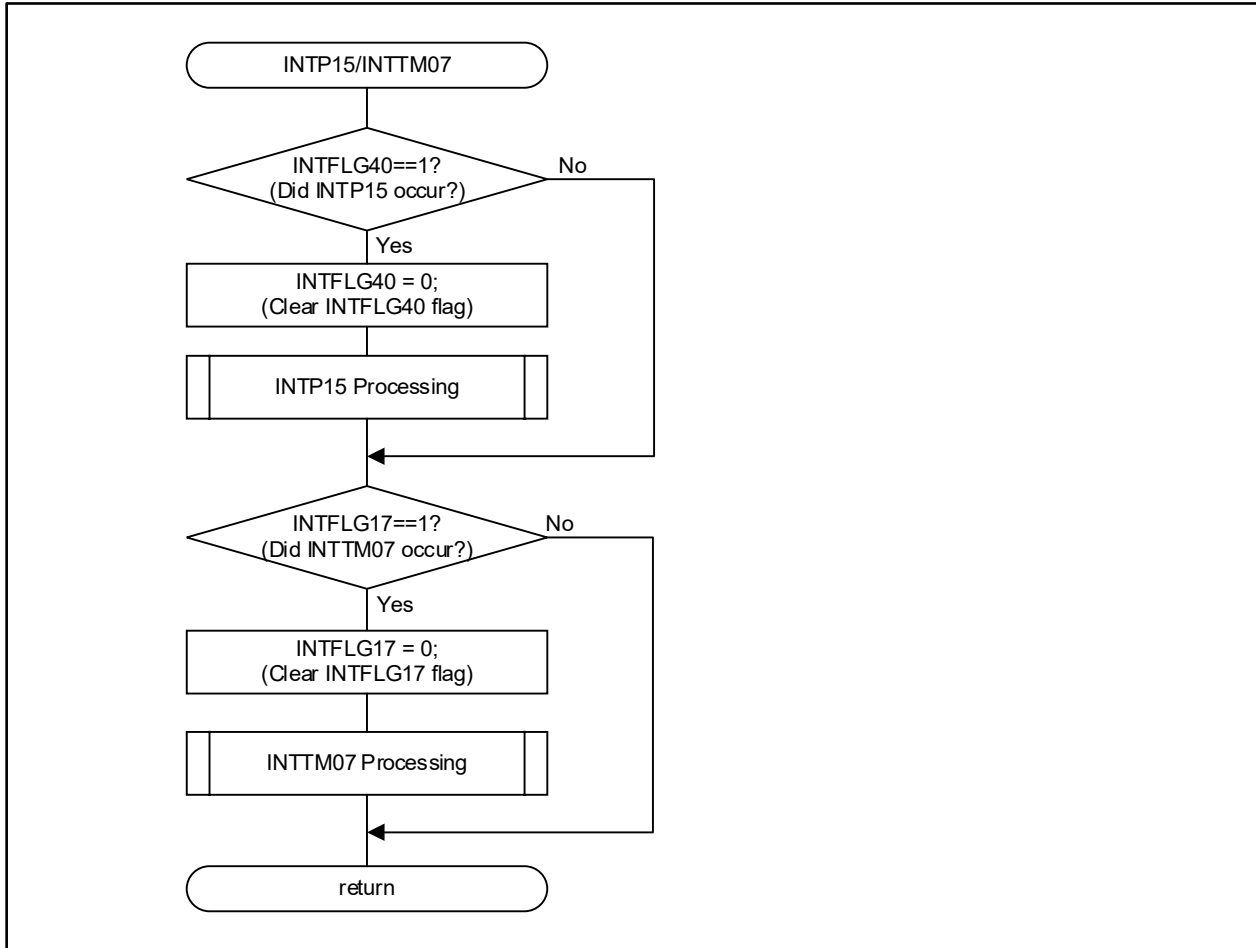


Figure 1-8 INTP15/INTTM07 Interrupt Judgement Example

1.9 Determination between INTTM1x and INTTM2x

Figure 1-9 shows an interrupt processing example in case of both INTTM07 (End of TAU1 channel x count/capture) and INTTM2x (End of TAU2 channel x count/capture) are enabled.

Interrupt by INTTM1x can be determined from INTFLG2x bit of INTFLG2 (Interrupt source determination flag register 2). And interrupt by INTTM2x can be determined from INTFLG3x bit of INTFLG3 (Interrupt source determination flag register 3).

Remarks: x = 0 to 7

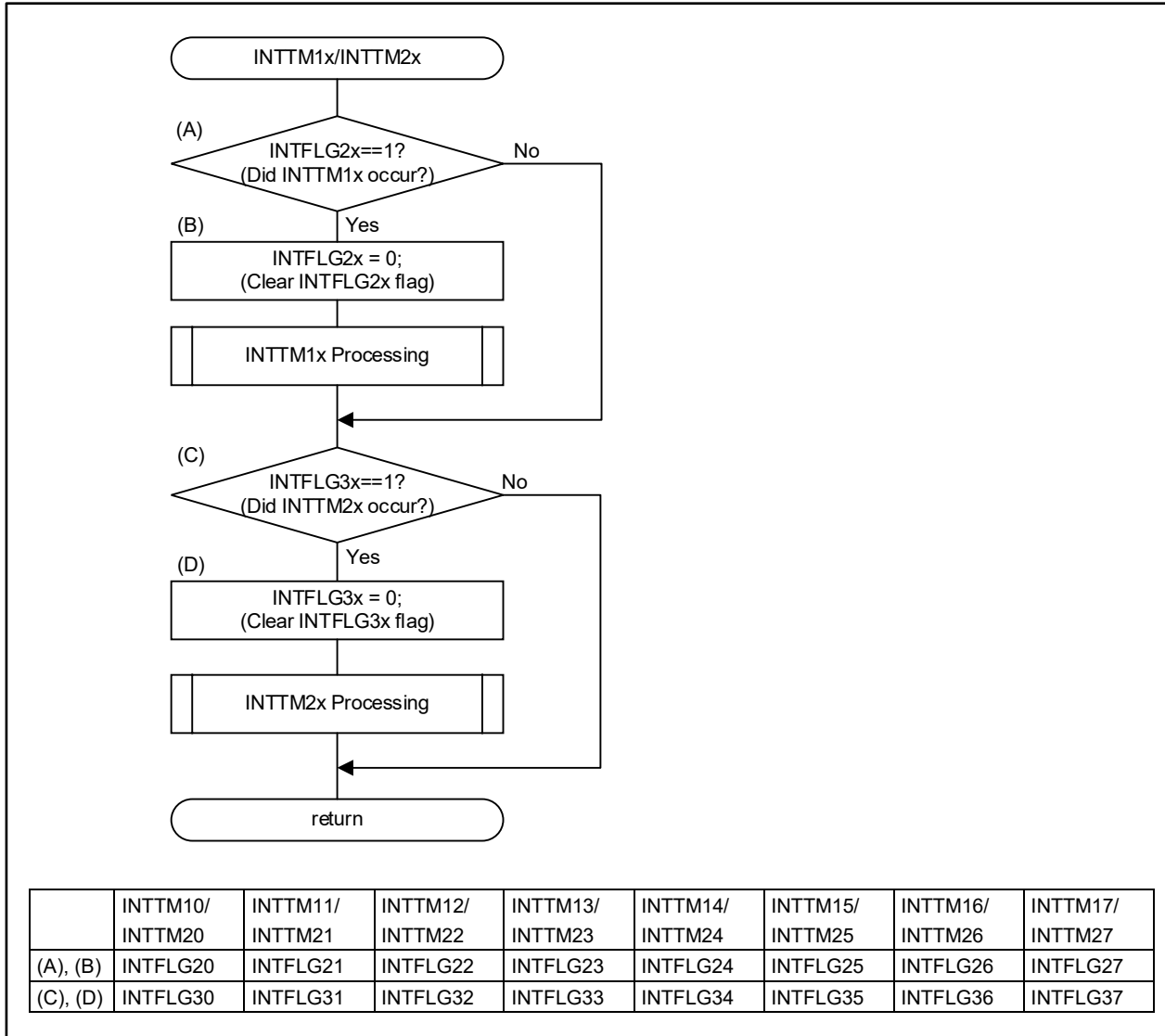


Figure 1-9 INTTM1x/INTTM2x Interrupt Judgement Example

2. Notes on Interrupt Source Determination

2.1 Notes when Clearing bit of INTFLGn Register

If a new interrupt of the same source occurs during interrupt processing, the interrupt request (IF bit) may become "1" even if the INTFLGnm bit of INTFLGn register is cleared. In this case, the interrupt is generated, but its interrupt factor INTFLGnm bit is "0" (no interrupt request), so its interrupt is terminated without processing.

The above case will be explained using the INTP4 / INTSPM interrupt as an example. After the INTFLG00 bit is determined to be "1" (INTP4 request is occurred) in the interrupt processing shown in **Figure 2-1** and if a new effective edge is input to the INTP4 pin before the INTFLG00 bit is cleared, the PIF4 bit of the IFOL register is set to "1". After that, the INTFLG00 bit is cleared and the INTP4 interrupt processing ends. And the INTP4 / INTSPM interrupt occurs again as the PIF4 bit is "1". However, at this time, since the INTFLG00 bit has already been cleared to "0", the next processing is executed without executing INTP4 Processing.

When using multiple interrupts with them enabled, consider the above notes when designing.

Remarks: n = 0 to 4
m = 0 to 8

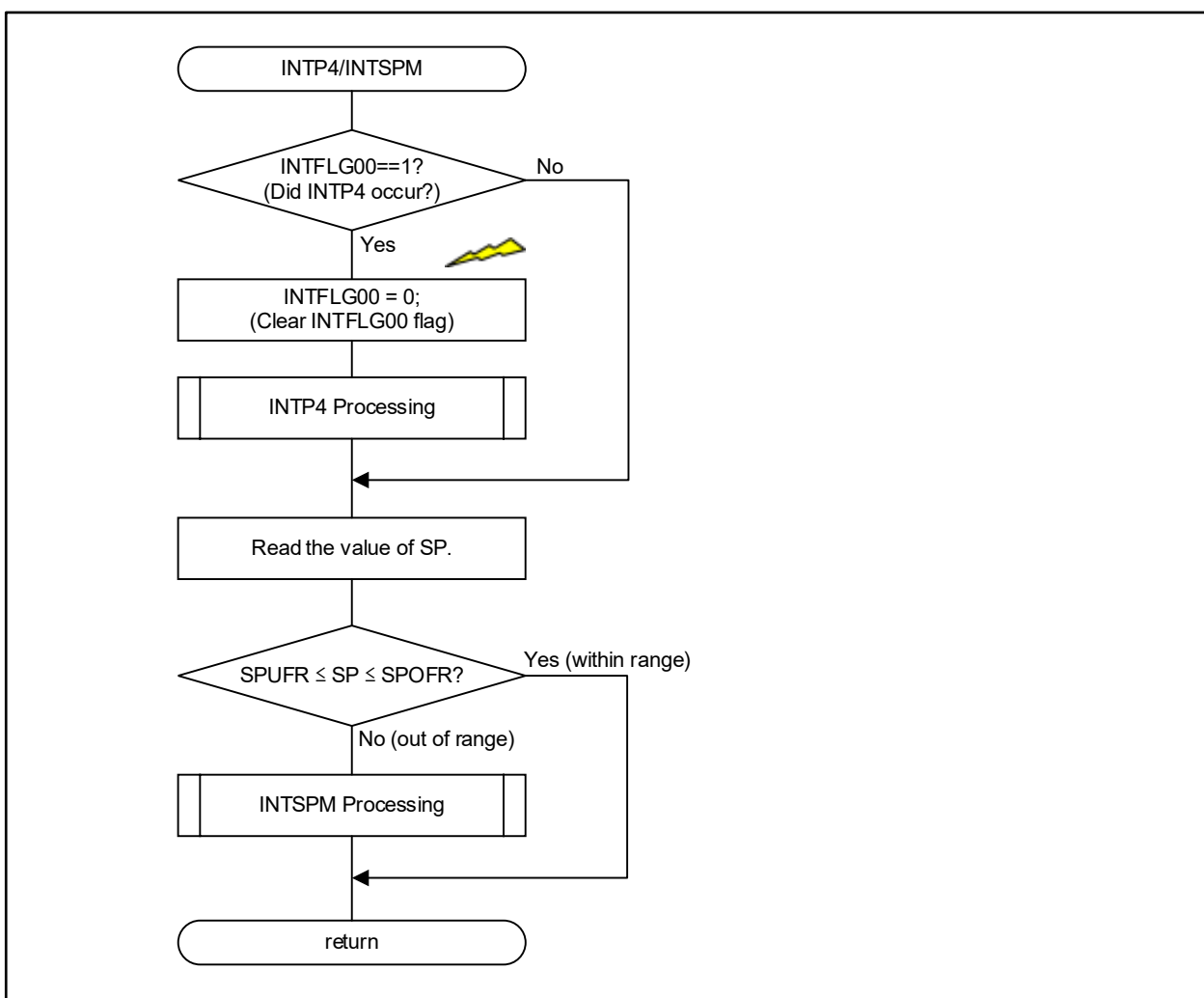


Figure 2-1 INTP4/INTSPM Interrupt Judgement Example (INTP4 occurs continuously)

2.2 Notes when Using INTSPM and INTCLM

The CPU stack pointer monitor function or Clock monitor function are a safety function, it is recommended to set those interrupt priority level high.

3. References

Documents referenced in this application note are shown below. When referring to these documents, make sure to obtain the latest version of each document from Renesas Electronics website.

- RL78/ F15 User's Manual: Hardware Rev. 1.00

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 30, 2021	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
 - "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
 - "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 November 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.