RL78/F13, F14

DTC Usage Example (Normal Transfer): A/D Converter

R01AN3259EJ0100
Rev.1.00
Nov 01, 2017

Summary

This document describes how to use the normal transfer mode of the data transfer controller (DTC) to transfer A/D conversion results to the conversion result storage area located in RAM.

Contents

1. Overview of DTC Operation

When a DTC activation request is generated, the DTC control data is loaded into the DTC module based on the address read from the DTC vector table entry assigned to the activation source. The transfer counter, transfer source address, and transfer destination address are updated and written back to the DTC control data area. After the writing of data finishes, control data (transfer counter, transfer source address, and transfer destination address) are updated and written back.

1.1 Normal Mode and Repeat Mode

DTC transfer has two modes: normal mode and repeat mode.

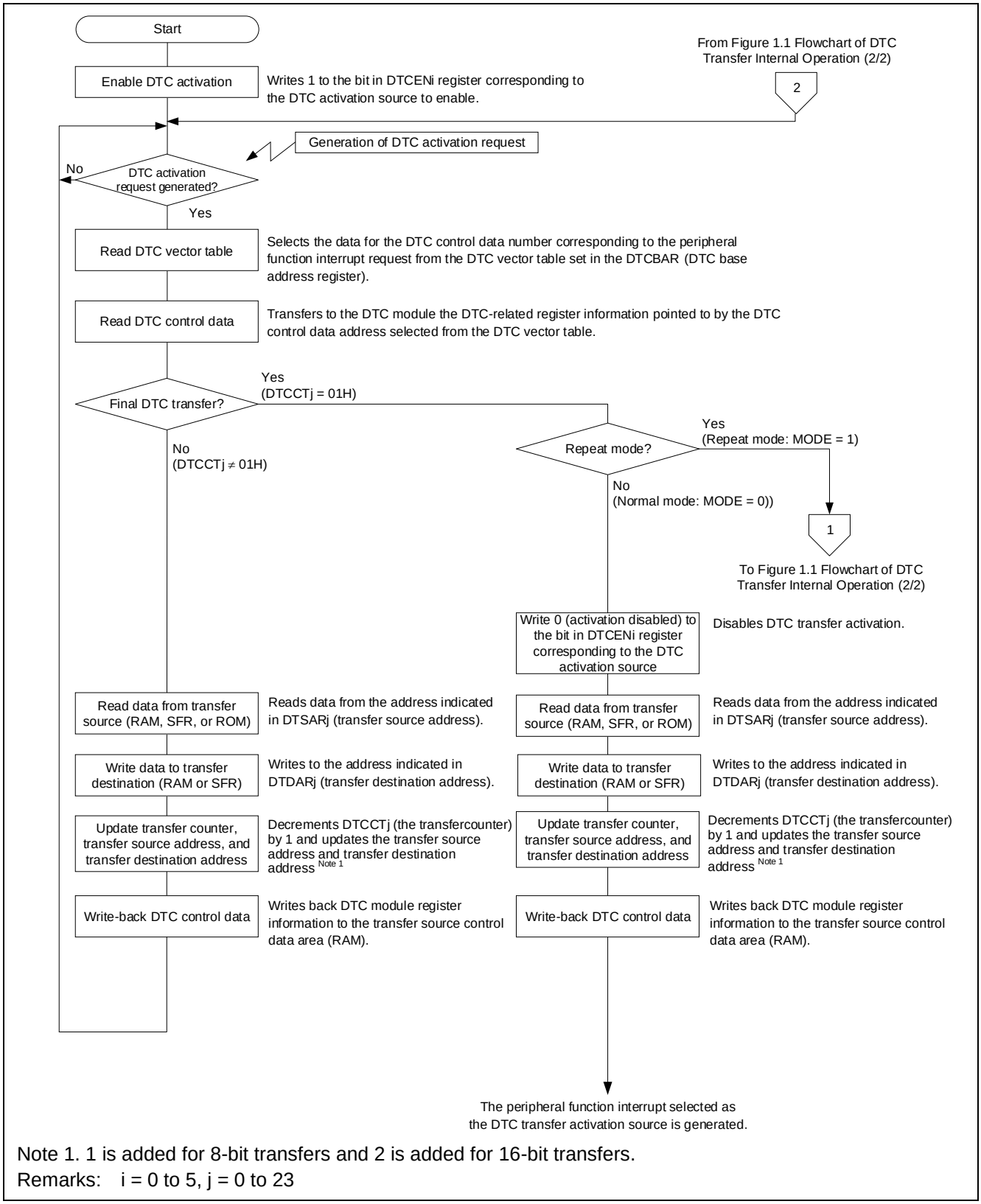
1.1.1 Normal Mode

In normal mode 1 to 256 bytes of data are transferred for each activation when 8-bit transfer is used, and 2 to 512 bytes of data are transferred when 16-bit transfer is used. The transfer count can be set to any value between 1 and 256. Data is transferred and the transfer count is decremented each time the activation source is generated until the specified transfer count reaches 0. When the transfer count value is 0, DTC transfer activation is disabled, and after the data transfer ends a DTC transfer-end interrupt is generated.

1.1.2 Repeat Mode

In repeat mode 1 to 255 bytes of data are transferred for each activation. The transfer count can be set to any value between 1 and 255. Data is transferred and the transfer count is decremented each time the activation source is generated until the specified transfer count reaches 0.the transfer counter and repeat area address are initialized, and the transfer operation is repeated. If interrupt generation is enabled, a DTC transfer-end interrupt is generated after completion of the transfer that brings the transfer count to 0.

Figure 1.1 is a flowchart of DTC transfer internal operation in normal mode and repeat mode.



Note 1. 1 is added for 8-bit transfers and 2 is added for 16-bit transfers.

Remarks: i = 0 to 5, j = 0 to 23

Figure 1.1 Flowchart of DTC Transfer Internal Operation (1/2)

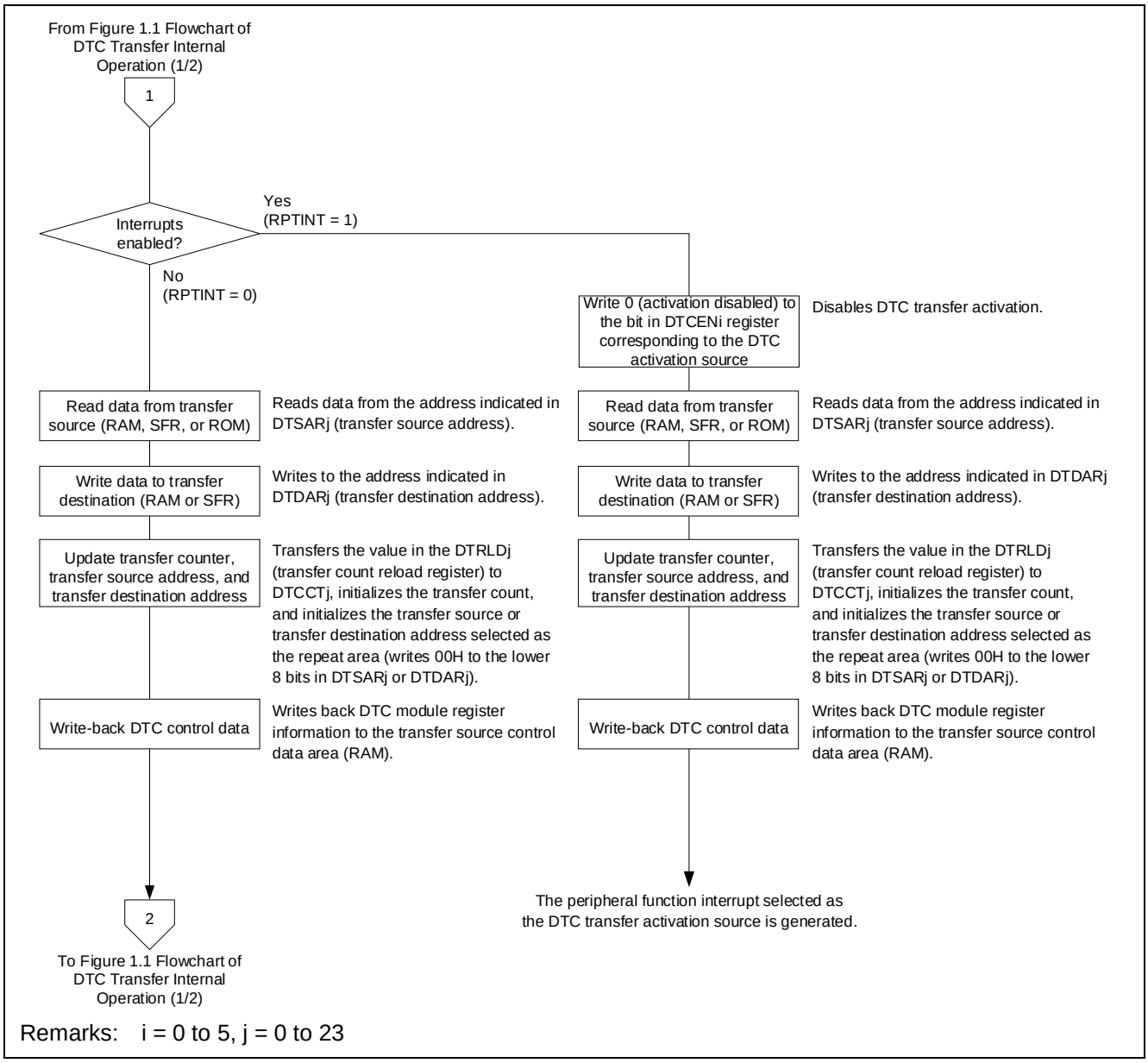


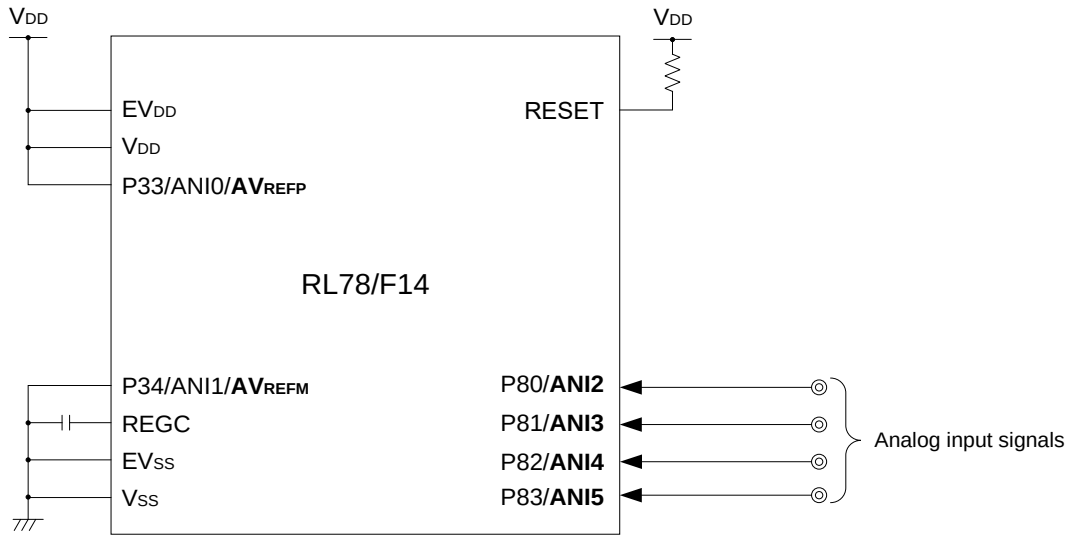
Figure 1.1 Flowchart of DTC Transfer Internal Operation (2/2)

2. Specifications

A usage example combining the DTC, A/D converter, and timer array unit (TAU) channel 0 (TAU00) and channel 1 (TAU01) is presented below.

TAU00 (2 ms) and TAU01 (1 ms) count in coordinated fashion, and the A/D converter uses the TAU01 interrupt request signal as the trigger to start A/D conversion. The DTC uses A/D conversion end as the DTC activation source and stores the A/D conversion result in RAM. Thereafter the processing is repeated.

Figure 2.1 is a connection diagram showing the pins used, Table 2.1 lists the peripheral functions used and their applications, Figure 2.2 is a configuration diagram of the peripheral functions used, and Figure 2.3 shows the DTC transfer timing.



In the application described in this document AV_{REFP}, AV_{REFM}, ANI2, ANI3, ANI4, and ANI5 are used.

Figure 2.1 Connection Diagram of Pins Used

Table 2.1 Peripheral Functions Used and Their Applications

Peripheral Function	Application
DTC	Transfers the A/D conversion results to RAM at A/D conversion end. • DTC activation source: A/D conversion end • Transfer source address: ADCR register • Transfer destination address: RAM • Transfer count: 4 • Operating mode: Repeat mode
A/D converter	Performs A/D conversion on the analog input signals from pins ANI2 to ANI5. • 10-bit resolution • Hardware trigger no-wait mode (source: INTTM01 signal) • Scan mode (4-pin) • One-shot conversion mode
TAU00	Constant-period timer • Internal timer mode (2 ms) • Used as master channel.
TAU01	Generates A/D conversion trigger (INTTM01 signal). • One-count mode (1 ms) • Used as slave channel.

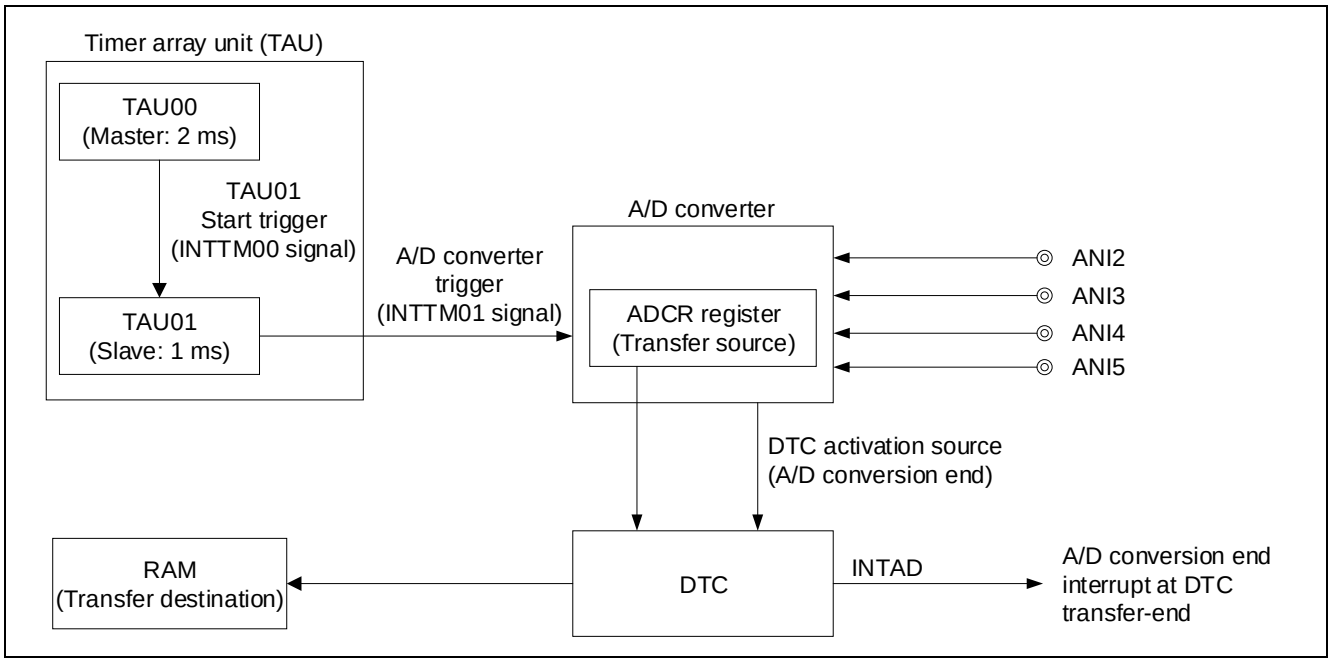
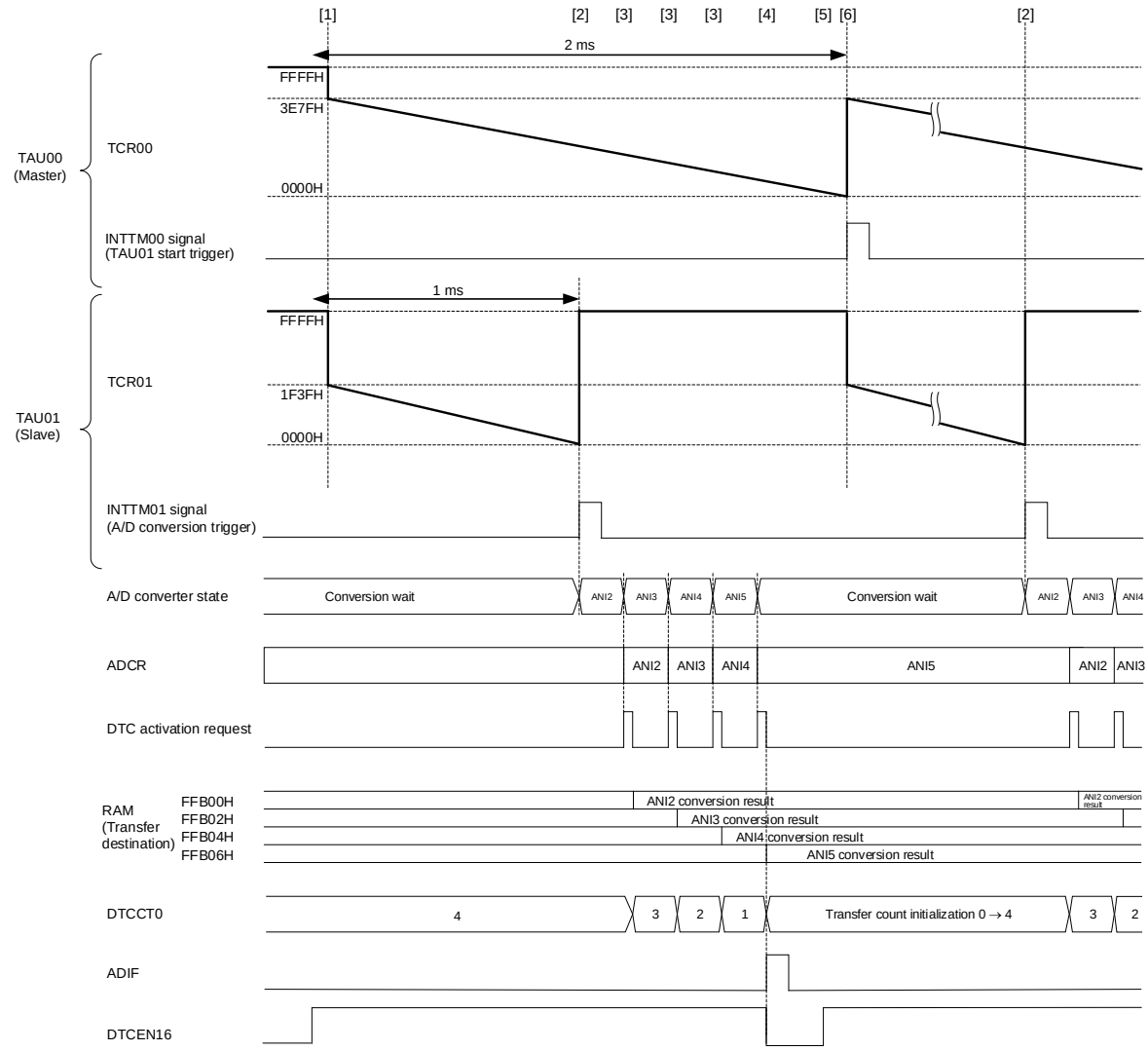


Figure 2.2 Configuration Diagram of Peripheral Functions Used



[1] The DTCEN16 bit in the DTCEN1 register is set to 1 (DTC activation enabled (source: A/D conversion end)) by software. Also, bits TS00 and TS01 in the TS0 register are set to 1 (TAU00 and TAU01 start counting) by software.
[2] When TAU01 finishes counting, the INTTM01 signal is output. Also, A/D conversion starts, using this signal as the trigger.
[3] At A/D conversion end, the DTC performs a memory transfer (ADCR register → RAM). Also, DTCCT0 is decremented and the DTC transfer destination address is incremented when the DTC transfer takes place.
[4] When the transfer that causes the value of DTCCT0 to change from 1 to 0 is executed, the following operations are performed:
- The DTCEN16 bit is cleared to 0 (DTC activation disabled).
- The ADIF bit changes to 1 (generation of A/D conversion end interrupt request at DTC transfer-end).
- A DTC data transfer is performed (ADCR register → RAM).
- The value of DTRLD0 is stored in DTCTC0 (initialization of DTC transfer count).
- 00H is stored in the lower byte in DTDAR0 (initialization of transfer destination address).

[5] The DTCEN16 bit in the DTCEN1 register is set to 1 (DTC activation enabled (source: A/D conversion end)) by software.
[6] When TAU00 finishes counting, the INTTM00 signal is output (generation of TAU00 interrupt request signal). Also, TAU01 (slave) starts counting.

Notes: TCR00: Timer counter register 00
INTTM00 signal: TAU00 count-end/capture-end interrupt request signal
TCR01: Timer counter register 01
INTTM01 signal: TAU01 count-end/capture-end interrupt request signal
(Used as A/D conversion-start trigger.)
ADCR: 10-bit A/D conversion result register
DTC activation request: A/D conversion end interrupt signals for each pin
FFB00H to FFB07H: RAM area (conversion result storage area) indicated by DTDAR0
(DTC transfer destination address in DTC control data area)
DTCCT0: DTC transfer count register 0 in DTC control data area
ADIF: A/D conversion end interrupt flag
DTCEN16: DTCEN16 bit in DTCEN1 register
The TAU count clock is CK02 (8 MHz).

Figure 2.3 DTC Transfer Timing

3. Setting Procedures of Peripheral Functions

The setting procedures of the peripheral functions (DTC, A/D converter, TAU00, and TAU01) are described in this section.

3.1 Peripheral Function Initialization Procedure

Initialization of the peripheral functions (DTC, A/D converter, TAU00, and TAU01) is described below.

Figure 3.1 shows the peripheral function initialization procedure.

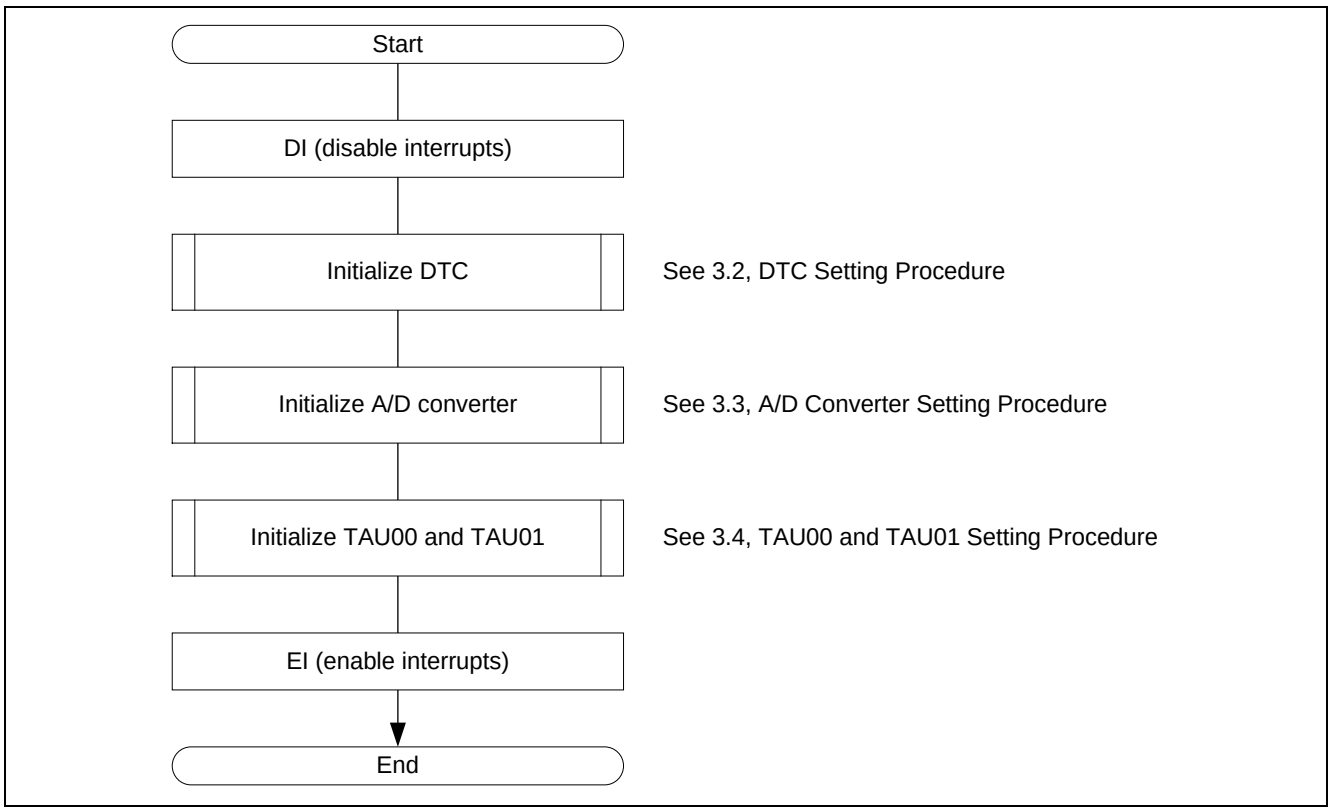


Figure 3.1 Peripheral Function Initialization Procedure

3.2 DTC Setting Procedure

The DTC transfers the A/D conversion results to the conversion result storage area in RAM, using the end of A/D conversion as the activation source.

Figure 3.2 shows the DTC initialization procedure.

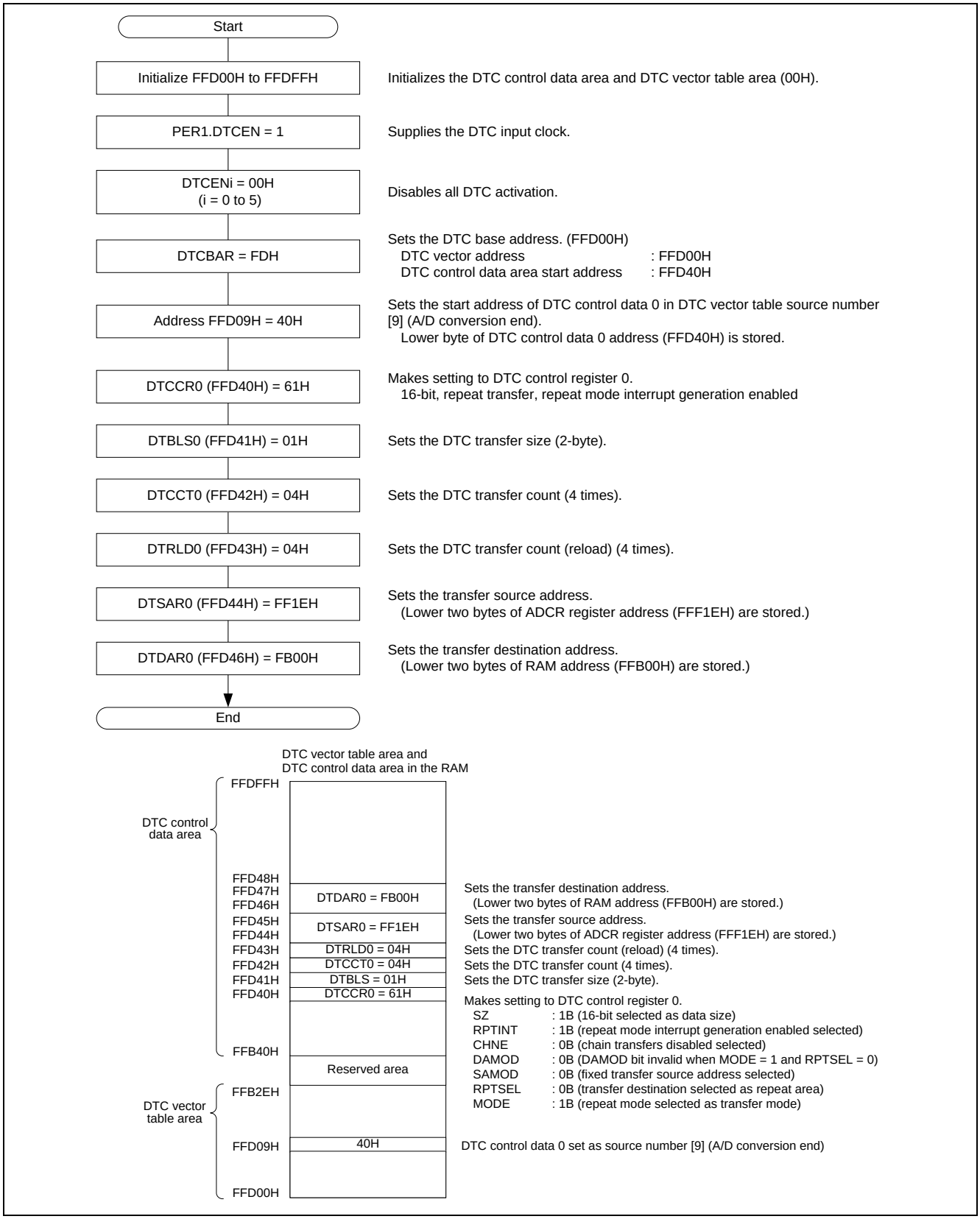


Figure 3.2 DTC Initialization Procedure

3.3 A/D Converter Setting Procedure

The following settings are used to perform A/D conversion of the analog input signals on pins ANI2 to ANI5.

Figure 3.3 shows the initialization procedure for the A/D converter.

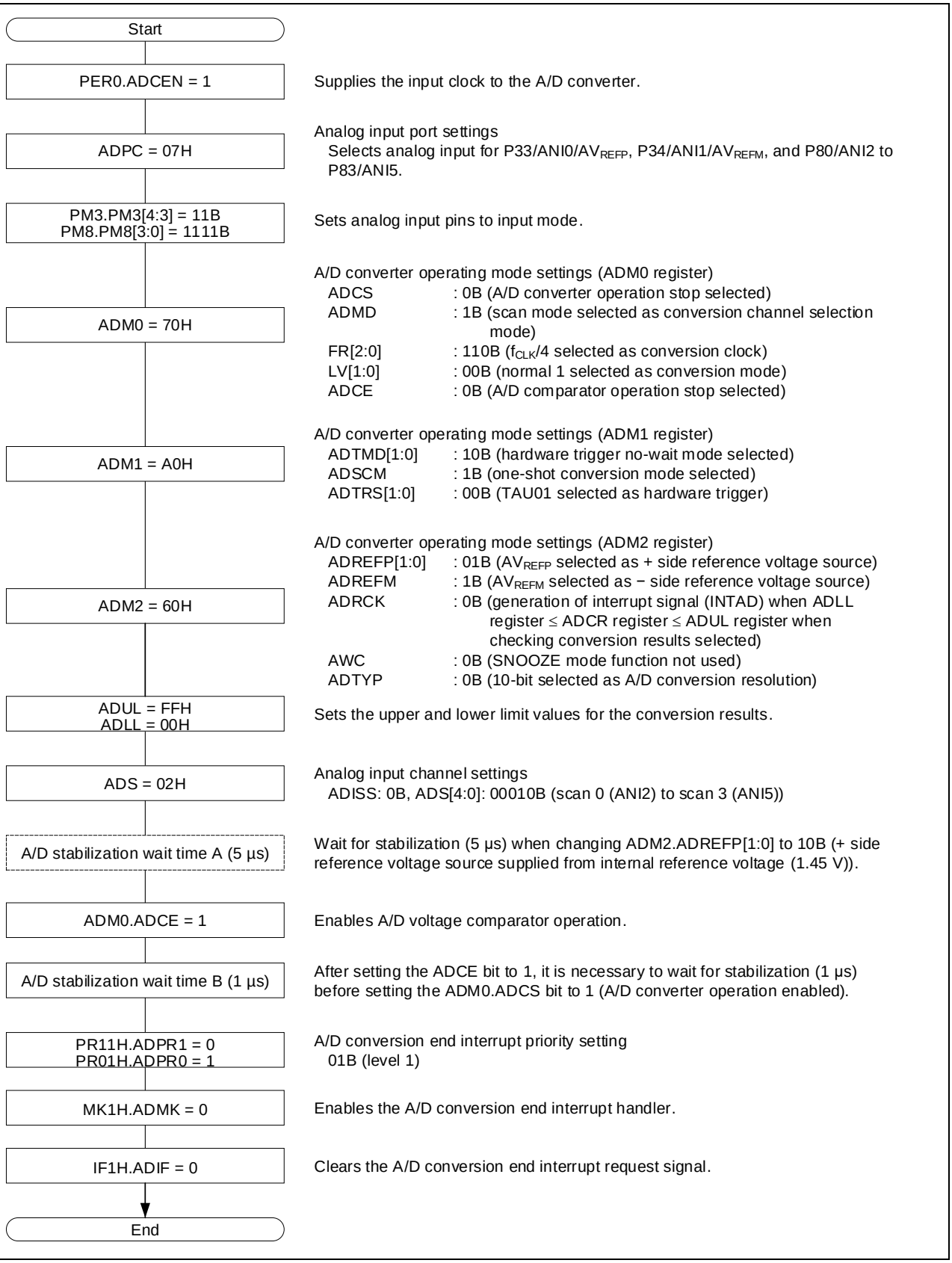


Figure 3.3 A/D Converter initialization Procedure

3.4 TAU00 and TAU01 Setting Procedure

The timer array unit (TAU) is used as a PWM function. TAU00 is set as the master channel and TAU01 as the slave channel, and a PWM signal is generated with a period of 2 ms and 50% duty. Note that PWM waveforms are not used in this example.

Figure 3.4 shows the initialization procedure for TAU00 and TAU01.

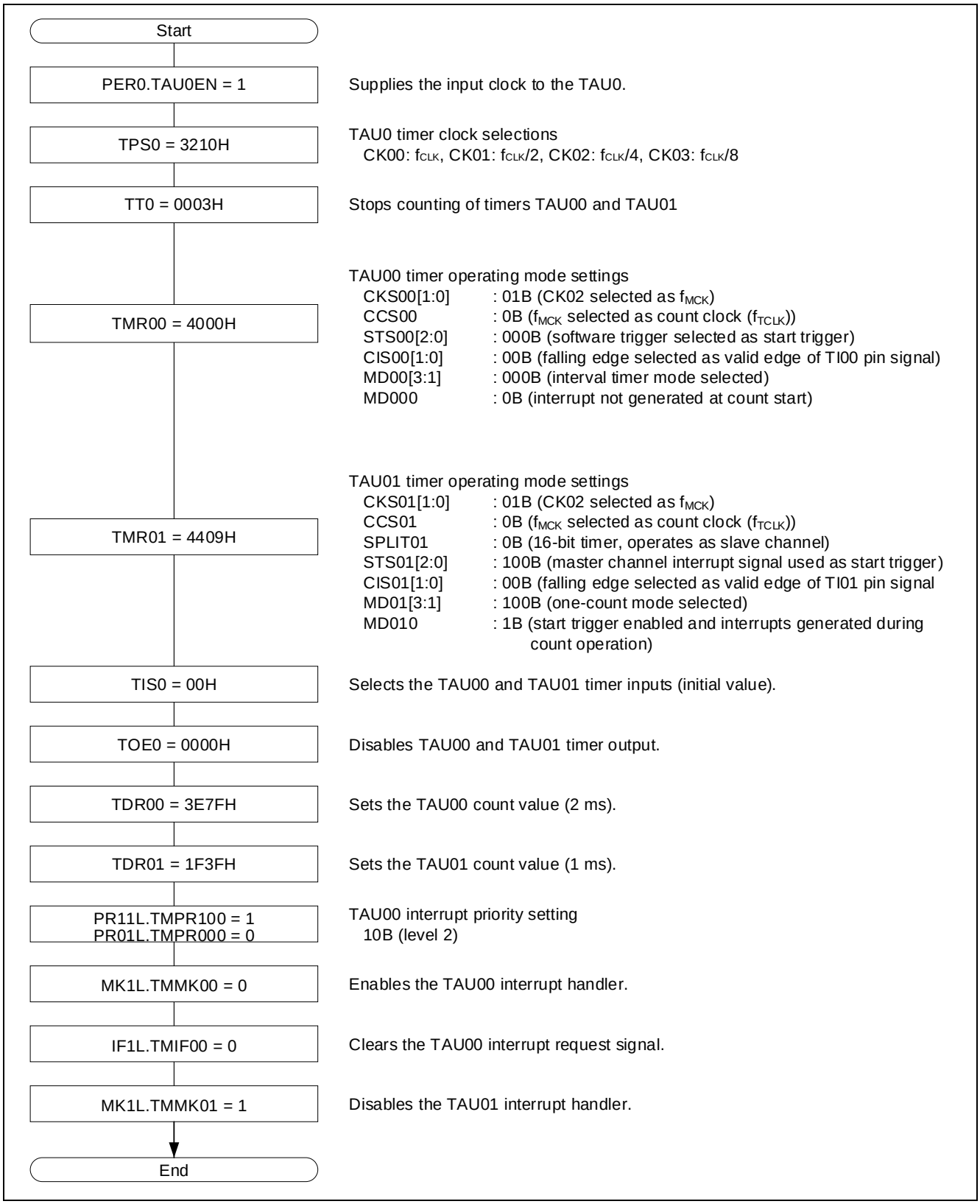
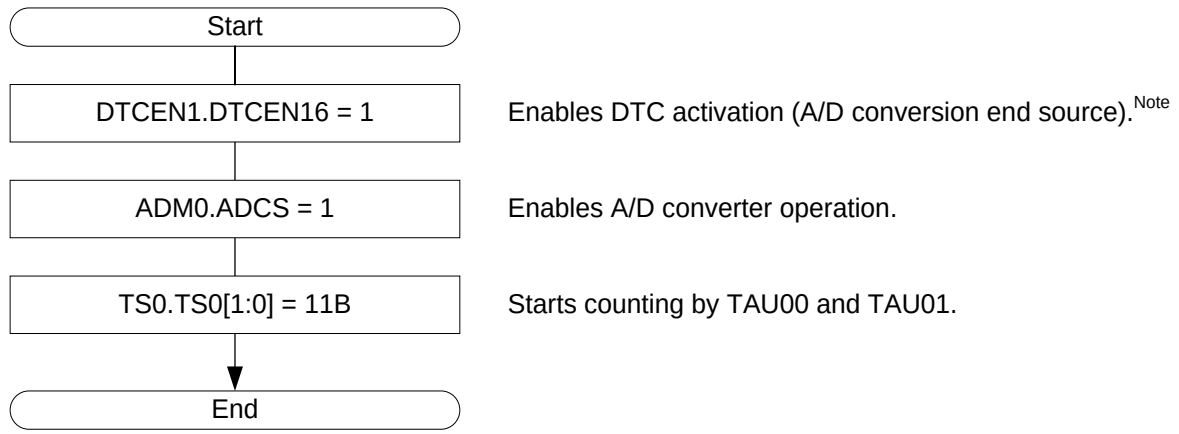


Figure 3.4 TAU00 and TAU01 Initialization Procedure

3.5 Procedure for Enabling Peripheral Functions (DTC Transfer Start)

After initializing the peripheral functions (DTC, A/D converter, TAU00, and TAU01), the operation is enabled (started).

Figure 3.5 shows the procedure for enabling the operation of the peripheral functions (DTC transfer start).



Note Writing to the DTCEN16 bit should be performed when interrupt sources for which DTC activation is enabled in the DTCEN1 register, and the interrupt source (A/D conversion end) set as activation-enabled, will not be generated.

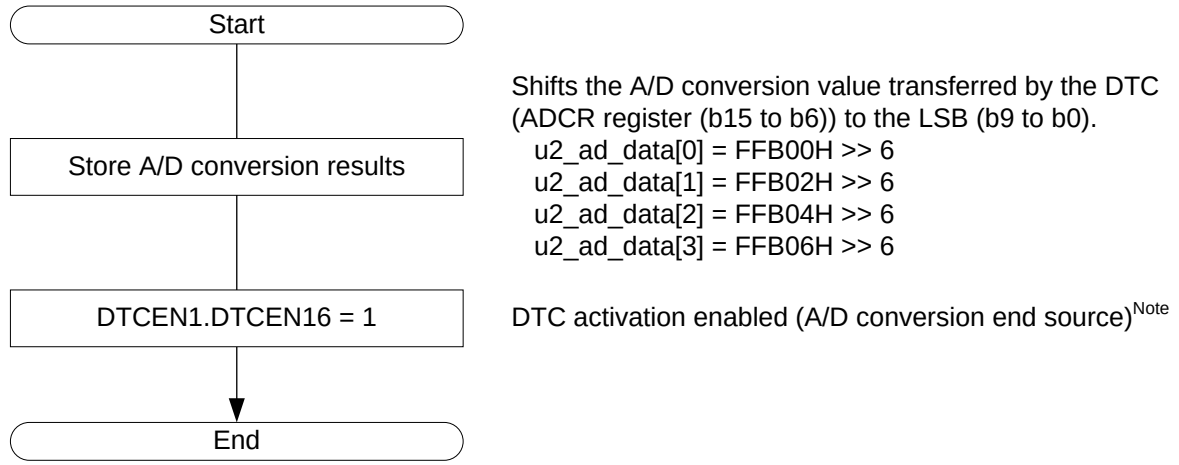
Figure 3.5 Procedure for Enabling Peripheral Functions (DTC Transfer Start)

3.6 DTC Transfer-End Interrupt Handler

It is possible to generate an interrupt corresponding to the end of a DTC transfer (the A/D conversion end interrupt in the example described in this document).

Figure 3.6 shows the DTC transfer-end interrupt (A/D conversion end interrupt) handler.

The contents of the upper 10 bits (b15 to b6) of the A/D conversion results stored in memory after the DTC transfer are shifted to the lower 10 bits (b9 to b0). Then, DTC transfer operation is re-enabled.



Note Writing to the DTCEN16 bit should be performed when interrupt sources for which DTC activation is enabled in the DTCEN1 register, and the interrupt source (A/D conversion end) set as activation-enabled, will not be generated.

Figure 3.6 DTC Transfer-End Interrupt (A/D Conversion End Interrupt) Handler

4. Important Points

4.1 DTC Transfer Cycle Count

When using the DTC under the specifications indicated in the usage example presented in this document, the DTC transfer cycle count is nine clock cycles per transfer. See Table 4.1 for details.

Table 4.1 DTC Transfer Clock Cycle Count (Transfer Source: ADCR Register, Transfer Destination: RAM, Repeat Mode)

Vector Read	Control Data		Data Read	Data Write	Total
	Read	Write-Back			
1	4	2	1	1	9

Note: See Table 4.2 for the control data write-back clock cycle count, Table 4.3 for the data read clock cycle count, and Table 4.4 for the data write clock cycle count. The settings used in the example presented in this document are indicated in Table 4.2 to Table 4.4 by the white unshaded cells.

Table 4.2 Clock Cycle Count Necessary for DTC Control Data Write-Back

DTCCR Register				Address Fixed/Incremented		Write-Back Registers in Control Data Area				Clock Cycles
DAMOD	SAMOD	RPTSEL	MODE	Transfer Source	Transfer Destination	DTCCTj	DTRLDj	DTSARj	DTDARj	
0	0	X	0	Fixed	Fixed	Write-back	Write-back	—	—	1
0	1	X	0	Incremented	Fixed	Write-back	Write-back	Write-back	—	2
1	0	X	0	Fixed	Incremented	Write-back	Write-back	—	Write-back	2
1	1	X	0	Incremented	Incremented	Write-back	Write-back	Write-back	Write-back	3
0	X	1	1	Repeat	Fixed	Write-back	Write-back	Write-back	—	2
1	X	1	1	Repeat	Incremented	Write-back	Write-back	Write-back	Write-back	3
X	0	0	1	Fixed	Repeat	Write-back	Write-back	—	Write-back	2
X	1	0	1	Incremented	Repeat	Write-back	Write-back	Write-back	Write-back	3

Note: X: 0 or 1, —: no write-back, j = 0 to 23

Table 4.3 DTC Data Read Clock Cycle Count

RAM	Flash Memory		SFR		
	Code Flash	Data Flash	1st SFR	2nd SFR (No Wait)	2nd SFR (Wait)Note
1	2	4	1	1	1 + wait cycle count

Note A wait (1 clock cycle) is necessary when accessing the CAN- and LIN-related registers and the TRJ0 register of timer RJ.

Table 4.4 DTC Data Write Clock Cycle Count

RAM	Flash Memory		SFR		
	Code Flash	Data Flash	1st SFR	2nd SFR (No Wait)	2nd SFR (Wait)Note
1	—	—	1	1	1 + wait cycle count

Note A wait (1 clock cycle) is necessary when accessing the CAN- and LIN-related registers and the TRJ0 register of timer RJ.

4.2 DTC Usage Notes

- Do not use a DTC transfer to access DTC-related registers (DTCBAR, SELHSm, HDTCCRm, HDTCCTm, HDTRLDm, HDTSARm, and HDTDARm) or the DTC control data area, DTC vector table area, or the general-register (FFEE0H-FFEFFH) space in RAM. Also, when using self-programming, the data flash libraries, the on-chip trace function, or the hot plugin function, do not access the memory areas associated with those functions.
- Write to or change the DTCENi register only when the interrupt sources for which the DTC activation is enabled in the target register, and the interrupt sources set as activation-enabled will not be generated.
- Do not use the memory areas associated with the general-register (FFEE0H-FFEFFH) space, self-programming, the data flash libraries, the on-chip trace function, or the hot plugin function as the DTC control data area or DTC vector table area.
- Only make changes to the DTC-related registers (DTCBAR, SELHSm, HDTCCRm, HDTCCTm, HDTRLDm, HDTSARm, and HDTDARm), the registers assigned to the DTC control data area (DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj), and the DTC vector table area when all DTC activation sources are set as activation-disabled (corresponding bits in DTCENi register cleared to 0).
- Make initial settings (write random values) to the DTC control data area and DTC vector table area in the RAM. The DTC vector table area (64 bytes including reserved areas) must not be used as general-purpose RAM by user programs. Note that portions of the DTC control data area (192 bytes) that are not used by the DTC can be used as general-purpose RAM.
- Do not overwrite DTCBAR more than once.
- When a DTC transfer-pending instruction (call or return instruction, unconditional or conditional branch instruction, instruction for accessing code flash memory, instruction for accessing interrupt-related registers (IFxx, MKxx, and PRxx) or PSW, instruction for accessing the data flash, or multiply, divide, or multiply-and-accumulate instruction - except for the MULU instruction) is executed, the DTC transfer does not take place and the request is put on hold. Also, no DTC transfer takes place during a PREFIX instruction and for a period equal to one instruction immediately following it.
- If a data flash access instruction is executed during the period equal to one instruction after the activation of a DTC data transfer, a wait of three clock cycles occurs due to the specifications of the internal bus.
- The DTC transfer is put on hold when an access is made to an SFR requiring a wait (CAN or LIN register, or the TRJ0 register of timer RJ).
- From the point at which a DTC activation source is generated until the point at which the DTC transfer completes, the same activation source should not be generated again.
- If there is a conflict between DTC activation sources, the priorities of the activation sources are considered. The source with the higher priority (based on the source number) takes effect, and the source with the lower priority is put on hold.
- In repeat mode, the lower byte of the address (setting value) of the repeat area must have a value of 00H. Also note that the transfer count and reload transfer count will differ according to the transfer data size.
  - 8-bit transfer: 01H to FFH (1 to 255 times)
  - 16-bit transfer: 01H to 7FH (1 to 127 times)

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Nov. 1, 2017	—	First edition issued

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