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H8SX Family

Ring Buffer Processing Using Extended Repeat Area Function of the DMAC

Introduction

The direct memory access controller (DMAC) performs ring buffer processing using the extended repeat area function.

Target Device

H8SX/1653

Contents

1. Specifications

- A 256-byte ring buffer is allocated in on-chip RAM.
- The DMAC transfers 192-byte data blocks from the ring buffer to the destination area in on-chip RAM.
- The block transfer ends after a total of 512 bytes of data have been transferred.

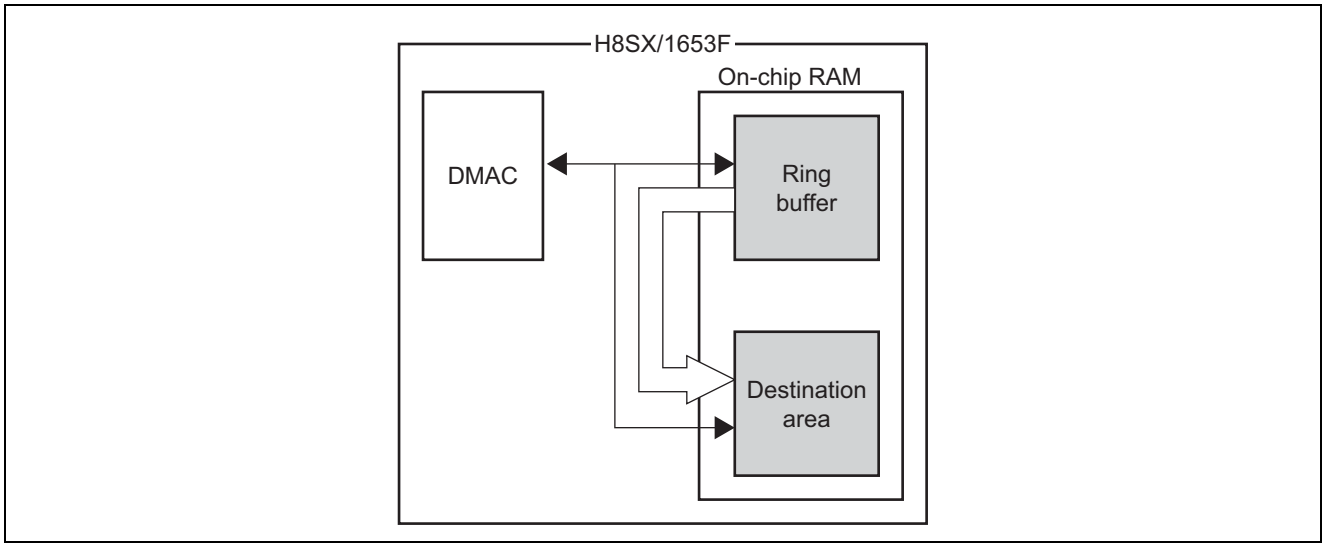


Figure 1 Ring Buffer Processing by DMAC Extended Repeat Transfer

Table 1 DMA Transfer Settings

Item	Contents
DMA transfer request	Auto request mode
Bus mode	Cycle stealing mode
Transfer mode	Block transfer mode
Address mode	Dual address mode
Unit of transfer	Longword

2. Conditions for Application

Table 2 Conditions for Application

Item	Contents
Operating frequency	Input clock: 12 MHz System clock (Iϕ): 48 MHz Peripheral module clock (Pϕ): 24 MHz External bus clock (Bϕ): 48 MHz
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)
Development tool	High-performance Embedded Workshop Version 4.00.03
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Version 6.01.01 (from Renesas Technology Corp.)
Compile option	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register,shift,struct,expression)

Table 3 Section Settings

Address	Section Name	Description
H'001000	P	Program area
H'FF2000	B	Uninitialized data area (RAM area)

3. Description of Modules Used

Figure 2 shows a block diagram of the DMAC. The block diagram of the DMAC is described below.

- DMA source address register_0 (DSAR_0)
  A 32-bit readable/writable register that specifies the source address of DMA transfer. This register has an address updating function so the value of this register is changed to the next source address after each transfer processing.
- DMA destination address register_0 (DDAR_0)
  A 32-bit readable/writable register that specifies the destination address of DMA transfer. This register has an address updating function so the value of this register is changed to the next destination address after each transfer processing.
- DMA offset register_0 (DOFR_0)
  A 32-bit readable/writable register that specifies the offset used in updating the source or destination address when offset addition is specified.
- DMA transfer count register_0 (DTCR_0)
  A 32-bit readable/writable register that specifies the size of the data to be transferred (total transfer size). The value of this register will be decremented by a value corresponding to the access size of the transferred data after each data transfer. In this sample task, the size of the data for transfer is set as 512 bytes (H'00000200) and the unit of data access is a longword. Accordingly, the value of this register is decremented by four during DMA transfer, indicating the size of the remaining data.
- DMA block size register_0 (DBSR_0)
  DBSR is enabled in repeat transfer mode or block transfer mode and specifies the repeat size or block size. It is disabled in normal transfer mode. In this sample task, the DMAC operates in block transfer mode with the block size specified as 192 bytes.
- DMA mode control register_0 (DMDR_0)
  Controls operation of the DMAC.
- DMA address control register_0 (DACR_0)
  Sets the operating mode and transfer mode.

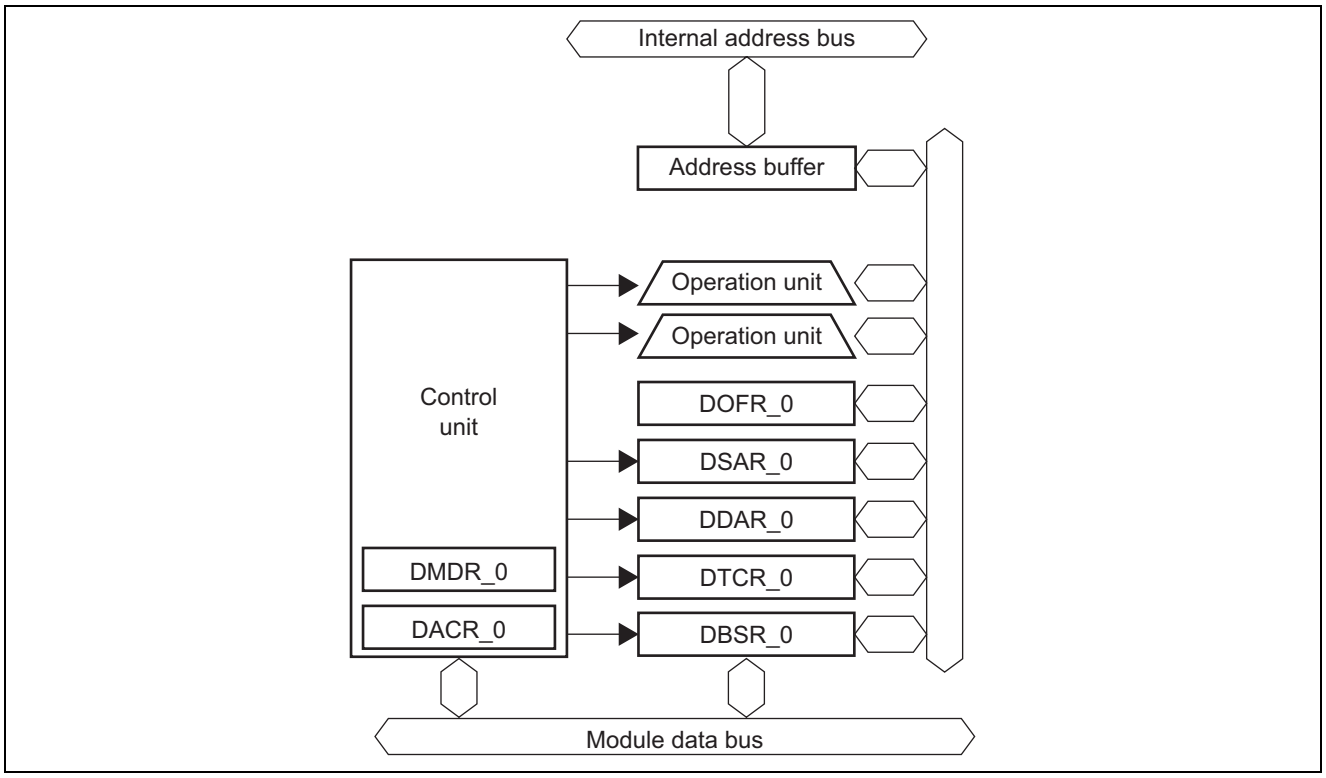


Figure 2 Block Diagram of DMAC

4. Description of Operation

The following gives an overview of the extended repeat transfer in block transfer mode.

- First transfer
  - 192 bytes of data is transferred from the ring buffer to the destination area.

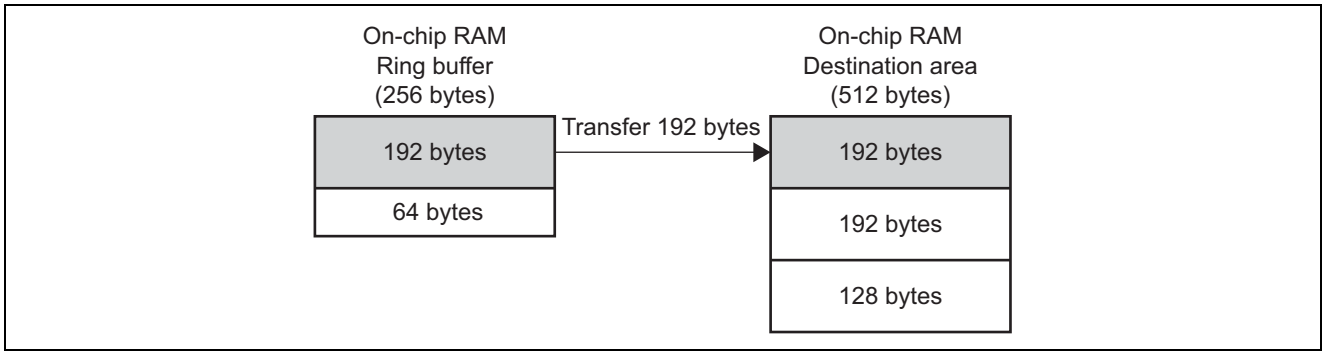


Figure 3 Example of Extended Repeat Transfer (1)

- Second transfer
  - 192 bytes of data is transferred from the ring buffer to the destination area.
  - When 64 bytes have been transferred, the source address is initialized to the start address of the ring buffer and data transfer to the destination area is continued.

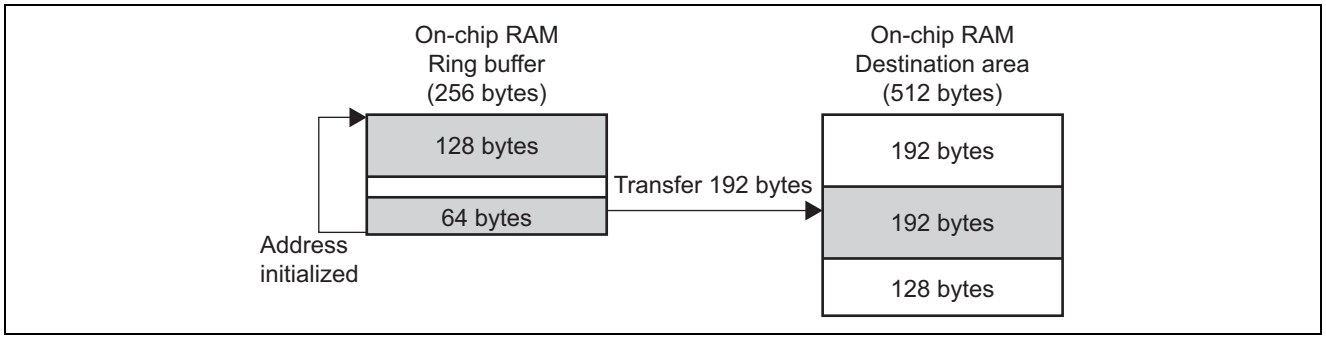


Figure 4 Example of Extended Repeat Transfer (2)

- Third transfer
  - 128 bytes of data is transferred from the ring buffer to the destination area.

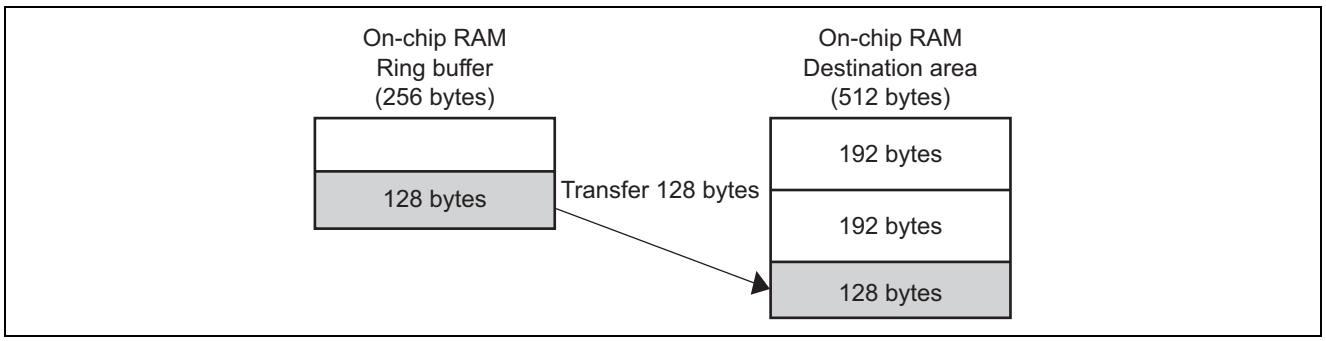


Figure 5 Example of Extended Repeat Transfer (3)

5. Description of Software

5.1 List of Functions

Table 4 List of Functions

Function Name	Functions
init	Initialization routine Sets the CCR, configures the clocks, cancels the module stop mode, and calls the main function.
main	Main routine Makes the settings for block transfer mode, source and destination addresses, and extended repeat transfer.
dmtend0_int	DMAC0 transfer end interrupt handling routine Disables transfer by the DMAC and clears the flags. This interrupt processing is performed when transfer has been completed for the total transfer size.
dmeend0_int	DMAC0 repeat size end interrupt handling routine Enables transfer by the DMAC. This interrupt processing is performed when transfer of the data for the extended repeat size has been completed.

5.2 Vector Table

Table 5 Interrupt and Exception Handling Vector Table

Exception Handling Source	Vector Number	Vector Table Address	Exception Handling Routine
Reset	0	H'000000	main
DMAC0 TEND	128	H'000200	dmtend0_int
DMAC0 EEND	136	H'000220	dmeend0_int

5.3 RAM Usage

Table 6 RAM Usage

Type	Variable Name	Description	Used In
unsigned char	ramarea1[256]	Ring-buffer RAM area	main
unsigned char	ramarea2[512]	Destination RAM area	main
unsigned char	userf	Transfer end flag userf = 0: Transfer is in progress userf = 1: Transfer has been completed	main, dmtend0_int

5.4 Description of Functions

5.4.1 init Function

(1) Functional overview

Initialization routine which cancels the module stop mode, sets up the clocks, and calls the main function.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- System clock control register (SCKCR) Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Function
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock, which is
8	ICK0	0	R/W	supplied to the CPU, DMAC, and DTC. 000: Input clock × 4
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module
4	PCK0	1	R/W	clock. 001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	0	R/W	000: Input clock × 4

- MSTPCRA, MSTPCRB, and MSTPCRC control module stop mode. Setting a bit in these registers to 1 places the corresponding module in module stop mode, while clearing the bit to 0 cancels module stop mode.

- Module stop control register A (MSTPCRA) Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Function
15	ACSE	0	R/W	All-module-clock-stop mode enable Enables or disables transition to all-module-clock-stop mode. If this bit is set to 1, all-module-clock-stop mode is entered when the SLEEP instruction is executed by the CPU while all the modules under control of the MSTPCR registers are placed in module stop mode. In all-module-clock-stop mode, even the bus controller and I/O ports are stopped to reduce the supply current. 0: Disables transition to all-module-clock-stop mode. 1: Enables transition to all-module-clock-stop mode.
13	MSTPA13	0	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer (TMR_3, TMR_2)
8	MSTPA8	1	R/W	8-bit timer (TMR_1, TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

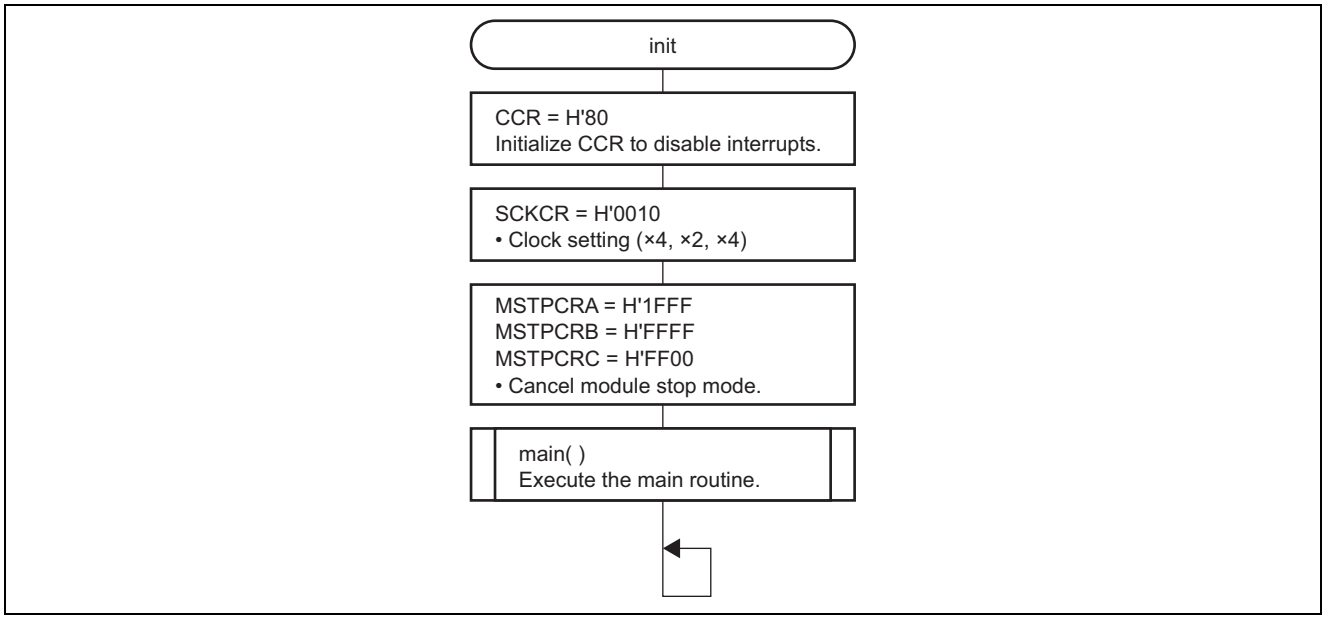
- Module stop control register B (MSTPCRB) Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Function
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communication interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communication interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communication interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communication interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface_1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface_0 (IIC_0)

- Module stop control register C (MSTPCRC) Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Function
15	MSTPC15	1	R/W	Serial communication interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communication interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy check
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

(5) Flowchart


init
CCR = H'80
Initialize CCR to disable interrupts.
SCKCR = H'0010
• Clock setting (×4, ×2, ×4)
MSTPCRA = H'1FFF
MSTPCRB = H'FFFF
MSTPCRC = H'FF00
• Cancel module stop mode.
main( )
Execute the main routine.

5.4.2 main Function

(1) Functional overview

Makes settings for DMAC transfer and starts transfer.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- DMA source address register_0 (DSAR_0) Address: H'FFFC00
  Function: Specifies the source address for data transfer.
  Setting: Start address of ramarea1
- DMA destination address register_0 (DDAR_0) Address: H'FFFC04
  Function: Specifies the destination address for data transfer.
  Setting: Start address of ramarea2
- DMA transfer count register_0 (DTCR_0) Address: H'FFFC0C
  Function: Specifies the size of the data to be transferred.
  Setting: H'00000200
- DMA block size register_0 (DBSR_0) Address: H'FFFC10
  Function: Specifies the block size in block transfer mode. When DBSR_0 = H'00300030 and DTSZ = B'10 in DMDR_0 (longword size), the block size is 192 bytes.
  Setting: H'00300030

- DMA mode control register_0 (DMDR_0) Address: H'FFFC14

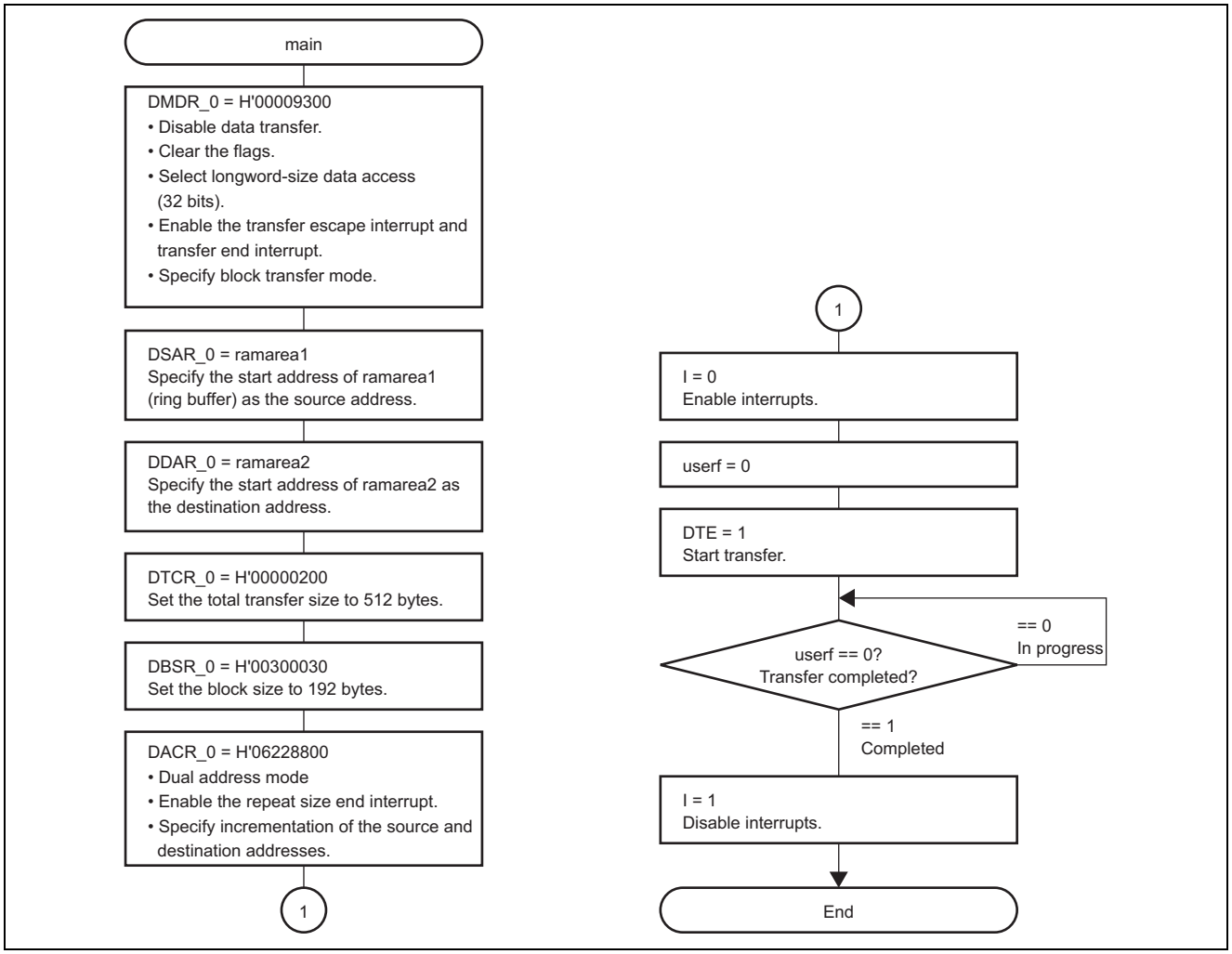
Bit	Bit Name	Setting	Function	
31	DTE	0/1	R/W	Data Transfer Enable 0: Data transfer is disabled 1: Data transfer is enabled
26	NRD	0	R/W	Next Request Delay 0: Starts accepting the next transfer request after completion of the current transfer 1: Starts accepting the next transfer request one cycle after completion of the current transfer
16	DTIF	0	R/(W)*	Data Transfer Interrupt Flag 0: Transfer end interrupt by the transfer counter has not been requested 1: Transfer end interrupt by the transfer counter has been requested
15	DTSZ1	1	R/W	Data Access Size 1, 0
14	DTSZ0	0	R/W	10: Data is accessed in longword (32 bits) units
13	MDS1	0	R/W	Transfer Mode Select 1, 0
12	MDS0	1	R/W	01: Block transfer mode
9	ESIE	1	R/W	Transfer Escape Interrupt Enable 0: Disables transfer escape end interrupts 1: Enables transfer escape end interrupts
8	DTIE	1	R/W	Data Transfer End Interrupt Enable 0: Disables transfer end interrupts 1: Enables transfer end interrupts
7	DTF1	0	R/W	Data Transfer Factor 1, 0
6	DTF0	0	R/W	00: DMAC is activated by an auto request (cycle stealing)

Note: * Only 0 can be written to clear the flag after reading the flag as 1.

- DMA address control register_0 (DACR_0) Address: H'FFFC18

Bit	Bit Name	Setting	R/W	Function
31	AMS	0	R/W	Address Mode Select 0: Dual address mode 1: Single address mode
26	RPTIE	1	R/W	Repeat Size End Interrupt Enable 0: Disables repeat size end interrupts 1: Enables repeat size end interrupts
25	ARS1	1	R/W	Area Select 1, 0
24	ARS0	0	R/W	10: Does not specify the block area in block transfer mode
21	SAT1	1	R/W	Source Address Update Mode 1, 0
20	SAT0	0	R/W	10: Source address is incremented When the unit of data access is a longword, incremented by 4
17	DAT1	1	R/W	Destination Address Update Mode 1, 0
16	DAT0	0	R/W	10: Destination address is incremented When the unit of data access is a longword, incremented by 4
15	SARIE	1	R/W	Interrupt Enable for Source Address Extended Area Overflow 0: Disables an interrupt request for an extended area overflow on the source address 1: Enables an interrupt request for an extended area overflow on the source address
12	SARA4	0	R/W	Source Address Extended Repeat Area
11	SARA3	1	R/W	These bits specify the extended repeat area on the source address.
10	SARA2	0	R/W	
9	SARA1	0	R/W	01000: Specifies 256 bytes starting from the address set in DSAR as the repeat area
8	SARA0	0	R/W	

(5) Flowchart


main
DMDR_0 = H'00009300
• Disable data transfer.
• Clear the flags.
• Select longword-size data access (32 bits).
• Enable the transfer escape interrupt and transfer end interrupt.
• Specify block transfer mode.
DSAR_0 = ramarea1
Specify the start address of ramarea1 (ring buffer) as the source address.
DDAR_0 = ramarea2
Specify the start address of ramarea2 as the destination address.
DTCR_0 = H'00000200
Set the total transfer size to 512 bytes.
DBSR_0 = H'00300030
Set the block size to 192 bytes.
DACR_0 = H'06228800
• Dual address mode
• Enable the repeat size end interrupt.
• Specify incrementation of the source and destination addresses.
1
1
I = 0
Enable interrupts.
userf = 0
DTE = 1
Start transfer.
userf == 0?
Transfer completed?
== 0
In progress
== 1
Completed
I = 1
Disable interrupts.
End

5.4.3 dmtend0_int Function

(1) Functional overview

DMAC0 transfer end interrupt handling routine

(2) Argument

None

(3) Return value

None

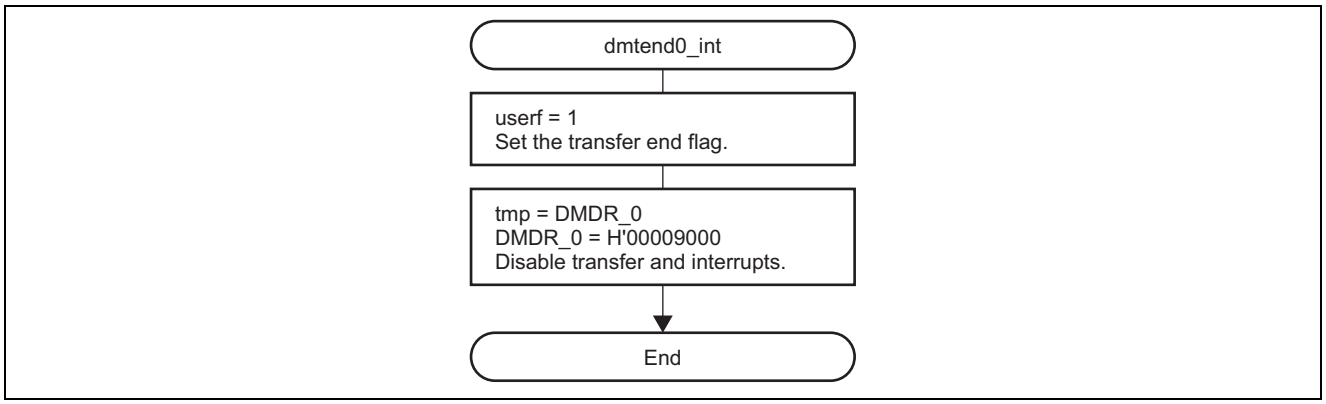
(4) Description of internal registers

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- DMA mode control register_0 (DMDR_0) Address: H'FFFC14

Bit	Bit Name	Setting	R/W	Function
31	DTE	0	R/W	Data Transfer Enable 0: Disables data transfer 1: Enables data transfer
9	ESIE	0	R/W	Transfer Escape Interrupt Enable 0: Disables transfer escape end interrupts 1: Enables transfer escape end interrupts
8	DTIE	0	R/W	Data Transfer End Interrupt Enable 0: Disables transfer end interrupts 1: Enables transfer end interrupts

(5) Flowchart



5.4.4 dmeend0_int Function

(1) Functional overview

DMAC0 repeat size end interrupt handling routine

(2) Argument

None

(3) Return value

None

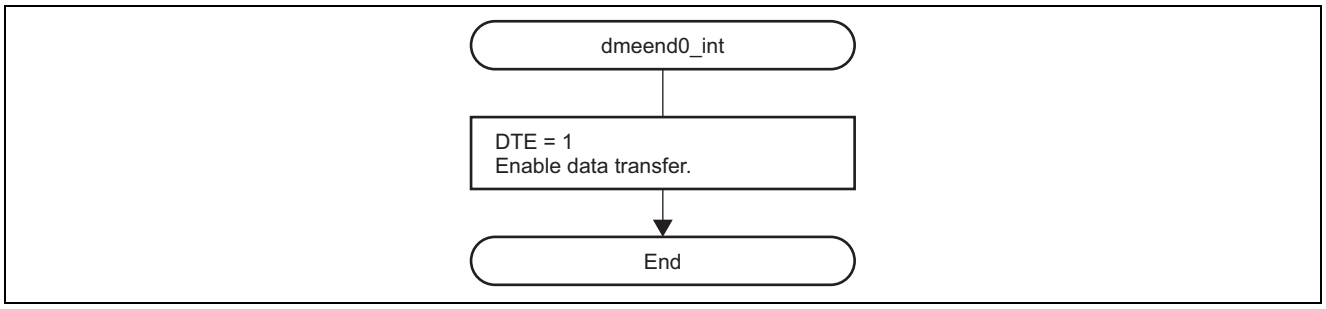
(4) Description of internal registers

The internal registers used in this sample task are described below. Note that the settings shown below are not initial values but the values used in this sample task.

- DMA mode control register_0 (DMDR_0) Address: H'FFFC14

Bit	Bit Name	Setting	R/W	Function
31	DTE	1	R/W	Data Transfer Enable 0: Data transfer is disabled 1: Data transfer is enabled

(5) Flowchart



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