RH850/U2C Group

Test Mode Procedure (CAN FD Mode) Application Note

Summary

This document applies to RH850 series. This document and the program are intended to promote understanding of the installed functions in the RH850/U2C, and it is not intended for mass production. design. It also does not reflect the latest manuals, errata, technical updates, and development environment updates. When using the corresponding function, please treat this program as a reference, and use the latest documents and development environment at your own risk. RSCFDnCFD is omitted from the register name in the text.

Target Device

- RH850/U2Cx

Items

1. Test Function

The RH850 series has the following test functions. By using these functions, it is possible to perform the self-diagnosis test for CAN communication using a CAN transceiver or MCU, and the self-diagnosis test for RAM. For details of each process, refer to the following chapters.

- Communication Test Function
  - Standard test mode
  - Listen-only mode
  - Self-test mode 0 (external loopback mode)
  - Self-test mode 1 (internal loopback mode)
  - Restricted operation mode (Only in CAN FD mode)

- Global Test
  - RAM test (read/write test)
  - Inter-channel communication test UCRC (error test enabled)

2. Communication Test Function

2.1 Standard Test Mode (CRC Test)

When the communication test mode is enabled (CTME bit in CmCTR register is "1"), the CRC value calculated based on the transmitted or received message can be read from the register where CRC calculation data is stored. If the communication test mode is disabled (CTME bit in the CmCTR register is "0"), the CRC calculation data can always be read as "0".

The registers that read the CRC operation data are as follows.

- Classical CAN frame: CRCREG [14: 0] bit in CmERFL register
- CAN FD frame: CRCREG [20: 0] bit in FDCRC register

By using the inter-channel communication test, communication between channels is possible inside the MCU, so by comparing the CRC calculation data of the transmitted channel with the CRC calculation data of the received channel, the CRC calculation circuit test of the MCU alone can be performed. For the inter-channel communication test, refer to "2.5 Inter-channel Communication Test".

Figure 2-1 shows the inter-channel communication test connection diagram.

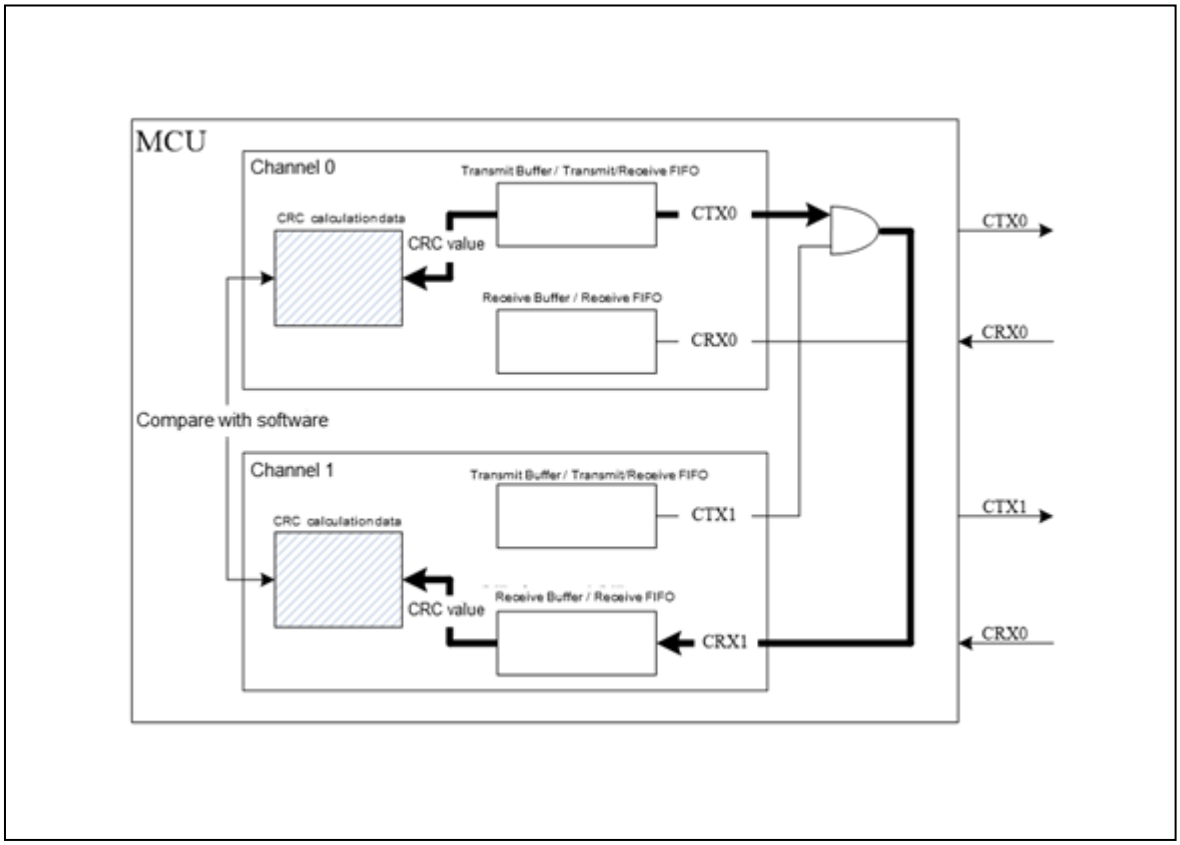
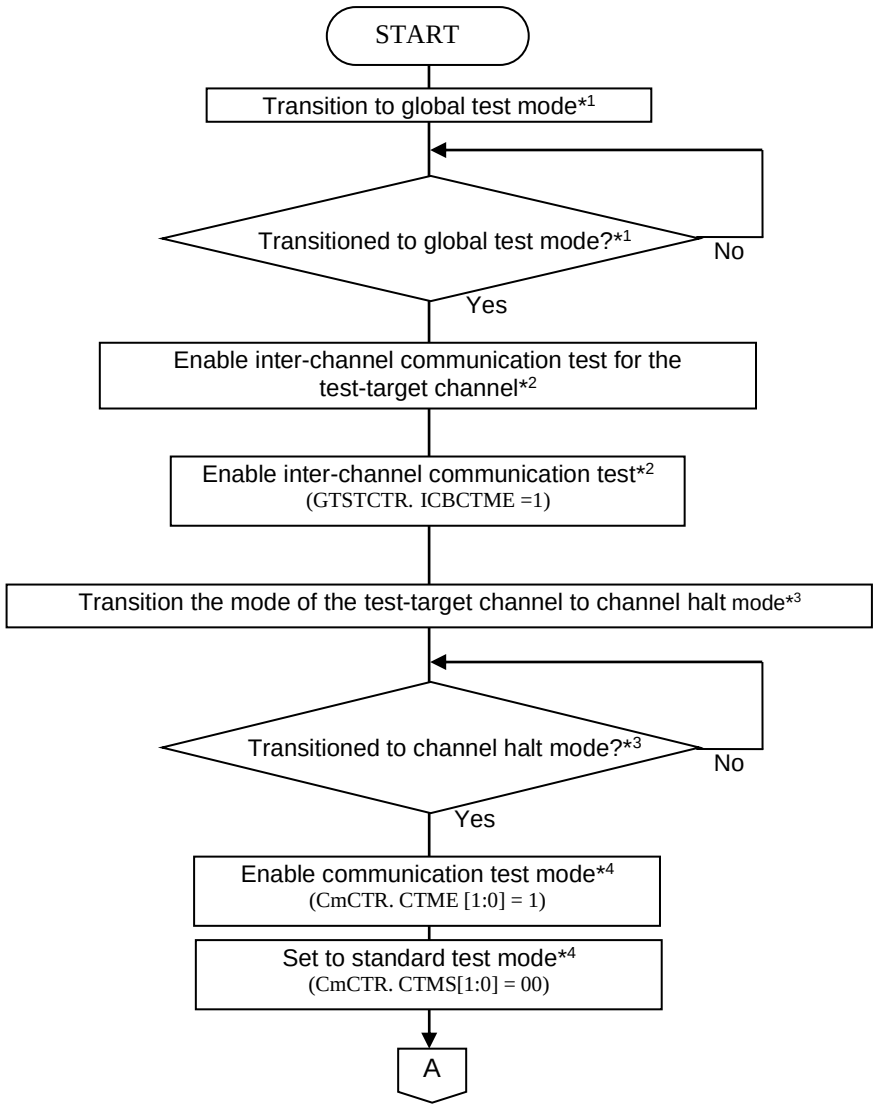


Figure 2-1 Image of CRC Test (Between Channel 0 and 1)

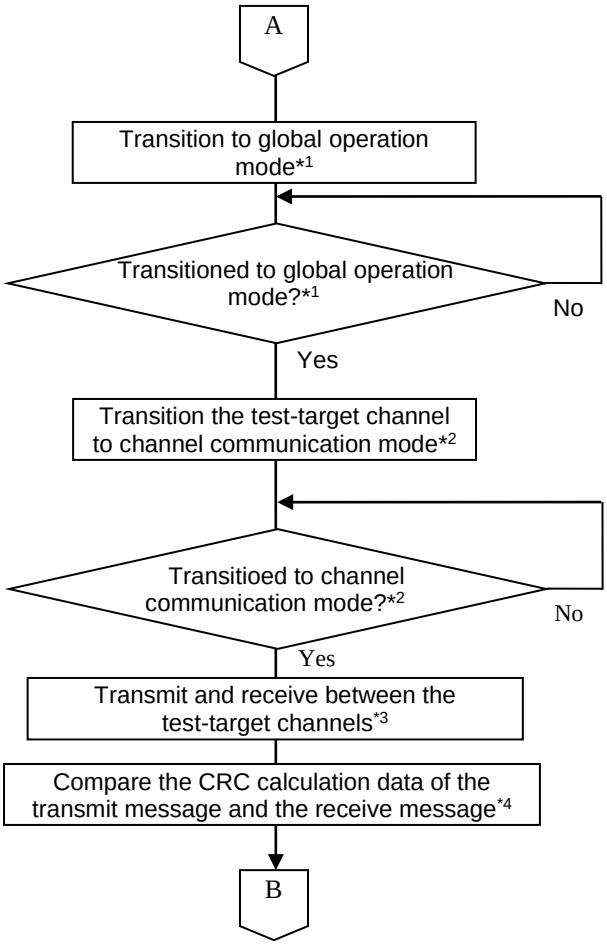
2.1.1 Setting Procedure of Standard Test Mode

Figure 2-2 to Figure 2-4 show the setting procedure of standard test mode.



[Note] 1. If you change the global mode (the GSLPR bit of the GCTR register, GMDC [1: 0] bit), check that the mode is switched in the GSTS register. Do not change the mode selection bit until the mode is switched.
2. Rewrite the CmICBCE bit and ICBCTME bit in the global test mode.
3. If you change the channel mode (the CSLPR bit of the CmCTR register, CHMDC [1: 0] bit), check that the mode is switched in the CmSTS register. Do not change the mode selection bit until the mode is switched.
4. Rewrite the CTMS [1: 0] bit and CTME bit of the CmCTR register in channel halt mode.

Figure 2-2 Standard Test Mode Setting Procedure 1



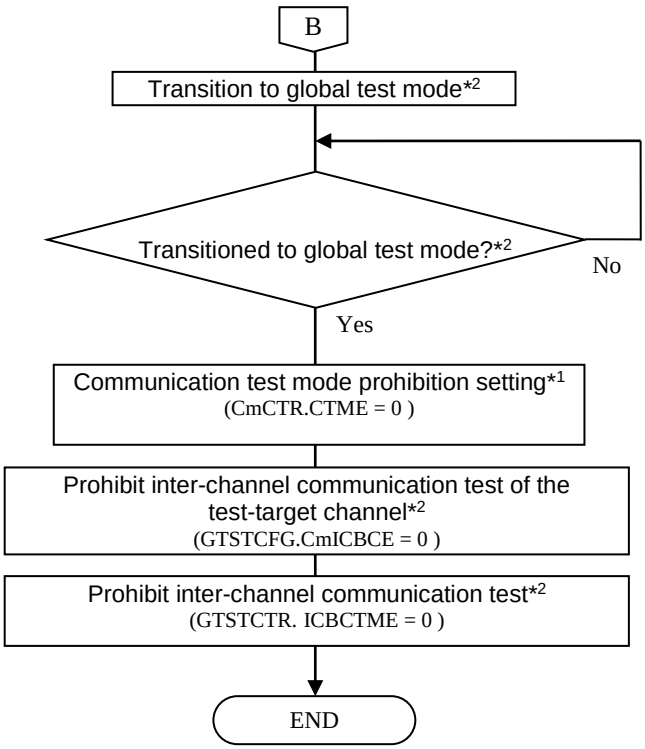
[Note] 1. If you change the global mode (the GSLPR bit of the GCTR register, GMDC [1: 0] bit), check that the mode is switched in the GSTS register. Do not change the mode selection bit until the mode is switched.

2. If you change the channel mode (the CSLPR bit of the CmCTR register, CHMDC [1: 0] bit), check that the mode is switched in the CmSTS register. Do not change the mode selection bit until the mode is switched.

3. Set the transmit/receive settings for the channel to be tested.

4. When the communication test mode is enabled (CmCTR.CTME = 1), the CRC calculation data can be checked with the CRCREG[14:0] bit of the CmERFL register for a classical CAN frame, or with the CRCREG[20:0] bit of the FDCRC register for a CAN FD frame. When the communication test mode is disabled (CmCTR.CTME = 0), the CRCREG [14: 0] bit of the CmERFL register and the CRCREG [20: 0] bit of the FDCRC register is always "0".

Figure 2-3 Standard Test Mode Setting Procedure 2



[Note] 1. Rewrite the CTME bit in the CmCTR register in channel halt mode.
2. If you change the global mode (GSLPR bit of GCTR register, GMDC [1: 0] bit), check that the mode is switched in the GSTS register. Do not change the mode selection bit until the mode is switched.
3. Rewrite the CmICBCE bit and ICBCTME bit in global test mode.

Figure 2-4 Standard Test Mode Setting Procedure 3

2.2 Listen-only Mode

In listen-only mode, only the receptive bit is transmitted on the CAN bus, not the ACK bit, the overload flag, or the active error flag. Both data frames and remote frames can be received. Therefore, listen-only mode can be used for bus monitoring and communication speed detection.

Do not transmit in listen-only mode (do not request transmission to the transmit/receive FIFO buffer, the transmit buffer, or the transmit queue).

Figure 2-5 shows the connection when listen-only mode is selected.

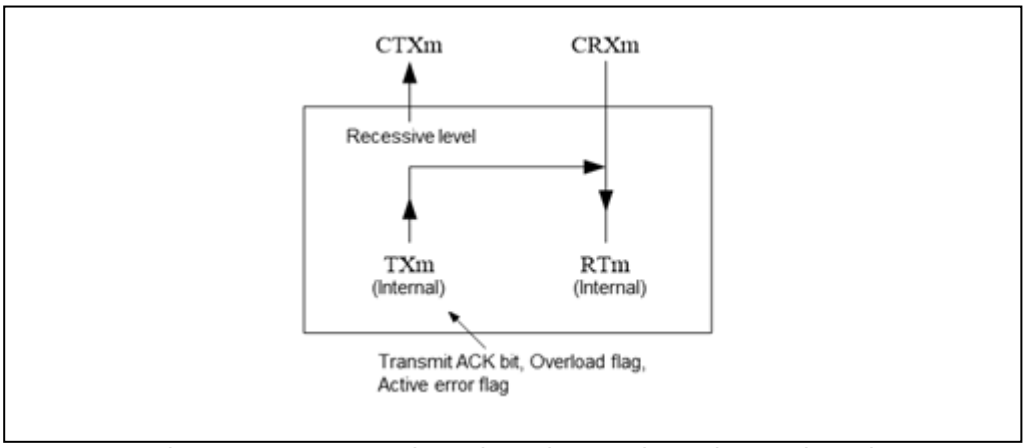
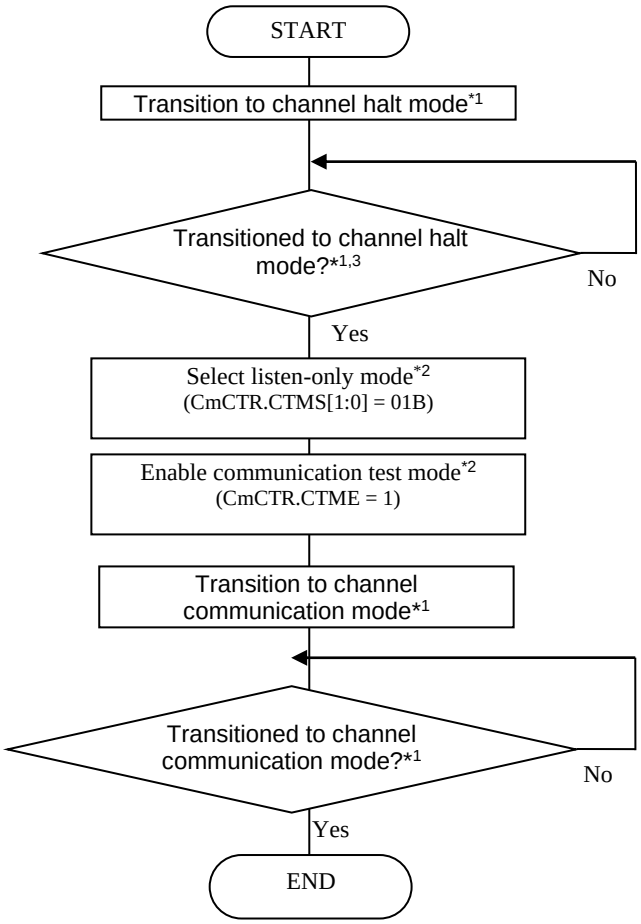


Figure 2-5 Connection When Listen-only Mode Is Selected

2.2.1 Listening-only Mode Setting Procedure

Figure 2-6 shows the procedure for setting the listen-only mode.



[Note] 1. If you change the channel mode (the CSLPR bit in the CmCTR register, CHMDC [1: 0] bit), check that the mode is switched in the CmSTS register. Do not change the mode selection bit until the mode is switched.
2. Rewrite the CTMS [1: 0] bit and CTME bit of the CmCTR register in channel halt mode.
3. If necessary, set the reception settings for the channel used in listen-only mode.

Figure 2-6 Listening-only Mode Setting Procedure

2.3 Self-test Mode (Loopback Mode)

In self-test mode, the message sent by the own node is compared with the receive rule, and the filtered message is stored in the buffer.

Messages sent by other CAN nodes will be compared only with the receive rule set to receive messages sent by other CAN nodes (GAFLIDj.GAFLLB = 0). When the mirror function and self-test mode are enabled at the same time, the self-test mode setting takes priority.

Table 2-1 Comparison of Receive Rules in Self-test Mode

Receive rule target message	Message transmit node	Comparison with receive rule
GAFLIDj.GAFLLB = 0	Other node	Yes
	Own node	Yes
GAFLIDj.GAFLLB = 1	Other node	No
	Own node	Yes

2.3.1 Self-test Mode 0 (External Loopback Mode)

Self-test mode 0 performs a loopback test of the channel, including the CAN transceiver.

In self-test mode 0, the message sent by the local node is received via the CAN transceiver. Received messages are stored in the buffer according to the receive rule. It also generates the ACK bit to receive the message sent by own node.

Figure 2-7 shows the connection when self-test mode 0 is selected.

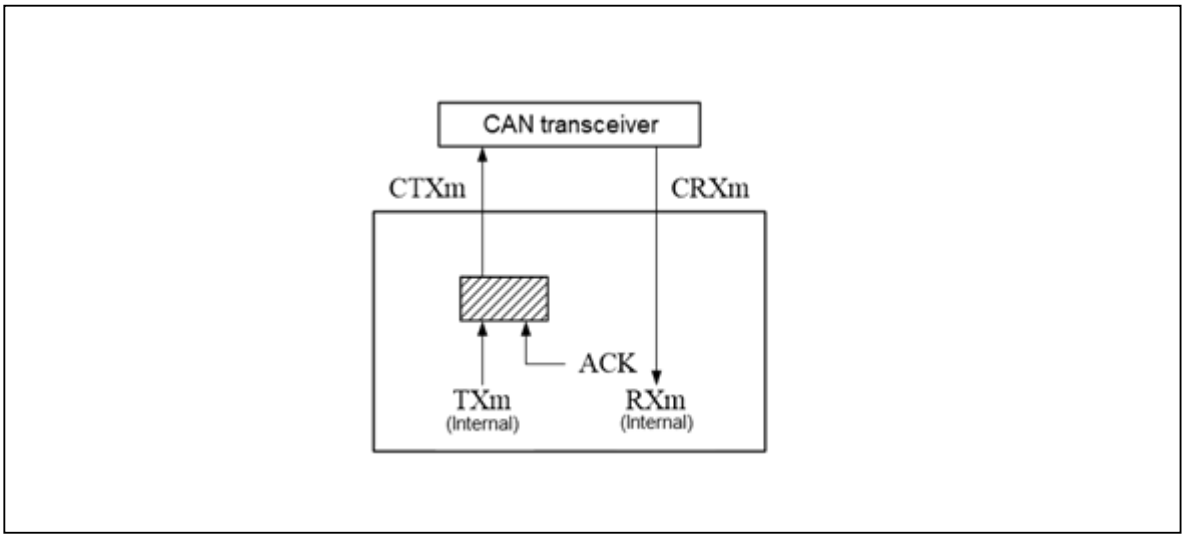


Figure 2-7 Connection When Self-test Mode 0 Is Selected

2.3.2 Self-test Mode 1 (Internal Loopback Mode)

Self-test mode 1 performs a loopback test of the channel inside the MCU.

In self-test mode 1, the message sent by the own node is received via the internal pin of the MCU. Received messages are stored in the buffer according to the receive rules. It also generates the ACK bit to receive the message sent by own node.

In this test, only the internal feedback from TXm to RXm inside the channel is performed. The external CTXm pin and external CRXm pin are disconnected from the internal pins, and the external CTXm pin outputs the recessive bit. (The CAN transceiver is not used.)

Figure 2-8 shows the connection when self-test mode 1 is selected.

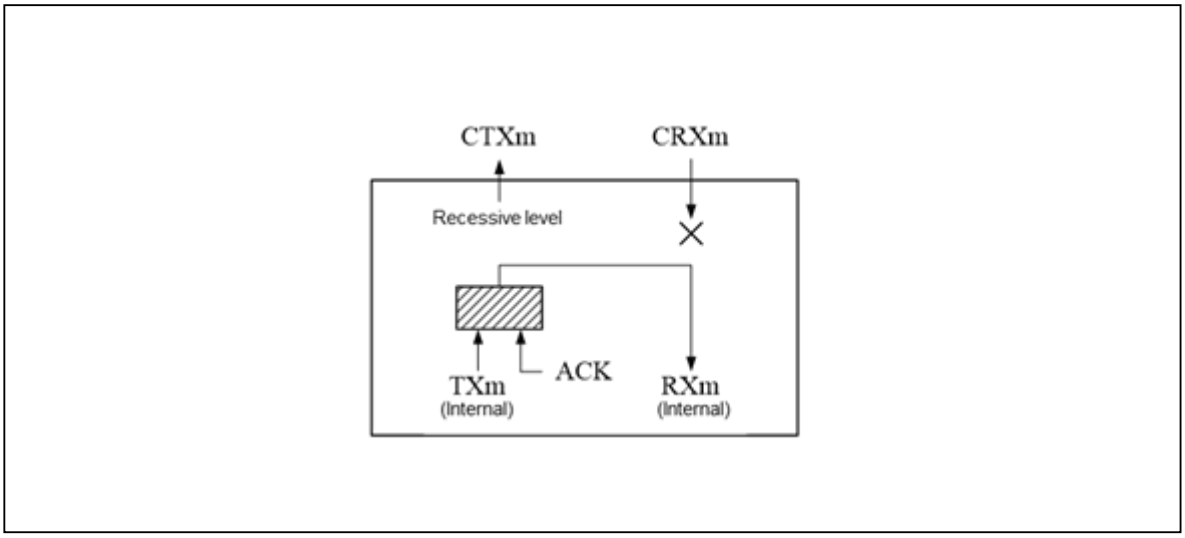
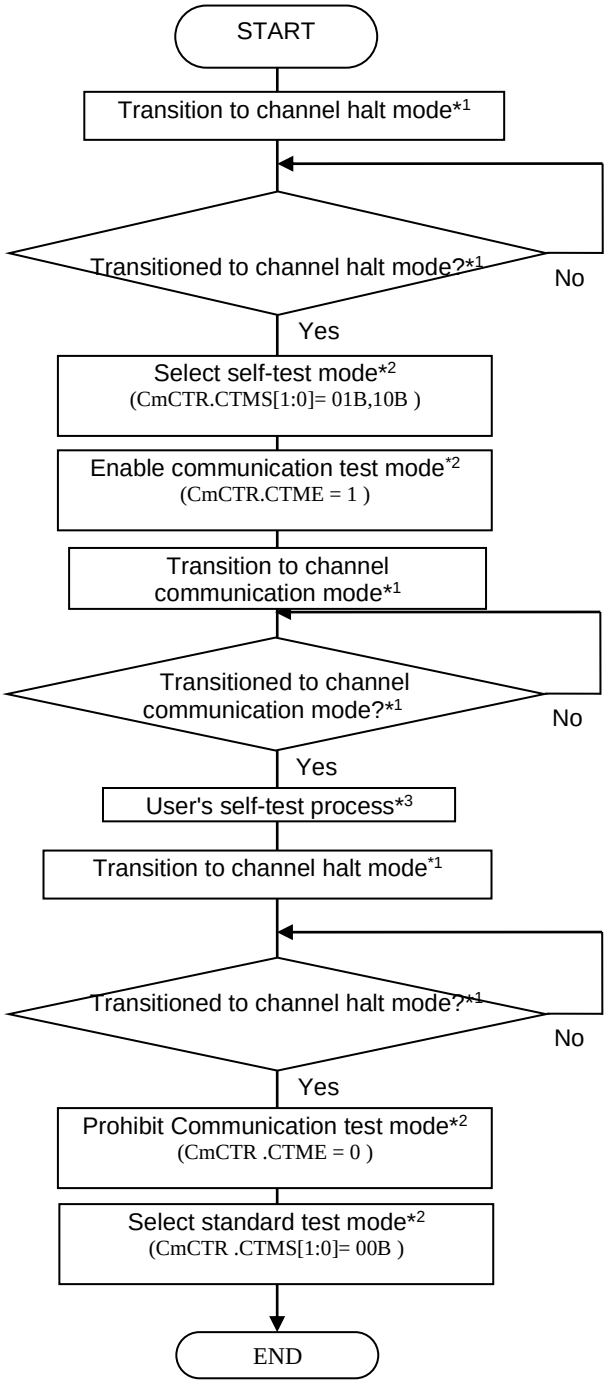


Figure 2-8 Connection When Self-test Mode 1 Is Selected

2.3.3 Self-test Mode Setting Procedure

Figure 2-9 shows the procedure for setting the self-test mode.



[Note] 1. If you change the channel mode (the CSLPR bit in the CmCTR register, CHMDC [1: 0] bit), check that the mode is switched in the CmSTS register.Do not change the mode selection bit until the mode is switched.
2. Rewrite the CTMS [1: 0] bit and CTME bit of the CmCTR register in channel halt mode.
3. Set the transmit/receive settings for the channel to be tested.

Figure 2-9 Self-test Mode Setting Procedure

2.4 Restricted Operation Mode (Only in CAN FD Mode)

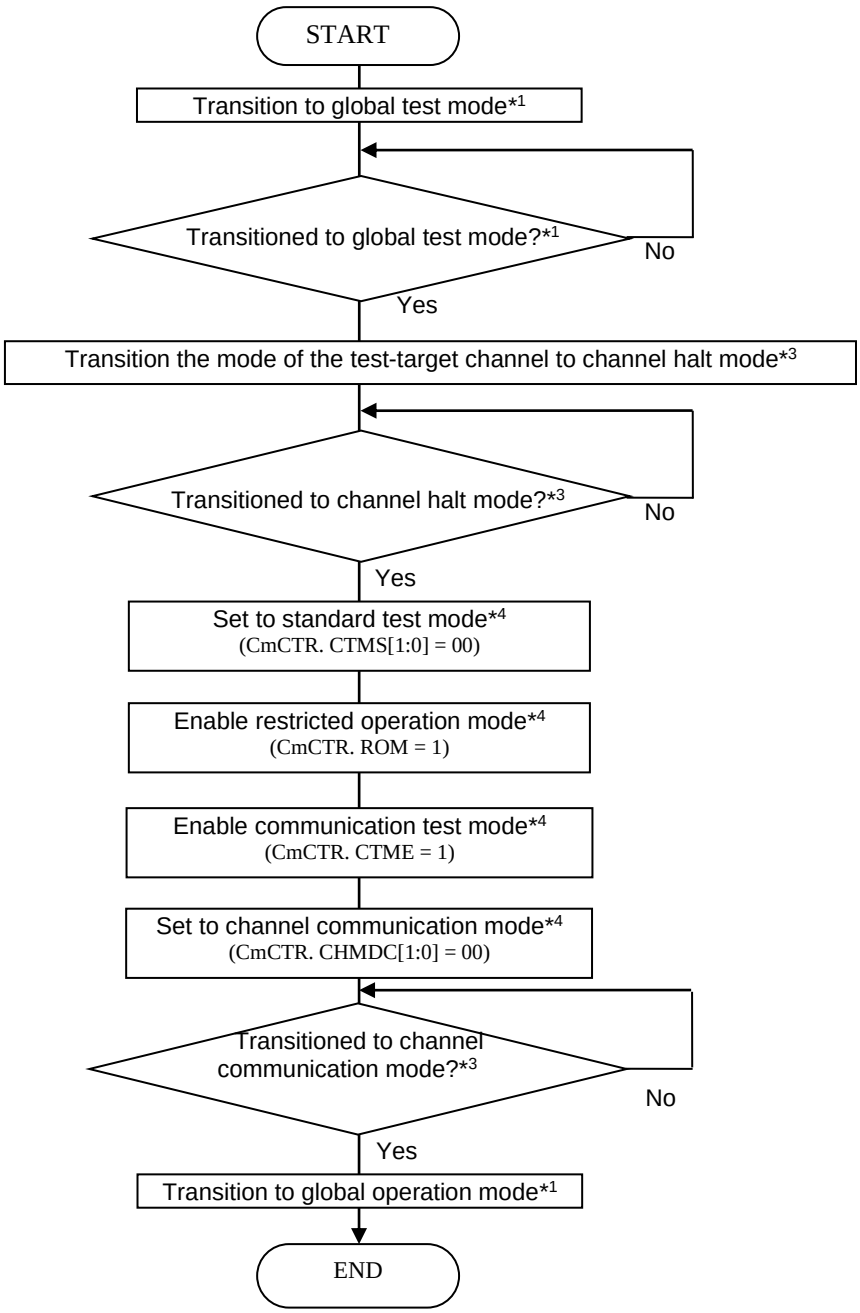
In restricted operation mode, it generates an ACK bit when it receives valid data frames and remote frames, but it does not send these frames when it detects an error frame or overload frame transmit condition. When a condition is detected, it waits for the bus idle state to resynchronize to CAN communication. The receive error counter (REC) and transmit error counter (TEC) do not change when an error occurs.

Use the restricted operation mode only in the standard test mode (the CTMS [1: 0] bit of the CmCTR register is "00B").

Any transmission request is possible, and there are no restrictions.

2.4.1 Restricted Operation Mode Setting Procedure

Figure 2-10 shows the setting procedure of the restricted operation mode.



【Note】 1. If you change the global mode (the GSLPR bit of the GCTR register, GMDC [1: 0] bit), check that the mode is switched in the GSTS register. Do not change the mode selection bit until the mode is switched.

2. Rewrite the CmICBCE bit and ICBCTME bit in global test mode.
3. If you change the channel mode (the CSLPR bit of the CmCTR register, CHMDC [1: 0] bit), check that the mode is switched in the CmSTS register. Do not change the mode selection bit until the mode is switched.
4. Rewrite the CTMS [1: 0] bit and CTME bit of the CmCTR register in channel halt mode.

Figure 2-10 Setting Procedure of Restricted Operation Mode

2.5 Inter-channel Communication Test

The inter-channel communication test function allows CAN channels to be internally connected for the communication test.

In this test, only the internal feedback from the CTXm pin inside the channel to the CRXm pin is performed. The external CRXm pin and external CTXm pin are disconnected from the internal pins, and the external CTXm pin outputs the recessive bit. (The CAN transceiver is not used.)

After setting transmission/reception for each channel, transmit/receive in channel communication mode. For the setting procedure, refer to "2.1.1 Setting Procedure of Standard Test Mode".

By using the inter-channel communication function and the standard test mode, it is possible to test the CRC calculation circuit. For details on the CRC test, refer to "2.1 Standard Test Mode (CRC Test)".

Figure 2-11 shows the inter-channel communication test connection diagram.

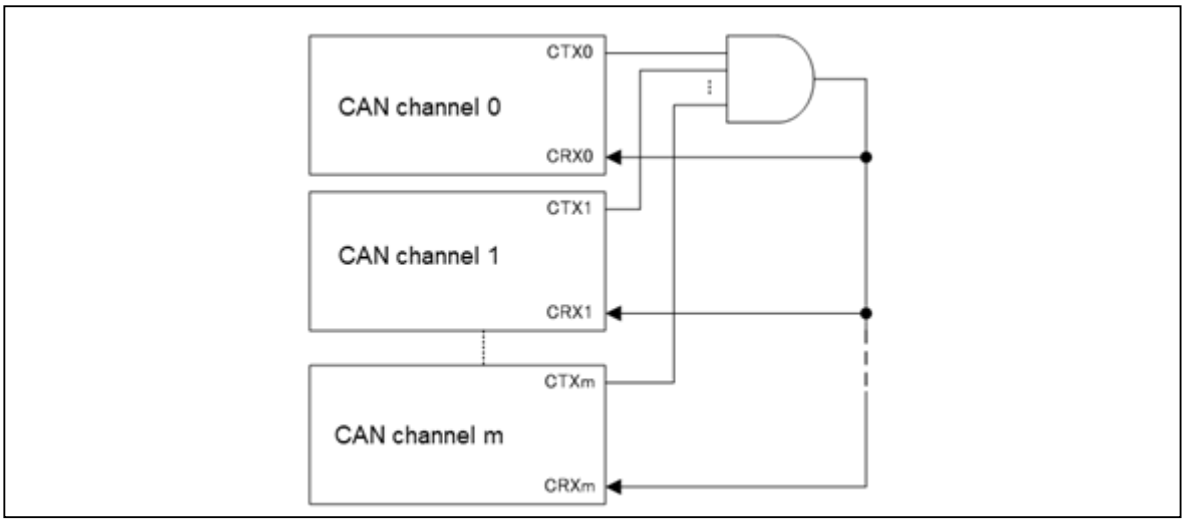


Figure 2-11 Inter-channel Communication Test Connection Diagram

3. RAM Test Function

3.1 RAM Read/write Test

When RAM test is enabled (GTSTCTR.RTME = 1), RAM read/write test can be performed for the entire RAM for CAN.

When the RAM test function is used, the RAM is divided into pages of 256 bytes each, and the page selection is set by the RTMPS [6:0] bit of the GTSTCFG register. The RAM in a page can be read or written by the RPGACCr register. The number of pages depends on the number of TXMB and AFL rules set in the PSI bit of the RSCFDnCFDGIPV register.

Ex. PSI bit value 0x124

- [29:27] Number of channel：8
- [26:24] Number of TXMB：32/ch
- [23:21] Number of AFL rule：128/ch
- [20:17] Number of Pool Buffer：64/ch

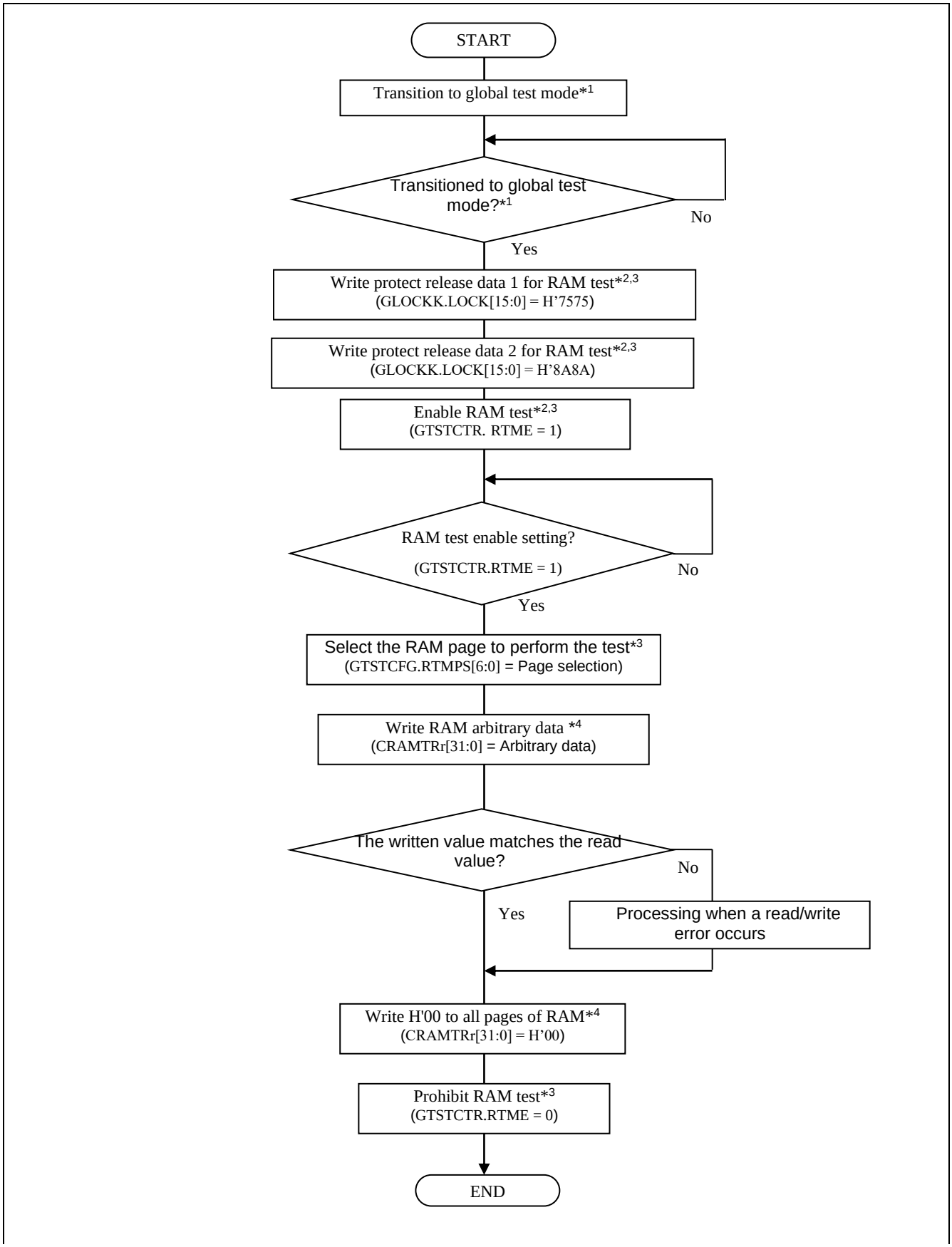
In the above, the RAM capacity is 16384 bytes for AFL: 64Pages and 61696 bytes for TXMB + THL + OTB + Message Buffer: 241Pages.

You can check that the RAM is normal by comparing the written value and the read value for the entire CAN RAM.

After performing the RAM read / write test, write "H'00" to the CAN RAM to finish.

3.2 RAM Test Setting Procedure

Procedure shows the procedure for setting the RAM test (RAM read/write test).



【Note】 1. If you change the global mode (the GSLPR bit of the GCTR register, GMDC [1: 0] bit), check that the mode is switched in the GSTS register. Do not change the mode selection bit until the mode is switched.
2. Be sure to execute the three instructions of writing the unprotect data 1 and 2 for the test function to the GLOCKK.LOCK [15: 0] bit and permitting the RAM test consecutively.
3. Rewrite the LOCK [15: 0] bit of the GLOCKK register, the RTME bit of the GTSTCTR register, and the RTMPS bit of the GTSTCFG register in global test mode.
4. Rewrite the CRAMTRr register in the global test mode with RAM test enabled.

Figure 3-1 RAM Test Setting Procedure

4. Bus Load Measurement Function

Bus load counter can mesrue the idle time of the CAN bus to use the clkc clock or the clk_xincan clock. It makes possible to meseure the CAN bus load by the idle time.

Figure 4-1 shows the overview of the bus load measurement function.

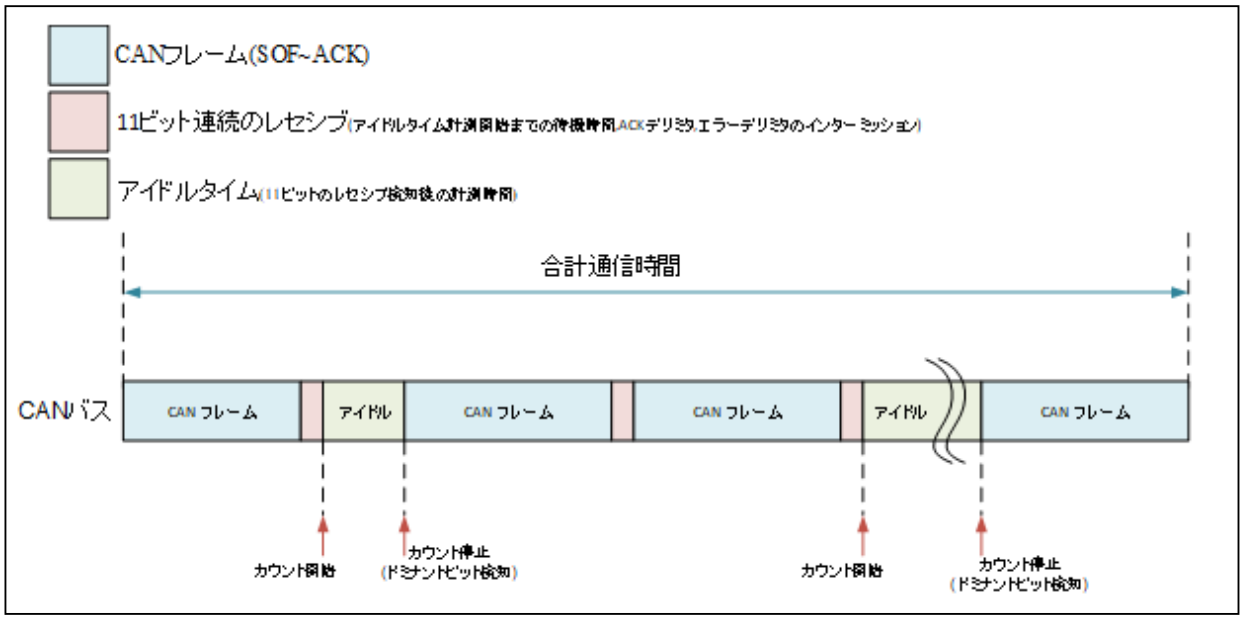


Figure 4-1 Communication Test Connection Diagram between Channels

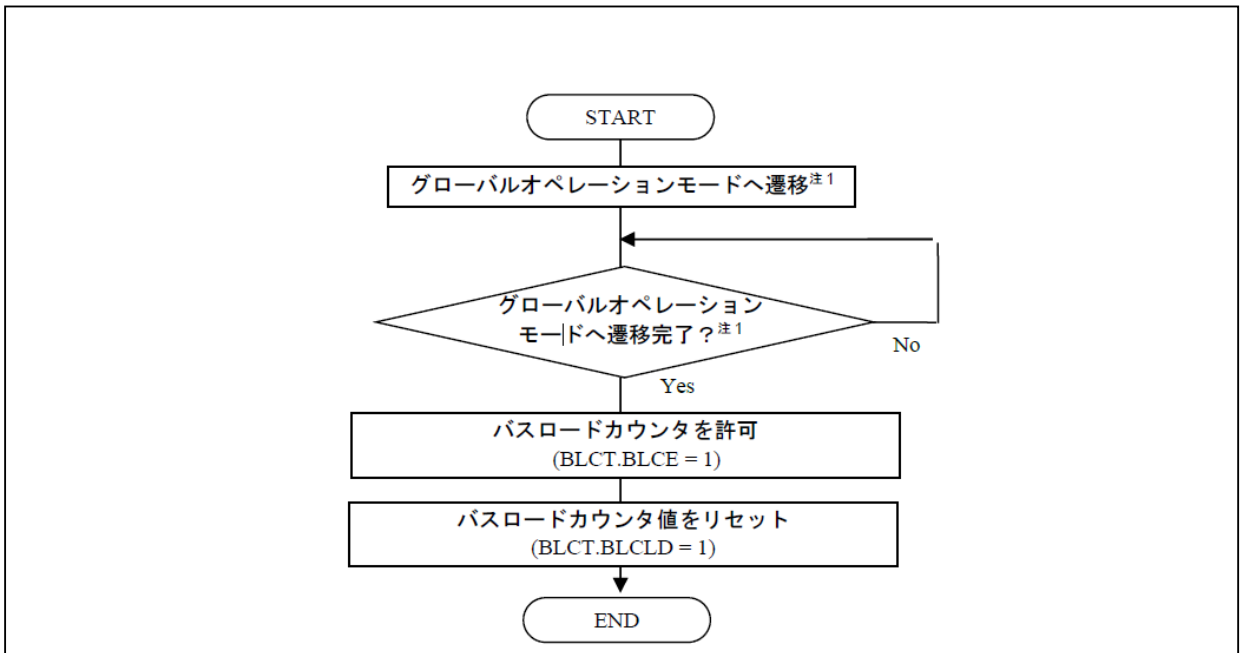
The bus load counter stars counting when the nominal bit of the recessive level is measured continuously 11bits on the CAN bus.

The bus load counter keeps counting until it measures the dominant on the CAN bus.

When a dominant bit is detected on the CAN bus, counting is stopped, and when the recessive level nominal bit is measured again for 11 consecutive bits, counting is resumed.

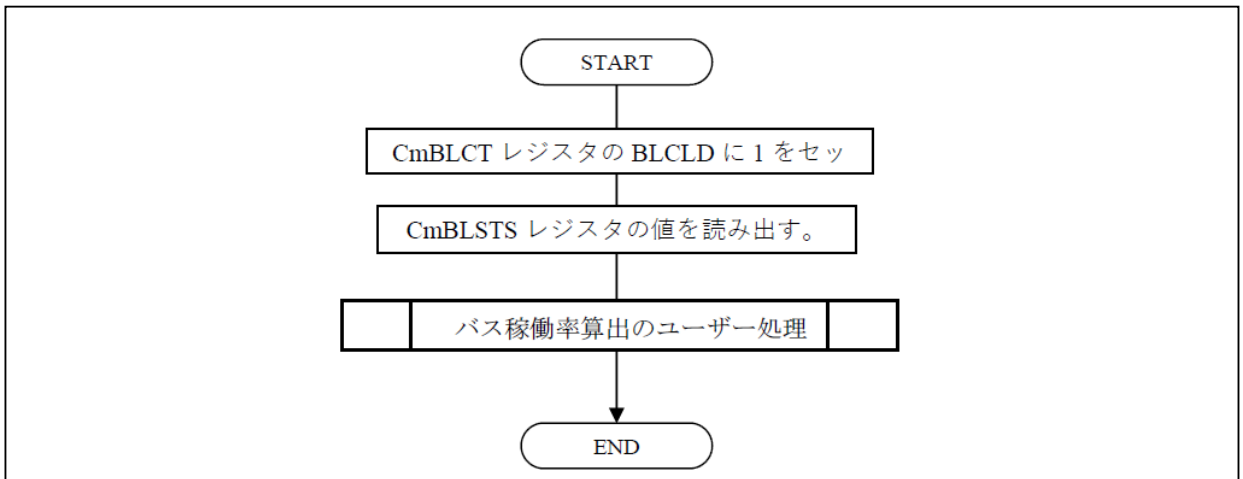
4.1 Measurement Procedure of Bus Load Measurement Function

Figure 4-2 shows setting procedure of bus load counter. Figure 4-3 shows the read procedure of the bus load counter.



【注】 1. グローバルモード（GCTR レジスタの GSLPR ビット、GMDC[1:0]ビット）を変更した場合は GSTS レジスタでモードが切り替わることを確認して下さい。モードが切り替わるまでモード選択ビットは変更しないでください。

Figure 4-2 Bus Load Counter Setting Procedure



【注】 1. CmBLCT.BLCLD に 1 がセットされると同時にカウンタがクリアされ、CFDCmBLSTS レジスタにカウンタ値がロードされます。

Figure 4-3 Bus Load Counter Read Procedure

4.2 Bus Occupancy Calculation Method

The CAN bus utilization rate can be calculated using the following formula. Total communication time – Total idle time total communication time = Total bus operating time total communication time = Bus operating rate

Total idle time:BLC value of BLSTS register × Number of clck cycles
Total communication time: Interval time to set the BLCLD bit of the BLCT register
Calcuration Example)
Bit rate：1Mbps
clkc Clock：40MHz(25ns)
CFDCnBLCT.BLCLD setting：1ms period
CFDCnBLSTS register value：4E20H(20000D)

(Total communication time −Total idle time) / Total communication time= (1000000ns − 20000 × 25ns) 1000000ns = 50%

5. Precautions for Processing Flow

5.1 About Functions

In this application note, there is a part that is functionalized even in the processing of single line, but this is only described as a function to clarify the processing for each function. When you actual create a program, you don't necessarily have to make it functional.

5.2 Settings for Each Channel, FIFO, and Buffer

In this application note, even if processing is required for each channel, FIFO, or buffer, only one processing is described. When actual creating a program, perform multiple processes as necessary.

5.3 Infinite Loop

To simplify the notation, there are some infinite loops in the processing flow. When actual creating a program, give each loop a time limit so that it can be exited during overtime. Figure 5-1 shows an example of processing when the loop time limit is set. Table 5-1 shows the transition time in global mode, and Table 5-2 shows the maximum transition time in channel mode.

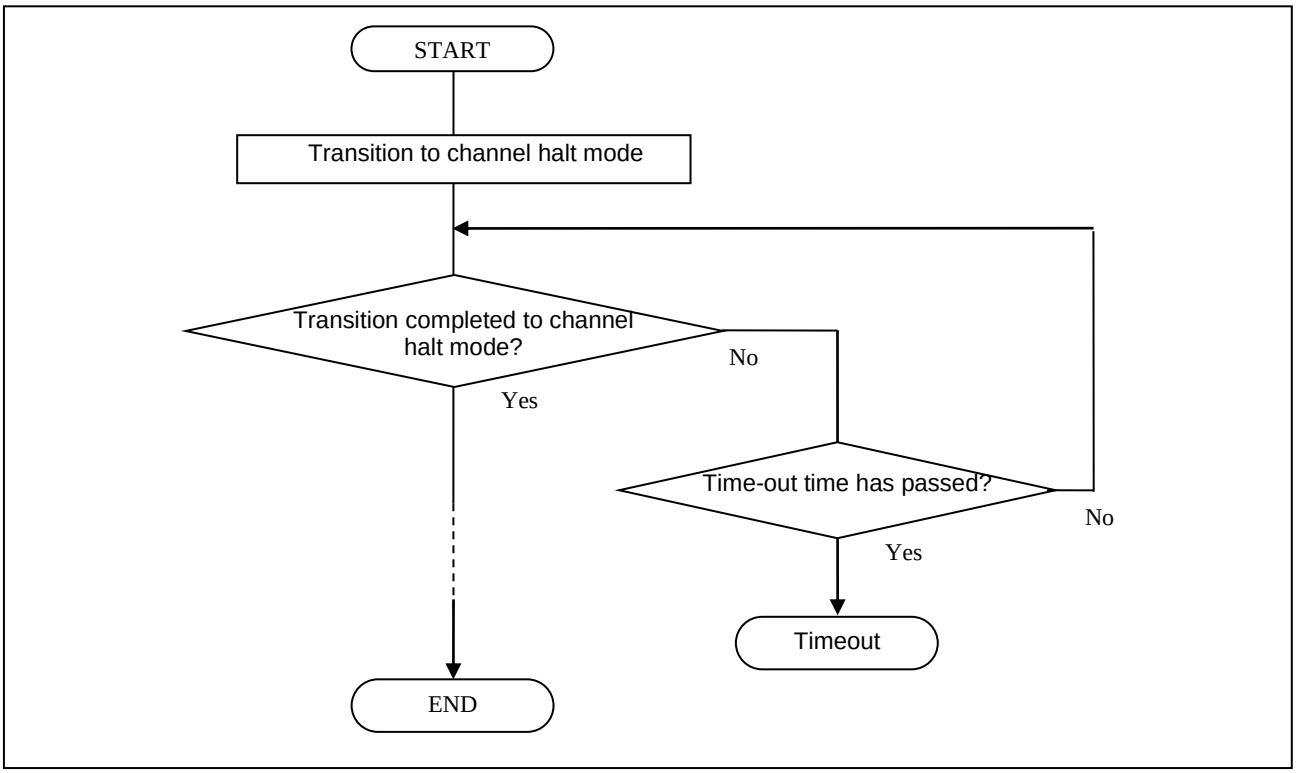


Figure 5-1 Example of Processing with Loop Time Limit

Table 5-1 Transition Time in Global Mode

Mode before transition	Mode after transition	Maximum transition time
Global stop	Global reset	3 clocks of pclk
Global reset	Global stop	3 clocks of pclk
Global reset	Global test	10 clocks of pclk
Global reset	Global operation	10 clocks of pclk
Global test	Global reset	2 CAN bit time*1、*2
Global test	Global operation	3 clocks of pclk
Global operation	Global reset	2 CAN bit time*1、*2
Global operation	Global test	2 CAN frames*1

*1. It is the CAN bit time and CAN frame time of the slowest communication speed among the channels used.

*2. In CAN FD mode, the normal bit rate is CAN bit time.

Table 5-2 Transition Time in Channel Mode

Mode before transition	Mode after transition	Maximum transition time
Channel stop	Channel reset	3 clocks of pclk
Channel reset	Channel stop	3 clocks of pclk
Channel reset	Channel halt	3CANm bit time*1
Channel reset	Channel communication	4CANm bit time*1
Channel halt	Channel reset	2CANm bit time*1
Channel halt	Channel communication	4CANm bit time*1
Channel communication	Channel reset	2CANm bit time*1
Channel communication	Channel halt	2 CANm frames

*1. In CAN FD mode, the normal bit rate is CANm bit time.

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Nov. 5, 2024	-	Newly issued.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact information

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