RH850/U2C

SSIF Application Note

Introduction

The U2C device is equipped with Serial Sound Interface, referred to as SSIF in this document. The Serial Sound Interface (SSIF-2) transmits and receives audio data to and from various devices, compatible with I2S, monaural, and TDM format. This document with the accompanying demo code presents the usage and configuration of SSIF for I2S.

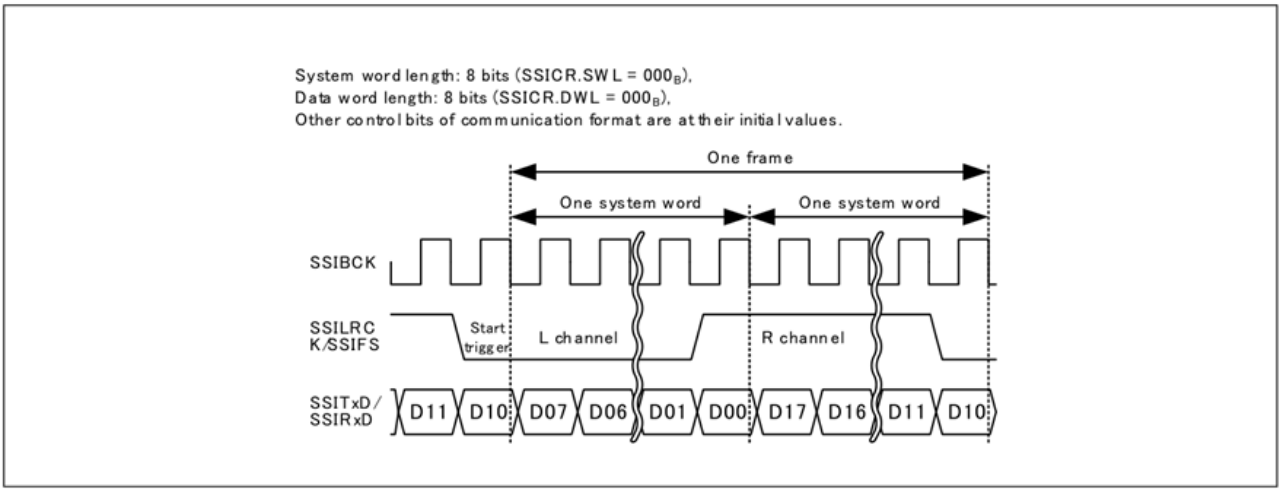

Fig 1. I2S Format (Without Padding: System Word Length = Data Word Length)

Used components

Target Device:	RH850/U2C4 (R7F702606AFABB)
Piggyback Board:	RH850/U2C Y-RH850-U2C-292PIN-PB-T1-V1
Toolchain:	Multi v8.1.6 with GHS 202514

Table 1. Abbreviations

Name	Description
SSIF	Serial Sound Interface
TAUJ	Timer Array Unit J
SSIFACK	Common Audio Clock Input
AUCKE	Audio Clock Enable in Master-mode Communication
SSITXD	Serial Transmit Data Output
DTS	Data Transfer Service
TDE	Transmit Data Empty
FDTR	Transmit FIFO Data Register

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1. System

SSIF needs an external clock common for SSIF channels to operate. TAUJ pulse is provided to SSIFACK. For this setup to work, it is mandatory to connect the TAUJ output (P17_6) to the SSIFACK (P20_0). The demo is using a DAC with 3 lines for I2S, TXD, BCK and LRCK.

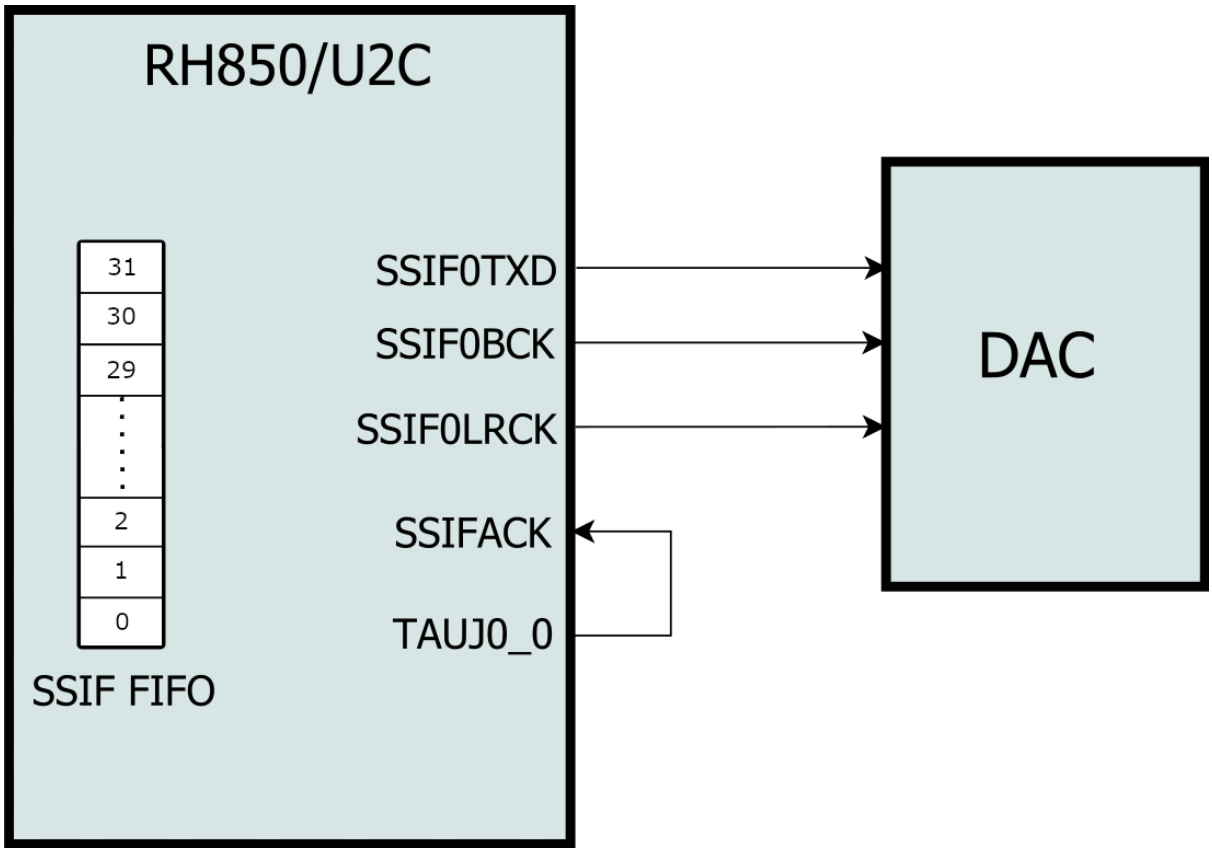


Fig. 2 System setup

2. Operation

A sequence diagram is present in Fig. 3. The application cyclically outputs a sine wave.

DTS is used to copy a constant (32 samples of 16bit each) sine to both channels of the SSIF FIFO.

Initially enabling of the input clock (AUCKE) and transmission (TEN) triggers a DTS transfer request. The DTS will fill the SSIF FIFO with a single period constant sine wave data. SSIF will start outputting data from the FIFO and will trigger a new DTS write request when the FIFO is empty.

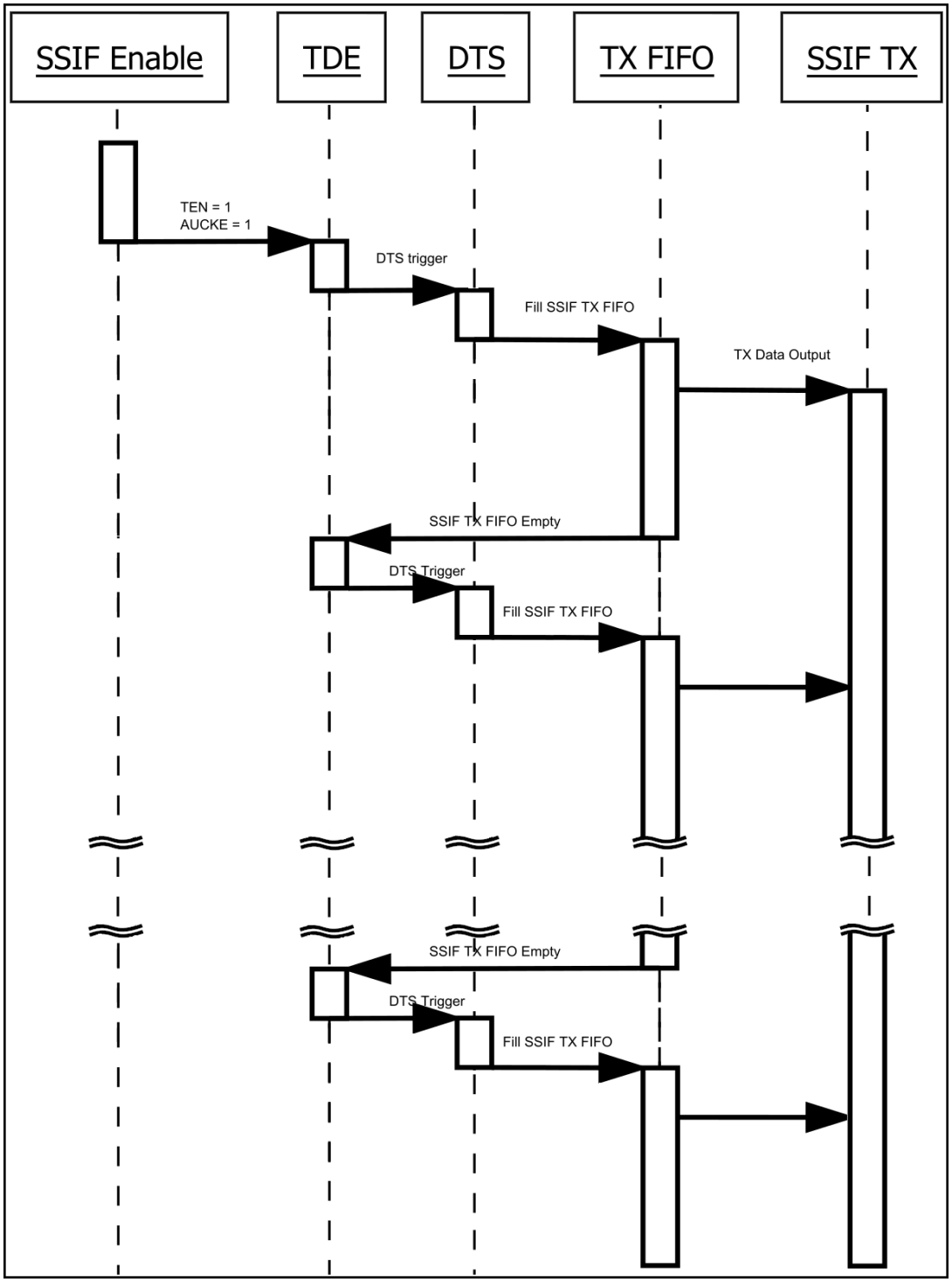


Fig. 3 Sequence diagram

3. Code organization

The code is structured in a few logical components. All components are in src_mca directory of the main project dir. SmartConfigurator was used for configuration and code generation of the clock, pins, TAUJ and DTS.

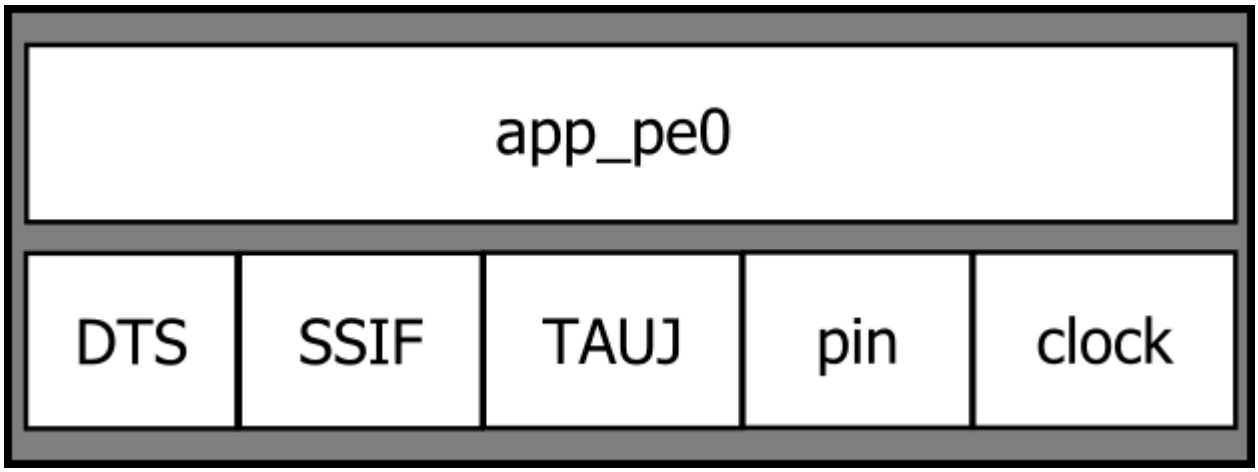


Fig. 4 Software application modules

app_pe0.c is where the main function is. The clock, interrupts, DTS, TAUJ, pin for the demo application are configured from this component.

DTS.c holds the DTS specific configuration and the template sine data (const uint16_t src[SSI_FIFO_BUFFER_SIZE]) in DTS.c. For more information check DTS Configuration.

SSIF.c is the sound interface configuration. For more information check SSIF Configuration.

TAUJ.c is the timer configuration. The timer is used as an input to SSIF for master mode communication. For more information check TAUJ Configuration.

pin.c contains the R_Pins_Create(void), that configures the pins used in the demo. For more information Port Configuration.

4. Port Configuration

Table 2. List of Port Pins Alternative Functions

Name	Function	Direction	Port Pin	U2C Board Pin
SSIF0BCK	Data Clock	Output	P21_0	CN13_73
SSIF0LRCK	Left Right Clock	Output	P21_1	CN13_74
SSIF0TXD	Transmit Data	Output	P21_3	CN13_78
SSIFACK	Audio Clock	Input	P20_0	CN13_56
TAUJ0O0	Audio Clock	Output	P17_6	CN13_35

5. TAUJ Configuration

TAUJ clock resolution is 80MHz and the target sampling frequency is 96kHz. TAUJ is configured to work in interval timer mode. The timer generates 2x32 pulses in one sampling frequency cycle (1/96kHz).

According to the UM

$$TAUJnTTOUTm\ square\ wave\ cycle = count\ clock\ cycle * (TAUJCDR + 1) * 2$$

$$TAUJCDR = INT\left({}^{TAUJ\ frequency}\Big/_{(bits\ per\ sampling\ period * 2 * sampling\ period\ frequency)}\right) - 1$$

$$TAUJCDR = INT\left({}^{80000000Hz}\Big/_{(32 * 2 * 96000Hz)}\right) - 1 = 12$$

TAUJCDR cannot accept a decimal, and the value is rounded to 12, resulting in the following target frequency:

$$CLK\ actual = (12 + 1) * \left(\frac{1}{80000000Hz}\right) = \sim 6{,}153{,}846\ Hz$$

$$Sampling\ Rate\ actual = {}^{6{,}153{,}846}\Big/_{32 * 2} = 96153\ Hz$$

The clock deviation from 96000 is close to 153Hz.

Table 3. TAUJ Control Registers

Register	Value	Description
SYSCTRLMSR_TAUJ_ISO_0	0	Module Standby Register Clock supply for TAUJ_ISO_0
TAUJ0.CMOR0	0	TAUJnCKS: SELECTION_CK0 TAUJnCCS: COUNT_CLOCK_PCLK TAUJnMAS: INDEPENDENT_CHANNEL TAUJnSTS: START_TRIGGER_SOFTWARE TAUJnCOS: OVERFLOW_AUTO_CLEAR TAUJnMD: INTERVAL_TIMER_MODE TAUJnMD0: START_INT_NOT_GENERATED
TAUJ0.CMUR0	0	TAUJnTIS: INPUT_EDGE_UNUSED
TAUJ0.CDR0	12	Data Register for Capture/Compare Values

6. SSIF Configuration

SSIF is configured in master mode to output 16 bits per I2S channel with no padding at ~96kHz. The interface supports few interrupts for better handling and managing of the FIFO and possible errors. Since the demo uses a fixed data size only one trigger for DTS copy is used. The SSIF Transmit FIFO (SSIFTDR) is configured to trigger DTS write cycle when the transmit FIFO has 31 (SSIF0TDES = 0x1f) stages or more free space.

The SSIF Transmit FIFO can be configured to output Transmit Data Empty (TDE) flag on specific FIFO data count, by writing the corresponding value to SSIFnSSCR.TDES register. The output frequency for this demo will always be equal to $\frac{sample\ frequency}{16}$.

Table 4. SSIF Control Registers

Register	Value	Description
SYSCTRLMSR_SSIF_0	0	Module Standby Register. Enable clock for SSIF
SSIF0OMOD	0	Communication Format I2S
SSIF0FRM	0	Frame Word Number: 0 for I2S
SSIF0DWL	1	Data Word Length: 16 bits
SSIF0SWL	1	System Word Length: 16 bits
SSIF0MST	1	Master Enable
SSIF0BCKASTP	0	Enable Output of BCK
SSIF0LRCONT	1	Enable LRCK Continuation
SSIF0TDES	0x1F	TDE Setting Condition Select
SSIF0TIE	1	Transmit Data Empty Interrupt Output Enable
SSIF0AUCKE	1	AUDIO_MCK Enable in Master-mode Communication

7. DTS Configuration

DTS writes the complete SSIF Transmit FIFO buffer on one trigger. The FIFO is accessible through a single register SSIFTDRL, protected by the Peripheral bus guard. Writing is enabled by setting PBG41UM to 1 in r_Config_DTS030_init. DTS is configured to transfer 16 bits 32 consecutive times to a fixed address (SSIFTDRL), incrementing the source address, on a single trigger. The access size of SSIFTDRL differs for different data word sizes. This demo uses 16 bits and writes to the lower part SSIF0SSIFTDRL.

DTS channel 30 is used, since according to the DTS Transfer request table, channel 30 is triggered by INTSSIF0TX. The trigger configuration (DMATRGSELDTSSEL3) is inside R_Config_DTS030_Create function of DTS.c file.

Table 5. DTS Control Registers

Register	Value	Description
DMATRGSELDTSSEL3	0	DTS Group Selection
PBG41UM	1	Peripheral Bus Guard for SSIF
DTSCNT.DTSA030	0x1A0BC	Sine Lookup Data Source Address
DTSCNT.DTDA030	&SSIF0SSIFTDRL	SSIF Transmit FIFO Destination Address
DTSCNT.DTTC030	32	Transfer Count
DTSCNT.DTTCT030	0x4105	TRM: BLOCK_TRANSFER_1 DS: TRANSFER_DATA_16BITS SACM: SOURCE_ADDRESS_INCREMENT DACM: DESTINATION_ADDRESS_FIXED RLD1M: RELOAD1_DISABLE RLD2M: RELOAD2_DISABLE TCE: TRANSFER_COMPLETION_INTERRUPT_ENABLE CCE: TRANSFER_COUNT_INTERRUPT_DISABLE CHNE: CHAIN_DISABLE ESE: TRANSFER_CONTINUES

8. Project Build and Run

The demo can be used along with the GHS tools for projects using the g-cores utility. To start, please change into SSIF directory and open SSIF.gpj project with Multi. Build the project with F7 or by pressing the Build Button in Multi Project Manager. After the build has successfully finished, press the F5 or the Debug button to load Multi Debugger.

Starting the debugger requires a working target connection. Please start the script SSIF.rc from Multi debuggers command pane, like this:

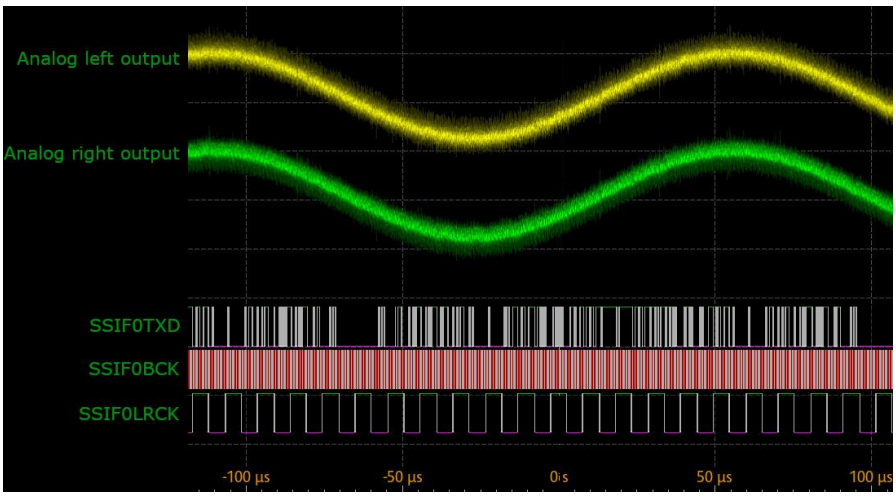
```
MULTI> <SSIF.rc
```

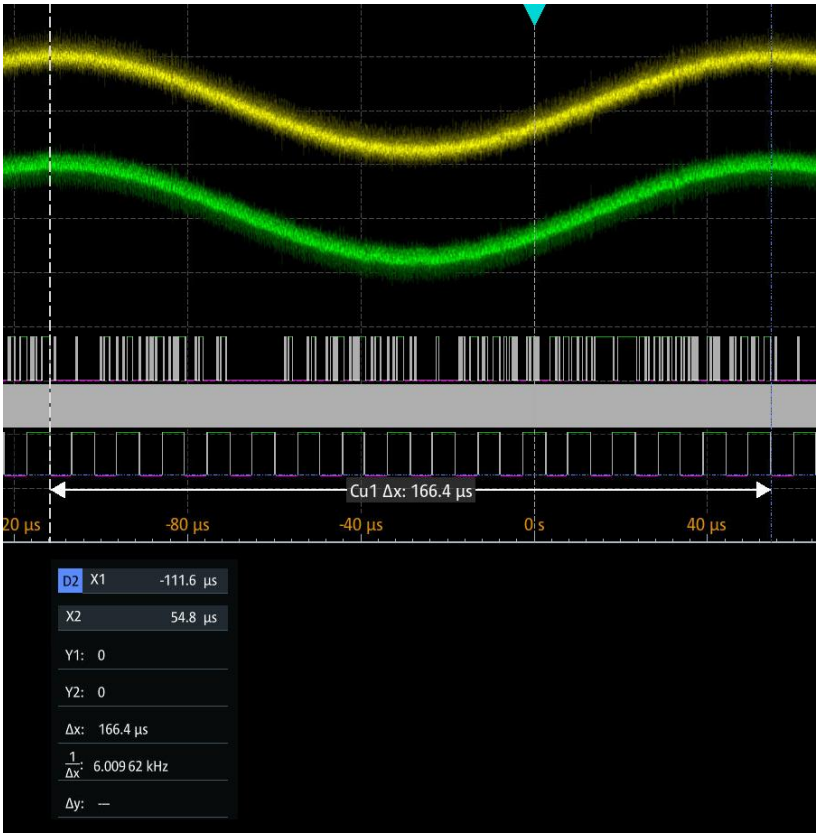
The script will connect to the target board and guide you through the debug process. These basic options are used to establish a connection:

Core:	-rh850
Connection method:	-e2lpd4=default
target clock:	-dclock=20000,0,swoff
Power Supply:	-t3v (Supply 3 Volt from emulator to target), or
	-t5v to supply 5 Volt from emulator

9. Test Results

Measurement results are present below. The measured output frequency is as expected 6009 Hz. 32 (16 samples per channel) sample buffer is sent on 96153 Hz.





$$\boldsymbol{Freq\ out} = \frac{\mathbf{96153}}{\mathbf{16}} = \mathbf{6009\ Hz}$$

Revision History

Rev.	Date	Description	
		Page	Summary
0001	11.05.2026		Initial revision.

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   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
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   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
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