RH850/U2C Series

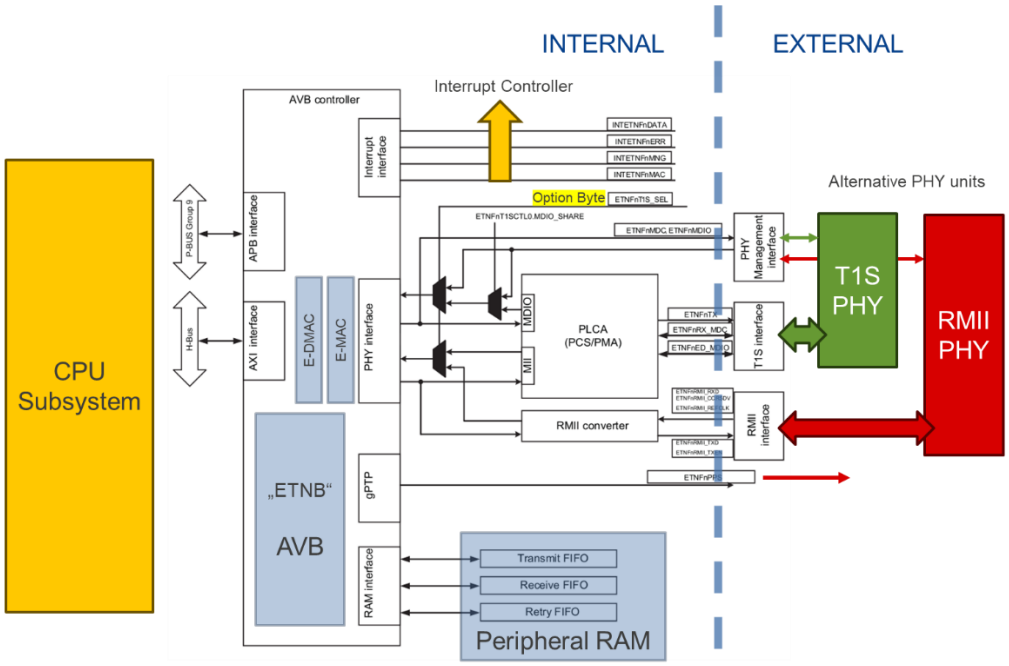
Ethernet 10BASE-T1S (ETNF) Initialization and Loopback Test

Introduction

This application note describes how to use the ETNF functionality (10BASE-T1S Ethernet) of RH850/U2C in principle and how to perform a loopback test of this system.

The provided sample code runs on the RH850/U2x application hardware development system by Renesas, in combination with the Renesas E2 debugger. The required hardware is described in references [1] and [2]. The required hardware needs to be configured separately, by using the configurator tool [5].

Figure 1: RH850 ETNF 10BASE-T1S Ethernet Function



Target Device

RH850/U2C: ETNF 10BASE-T1S Ethernet Interface

References

[1] R20UT5305[…]: Common Main Board for RH850 and R-Car U5x
[2] R20UT5390[…]: RH850/U2C 292pin User's Manual: Piggyback Board
[3] R01UH1018[…]: RH850/U2C User's Manual
[4] R01AN4449[…]: RH850/F1x Ethernet AVB (ETNB) Initialization and Loopback Test
[5] Main Board Configurator Tool, https://www.renesas.com/en/document/swo/mainboard-configurator-tool-v1500
[6] CT2505© Documentation: https://www.canovatech.com

Contents

1. Hardware / System Requirements

The following conditions on hardware are valid to use 10BASE-T1S on RH850/U2C:

- In case that the Renesas evaluation board hardware is used:
  - An external 10BASE-T1S PHY extension board is required to operate the ETNF Open Alliance (***OA***) 3-pin digital interface with the 10BASE-T1S wiring system.
    Such boards are available by Renesas upon request.
    The PHY extension board has to be plugged into the “ETH-T1S 0/1” socket on the main board [1].
    The line-side terminations on the PHY extension board have to be activated.
  - The I/O power supply voltage of the RH850/U2C piggy board has to be set to 3.3V.
  - Any other I/O functionality, which is using the same ports as the ETNF OA interface must be disconnected. 10BASE-T1S requires fast speed, and therefore any other connected parts may cause signal disturbances. This includes any activated peripherals of the main board too, which are sharing the same signals as the OA interface. In any setting of the board configurator [5], such peripherals shall be set as disconnected and disabled.
  - To enable the 10BASE-T1S PHY with power supply and releasing its standby condition, the board configurator [5] has to be set as follows:

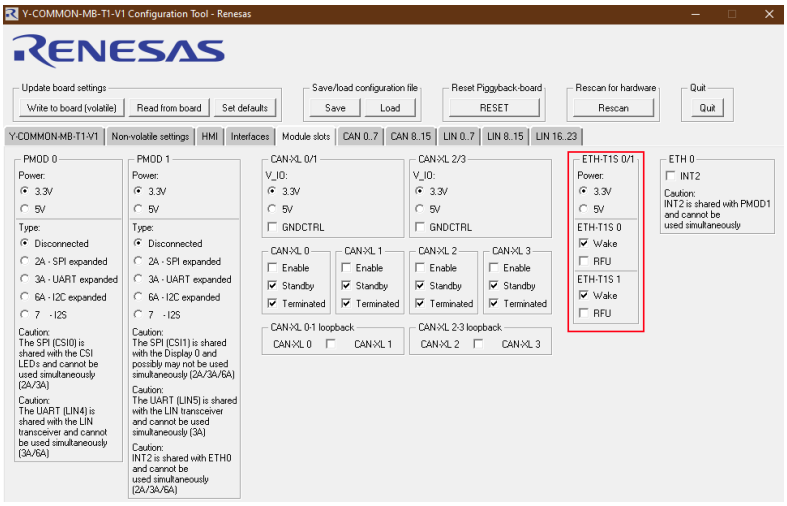


Figure 2: Board Configurator GUI

- In any case, when using any kind of hardware:
  - Keep the ETNF OA interface signals as short as possible.
  - Enable maximum drive strength for the I/O ports used.
    Allow ETNF port direction control of the OA interface.
    The following instructions on port settings will provide these settings on RH850/U2C:

    Assuming that the OA signals are used by following ports:
    ED_MDIO = P20.13; RX_MDC = P20.3; TX = P20.4

```
/* Activate ETNF T1S operation */
/* Set Port 20 Bits 3+13 (ED_MDIO, RX_MDC) for ETNF0 controlled output direction */
PORT0.PIPC20.UINT16 |= 0x2008;

/* Activate maximum drive strength for ETNF ED_MDIO, RX_MDC and TX ports */
PORT0.PDSC20.UINT16 |= 0x2018;
PORT0.PUCC20.UINT16 |= 0x2018;
```

2. Architecture of 10BASE-T1S ETNF Functionality

The ETNF unit, as shown in the overall block diagram in figure 1, consists of an Ethernet MAC unit and some add-on functionality for the 10BASE-T1S adaptation.

The MAC unit is inherited from the Ethernet controller type “ETNB”, which is already existing in several other products of the RH850 series, like RH850/U2A or RH850/F1KM. Therefore, in principle the software approach to work with this MAC can be imported from projects of these product series. The MAC internally is using an MII interface.

Its connectivity to 10BASE-T1S is provided by an additional PLCA component, which converts the MII interface into an Open Alliance ® interface (OA), with its three signals TX, RX and ED.

In addition, the connectivity of the MAC to external PHY units is given by an RMII interface, which is provided by an MII to RMII converter. Therefore, it is possible to use ETNF as a standard 100BASE-TX Ethernet adapter, too, when attaching such a PHY to the RMII interface. The details for this kind of connection in not in focus of this application note, however.

Having some internal RAM for its FIFO structures and interconnection with the interrupt controller and the bus systems completes the architecture of ETNF. Two connections to bus systems are provided: the peripheral bus for register configuration, and the high-speed multi-master bus system to handle the Ethernet data exchange. To handle the data flow, ETNF has a built-in bus master, which works like a DMA unit.

2.1 Integration of the 10BASE-T1S PLCA Functionality

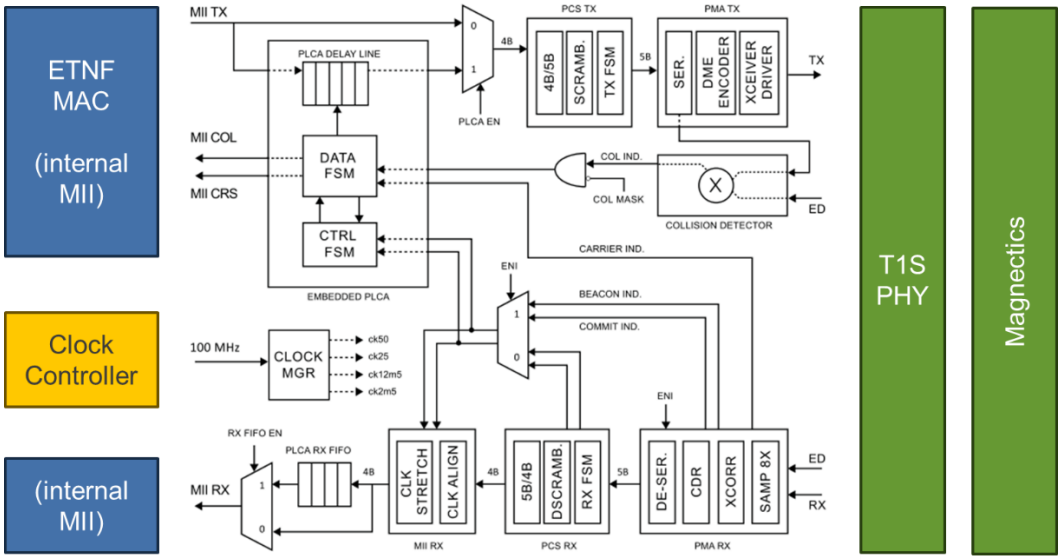


Figure 3: ETNF PLCA Block Diagram

The integrated 10BASE-T1S PLCA is designed by CanovaTech, type CT25205. Its detailed documentation can be retrieved from [6]. For our self-testing application and first steps of use, it is sufficient to know the following properties and settings, which need to be configured and used:

- Configuration method to set registers of the PLCA, using the MDIO interface of ETNF internally
- Activating the 10BASE-T1S beacon signal to provide timing master functionality, as node 0.
- Setting the amount of nodes on the line, to define the time-sharing system.
- Setting the loop-back configuration, so that the ETNF MAC can receive its own transmission.

2.2 PLCA Operation Modes and OA Interface Signaling

This chapter shall explain the rough functionality of the PLCA, when converting MII signals into OA compatible signals and vice versa.

First of all, the PLCA has to serialize and deserialize the MII (parallel bytes) data into serial single bit data stream of OA, which then connects to the PHY at the outside line. Doing that, it also converts the MII bit coding into a RZ (return-zero) bit coding, so that each bit is represented by a pulse on the TX side, whereas the RZ coded serial bits are converted to 8-bit groups and the RZ coding is converted to NRZ.

In addition, the OA interface also manages the external PHY by providing a configuration mode, where its ED pin gets MDIO signal functionality, and its RX pin gets MDC signal functionality. MDC/MDIO are commonly used by PHY units in xMII systems, too. By these signals, registers in the external PHY can be read or written.

The figure below shows the operation modes of the PLCA, which can be set by using a setting inside of the PLCA register set.

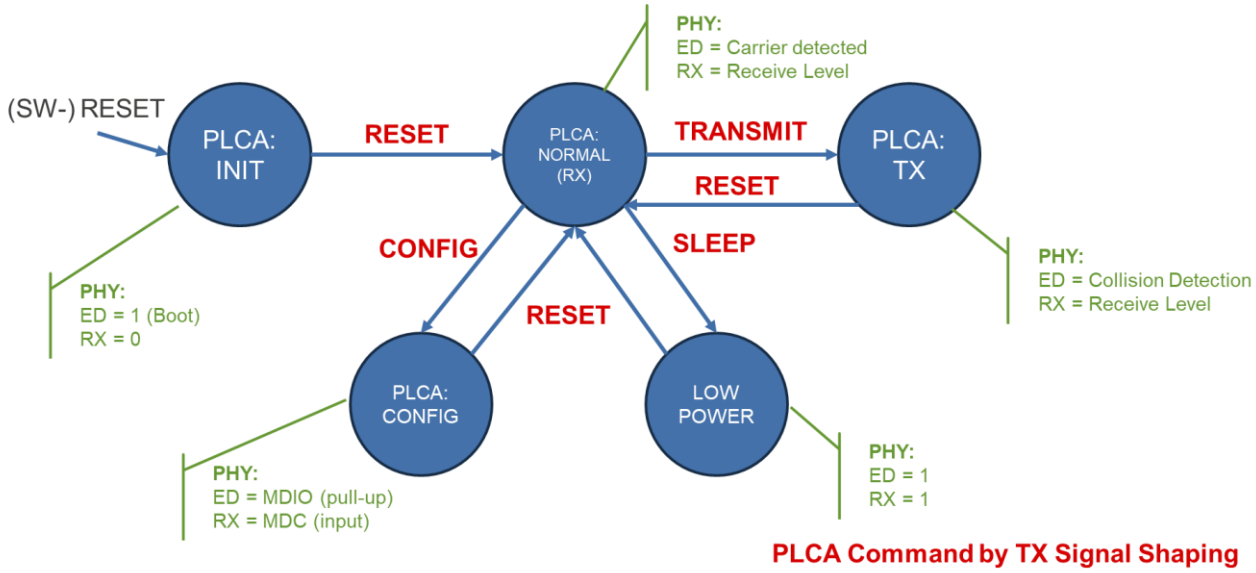


Figure 4: PLCA Operation Modes

To indicate the operation mode and also to set the external PHY into the same mode, the PLCA generates specially shaped waveforms on its TX signal. The five modes are:

1. Init Mode
   In this mode the PLCA starts, and it waits there until from the external PHY is indicated that its boot process is finished. The external PHY will pull ED high to indicate this.
2. Normal Mode (RX)
   This mode is receiving data from the external PHY. It is the default operation mode, whenever no own transmission is ongoing, and no configuration is happening. All received data is forwarded from the OA interface (RX) to the MII, as soon as the PHY activates ED to high, to indicate that a carrier on the external line has been detected.
3. Transmission (TX)
   As soon as the MAC initiates a data transmission on MII, the PLCA moves to this mode and indicates this by a specially shaped waveform on TX first. After that, the data is forwarded from MII to TX of the OA interface. The external PHY will indicate any media collision by setting ED to high, and it will return the transmitted signal on its RX signal. By this, the PLCA can determine whether a transmission could be performed without disturbances.

4. Configuration Mode
   From CPU side (by software), the configuration mode can be requested by setting a register inside of the PLCA. This causes the PLCA to enter configuration mode and re-use the OA interface signals in a different manner: ED becomes MDIO, and RX becomes MDC. The internal MDIO bus is in addition routed to the external PHY by that, so that PLCA and external PHY registers now are accessible through the MDIO system, which can be controlled by ETNF registers.
   It is important to set different MDIO base addresses for the PLCA and for the external PHY; otherwise, selective access of the registers of each part could not be achieved. Many external PHY units do not allow the modification of their MDIO base address. In this case, the MDIO base address of the PLCA attached to ETNF is configurable to a different one.

5. Low Power / Sleep Mode
   The low power mode is initiated from CPU side to the PLCA, which in turn will send the sleep command as a specifically shaped waveform on TX to the external PHY.
   As soon as the external PHY detects energy on the line side again, it will toggle the ED signal, which can wake up the CPU side by an edge triggered interrupt.
   To finally wake up the external PHY again, the request for normal mode is given to the PLCA, which will then convert this command into a specifically shaped waveform on TX, which in turn will re-activate the external PHY again.
   The low power / sleep mode isn’t part of the focus of this application note.

3. Software Components

The architecture of the software package associated with this application note looks like this:

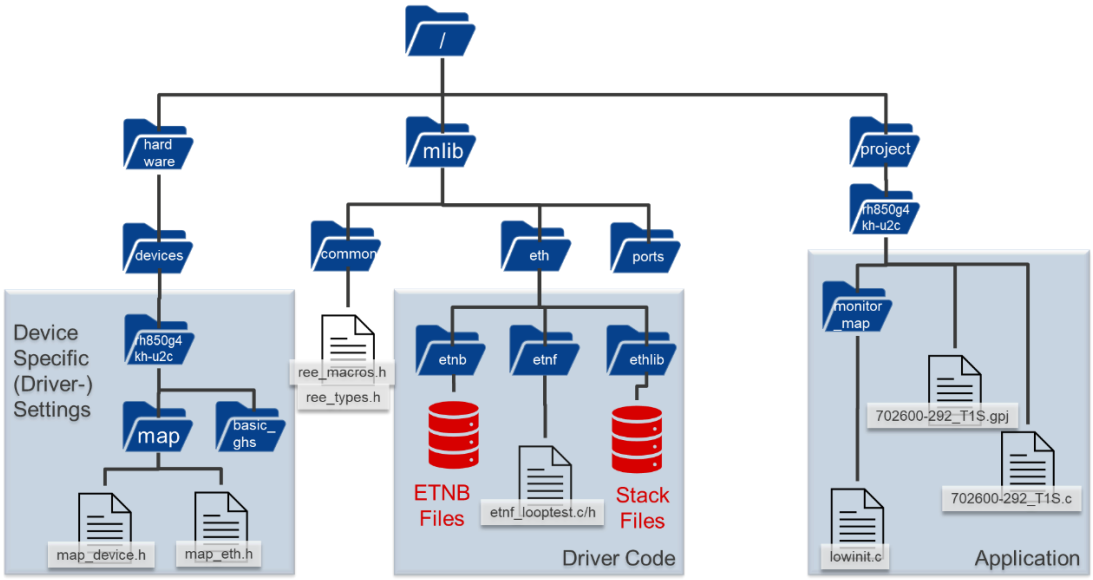


Figure 5: Software Package Architecture

When running in the delivered default configuration, the application “702600-292_T1S.c” runs the self-test procedure of ETNF, which is completely contained in the file “etnf_looptest.c”, with exception of port settings; for those an additional function set is given in the “ports” folder.
The “basic_ghs” folder and “lowinit.c” functions are providing proper startup code for the target product.
The GHS project “702600-292_T1S.gpj” includes all code and settings and is the starting point.

If the default definition of “SELFTEST” in “702600-292_T1S.c” is removed, then the application also calls the ETNB MAC layer functionality in the “etnb” folder and TCP/IP stack initialization within the “ethlib” folder. This is additional software, which can be tried to examine the T1S network capabilities, yet it is beyond this document.

4. General Operation Steps for ETNF

Within this chapter, the principles of setup are described, which are necessary to allow 10BASE-T1S operation with ETNF and an OpenAllicance ® PHY type (using the 3-pin OA interface of the RH850/U2C products).

4.1 Option Bytes of RH850/U2C

Setting of option bytes is a precondition to allow the ETNF MAC to operate with an OA PHY unit.

The following settings must be done:

4.1.1 Option Byte 8

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	ETNF0_T1S_SEL	—	—	—	ETND0_IF_SEL[1:0]		—	CKSEL_GTM	CLMA1SEL	—	—	—	—	—	—
Value after reset:	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RESET_PD_EN	—
Value after reset:	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1	0/1*1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note 1. This value is dependent on the value in the flash memory which is specified by the user.

Figure 6: Option Byte 8

Set bit 30 to 1 = T1S.

4.2 PORT Configuration

The direction, alternative function and drive strength of the output direction ports must be set accordingly. When using Renesas Application Hardware [1] and [2], the corresponding ports are those:

P20<4>	ETH0_T1S_TX
P20<3>	ETH0_T1S_RX_MDC
P20<13>	ETH0_T1S_ED_MDIO

Figure 7: Ports of 10BASE-T1S used on RH850/U2C Piggy Boards

P20<4>: Output port, set output direction, highest drive strength, and ETNF alternative function.
P20<3>: Input/output port, set input direction, highest drive strength, and ETNF alternative function. Set the PIPC flag for this port to allow direction control by ETNF.
P20<13>: Input/output port, set input direction, highest drive strength, and ETNF alternative function. Set the PIPC flag for this port to allow direction control by ETNF.

```
/* Activate ETNF T1S operation */
/* Set Port 20 Bits 3+13 (ED_MDIO, RX_MDC) for ETNF0 controlled output direction */
PORT0.PIPC20.UINT16 |= 0x2008;
/* Activate drive strength 2 for ETNF ED_MDIO, RX_MDC and TX ports */
PORT0.PDSC20.UINT16 |= 0x2018;
PORT0.PUCC20.UINT16 |= 0x2018;
```

4.3 Initial Reset and Standby Release

When using the first time after reset and to prevent issues when re-entering the application, it is making sense to first clear the ETNF completely by a soft-reset.

To perform a soft-reset, the RH850/U2C hardware provides a dedicated functionality for ETNF, used like this:

```
/* Generate Soft-Reset for ETNF */

SYSCTRL.RESKCPROT0.UINT32 = 0xA5A5A501;
SYSCTRL.SWMRESA_ETNF.UINT32 = 0x00000001L;
while( SYSCTRL.SWMRESS_ETNF.UINT32 == 0x00000000L );
SYSCTRL.SWMRESA_ETNF.UINT32 = 0x00000000L;
while( SYSCTRL.SWMRESS_ETNF.UINT32 == 0x00000001L );
SYSCTRL.RESKCPROT0.UINT32 = 0xA5A5A500;
```

The ETNF function also is disabled, when starting up from power-on or from standby modes. Therefore, the module needs to be activated within the standby controller by this sequence:

```
SYSCTRLMSRKCPROT     = 0xA5A5A501;  // unprotect the module standby control register
ETNF_STANDBYCONTROL  &= ~( 0x00000001L );
SYSCTRLMSRKCPROT     = 0xA5A5A500;  // protect the module standby control register
```

5. Operation of the Self-Test Software

After following the steps of chapter 4, the self-testing sequence can be initiated by the next actions.

5.1 MAC Configuration

MAC configuration consists of the following steps, they are described in detail within the related source code functions.

1. Setting configuration mode
   Function: R_ETNF_OpModeChange( )
2. Basic MAC settings
   Function: R_ETNF_EMACInit( )
3. Setting the operation mode of the MAC
   Function: R_ETNF_DMACMode( )
4. Initialize the descriptor chains and enter the address of the chains in the MAC table vectors
   Function: R_ETNF_DMACDescriptorTable( )
5. Set reception and transmission properties
   Function: R_ETNF_DMACRxConfig( ) and R_ETNF_DMACTxConfig( )
6. Set the transfer speed to 10 Mbit/s (which is essential for 10BASE-T1S)
   Function: R_ETNF_RMIILSpeed( )
7. Define interrupt settings
   Function: R_ETNF_interrupt( )
8. Set operation mode to start communication capability
   Function: R_ETNF_OpModeChange( )

These steps are also described in the referred application note of ETNB, [4].
The functionality of the MAC of ETNB (in RH850/F1x) and ETNF (in RH850/U2C) is equal.

5.2 PLCA Configuration

The PLCA configuration is done within the function “R_ETNF_ConfigPLCA( )” of the file “etnf_looptest.c”, and consists of the following steps:

- Setting the PLCA PHY address to a different one than the external T1S PHY attached to the OA interface. This is important to do, since without that it would not be possible to address PLCA and T1S separately using the unique MDIO management interface (see chapter 2, “Configuration”). We are using the PLCA MDIO address 2, most external PHY types are using address 1:

  ```
  ETNF_PLCAPHYADDR = 0x01FFFFE2; /* set PLCA PhyAddr = 2 */
  ```

- Reading of a few PLCA internal version registers, to make sure that the PLCA is available and responsive. For example, we are reading the PHYID and CTIPVER registers through the MDIO. The PLCA registers can be read anytime through MDIO, even if the PLCA has not set the external PHY to configuration mode. In this case, the MDIO management interface is kept internal between ETNF and PLCA.
- Activation of the loopback within the PLCA, to make sure that we can get back the transmitted frames, even if the external PHY would have no line or a shorted line to the outside. The principle of the self-testing is to verify the functionality by getting back a transmitted frame.

  ```
  R_AVB_MacPhyWr45 (0x3F8001, 0x8003); // T1STWEAKS, set PKTLOOP
  ```

- Activation of the PLCA operation to get it ready for communication. This is done by setting the LCTL flag in the CONTROL register.

  The CONTROL register is, in contrary to the T1STWEAKS register, addressable directly by an IEEE clause 22 access (8-bit standard addressing of MDIO). Therefore, the wrapping function "R_AVB_MacPhyWr45( )" is not necessary here; which would extend the addressing to the IEEE clause 45 access format, using a separate 16-bit address register.

```
R_AVB_MacPhyWr22 (2, 0, 0x1000); // CONTROL, set LCTL
```

- Configuration of the T1S architecture, by setting the local node ID and specifying the amount of network nodes. We are using ID=0, which means this local node will be the bus master and will send out the "beacon" signal for all other nodes on the bus. With the amount of bus nodes set to 8, a typical value is used, which allows up to 8 bus nodes. These nodes will have to use the given T1S timeslots in the order of their local ID, after the bus master has started the T1S bus cycle by the beacon.
  For the self-testing functionality, it is making sure that we may immediately start to send, without having to wait for a bus master.

```
R_AVB_MacPhyWr45 (0x3FCA02, 0x0800); // PLCACTRL1, set NCNT=8, ID=0
```

- After the PLCA initialization, the external PHY can be configured, too.
  Within this application note, it is not possible to share the initialization code for an external PHY, because this is specific for the PHY and requires information from PHY 3rd party side.
  Nevertheless, the following steps are performed to set the external PHY into configuration mode and activating the external management interface by this step. The configuration mode can be entered, after waiting until the PLCA is in normal operation mode:

```
do
{
  vs = R_AVB_MacPhyRd45( 0x3F8006 ); // T1STXCST, check TXCST status NORMAL

} while( ( vs & 0x07 ) != 0x00 );

R_AVB_MacPhyWr45( 0x3F8005, 0x0002 ); // T1STXCCTL: PHY CONFIG Request
```

  After the configuration request the external PHY can be addressed by its MDIO address, and, for example, its identification registers can be read out by using the standard addresses of IEEE clause 22:

```
vs = R_AVB_MacPhyRd22 ( 1, 2 ); // PHYID0 -> 0x…
vs = R_AVB_MacPhyRd22 ( 1, 3 ); // PHYID1 -> 0x…
```

  After the external PHY has been configured, the PLCA needs to be returned into normal mode.

```
R_AVB_MacPhyWr45( 0x3F8005, 0x0000 ); // T1STXCCTL: PHY RESET/NORMAL Request

do
{
  vs = R_AVB_MacPhyRd45( 0x3F8006 ); // T1STXCST, check TXCST status NORMAL

} while( ( vs & 0x07 ) != 0x00 );
```

  As last step of configuration, the PLCA reconciliation is started. This is the functionality which operates the T1S time slots and the beacon transmission, so that other nodes on the T1S bus would be able to find their communication slot. In other words, this step enables the major T1S functionality.

```
R_AVB_MacPhyWr45 (0x3FCA01, 0x8000); // PLCACTRL0, set PLCA EN
```

5.3 Transmission / Reception and Buffers

The function “R_ETNF_SetTxBuf( )” is setting up a transmit frame for the self-testing, filling in the frame data.

After that, on MAC side the communication is enabled by calling “R_ETNF_MACTxRxEnable( )”.

Finally, the transmit frame is sent out by calling “R_ETNF_Send_SingleDescFrame( )”. This activates the transmit descriptor into the status “FSINGLE” and triggers the transmission using the TCCR register of the ETNF MAC.

After that, the self-test algorithm is waiting until the receive descriptor interrupt occurs. When the interrupt hits, it sets a global variable, and the algorithm then continues to verify the received frame data. As the receive descriptors have already been defined beforehand, the address to check the received frame is known.

The self-test is pass, if all received data matches with the transmitted data.

6. Outlook: Additional Software Components

The provided sample code contains additional functionality, like a TCP/IP stack, and an alternative initialization routine to replace the self-test initialization.

In this alternative initialization, the ETNF settings and descriptors are defined by the needs of the stack, which allows “best effort” communication, based on the ETNB driver set.

The alternative initialization is enabled by removing the setting

```
#define SELFTEST
```

… in the main program “702600-292_T1S.c”.

After starting the sample code in this configuration, the U2C product provides a 10BASE-T1S master node (0), answering to Ethernet packets of TCP/IP (“ping”), ARP and HTTP. The IPV4 address is set to 192.168.0.2.

Revision History

Rev.	Date	Description	
		Page	Summary
01.00	12-DEC-2024	all	Initial creation.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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