RH850/U2C Group

R01AN7566EJ0100
Rev.1.00

Clock Monitor Application Note

Summary

This application note summarizes an example of the operation of the RH850/U2Cx Clock monitor program using a user program. The Clock monitor program is assumed to be in the user area.

This document and program are intended to facilitate understanding of the functions equipped in the RH850/U2C and are not intended for mass production design.

In addition, it does not reflect the latest manuals, errata, technical updates, or updates to the development environment. When using the relevant functions, please treat this program as a reference and ensure that you proceed at the user's own responsibility with the latest documentation and development environment.

Apply

This document applies to RH850/U2Cx.

When downloading to the Configuration Setting Area, set arbitrary option byte in "set_csa.c", allow downloading and rewrite the option byte. For details, refer to the RH850/U2C Series Startup Application Note.

(1) Select "***** (Debugging Tool)" from the project tree.

(2) Select the “Download File Settings” tab.

(3) Set “Allow downloads to Configuration Setting Area” = “Yes”

Contents

1. Introduction

This application note describes how to use the RH850/U2Cx clock monitor and provides examples of software creation.

1.1 Functions to use

The following shows the hardware functions of RH850/U2Cx used in this application note.

- Clock Monitor（CLMA）
- Error Control Module（ECM）

1.2 Overview of clock monitor functionality

The Clock Monitor (CLMA) detects frequency abnormalities in the monitored clock. When an abnormality in the clock frequency is detected, an error notification is sent to the error control module (ECM).

Table 1-1 shows the list of monitor clocks and sampling clocks.

Table 1-1 The list of monitor clocks and sampling clocks

Unit name	CLMATMON （Monitor Clock）	CLMATSMP （Sampling Clock）
CLMA0	CLK_MOSC	CLK_HSIOSC / 400
CLMA1	CLK_WDTB/ 2（CLMA1SEL=1）	CLK_LSIOSC
	CLK_HSIOSC / 20（CLMA1SEL=0）	CLK_MOSC /32
CLMA2	CLK_LSIOSC	CLK_HSIOSC / 6400
CLMA3	CLK_LSB	CLK_MOSC /32
CLMA4	CLK_LSB	CLK_HSIOSC / 20
CLMA5	CLKC_SBUS / 2 (CLEAN) (CKSEL_GTM=0)	CLKC_LSB / 8 (CLEAN)
	CLKC_UHSB / 2 (CLEAN) (CKSEL_GTM=1)	
CLMA6	CLK_CPU (PE0) / 4	CLKC_LSB / 8 (CLEAN)
CLMA7	CLK_CPU (PE1) / 4	CLKC_LSB / 8 (CLEAN)
CLMA8	CLKC_LSB(CLEAN)	CLK_MOSC / 32

2. Examples of clock monitor operation

2.1 Specification overview

This section explains how to use the clock monitor.

（1）CLMAn counts the rising edges of the monitored clock (CLMATMON) within 16 cycles of the sampling clock (CLMATSMP) and compares the count value with the predefined threshold.

- CLMAnCMPL.CLMAnCMPL[11:0] Definition of lower threshold
- CLMAnCMPH.CLMAnCMPH[11:0] Definition of upper threshold

（2）When the CLMATMON frequency is too low (Note 1), the count falls below CLMAnCMPL.CLMAnCMPL.

（3）When the frequency of CLMATMON is too high, the count exceeds CLMAnCMPH.CLMAnCMPH.

（4）In the case of (2) or (3), a frequency abnormality occurs and an error notification is sent to the ECM.

【Note 1】 If the monitored clock is completely stopped, the error may not be detected.

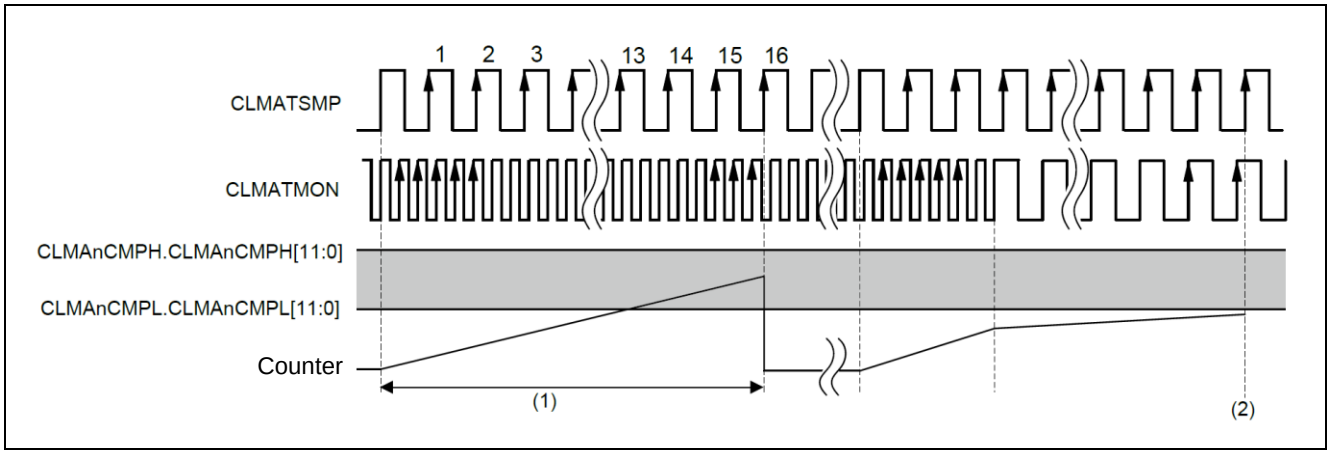

Figure 2-1 Example: fCLMATMON is lower than the lower limit

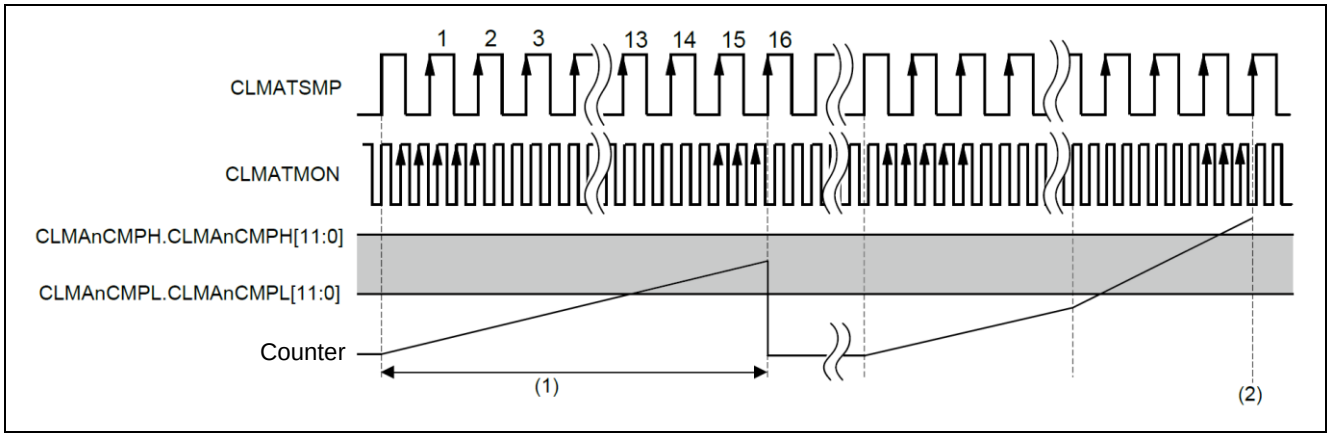

Figure 2-2 Example: fCLMATMON is higher than the upper limit

2.2 Functions to use

The hardware functions used in this example are as follows:

- Clock Monitor（CLMA0~8）
- Error Control Module（ECM）

2.3 Explanation of operation example

If a CLMA frequency abnormality occurs, an ECM error interrupt occurs. Table 2 1 shows the list of monitor clocks and sampling clocks in this operation example.

Table 2-1 List of monitor clocks and sampling clocks in this operation example

	CLMATMON			CLMATSMP		
	Clock	Frequency	Error	Clock	Frequency	Error
CLMA0	CLK_MOSC	20MHz	±0.1%	CLK_HSIOSC / 400	0.5 MHz	±5.0%
CLMA1	CLK_WDTB HS IntOSC /1280	0.1563 MHz	±5.0%	CLK_LSIOSC	0.0328 MHz	±10%
CLMA2	CLK_LSIOSC	0.0328 MHz	±10%	CLK_HSIOSC / 6400	0.03125 MHz	±5.0%
CLMA3	CLK_LSB	40 MHz	±0.1%	CLK_MOSC / 32	0.625 MHz	±0%
CLMA4	CLK_LSB	40 MHz	±0.1%	CLK_HSIOSC/ 20	10 MHz	±0%
CLMA5	CLKC_SBUS/2	100 MHz	±0.1%	CLKC_LSB / 8	5 MHz	±0%
CLMA6	CLK_CPU/4	80 MHz	±0.1%	CLKC_LSB / 8	5 MHz	±0.1%
CLMA7	CLK_CPU/4	80 MHz	±0.1%	CLKC_LSB / 8	5 MHz	±0.1%
CLMA8	CLKC_LSB (CLEAN)	40 MHz	±0.1%	CLK_MOSC / 32	0.625 MHz	±0%

2.3.1 Threshold calculation

The compare registers CLMAnCMPL and CLMAnCMPH specify the minimum and maximum values of the CLMATMON clock cycles that occur within 16 cycles of the sampling clock CLMATSMP, which defines the normal range for CLMATMON. N indicates the number of CLMATMON clock cycles that occur within 16 cycles of CLMATSMP.

N = (f CLMATMON / f CLMATSMP) × 16

Considering the allowable frequency deviations of CLMATMON and CLMATSMP, calculate the threshold using the following formula:

Note that the lower threshold value is rounded down to one decimal place, and the upper threshold value is rounded up to one decimal place.。

Lower threshold（Nmin）= (f CLMATMON(min) / f CLMATSMP(max)) × 16 − 1

Upper threshold（Nmax）= (f CLMATMON(max) / f CLMATSMP(min)) × 16 + 1

2.3.2 Option byte settings

Table 2-2 shows the option byte settings selected in this operation example.

Table 2-2 Contents of option byte (BT8).

Bit Position	Bit name	Function
23	CKSEL_GTM	GTM Clock selection 0：CLKC_SBUS
22	CLMA1SEL	CLMA1 Clock monitor target selection 1：CLK_WDT

2.4 Software description

Module description

The following is a list of modules for this operation example.

Table 2-3 Module list

Module name	Label name	Function
Main routine	main_pm0	Configure various settings and start applications.
Port initialization routine	port_init	Configure the initial settings for the port.
ECM initialization routines	ecm_init	Perform the initial settings of the error control module.
Interrupt initialization routines	intc_init	Perform the initial settings for the error control module.
Clock monitor initialization routine	clk_mon_init	Configure the initial settings for the clock monitor.
Enable clock monitor operation	clk_mon_start	Set the clock monitor to enabled.
Interrupt processing routine	ecm_int	Interrupt function. When an error occurs, the error status is stored in a variable.

- Register settings

The following shows the Register settings for each function in this operation example.

Table 2-4 Clock monitor register settings

Register name	Setting value	Function
CLMAKCPROT	0xA5A5A501	Enable write access to protected registers.
	0xA5A5A500	Disable write access to protected registers.
CLMA0CMPL	0x025F	CLMA0 Lower threshold
CLMA0CMPH	0x02A4	CLMA0 Upper threshold
CLMA1CMPL	0x0040	CLMA1 Lower threshold
CLMA1CMPH	0x005B	CLMA1 Upper threshold
CLMA2CMPL	0x000D	CLMA2 Lower threshold
CLMA2CMPH	0x0015	CLMA2 Upper threshold
CLMA3CMPL	0x03FD	CLMA3 Lower threshold
CLMA3CMPH	0x0403	CLMA3 Upper threshold
CLMA4CMPL	0x003E	CLMA4 Lower threshold
CLMA4CMPH	0x0042	CLMA4 Upper threshold
CLMA5CMPL	0x013E	CLMA5 Lower threshold
CLMA5CMPH	0x0142	CLMA5 Upper threshold
CLMA6CMPL	0x00FE	CLMA6 Lower threshold
CLMA6CMPH	0x0102	CLMA6 Upper threshold
CLMA7CMPL	0x00FE	CLMA7 Lower threshold
CLMA7CMPH	0x0102	CLMA7 Upper threshold
CLMA8CMPL	0x03FD	CLMA8 Lower threshold
CLMA8CMPH	0x0403	CLMA8 Upper threshold

Register name	Setting value	Function
CLMABCE	0x00	Disable the backup clock function
CLMA0CTL	0x01	CLMA0 Enable operation
CLMA1CTL	0x01	CLMA1 Enable operation
CLMA2CTL	0x01	CLMA2 Enable operation
CLMA3CTL	0x01	CLMA3 Enable operation
CLMA4CTL	0x01	CLMA4 Enable operation
CLMA5CTL	0x01	CLMA5 Enable operation
CLMA6CTL	0x01	CLMA6 Enable operation
CLMA7CTL	0x01	CLMA7 Enable operation
CLMA8CTL	0x01	CLMA8 Enable operation

Table 2-5 Interrupt Register settings

Register name	Setting value	Function
PWE	0x00000100	P10 Enable register access
PCR10_10	0x0000004E	ERROROUT_C function, Output ports

Table 2-6 Port Register settings

Register name	Setting value	Function
EIBD8	0x00000000	Bind interrupt to PE0 (CPU0)
EIC8	0x0040	Interrupt enabled, table reference method, priority level 0

Table 2-7 ECM Register settings

Register name	Setting value	Function
ECMKCPROT	0xA5A5A501	Enable write access to protected registers.
	0xA5A5A500	Disable write access to protected registers.
ECMPEM	0x00000003	ECM Mask/Slave Mask
ECMMECLR	0x00000001	Set the ERROROUT terminal to high level output
ECMCECLR	0x00000001	Set the ERROROUT terminal to high level output
ECMINCFG0_2	0x00002F80	CLMA0～CLMA5、CLMA8Enable interrupts when an error occurs.
ECMINCFG0_7	0x00000020	CLMA6 Enable interrupts when an error occurs.
ECMINCFG0_8	0x00000020	CLMA7 Enable interrupts when an error occurs.

- Operational flow
  The following shows flowchart of this operation example.

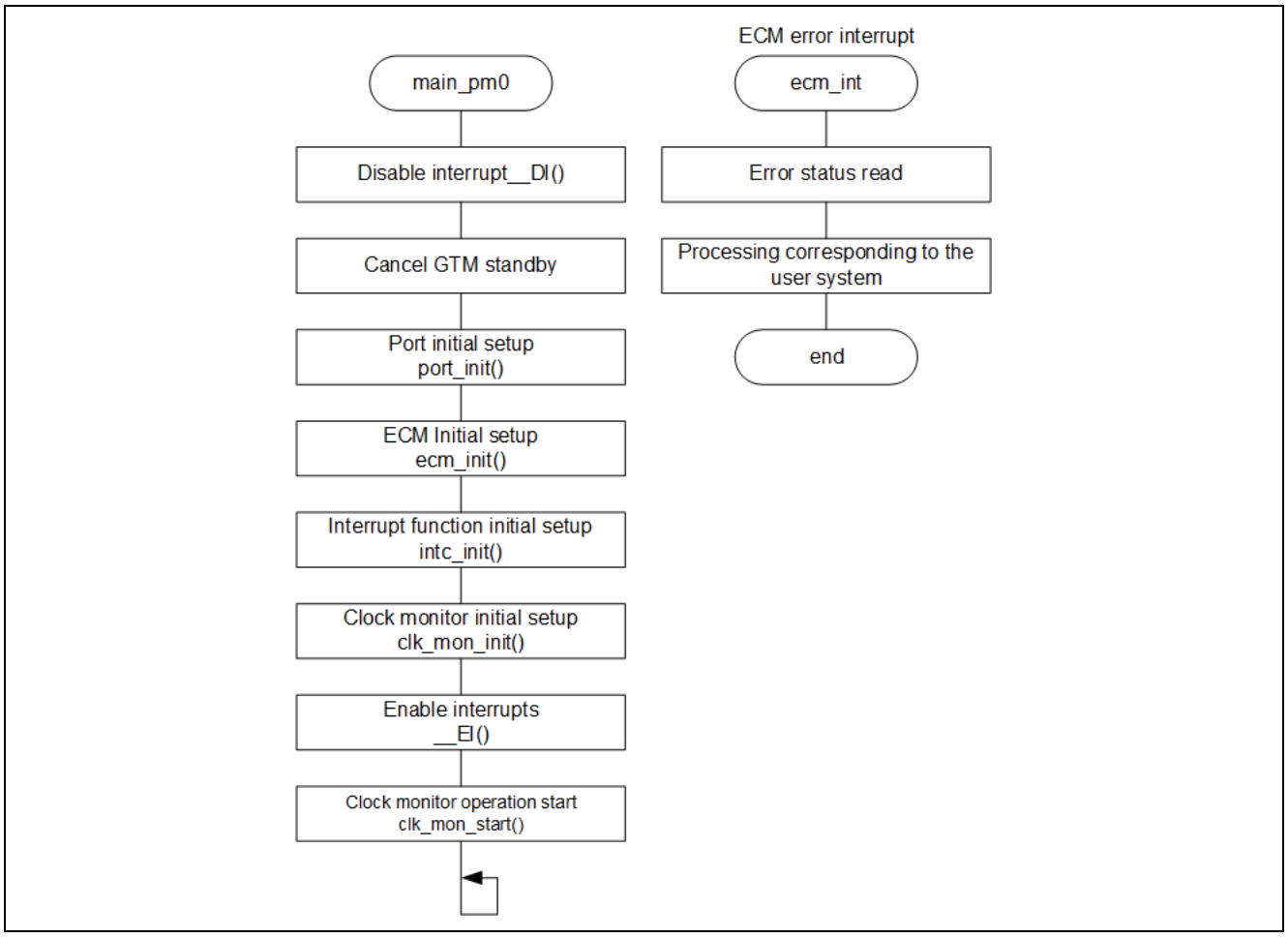

Figure 2-3 Flowchart

3. Revision Record

Rev.	Issue date	Revised contents	
		Page	Points
1.00	Nov 5, 2024	-	First edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
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   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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