RH850/U2B Group

R01AN6735EJ0110
Rev.1.10

RLIN3 UART Mode Application Note

Summary

This application notes explains the RLIN3 UART Mode function of automotive single-chip microcontroller RH850/U2B series for automobile (hereinafter called U2B).

Aim of this document and software is to provide supplemental information for the function on RH850/U2B. It is not intended to implement in the design for mass production. There is no guarantee to update in this document and software to reflect the latest manual, errata, technical update and development environment. You are fully responsible for the incorporation or any other use of the information of this document in the design of your product or system, and please refer to latest manual, errata, technical update and development environment.

Target Device

- RH850/U2B Group

Target Integrated Development Environment

CS+ (from RENESAS Electronics)

Device file :DR7F702Z21*.DVF

Reference Document

RH850/U2B User's Manual: Hardware

For function details and electrical characteristics, please refer to "User's Manual: Hardware".

This application note is based on the following manual.

・ RH850/U2B User's Manual (Rev.1.00): R01UH0923EJ0100

Summary

1. Introduction

This application note reports the making examples for the RLIN3 UART mode usage and farmwear mounted RH850/U2Bx.

1.1 Used Function

The RH850/U2Bx handwear functions used in this application note are shown below.

- RLIN3
- sDMAC
- OS Timer

2. Communication Format

The communication format used in this application example is mentioned. The communication format setting is performed in the RLN3nLBFC register.

2.1 Communication Mode

UART Mode

2.2 Communication Format

Character length	: 8 bits
Parity	: Even parity
Stop bit	: 1 bit

3. Operation Example

3.1 Loopback Communication

3.1.1 Specification Overview

Explains about the reception pin of RLIN3 UART mode and the loopback communication connected the transmission pin.

In this operation example, connect the reception pin in RLIN3 UART mode with the transmission pin, and transmit/receive.

The data transmission is started to store the transmit data to the UART transmit data register (RLN34LUTDR).

The next transmit data is stored to the UART transmit data register (RLN34LUTDR) when the following all conditions are satisfied.

-The previous data transmission is completed. (RLIN34 transmission completion interrupt (INTRLIN34UR0) generation)

-100ms is passed from the previous data transmission starting.

100ms is measured by OSTM.

When the transmitted data is received, the RLIN34 reception completion interrupt (INTRLIN34UR1) is generated. This operation example reads the data received in the interrupt processing from the UART receive data register (RLN34LURDR).

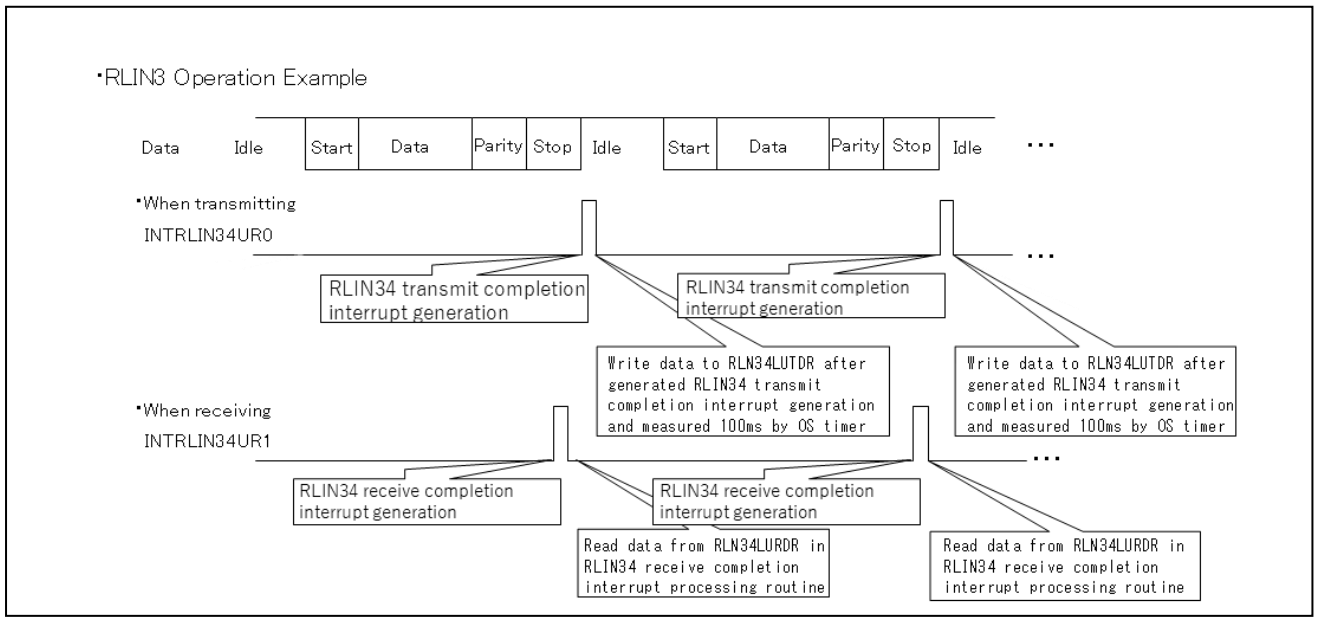

Figure 3-1 Transmit/Receive Operation by Loopback

3.1.2 System Configuration

Figure 3-2 shows the system configuration.

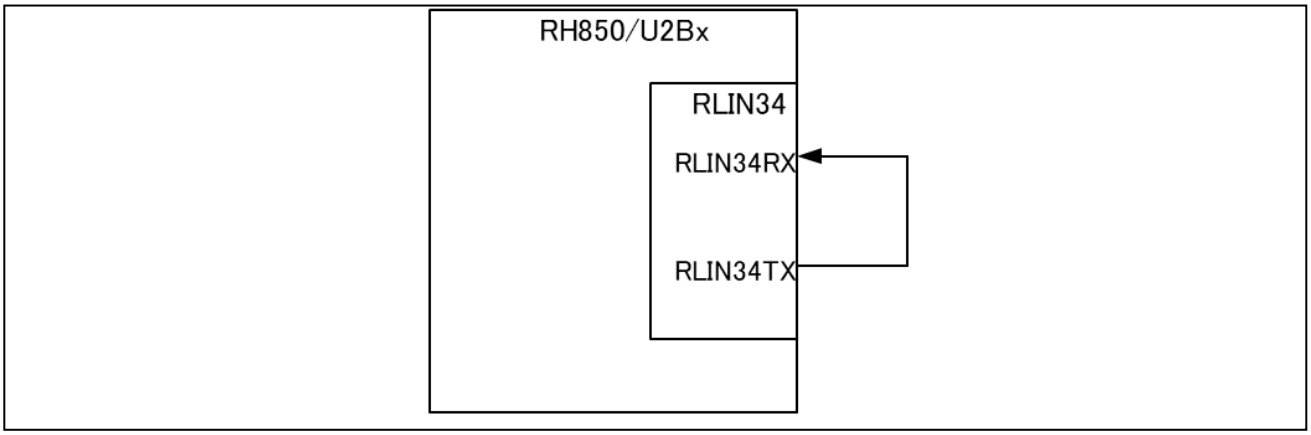

Figure 3-2 System Configuration

3.1.3 Explanation for Operation Example

In this operation example, perform the loopback communication connected the receive pin with the transmit pin in the channel 4 (RLIN34) of the RLIN3.

Set the baud rate to 25Mbps, and enable the RLIN34 transmit completion interrupt request (INTRLIN34UR0) and the reception completion Interrupt request (INTRLIN34UR1).

In transmission operation, the first transmit data “0xAA” is stored to UART transmit data register (RLN34LUTDR) after enabling the transmit processing. The transmit data is transmitted from the RLIN34TX pin. Due to the measuring by the OS timer after the transmit data storing, the next transmit data is written to RLN34LUTDR register after 100ms passes or the transmit completion interrupt (INTRLIN34UR0) generation. After that, this transmission operation is repeated.

In the reception operation after enabling the reception operation, the data inputted from the RLIN34RX pin is stored to UART receive data register (RLN34LURDR). When the receive data is stored to RLN34LURDR, RLIN34 reception completion interrupt (INTRLIN34UR1) request is issued. The receive data is stored to the variable in this interrupt processing. After that, this reception operation is repeated.

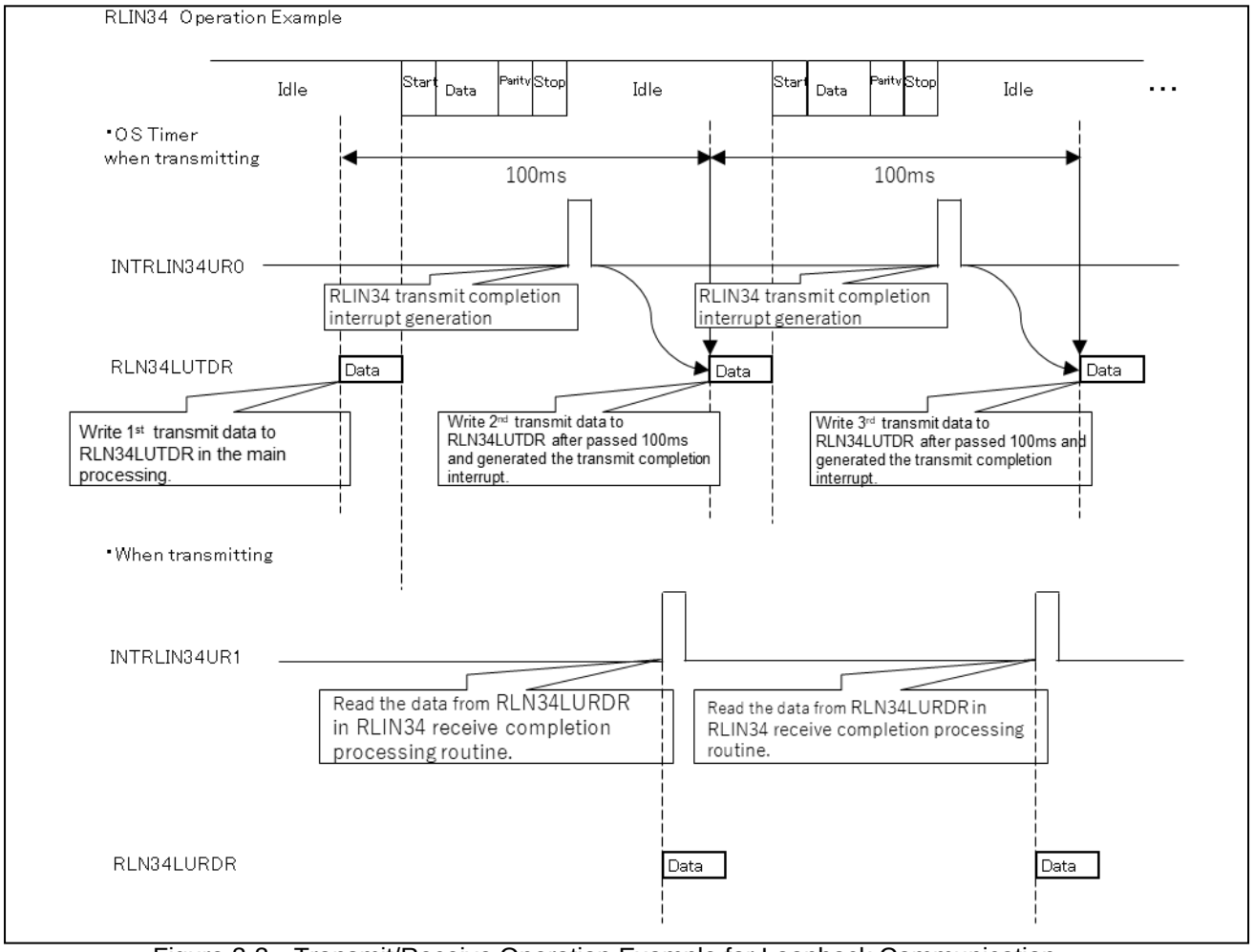

Figure 3-3 Transmit/Receive Operation Example for Loopback Communication

3.1.4 Software Explanation

- Module Explanation

The module list in this operation example is show below.

Table3-1 Module List

Module Name	Function Name	Function
Maine routine	main_pe0	Maine
RLIN3 Initialization routine	rlin3_init	Initialize RLIN3.
UART transmit processing routine	uart_sent	Perform transmit processing.
Interrupt function initialization routine	intc_init	Perform the initial setting of the interrupt function.
OSTM initialization routine	ostm_init	Initialize OSTM.
Transmit completion interrupt processing routine	eiint641	Set the transmit completion interrupt generation flag.
Receive completion interrupt processing routine	eiint642	Perform the receive processing.
Timer start	start_timer	Count 100ms in OS timer for prosecting wait.
Timer check	check_timer	Check 100ms passing from the timer starting.
Module standby release routine	standby_init	Release the standby of RLIN3 and OS Timer.
Port initialization routine	port_init	Perform the port setting.

- Register Setting

The register setting for each function in this operation example is shown below.

Table 3-2 RLIN3 Register Setting

Register Name	Setting value	Function
RLN34LWBR	0x74	Number of bit sampling selection: Select 8 sampling
		Prescaler frequency-division rate: 1/4
RLN34LBRP01	0x0000	UART baud rate prescaler 01 baud rate prescaler frequency-division rate: 1/(0+1)
RLN34LMD	0x01	Noize filter: Use
		LIN/UART mode selection: UART mode
RLN34LBFC	0x08	Output polarity switching: Transmit data normal output
		Input polarity switching: Receive data normal output
		Parity selection: Even parity
		Stop bit length selection: 1 bit
		Transfer format order selection: LSB first
		Character length selection: 8 bits communication
RLN34LSC	0x00	Inter byte space setting: 0T bit
RLN34LEDE	0x0C	Framing error detection: Enable
		Overrun error detection: Enable
		Bit error detection: Disable
RLN34LCUC	0x01	LIN reset: Release reset mode

Register Name	Setting value	Function
RLN34LUOR1	0x08	Extended bit comparison: Enable
		Transmit interrupt generation timing selection: Generate the transmit interrupt when completing transmission.
		Extended bit data comparison: Disable
		Extended bit detection level selection: Select extended bit value “0” to the extended bit detection level.
		Extended bit enable: Disable
RLN34LUTDR	0xAA	0xAA First transmit data: 0xAA
RLN34LUOER	0x03	Receive operation enabling
		Transmit operation enabling

Table 3-3 Interrupt Register Setting

Register Name	Setting Value	Function
EIBD641	0x00000000	Simultaneous notice interrupt enabling bit: Disable
		Simultaneous notice interrupt port number setting bit: Unnecessary
		Host/Guest partition selection bit: unnecessary to set since it incorporated to INTC1 virtualization configuration register (IHVCFG).
		Interrupt bind destination PEID: PE0 (CPU0)
EIC641	0x0040	Interrupt request flag: No interrupt request
		Interrupt mask bit: No mask
		Interrupt vector method: Table reference method
		Interrupt priority: 0 (highest)
EIBD642	0x00000000	Simultaneous notice interrupt enabling bit: Disable
		Simultaneous notice interrupt port number setting bit: Unnecessary
		Host/Guest partition selection bit: unnecessary to set since it incorporated to INTC1 virtualization configuration register (IHVCFG).
		Interrupt bind destination PEID: PE0 (CPU0)
EIC642	0x0040	Interrupt request flag: No interrupt request
		Interrupt mask bit: No mask
		Interrupt vector method: Table reference method
		Interrupt priority: 0 (highest)

Table 3-4 OS Timer Register Setting

Register Name	Setting Value	Function
OSTM0CMP	0x007A1200-1	Down counter start value: 100ms
OSTM0TS	0x01	Start counting.
OSTM0CTL	0x80	OSTM interrupt: Enable
		Count operation when starting the count: Load OSTM0CM to OSTM0CNT.
		Operation mode: Interval timer mode
		Interrupt when staring the count: Disable

Table 3-5 Standby Register Setting

Register Name	Setting Value	Function
MSRKCPROT	0xA5A5A501	Write protection of standby register: Release
	0xA5A5A500	Write protection of standby register: Enable
MSR_RLIN3	0xFFFFFFEF	RLIN34 standby releasing
MSR_OSTM	0xFFFFFFFE	OS Timer standby releasing

Table 3-6 Clock controller Register Setting

Register Name	Setting Value	Function
CLKKCPROT	0xA5A5A501	Write protection of clock controller: Release
	0xA5A5A500	Write protection of clock controller: Enable
CKS_RLINC	0x00000001	CLK_RLIN3 : CLKC_HSB

Table 3-7 Port Register Setting

Register Name	Setting Value	Function
PKCPROT	0xA5A5A501	Port write enable register (PWE): Release protection
	0xA5A5A500	Port write enable register (PWE): Enable protection
PWE	0x00000020	P12 register: Release protection
	0x00000000	P12 register: Enable protection
PCR12_5	0x03000057	Drive strength: high
		Port mode controller: Share mode
		Port mode: Input mode
		Port function controller: Share mode 8 (RLIN34RX)
PCR12_6	0x03000047	Drive strength: high
		Port output: Low level
		Port mode controller: Share mode
		Port mode: Output mode
		Port function controller: Share mode 8 (RLIN34RX)

- Operation Flow

The flowchart in this operation example is shown below.

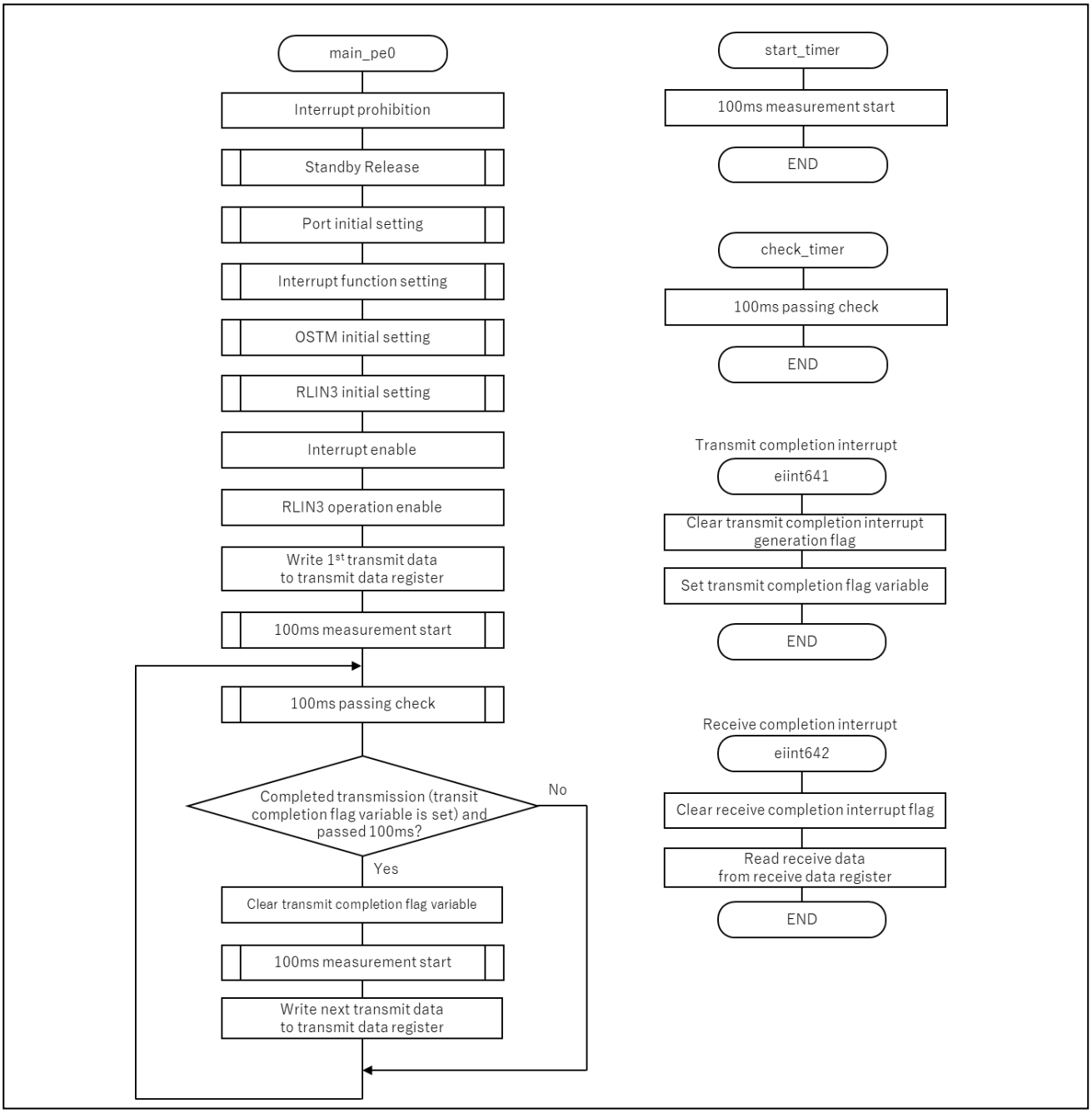

Figure 3-4 Flowchart

3.2 Transmit/Receive Operation by PC Connection

3.2.1 Specification Overview

Explains about the transmit/receive operation connecting with PC.

In this operation example, connect with PC and communicate with the terminal soft booted on PC.

In transmit/receive operation, the data transmission to PC is started to store the transmit data to UART transmit data register (RLN34LUTDR).

In transmit/receive operation, the data transmitted from the terminal soft is received, the RLIN34 transmit completion interrupt (INTRLIN34UR1) is issued.

In this operation example, the data received in the interrupt processing is read by UART receive data register (RLN34LURDR).

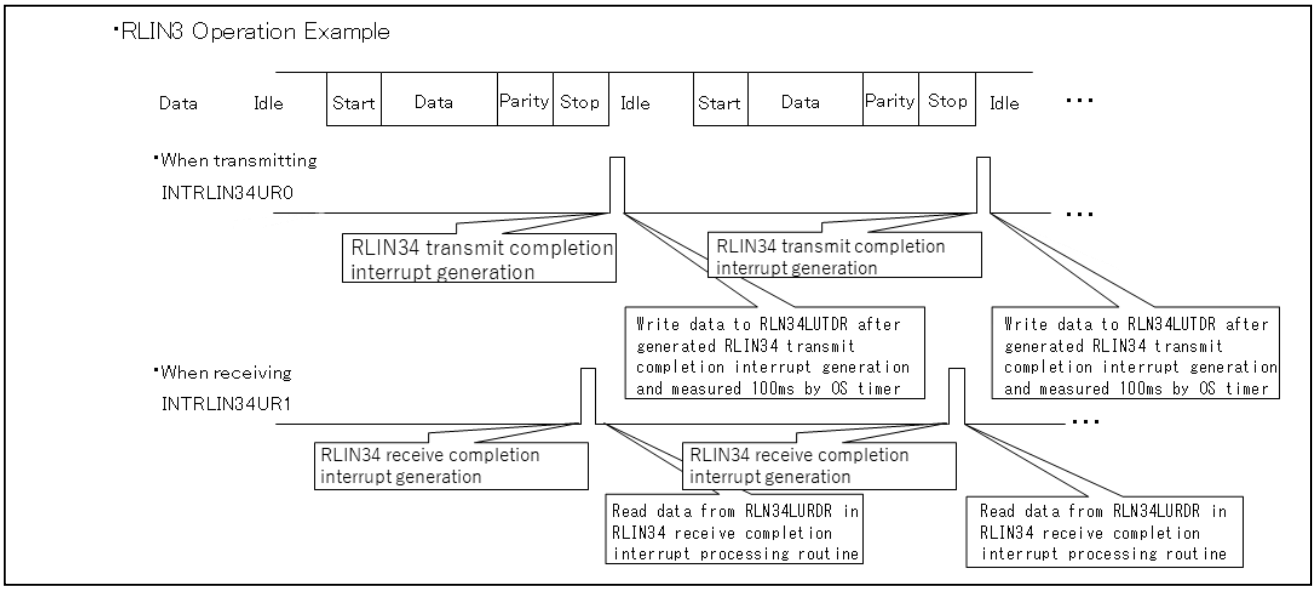

Figure 3-5 Transmit/Receive Operation for PC Connection

3.2.2 System Configuration

Figure 3-6 shows the system configuration.

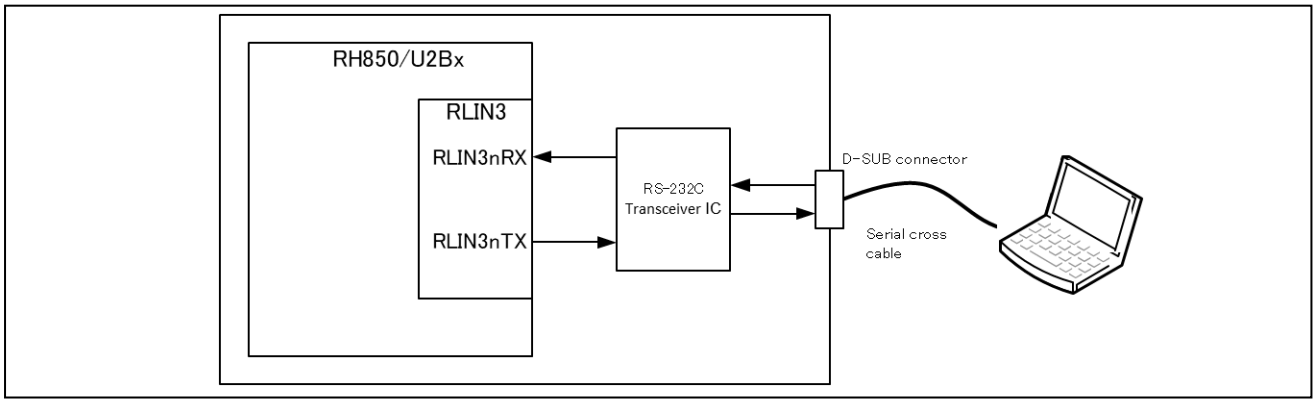

Figure 3-6 System Configuration

3.2.3 Explanation for Operation Example

In this operation example, connect the channel4 (RLIN34) of RLIN3 with PC, and perform the transmit/receive operation with the terminal soft on PC.

Set 38400bps to the baud rate, and enable RLIN34 transmit completion interrupt request and the receive completion interrupt request (INTRLIN34UR1).

In transmission operation, the first transmit data “0xAA” is stored to UART transmit data register (RLN34LUTDR) after enabling the transmit processing. The transmit data is transmitted from the RLIN34TX pin. Due to the measuring by the OS timer after the transmit data storing, the next transmit data is written to RLN34LUTDR register after 100ms passes or the transmit completion interrupt (INTRLIN34UR0) generation. After that, this transmission operation is repeated.

In the reception operation after enabling the reception operation, the data inputted from the RLIN34RX pin is stored to UART receive data register (RLN34LURDR). When the receive data is stored to RLN34LURDR, RLIN34 reception completion interrupt (INTRLIN34UR1) request is issued. The receive data is stored to the variable in this interrupt processing. After that, this reception operation is repeated.

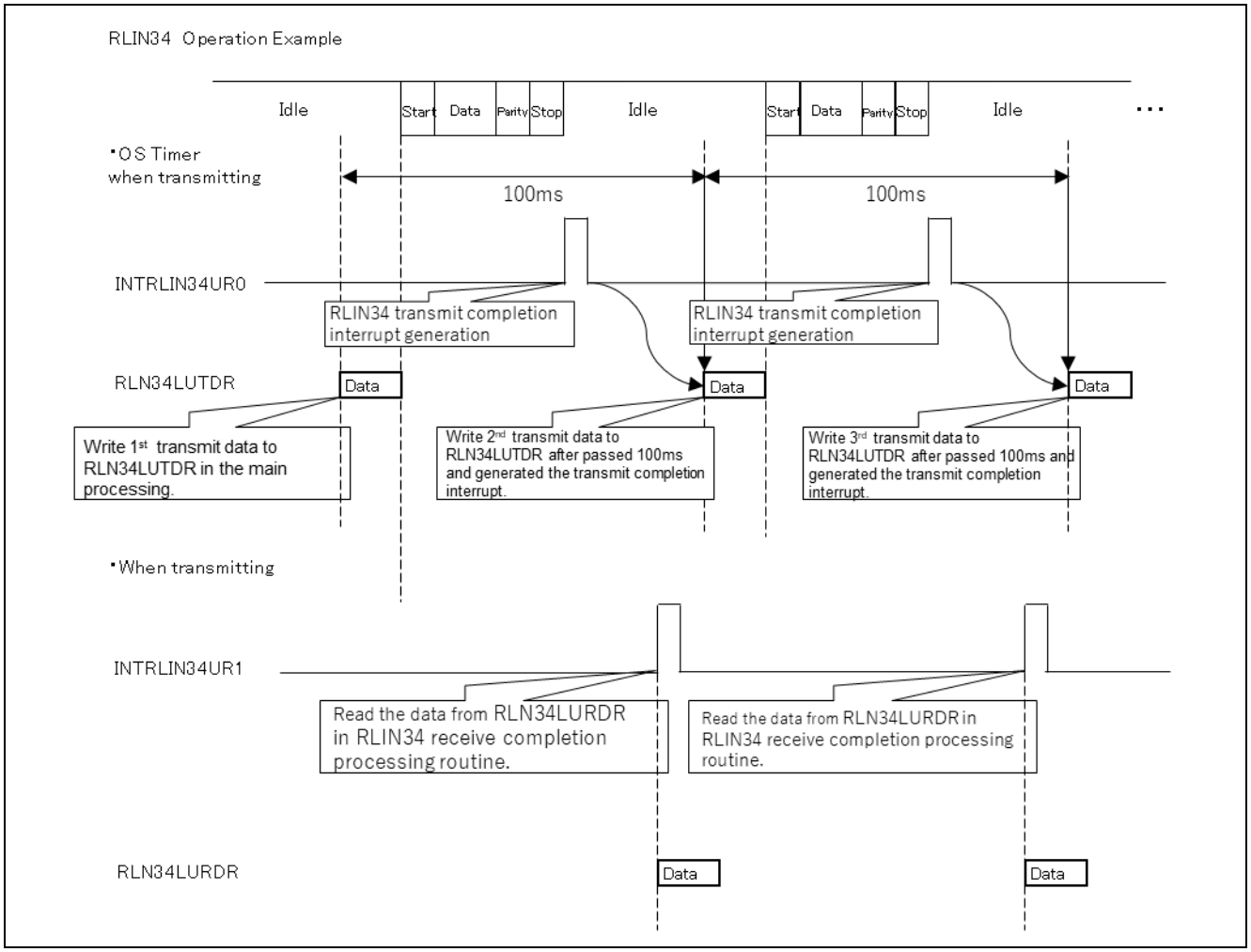

Figure 3-7 Transmit/Receive Operation Example for PC Connection

3.2.4 Software Explanation

- Module Explanation

The module list in this operation example is show below.

Table 3-8 Module List

Module Name	Function Name	Function
Maine routine	main_pe0	Maine
RLIN3 Initialization routine	rlin3_init	Initialize RLIN3.
UART transmit processing routine	uart_sent	Perform transmit processing.
Interrupt function initialization routine	intc_init	Perform the initial setting of the interrupt function.
OSTM initialization routine	ostm_init	Initialize OSTM.
Transmit completion interrupt processing routine	eiint641	Set the transmit completion interrupt generation flag.
Receive completion interrupt processing routine	eiint642	Perform the receive processing.
Timer start	start_timer	Count 100ms in OS timer for prosecting wait.
Timer check	check_timer	Check 100ms passing from the timer starting.
Module standby release routine	standby_init	Release the standby of RLIN3 and OS Timer.
Port initialization routine	port_init	Perform the port setting.

- Register Setting

The register setting for each function in this operation example is shown below.

Table 3-9 RLIN3 Register

Register Name	Setting value	Function
RLN34LWBR	0x74	Number of bit sampling selection: Select 8 sampling
		Prescaler frequency-division rate: 1/4
RLN34LBRP01	0x0040	UART baud rate prescaler 01 baud rate prescaler frequency-division rate: 1/(64+1)
RLN34LMD	0x01	Noize filter: Use
		LIN/UART mode selection: UART mode
RLN34LBFC	0x08	Output polarity switching: Transmit data normal output
		Input polarity switching: Receive data normal output
		Parity selection: Even parity
		Stop bit length selection: 1 bit
		Transfer format order selection: LSB first
		Character length selection: 8 bits communication
RLN34LSC	0x00	Inter byte space setting: 0T bit
RLN34LEDE	0x0C	Framing error detection: Enable
		Overrun error detection: Enable
		Bit error detection: Disable
RLN34LCUC	0x01	LIN reset: Release reset mode
RLN34LUOR1	0x08	Extended bit comparison: Enable

		Transmit interrupt generation timing selection: Generate the transmit interrupt when completing transmission.
		Extended bit data comparison: Disable
		Extended bit detection level selection: Select extended bit value “0” to the extended bit detection level.
		Extended bit enable: Disable
RLN34LUTDR	0x41	First transmit data: 0x41
RLN34LUOER	0x03	Receive operation enabling
		Transmit operation enabling

Table 3-10 Interrupt Register Setting

Register Name	Setting Value	Function
EIBD641	0x00000000	Simultaneous notice interrupt enabling bit: Disable
		Simultaneous notice interrupt port number setting bit: Unnecessary
		Host/Guest partition selection bit: unnecessary to set since it incorporated to INTC1 virtualization configuration register (IHVCFG).
		Interrupt bind destination PEID: PE0 (CPU0)
EIC641	0x0040	Interrupt request flag: No interrupt request
		Interrupt mask bit: No mask
		Interrupt vector method: Table reference method
		Interrupt priority: 0 (highest)
EIBD642	0x00000000	Simultaneous notice interrupt enabling bit: Disable
		Simultaneous notice interrupt port number setting bit: Unnecessary
		Host/Guest partition selection bit: unnecessary to set since it incorporated to INTC1 virtualization configuration register (IHVCFG).
		Interrupt bind destination PEID: PE0 (CPU0)
EIC642	0x0040	Interrupt request flag: No interrupt request
		Interrupt mask bit: No mask
		Interrupt vector method: Table reference method
		Interrupt priority: 0 (highest)

Table 3-11 OS Timer Register Setting

Register Name	Setting Value	Function
OSTM0CMP	0x007A1200-1	Down counter start value: 100ms
OSTM0TS	0x01	Start counting.
OSTM0CTL	0x80	OSTM interrupt: Enable
		Count operation when starting the count: Load OSTM0CM to OSTM0CNT.
		Operation mode: Interval timer mode
		Interrupt when staring the count: Disable

Table 3-12 Standby Register Setting

Register Name	Setting Value	Function
MSRKCPROT	0xA5A5A501	Write protection of standby register: Release

	0xA5A5A500	Write protection of standby register: Enable
MSR_RLIN3	0xFFFFFFEF	RLIN34 standby releasing
MSR_OSTM	0xFFFFFFFE	OS Timer standby releasing

Table 3-13 Clock controller Register Setting

Register Name	Setting Value	Function
CLKKCPROT	0xA5A5A501	Write protection of clock controller: Release
	0xA5A5A500	Write protection of clock controller: Enable
CKS_RLINC	0x00000001	CLK_RLIN3 : CLKC_HSB

Table 3-14 Port Register Setting

Register Name	Setting Value	Function
PKCPROT	0xA5A5A501	Port write enable register (PWE): Release protection
	0xA5A5A500	Port write enable register (PWE): Enable protection
PWE	0x00000020	P12 register: Release protection
	0x00000000	P12 register: Enable protection
PCR12_5	0x03000057	Drive strength: high
		Port mode controller: Share mode
		Port mode: Input mode
		Port function controller: Share mode 8 (RLIN34RX)
PCR12_6	0x03000047	Drive strength: high
		Port output: Low level
		Port mode controller: Share mode
		Port mode: Output mode
		Port function controller: Share mode 8 (RLIN34RX)

- Operation Flow

The flowchart in this operation example is shown below.

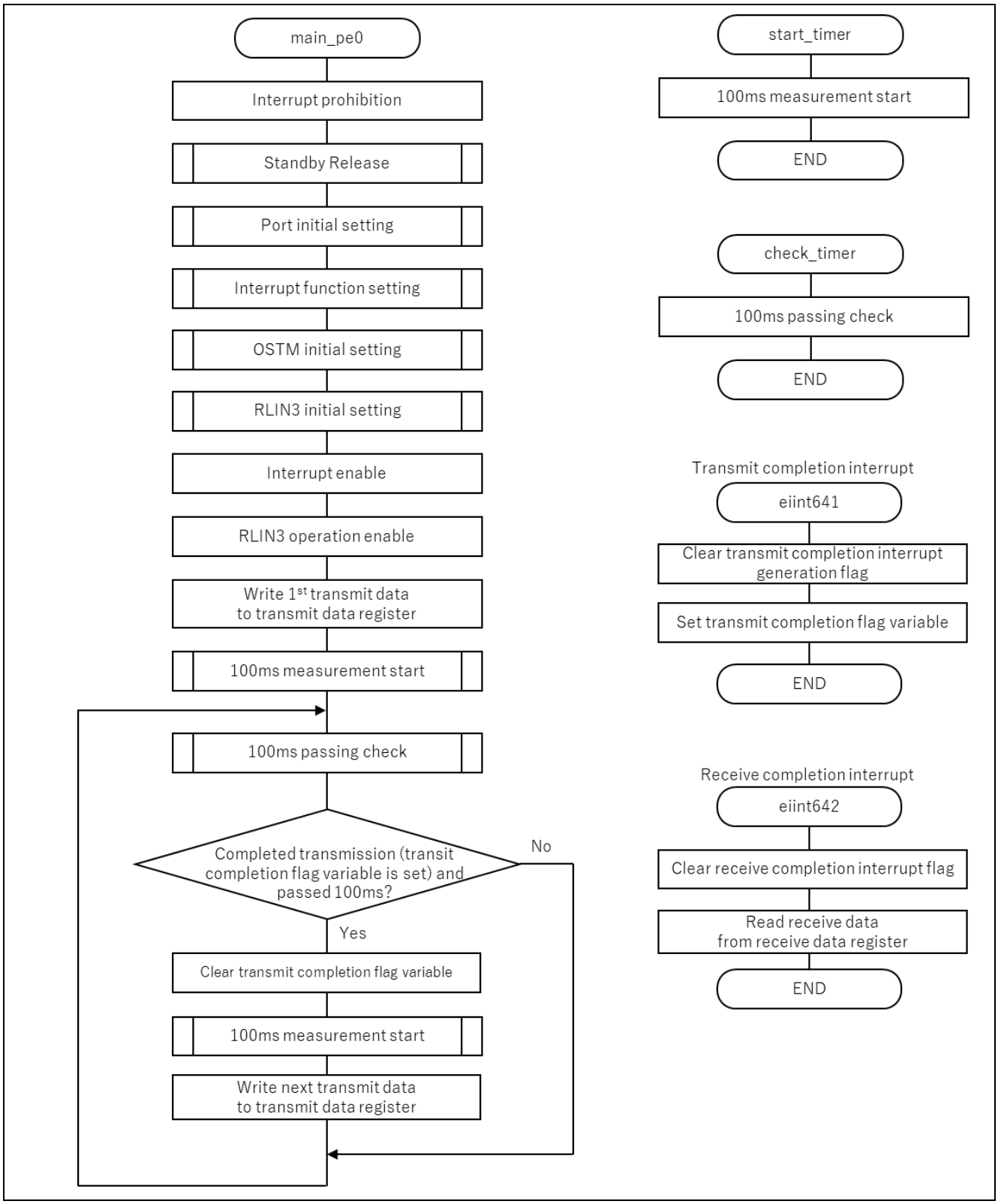

Figure 3-8 Flowchart

3.3 Receive Operation using DMA

3.3.1 Specification Overview

Explain the method for performing the receive operation using DMA (sDMAC).

Connect with PC, and perform the communication with the terminal soft booted on PC.

When the transmit data is received from the terminal soft, the RLIN 34 receive completion interrupt (INTRLIN34UR1) is generated, boot sDMAC due to the interrupt, read the UART receive data register (RLN34LURDR) set to the transmit source, and store the data to the variable of the transmit destination.

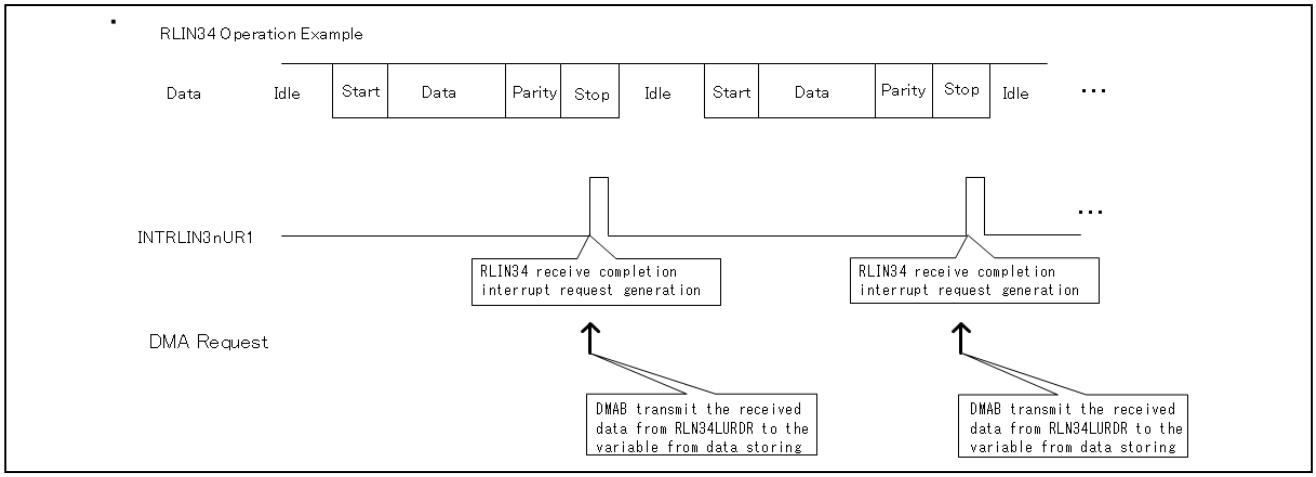

Figure 3-9 Receive Operation using DMA

3.3.2 System Configuration

Figure 3-10 shows the system configuration.

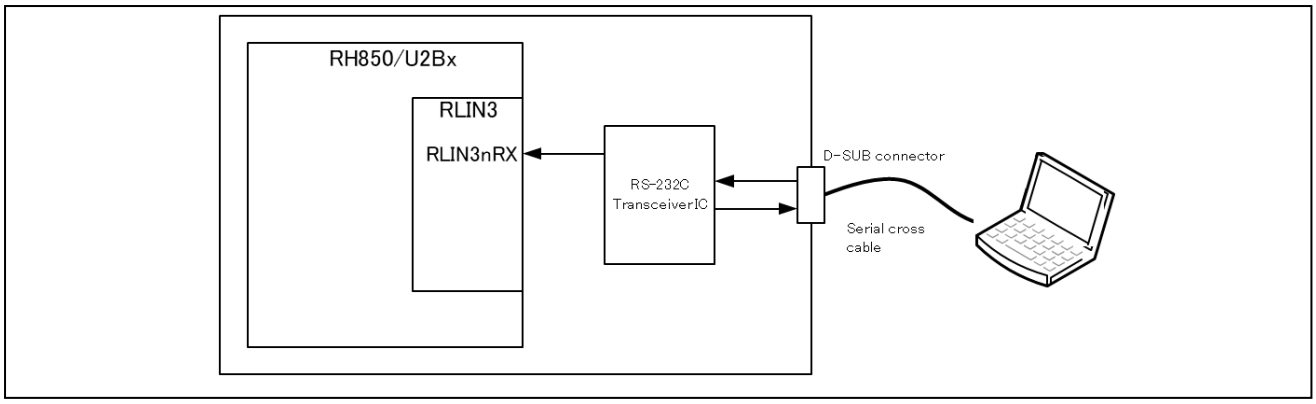

Figure 3-10 System Configuration

3.3.3 Explanation for Operation Example

In this operation example, connect the channel4 (RLIN34) of RLIN3 with PC, and perform the receive operation using sDMAC.

Set 38400bps to the baud rate, and enable the receive completion interrupt request (INTRLIN34UR1).

Connect with PC, and transmit the continuous data ”ABCDEFGH” (0x4142434445464748) from the terminal soft.

For sDMAC, set the UART receive data register (RLN34LURDR) to the transmit source, and the variable storing the receive data to the transmit source. The start trigger of sDMAC is the RLIN34 receive completion interrupt (group 0-183).

This start up the sDMAC when it receives data, the receive data can be stored to the variable. The clearing of the transmit completion flag, the receive data, etc. is reset by the sDMAC transmit completion interrupt. After that, this reception operation is repeated.

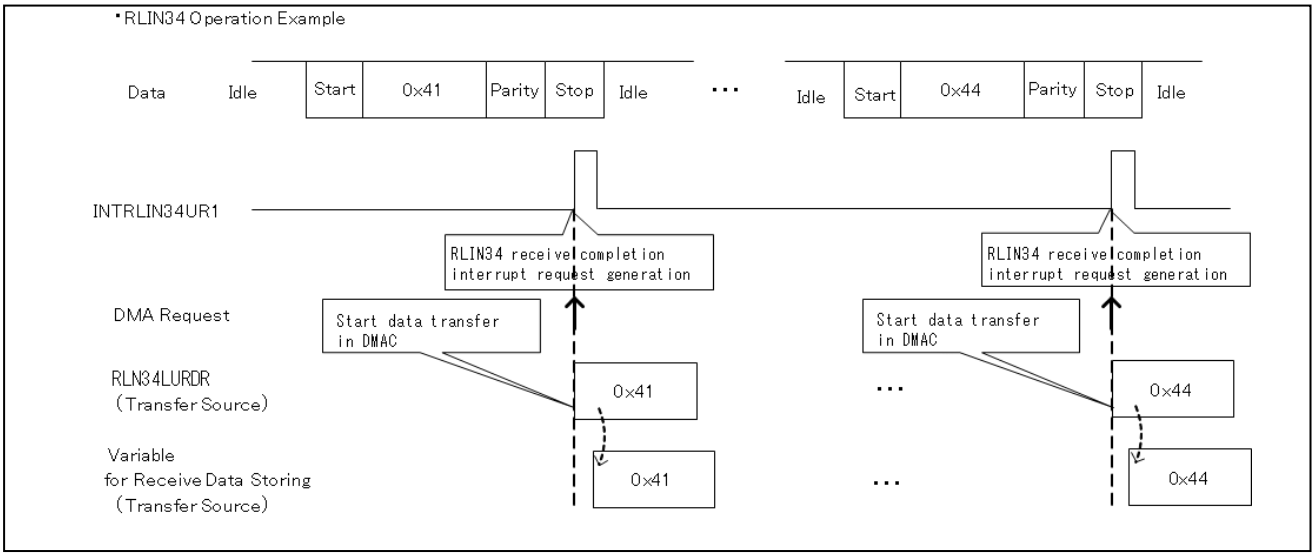

Figure 3-11 Receive Operation Example using sDMAC

3.3.4 Software Explanation

- Module Explanation

The module list in this operation example is show below.

Table 3-15 Module List

Module Name	Function Name	Function
Maine routine	main_pe0	Maine
RLIN3 initialization routine	rlin3_init	Perform the initialization of RLIN3.
sDMAC initialization routine	sdmac_init	Preform the initialization of sDMAC.
sDMAC0 transmission completion interrupt processing routine	eiint70	Perform the rest of sDMAC.
Interrupt function initialization routine	intc_init	Perform the initial setting of the interrupt function.
Receive completion interrupt processing routine	eiint642	Perform the receive processing.
Module standby release routine	standby_init	Release the standby of RLIN3.
Port initialization routine	port_init	Perform the port setting.

- Register Setting

The register setting of each function in this operation example is show below

Table 3-16 RLIN3 Register Setting

Register Name	Setting Value	Function
RLN34LWBR	0x74	UART baud rate prescaler 01 baud rate prescaler frequency-division rate: 1/(0+1)
		Noize filter: Use
RLN34LBRP01	0x0040	LIN/UART mode selection: UART mode
RLN34LMD	0x01	Output polarity switching: Transmit data normal output
		Input polarity switching: Receive data normal output
RLN34LBFC	0x08	Parity selection: Even parity
		Stop bit length selection: 1 bit
		Transfer format order selection: LSB first
		Character length selection: 8 bits communication
		Inter byte space setting: 0T bit
		Framing error detection: Enable
RLN34LSC	0x00	Overrun error detection: Enable
RLN34LEDE	0x0C	Bit error detection: Disable
		LIN reset: Release reset mode
		UART baud rate prescaler 01 baud rate prescaler frequency-division rate: 1/(0+1)
RLN34LCUC	0x01	Noize filter: Use
RLN34LUOR1	0x08	Extended bit comparison: Enable
		Extended bit data comparison: Disable
		Extended bit detection level selection: Select extended bit value

		“0” to the extended bit detection level.
		Extended bit enable: Disable
RLN34LUOER	0x03	Receive operation enabling

Table 3-17 sDMAC Register Setting

Register Name	Setting Value	Function
DMA0CM_0	0x00001C00	Channel master SPID setting SPID=0x1C (Setting Value)
		Supervisor Mode
DMA0SAR_0	0xFFC7C426	RLN34LURDR register address
DMA0DAR_0	Address of read_receive variable	Transmission destination address
DMA0TSR_0	0x00000008	Transfer size: 8 bytes
DMA0TMR_0	0x00001400	DMA transfer request selection interrupt: Hardware DMA transfer request
		Destination address count direction: Increment
		Source address count direction: fixed
		DMA destination transaction size: 1 byte
		DMA source transaction size: 1 byte
DMA0RS_0	0x000100B7	Transmission times of every hardware request: 1 time
		Hardware DMA transmission source selection: group 0-183
		(RLIN34 reception completion interrupt)
DMA0OR	0x0001	Transmission enable
DMA0CHCR_0	0x0003	Transfer completion interrupt enable
		Channel operation enable

Table 3-18 Interrupt Register Setting

Register Name	Setting Value	Function
EIBD642	0x00000000	Simultaneous notice interrupt enabling bit: Disable
		Simultaneous notice interrupt port number setting bit: Unnecessary
		Host/Guest partition selection bit: unnecessary to set since it incorporated to INTC1 virtualization configuration register (IHVCFG).
		Interrupt bind destination PEID: PE0 (CPU0)
EIC642	0x0040	Interrupt request flag: No interrupt request
		Interrupt mask bit: No mask
		Interrupt vector method: Table reference method
		Interrupt priority: 0 (highest)
EIBD70	0x00000000	Simultaneous notice interrupt enabling bit: Disable
		Simultaneous notice interrupt port number setting bit: Unnecessary
		Host/Guest partition selection bit: unnecessary to set since it incorporated to INTC1 virtualization configuration register (IHVCFG).
		Interrupt bind destination PEID: PE0 (CPU0)

EIC70	0x0040	Interrupt request flag: No interrupt request
		Interrupt mask bit: No mask
		Interrupt vector method: Table reference method
		Interrupt priority: 0 (highest)

Table 3-19 Standby Register Setting

Register Name	Setting Value	Function
MSRKCPROT	0xA5A5A501	Write protection of standby register: Release
	0xA5A5A500	Write protection of standby register: Enable
MSR_RLIN3	0xFFFFFFEF	RLIN34 standby releasing

Table 3-20 Clock controller Register Setting

Register Name	Setting Value	Function
CLKKCPROT	0xA5A5A501	Write protection of clock controller: Release
	0xA5A5A500	Write protection of clock controller: Enable
CKS_RLINC	0x00000001	CLK_RLIN3 : CLKC_HSB

Table 3-21 Port Register Setting

Register Name	Setting Value	Function
PKCPROT	0xA5A5A501	Port write enable register (PWE): Release protection
	0xA5A5A500	Port write enable register (PWE): Enable protection
PWE	0x00000020	P12 register: Release protection
	0x00000000	P12 register: Enable protection
PCR12_5	0x03000057	Drive strength: high
		Port mode controller: Share mode
		Port mode: Input mode
		Port function controller: Share mode 8 (RLIN34RX)
PCR12_6	0x03000047	Drive strength: high
		Port output: Low level
		Port mode controller: Share mode
		Port mode: Output mode
		Port function controller: Share mode 8 (RLIN34RX)

- Operation Flow

The flowchart in this operation example is shown below.

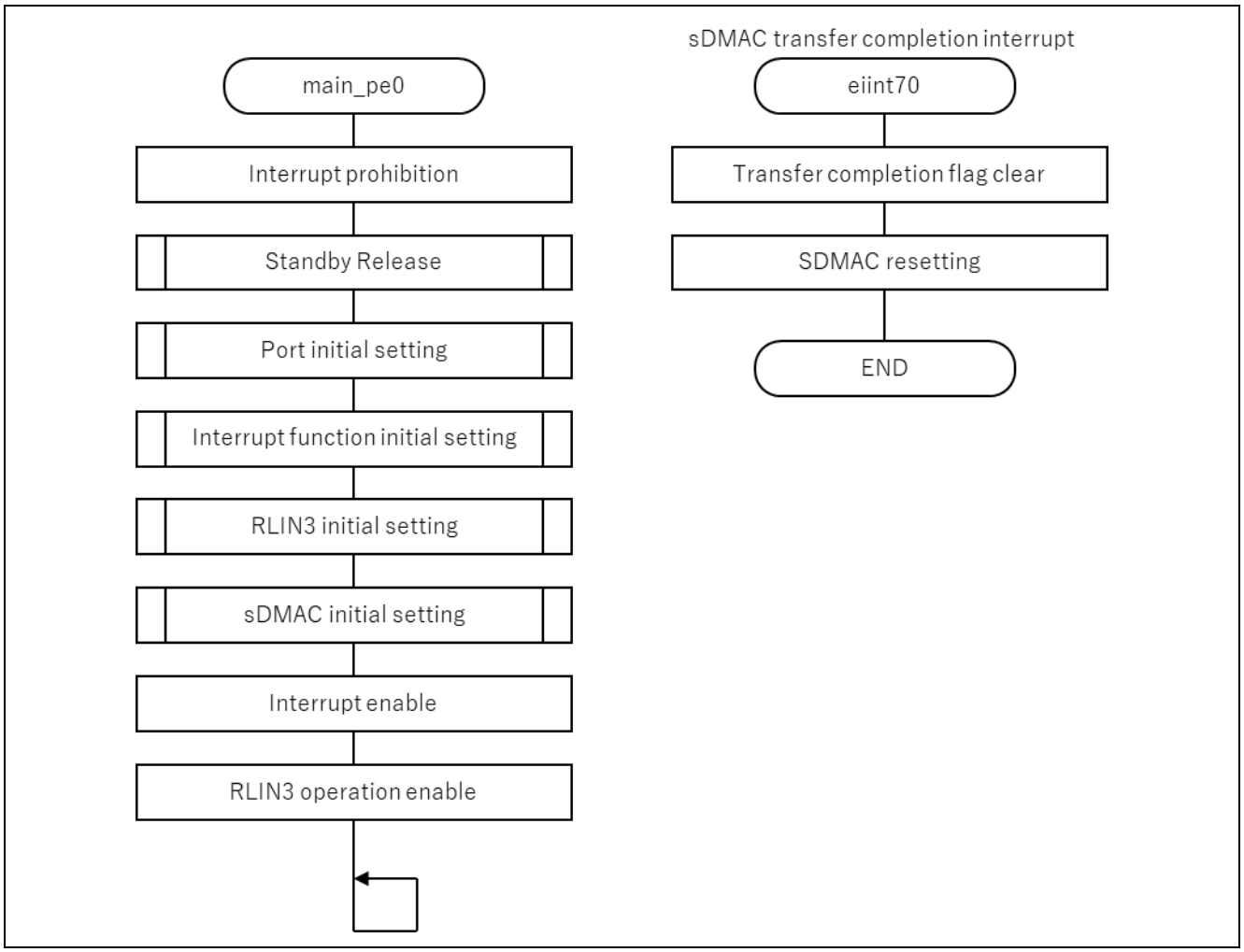

Figure 3-12 Flowchart

3.4 Transmit Operation using DMA

3.4.1 Specification Overview

Explains about the method for performing the transmit operation using DMA (sDMAC).

This operation example is the operation that the transmit data write of "3.1 Loopback Communication" is changed to DMA transmission.

3.4.2 System Configuration

Figure 3-13 shows the system configuration.

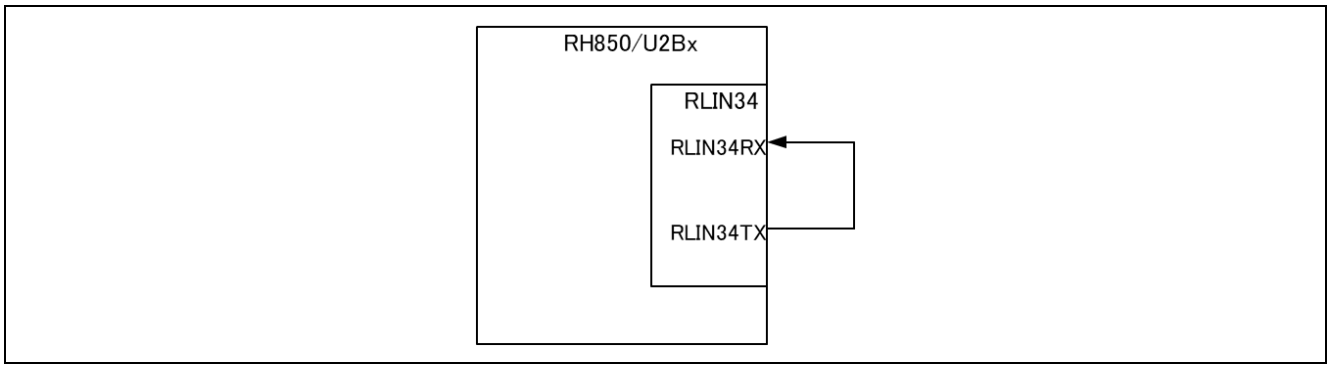

Figure 3-13 System Configuration Diagram

3.4.3 Explanation of Operation Example

In this operation example, perform the loopback communication connected the receive pin with the transmit pin in the channel 4 (RLIN34) of the RLIN3.

Set the baud rate to 25Mbps, and enable the RLIN34 transmit completion interrupt request (INTRLIN34UR0) and the reception completion Interrupt request (INTRLIN34UR1).

OS timer is used in interval timer mode for 100ms measurement, and the measurement start interrupt (OSTM0TINT) is generated in every 100ms.

For sDMAC, the OS timer measurement start interrupt request is set to the start trigger.

The transmit operation stores the UART transmit data register (RLN34LUTDR) to the transmit data “0xAA”. The transmit data is transmitted by the RLIN34TX pin. DMA is booted by OS timer measurement start interrupt (OSTM0TINT) request, and the next transmit data is transferred to the UART transmit data register (RLN34LUTDR).

The transmit operation is same with “3.1 Loopback Communication”.

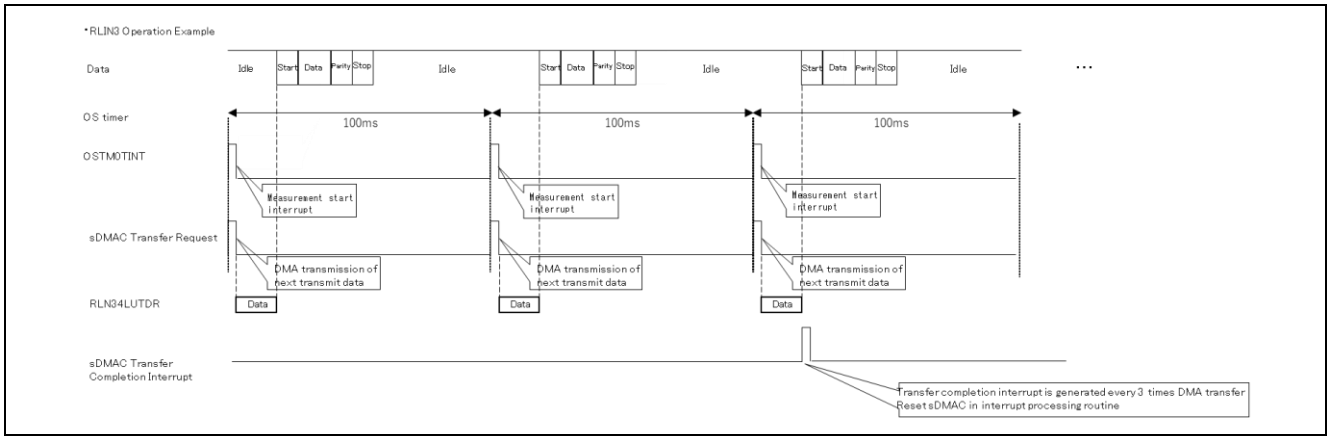

Figure 3-14 Transmit Operation Example using sDMAC.

3.4.4 Software Explanation

- Module Explanation

The module list in this operation example is show below.

Table 3-22 Module List

Module Name	Function Name	Function
Maine routine	main_pe0	Maine
RLIN3 Initialization routine	rlin3_init	Initialize RLIN3.
UART transmit processing routine	uart_sent	Perform transmit processing.
sDMAC initialization routine	sdmac_init	Perform the initialization of sDMAC.
sDMAC0 channel 0 transmit completion interrupt processing routine	eiint70	Permorn the restarts of sDMAC.
Interrupt function initialization routine	intc_init	Perform the initial setting of the interrupt function.
OSTM initialization routine	ostm_init	Initialize OSTM.
Receive completion interrupt processing routine	eiint642	Perform the reception processing.
Timer start	start_timer	Count 100ms in OS timer for prosecting wait.
Timer check	check_timer	Check 100ms passing from the timer starting.
Module standby release routine	standby_init	Release the standby of RLIN3 and OS Timer.
Port initialization routine	port_init	Perform the port setting.

- Register Setting

The register setting for each function in this operation example is shown below.

Table 3-23 RLIN3 Register Setting

Register Name	Setting value	Function
RLN34LWBR	0x74	Number of bit sampling selection: Select 8 sampling
		Prescaler frequency-division rate: 1/4
RLN34LBRP01	0x0000	UART baud rate prescaler 01 baud rate prescaler frequency-division rate: 1/(0+1)
RLN34LMD	0x01	Noize filter: Use
		LIN/UART mode selection: UART mode
RLN34LBFC	0x08	Output polarity switching: Transmit data normal output
		Input polarity switching: Receive data normal output
		Parity selection: Even parity
		Stop bit length selection: 1 bit
		Transfer format order selection: LSB first
		Character length selection: 8 bits communication
RLN34LSC	0x00	Inter byte space setting: 0T bit
RLN34LEDE	0x0C	Framing error detection: Enable
		Overrun error detection: Enable
		Bit error detection: Disable
RLN34LCUC	0x01	LIN reset: Release reset mode
RLN34LUOR1	0x08	Extended bit comparison: Enable

		Transmit interrupt generation timing selection: Generate the transmit interrupt when completing transmission.
		Extended bit data comparison: Disable
		Extended bit detection level selection: Select extended bit value “0” to the extended bit detection level.
		Extended bit enable: Disable
RLN34LUTDR	0xAA	0xAA First transmit data: 0xAA
RLN34LUOER	0x03	Receive operation enabling
		Transmit operation enabling

Table 3-24 sDMAC Register Setting

Register Name	Setting Value	Function
PBGKCPROT	0xA5A5A501	Keycode register Write protection release
	0xA5A5A500	Keycode register Write protection enable
PBG.51PBGPROT0_13.BIT.GEN	1	Protection enable
PBG.51PBGPROT0_13.BIT.DBG	1	R/W enable of debug master
PBG.51PBGPROT0_13.BIT.UM	0	R/W disable of user mode
PBG.51PBGPROT0_13.BIT.WG	0	Use writing PBGPROT as the judgement condition.
PBG.51PBGPROT0_13.BIT.RG	1	Not use writing PBGPROT as the judgement condition.
PBGPROT1_13	0x10000001	SPID28(sDMAC0)
		SPID0(CPU0)
DMA0CM_0	0x00001C00	Channel master SPID setting SPID=0x1C (Setting Value)
		Supervisor Mode
DMA0SAR_0	Address of transmit_data	Transmission source address
DMA0DAR_0	0xFFC7C424	RLN34LUTDR register address
DMA0TSR_0	0x00000003	Transfer size: 3 bytes
DMA0TMR_0	0x00001400	DMA transfer request selection interrupt: Hardware DMA transfer request
		Destination address count direction: Increment
		Source address count direction: fixed
		DMA destination transaction size: 1 byte
		DMA source transaction size: 1 byte
DMA0RS_0	0x0001008A	Transmission times of every hardware request: 1 time
		Hardware DMA transmission source selection: group 0-138
		(OSTM measurement start interrupt)
DMA0OR	0x0001	Transmission enable
DMA0CHCR_0	0x0003	Transfer completion interrupt enable
		Channel operation enable

Table 3-25 Interrupt Register Setting

Register Name	Setting Value	Function
EIBD641	0x00000000	Simultaneous notice interrupt enabling bit: Disable
		Simultaneous notice interrupt port number setting bit: Unnecessary
		Host/Guest partition selection bit: unnecessary to set since it incorporated to INTC1 virtualization configuration register (IHVCFG).
		Interrupt bind destination PEID: PE0 (CPU0)
EIC641	0x0040	Interrupt request flag: No interrupt request
		Interrupt mask bit: No mask
		Interrupt vector method: Table reference method
		Interrupt priority: 0 (highest)
EIBD642	0x00000000	Simultaneous notice interrupt enabling bit: Disable
		Simultaneous notice interrupt port number setting bit: Unnecessary
		Host/Guest partition selection bit: unnecessary to set since it incorporated to INTC1 virtualization configuration register (IHVCFG).
		Interrupt bind destination PEID: PE0 (CPU0)
EIC642	0x0040	Interrupt request flag: No interrupt request
		Interrupt mask bit: No mask
		Interrupt vector method: Table reference method
		Interrupt priority: 0 (highest)
EIBD70	0x00000000	Simultaneous notice interrupt enabling bit: Disable
		Simultaneous notice interrupt port number setting bit: Unnecessary
		Host/Guest partition selection bit: unnecessary to set since it incorporated to INTC1 virtualization configuration register (IHVCFG).
		Interrupt bind destination PEID: PE0 (CPU0)
EIC70	0x0040	Interrupt request flag: No interrupt request
		Interrupt mask bit: No mask
		Interrupt vector method: Table reference method
		Interrupt priority: 0 (highest)
EIBD360	0x00000000	Simultaneous notice interrupt enabling bit: Disable
		Simultaneous notice interrupt port number setting bit: Unnecessary
		Host/Guest partition selection bit: unnecessary to set since it incorporated to INTC1 virtualization configuration register (IHVCFG).
		Interrupt bind destination PEID: PE0 (CPU0)
EIC360	0x0040	Interrupt request flag: No interrupt request
		Interrupt mask bit: No mask
		Interrupt vector method: Table reference method
		Interrupt priority: 0 (highest)

Table 3-26 OS Timer Register Setting

Register Name	Setting Value	Function
OSTM0CMP	0x007A1200-1	Down counter start value: 100ms
OSTM0TS	0x01	Start counting.
OSTM0CTL	0x81	OSTM interrupt: Enable
		Count operation when starting the count: Load OSTM0CMP to OSTM0CNT.

		Operation mode: Interval timer mode
		Interrupt when starting the count: Enable

Table 3-27 Standby Register Setting

Register Name	Setting Value	Function
MSRKCPROT	0xA5A5A501	Write protection of standby register: Release
	0xA5A5A500	Write protection of standby register: Enable
MSR_RLIN3	0xFFFFFFEF	RLIN34 standby releasing
MSR_OSTM	0xFFFFFFFE	Release OS Timer standby

Table 3-28 Clock Controller Register Setting

Register Name	Setting Value	Function
CLKKCPROT	0xA5A5A501	Write protection of clock controller: Release
	0xA5A5A500	Write protection of clock controller: Enable
CKS_RLINC	0x00000001	CLK_RLIN3 : CLKC_HSB

Table 3-29 Port Register Setting

Register Name	Setting Value	Function
PKCPROT	0xA5A5A501	Port write enable register (PWE): Release protection
	0xA5A5A500	Port write enable register (PWE): Enable protection
PWE	0x00000020	P12 register: Release protection
	0x00000000	P12 register: Enable protection
PCR12_5	0x03000057	Drive strength: high
		Port mode controller: Share mode
		Port mode: Input mode
		Port function controller: Share mode 8 (RLIN34RX)
PCR12_6	0x03000047	Drive strength: high
		Port output: Low level
		Port mode controller: Share mode
		Port mode: Output mode
		Port function controller: Share mode 8 (RLIN34RX)

- Operation Flow

The flowchart in this operation example is shown below.

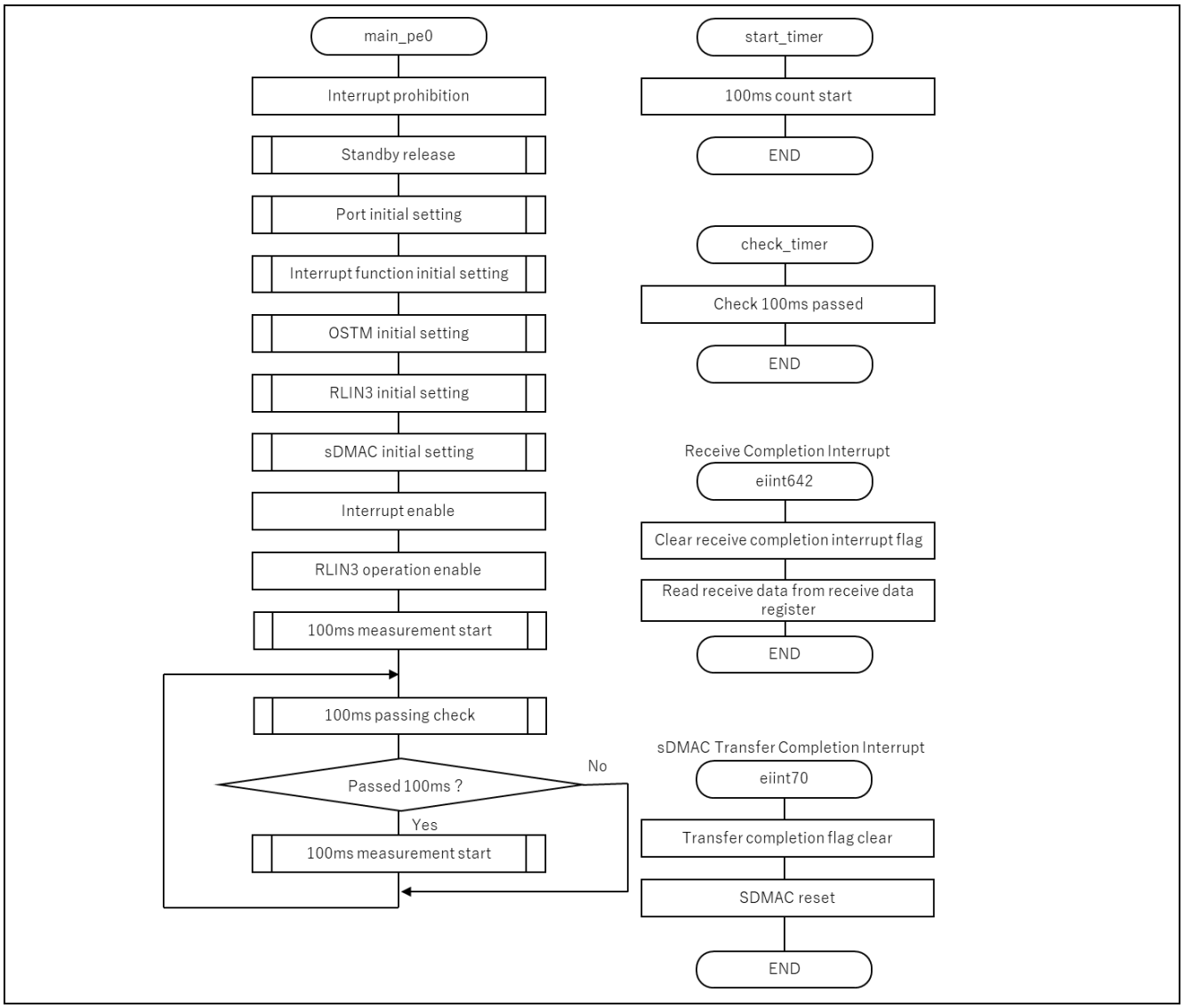

Figure 3-15 Flowchart

Revision History

Rev.	Date	Description	
		Page	Description
1.00	2022.12.7	-	Initial edition
1.10	2024.2.22	1	Target Integrated Development Environment and Reference Document is changed

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

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   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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