RH850/U2Bx

Motor Control Timer (TSG3)

Introduction

This application note describes examples of operation using the motor control timer (TSG3) of RH850/U2B6.

Examples of tasks and applications described in this application note have been verified. However, before using this motor control timer, be sure to check operating environment.

Target Device

This application note applies to RH850/U2B6.

Contents

1. Introduction

This application note describes how to use the motor control timer (TSG3) of RH850/U2B6.

1.1 Feature Used

RH850/U2B6 hardware features used in this application note are listed below.

- Motor control timer (TSG3)
- A/D converter (ADCK)
- Peripheral interconnection 2 (PIC2)

2. Example of Operation

2.1 HT-PWM Mode

2.1.1 Overview of Specifications

In this operation example, HT-PWM mode of TSG3 is used to output complementary 3-phase PWM.

In this operation example, the carrier cycle is set to 125 μs (8 kHz), the dead time is set to 2.5 μs, and the duty is updated by the INTTSG30IVLY interrupt (valley interrupt).

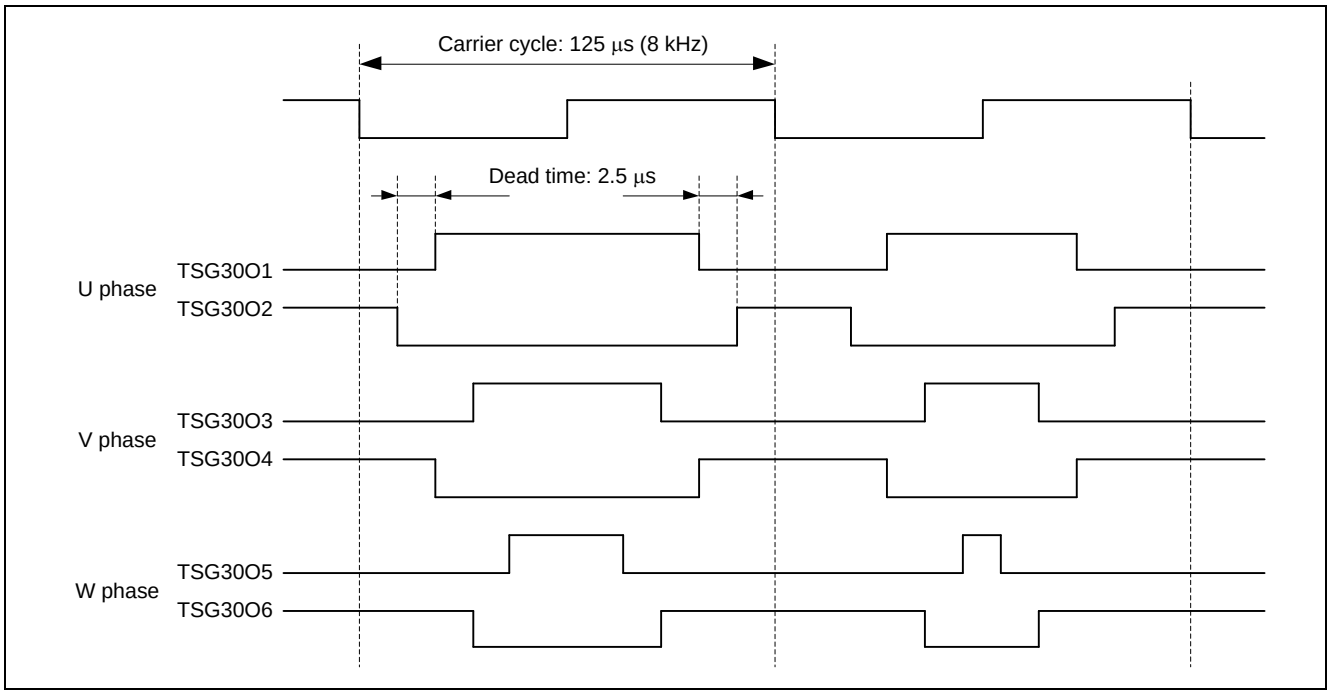


Figure 2-1 Schematic

2.1.2 Operating Conditions of Features Used

Operating conditions of features used in this operation example are shown below.

Table 2-1 Port Settings

Item	Description
Ports to be used	P2_5: TSG30O1 P2_6: TSG30O2 P2_7: TSG30O3 P2_8: TSG30O4 P2_9: TSG30O5 P2_10: TSG30O6

Table 2-2 TSG3 Settings

Item	Description
Clock supplied to TSG3	CLKC_HSB (unmodulated high-speed peripheral clock): 80 MHz
Feature to be used	HT-PWM mode
Carrier cycle	125 μs (8 kHz)
Dead time	2.5 μs
Compare register transfer timing	Reload mode (simultaneous rewrite mode)
Reload timing	Enables reload operation at the valley timing.
Interrupt	Enables generation of a valley interrupt.
Skipping rate	1/32

Table 2-3 Interrupt Feature Settings

Item	Description
TSG30 valley interrupt (INTTSG30IVLY)	Table reference method, Priority 15

2.1.3 Operation

In this operation example, an INTTSG30IVLY interrupt (valley interrupt) is enabled and reload operation at the valley timing is enabled. The complementary 3-phase PWM output duty is updated by the INTTSG30IVLY interrupt. The updated value is transferred to the compare registers (TSG30CMP1E to TSG30CMP6E) at the next reload timing and the complementary 3-phase PWM output duty changes. In this operation example, the INTTSG30IVLY interrupt and reload skipping rate is set to 1/32.

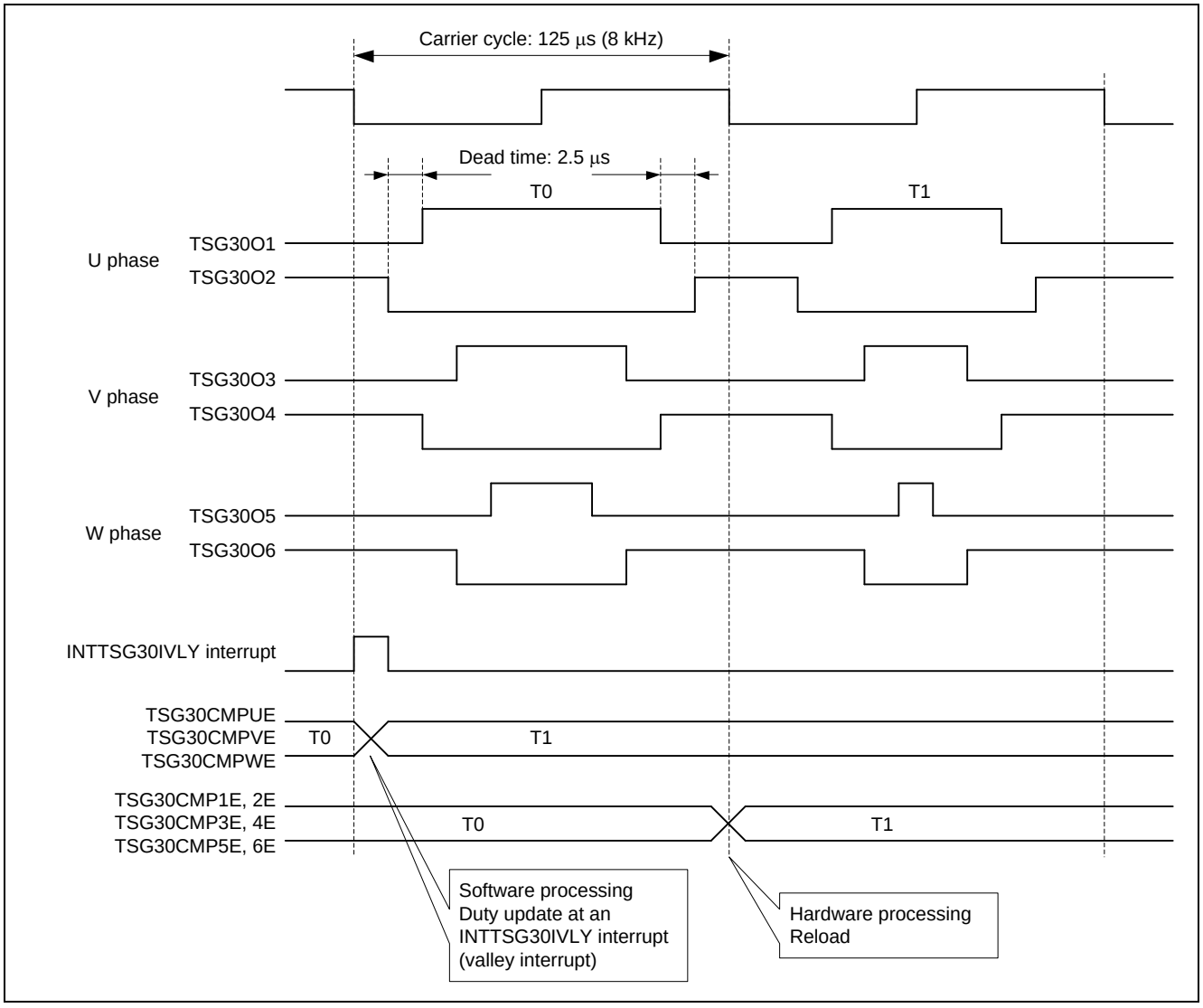


Figure 2-2 Description of Operations Used

2.1.4 Description of Software

Examples of settings for each register used in this operation example are provided in Table 2-4 to Table 2-6.

Table 2-4 Example of TSG3 Register Settings

Register Name	Set Value	Description
TSG30TRG1	0x01	This is a trigger bit that controls the stop of the timer. TSG3nTT 1: The timer is stopped.
TSG30CTL0	0x01	This register sets operating mode of TSG30. TSG30MD[2:0] 0x1: HT-PWM mode (HT-PWM)
TSG30CTL3	0x00	This register sets the compare register rewrite method. TSG30RIA 0: The reload timing occurs at the peak reload timing (set by TSG3nCTL4.TSG3nPRE) and the valley reload timing (set by TSG3nCTL4.TSG3nVRE). TSG30RMC 0: Reload mode (simultaneous rewrite mode)
TSG30CTL4	0x000000BF	This register controls peak interrupt, valley interrupt, and reload timing. TSG30PRE 0: Reload operation at the peak timing disabled TSG30VRE 1: Reload operation at the valley timing enabled TSG30PIE 0: Peak interrupt at the peak timing disabled TSG30VIE 1: Valley interrupt at the valley timing enabled TSG30RCC[04:00] 0x1F: Interrupt and reload skipping rate = 1/32
TSG30CMP0	10000	This register sets the PWM cycle. 1/80 MHz × 10000 = 125 μs (8 kHz)
TSG30TRG0	0x01	This register controls timer start. TSG30TS 1: Timer operation start
TSG30DTC0W	200	This register sets the dead time value (between negative-phase inactive and positive-phase active). TSG30DTC0 200: 1/80 MHz × 200 = 2.5 μs
TSG30DTC1W	200	This register sets the dead time value (between positive-phase inactive and negative-phase active). TSG30DTC1 200: 1/80 MHz × 200 = 2.5 μs
TSG30CMPU	-	This register sets the compare value for the U phase. (U-phase duty setting)
TSG30CMPV	-	This register sets the compare value for the V phase. (V-phase duty setting)
TSG30CMPW	-	This register sets the compare value for the W phase. (W-phase duty setting)

Table 2-5 Example of Interrupt Control Register Settings

Register Name	Set Value	Description
EIC376 TSG30 valley interrupt (INTTSG30IVLY)	0x004F	This register is provided for each EI-level interrupt source to set interrupt control conditions of each source. EIMKn 0: Interrupt processing enabled EITBn 1: Table reference method EIPn 0xF: Priority 15

Table 2-6 Example of Port Register Settings

Register Name	Set Value	Description	Selection
PCR2_5	0x00000048	PUCC, PDSC 0x0: Drive intensity low PBDC 0x0: Bidirectional mode disabled PIBC 0x0: Input buffer disabled PMC 0x1: Alternative mode PIPC 0x0: Software input/output control PM 0x0: Output mode (output enabled)	PFCEAE, PFCAE, PFCE, PFC 0x8: Alternative output mode 9 (ALT-OUT9)
PCR2_6	0x00000048		PFCEAE, PFCAE, PFCE, PFC 0x8: Alternative output mode 9 (ALT-OUT9)
PCR2_7	0x00000040		PFCEAE, PFCAE, PFCE, PFC 0x0: Alternative output mode 1 (ALT-OUT1)
PCR2_8	0x00000040		PFCEAE, PFCAE, PFCE, PFC 0x0: Alternative output mode 1 (ALT-OUT1)
PCR2_9	0x0000004C		PFCEAE, PFCAE, PFCE, PFC 0xC: Alternative output mode 13 (ALT-OUT13)
PCR2_10	0x0000004C		PFCEAE, PFCAE, PFCE, PFC 0xC: Alternative output mode 13 (ALT-OUT13)

Lists of functions, variables, and constants used in this operation example are provided in Table 2-7 to Table 2-9.

Table 2-7 List of Functions

Function Name	Description
main0	Calls each function.
tsg30_init	Makes initial settings for TSG30.
tsg30_init_duty	Makes initial settings for TSG30.
set_p2	Makes initial settings for ports (P2_5 to P2_10).
int_init	Makes initial settings for the interrupt feature.
tsg30_enable	Sets TSG30 to operation start.
int_tsg_dutychange	This function is an interrupt function that updates the duty of the U, V, and W phases.

Table 2-8 List of Variables

Variable Name	Description
u4_duty	Used to update the duty

Table 2-9 List of Constants

Constant Name	Description
NUM_TSGCARR	PWM cycle set value
NUM_TSGDT_IP	Dead time value (between negative-phase inactive and positive-phase active)
NUM_TSGDT_PI	Dead time value (between positive-phase inactive and negative-phase active)
MAX_DUTY	Maximum duty value

2.1.5 Operation Flow

The flowchart of this operation example is shown below.

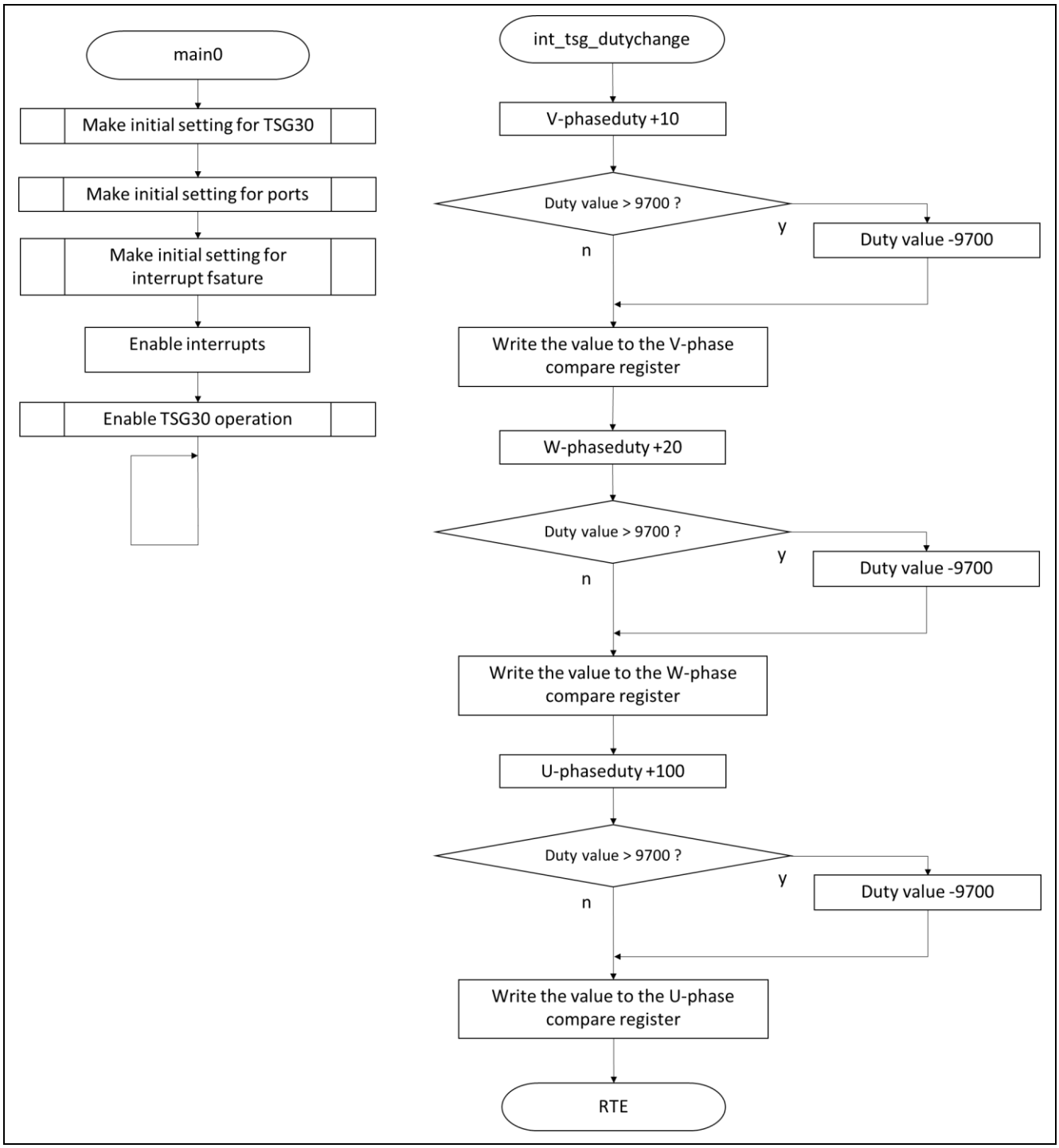


Figure 2-3 Operation Flow

2.2 Starting ADCK by Carrier Valley Trigger in HT-PWM Mode

2.2.1 Overview of Specifications

In this operation example, ADCK start at the carrier valley is added to the operation described in section 2.1.

Generation of an A/D conversion trigger (TSG30ADTRG0) at a valley interrupt is enabled in the TSG30 settings. The ADCK0 start trigger is set to TSG30ADTRG0 in peripheral interconnection 2 (PIC2). ADCK0 starts at each A/D conversion trigger (TSG30ADTRG0) to perform A/D conversion.

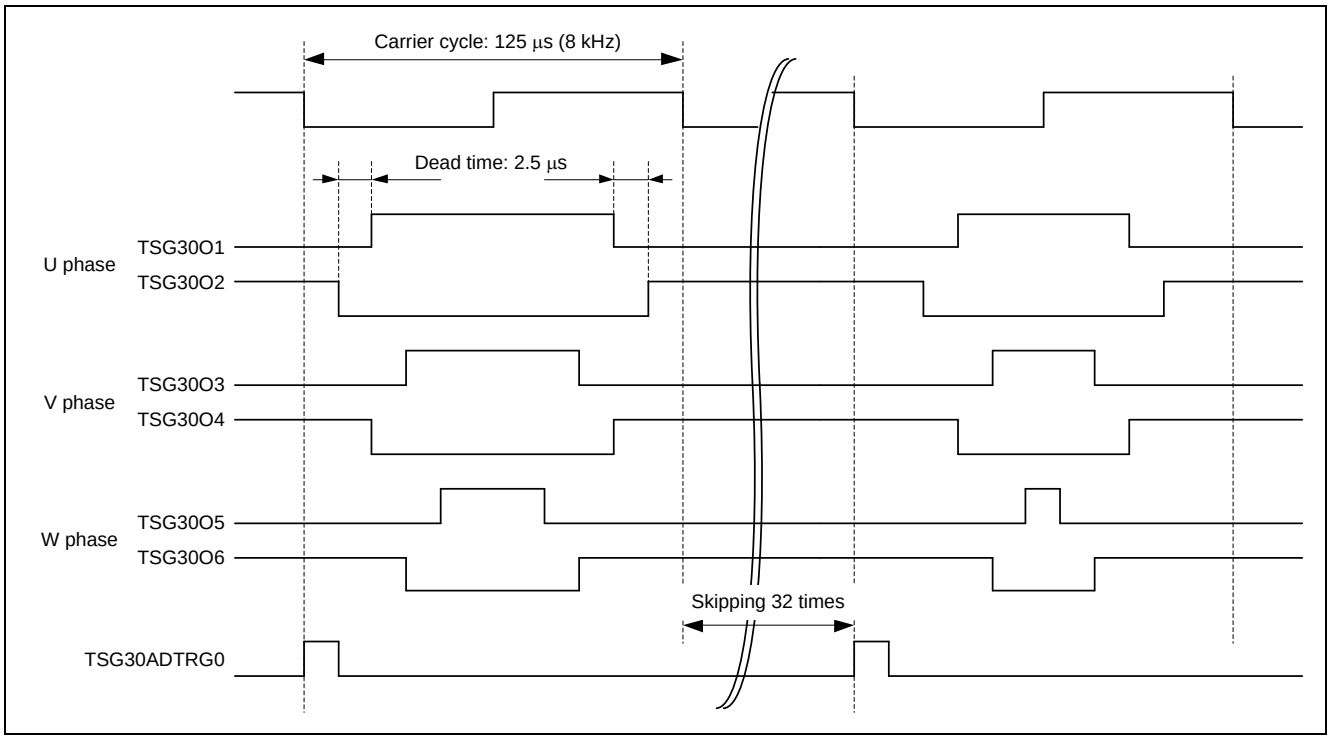


Figure 2-4 Schematic

2.2.2 Operating Conditions of Features Used

Operating conditions of features used in this operation example are shown below.

Table 2-10 Port Settings

Item	Description
Ports to be used	P2_5: TSG30O1 P2_6: TSG30O2 P2_7: TSG30O3 P2_8: TSG30O4 P2_9: TSG30O5 P2_10: TSG30O6 P11_0: Output port

Table 2-11 TSG3 Settings

Item	Description
Clock supplied to TSG3	CLKC_HSB (unmodulated high-speed peripheral clock): 80 MHz
Feature to be used	HT-PWM mode
Carrier cycle	125 μs (8 kHz)
Dead time	2.5 μs
Compare register transfer timing	Reload mode (simultaneous rewrite mode)
Reload timing	Reload operation at the valley timing enabled
Interrupt	Generation of valley interrupt enabled
Skipping rate	1/32
A/D conversion trigger	TSG30ADTRG0 enabled (valley interrupt, no skipping)

Table 2-12 PIC2 Settings

Item	Description
ADCK0 SG4 trigger source	TSG30ADTRG0
Selection of valid edge	Rising edge

Table 2-13 Interrupt Function Settings

Item	Description
TSG30 valley interrupt (INTTSG30IVLY)	Table reference method, Priority 15
ADCK0 scan group 4 end interrupt (INTADCK0I4)	Table reference method, Priority 0

Table 2-14 ADCK Settings

Item	Description
Pins to be used	ADCK0I30、ADCK0I31、ADCK0I32、ADCK0I33
Conversion mode	A/D conversion of hold value
Scan group	SG4
Scan mode	Multi-cycle scan mode
Scan group x4 end interrupt signal (ADI04)	Output enabled
A/D conversion start trigger input	Enabled

2.2.3 Operation

In this operation example, ADCK start at the carrier valley is added to the operation described in section 2.1.

An A/D conversion trigger (TSG30ADTRG0) is output when a valley interrupt (INTTSG30IVLY) is generated. ADCK0 starts at an A/D conversion trigger (TSG30ADTRG0) to perform A/D conversion. In this operation example, P11_0 is set as an output pin to check that A/D conversion has been performed to output a pulse by the A/D conversion end interrupt function. Processing for acquiring A/D-converted values is not performed in this operation example.

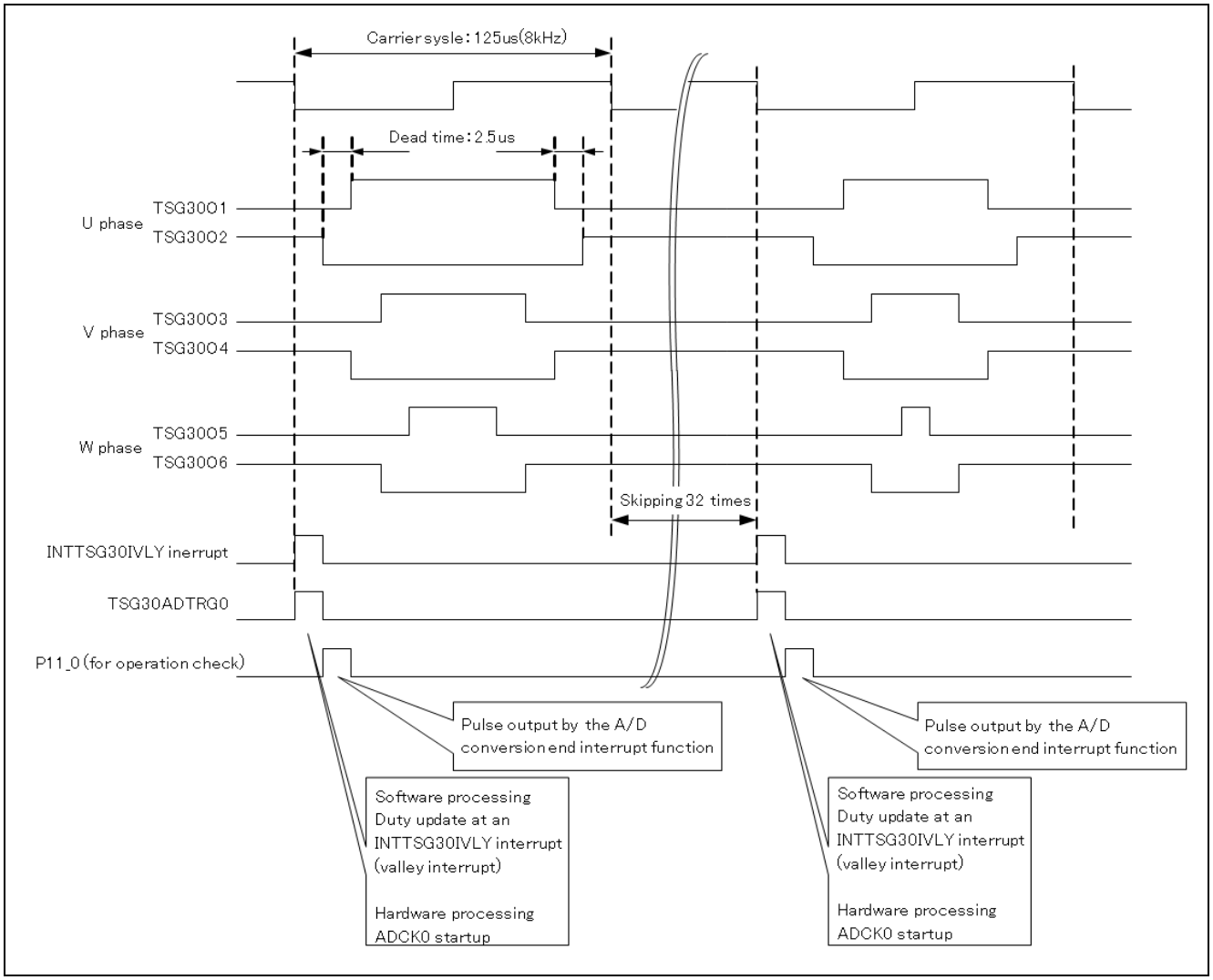


Figure 2-5 Description of Operations Used

2.2.4 Description of Software

Examples of settings for each register used in this operation example are provided in Table 2-15 to Table 2-19.

Table 2-15 Example of TSG3 Register Settings

Register Name	Set Value	Description
TSG30TRG1	0x01	This is a trigger bit that controls the stop of the timer. TSG3nTT 1: The timer is stopped.
TSG30CTL0	0x01	This register sets operating mode of TSG30. TSG30MD[2:0] 0x1: HT-PWM mode (HT-PWM)
TSG30CTL3	0x00	This register sets the compare register rewrite method. TSG30RIA 0: The reload timing occurs at the peak reload timing (set by TSG3nCTL4.TSG3nPRE) and the valley reload timing (set by TSG3nCTL4.TSG3nVRE). TSG30RMC 0: Reload mode (simultaneous rewrite mode)
TSG30CTL4	0x000000BF	This register controls peak interrupt, valley interrupt, and reload timing. TSG30PRE 0: Reload operation at the peak timing disabled TSG30VRE 1: Reload operation at the valley timing enabled TSG30PIE 0: Peak interrupt at the peak timing disabled TSG30VIE 1: Valley interrupt at the valley timing enabled TSG30RCC[04:00] 0x1F: Interrupt and reload skipping rate = 1/32
TSG30CTL5	0x0001	This register controls the A/D conversion trigger output (TSG30ADTRG0). TSG30ACC[01:00] 0x0: A/D conversion trigger skipping rate = No skipping TSG30AT00 1: A valley interrupt (INTTSG3nIVLY) is used as an A/D conversion trigger.
TSG30CMP0	10000	This register sets the PWM cycle. 1/80 MHz × 10000 = 125 μs (8 kHz)
TSG30TRG0	0x01	This register controls timer start. TSG30TS 1: Timer operation start
TSG30DTC0W	200	This register sets the dead time value (between negative-phase inactive and positive-phase active). TSG30DTC0 200: 1/80 MHz × 200 = 2.5 μs
TSG30DTC1W	200	This register sets the dead time value (between positive-phase inactive and negative-phase active). TSG30DTC1 200: 1/80 MHz × 200 = 2.5 μs
TSG30CMPU	-	This register sets the compare value for the U phase. (U-phase duty setting)
TSG30CMPV	-	This register sets the compare value for the V phase. (V-phase duty setting)
TSG30CMPW	-	This register sets the compare value for the W phase. (W-phase duty setting)

Table 2-16 Example of PIC2 Register Settings

Register Name	Set Value	Description
PIC20ADCK0TSEL4	0x00000020	This register selects a trigger of ADCK0 channel group 4. PIC20ADCK0TSEL405 1: TSG30ADTRG0 selected
PIC20ADCK0EDGSEL	0x0000	This register selects a valid edge. PIC2ADCK0EDGSEL [9:8] 0x0: Rising edge

Table 2-17 Example of Interrupt Control Register Settings

Register Name	Set Value	Description
EIC376 TSG30 valley interrupt (INTTSG30IVLY)	0x004F	This register is provided for each EI-level interrupt source to set interrupt control conditions of each source. EIMKn 0: Interrupt processing enabled EITBn 1: Table reference method EIPn 0xF: Priority 15
EIC445 ADCK0 scan group 4 end interrupt（INTAIRINTREQ8 Group 0 → INTADCK0I4）	0x0040	This register is provided for each EI-level interrupt source to set interrupt control conditions of each source. EIMKn 0: Interrupt processing enabled EITBn 1: Table reference method EIPn 0x0: Priority 0

Table 2-18 Example of Port Register Settings

Register Name	Set Value	Description	Selection
PCR2_5	0x00000048	PUCC, PDSC 0x0: Drive intensity low PBDC 0x0: Bidirectional mode disabled PIBC 0x0: Input buffer disabled PMC 0x1: Alternative mode PIPC 0x0: Software input/output control PM 0x0: Output mode (output enabled)	PFCEAE, PFCAE, PFCE, PFC: Alternative output mode 9 (ALT-OUT9)
PCR2_6	0x00000048		PFCEAE, PFCAE, PFCE, PFC: Alternative output mode 9 (ALT-OUT9)
PCR2_7	0x00000040		PFCEAE, PFCAE, PFCE, PFC: Alternative output mode 1 (ALT-OUT1)
PCR2_8	0x00000040		PFCEAE, PFCAE, PFCE, PFC: Alternative output mode 1 (ALT-OUT1)
PCR2_9	0x0000004C		PFCEAE, PFCAE, PFCE, PFC: Alternative output mode 13 (ALT-OUT13)
PCR2_10	0x0000004C		PFCEAE, PFCAE, PFCE, PFC: Alternative output mode 13 (ALT-OUT13)
PCR11_0	0x00000000	Out put (for operation check)	-
P11	P11_0~P11_0	Set output level of P11 P11_0 0：Lo level P11_0 1：Hi level	-

Table 2-19 Example of ADCK Register Settings

Register Name	Set Value	Description
ADCK0ADCR1	0x02	This register sets the ADCK common control (suspension method). SUSMTD[1:0] 0x2: Asynchronous suspension
ADCK0ADCR2	0x10	This register sets the ADCK common control (data format and addition count of addition A/D conversion). DFMT[2:0] 0x1: Resolution 12-bit signed integer format
ADCK0VCLMINTER1 ADCK0VCLMINTER2	0x00000000	An upper/lower limit check interrupt (INT_UL) is not output.
ADCK0THCR	0x00	This register controls T&H sampling. ASMPMSK 0: Auto sampling
ADCK0THGSR	0x0000	This register selects T&H group of each T&H. TH5GS 0: T&H group A of T&Hk5 is selected. TH4GS 0: T&H group A of T&Hk4 is selected. TH3GS 0: T&H group A of T&Hk3 is selected. TH2GS 0: T&H group A of T&Hk2 is selected. TH1GS 0: T&H group A of T&Hk1 is selected. TH0GS 0: T&H group A of T&Hk0 is selected.
ADCK0THER	0x3F	This register enables or disables each T&H circuit. TH5E 1: Track and hold operation of the T&H5 circuit is enabled. TH4E 1: Track and hold operation of the T&H4 circuit is enabled. TH3E 1: Track and hold operation of the T&H3 circuit is enabled. TH2E 1: Track and hold operation of the T&H2 circuit is enabled. TH1E 1: Track and hold operation of the T&H1 circuit is enabled. TH0E 1: Track and hold operation of the T&H0 circuit is enabled.
ADCK0SGVCPR4	0x0300	This register specifies the starting/end pointer of a virtual channel. VCSP[5:0] 0x00: Start virtual channel number of SG4 = Channel 0 VCEP[5:0] 0x03: End virtual channel number of SG4 = Channel 3
ADCK0SGMCYCR4	0x00	This register sets the A/D conversion count in multi-cycle scan mode. MCYC[7:0] 0x00: A/D conversion count = 1

Register Name	Set Value	Description
ADCK0VCR0	0x00000800	This register sets a virtual channel0. VCULLMTBS[3:0] 0x0：Upper/Lower limit check is disable. WTTS[3:0] 0x0：Wait time is disable. DFETN 0：DFE entry is disable CNVCLS[3:0] 0x1：A/D conversion of hold value ADIE 0：Virtual channel end interrupt is disable. GCTRL [5:0] 0x00：The T&H0 hold value is A/D converted.
ADCK0VCR1	0x00000801	This register sets a virtual channel1. VCULLMTBS[3:0] 0x0：Upper/Lower limit check is disable. WTTS[3:0] 0x0：Wait time is disable. DFETN 0：DFE entry is disable CNVCLS[3:0] 0x1：A/D conversion of hold value ADIE 0：Virtual channel end interrupt is disable. GCTRL [5:0] 0x00：The T&H0 hold value is A/D converted.
ADCK0VCR2	0x00000802	This register sets a virtual channel2. VCULLMTBS[3:0] 0x0：Upper/Lower limit check is disable. WTTS[3:0] 0x0：Wait time is disable. DFETN 0：DFE entry is disable CNVCLS[3:0] 0x1：A/D conversion of hold value ADIE 0：Virtual channel end interrupt is disable. GCTRL [5:0] 0x00：The T&H0 hold value is A/D converted.
ADCK0VCR3	0x00000803	This register sets a virtual channel3. VCULLMTBS[3:0] 0x0：Upper/Lower limit check is disable. WTTS[3:0] 0x0：Wait time is disable. DFETN 0：DFE entry is disable CNVCLS[3:0] 0x1：A/D conversion of hold value ADIE 0：Virtual channel end interrupt is disable. GCTRL [5:0] 0x00：The T&H0 hold value is A/D converted.
ADCK0THACR	0x33	This register controls T&H group A. HLDCTE 1: Hold control is enabled. HLDTE 1: Hardware trigger signals are enabled. SGS[1:0] 0x3: SG4
ADCK0SGCR4	0x11	This register controls SG4. ADSTARTE 0：A/D conversion simultaneous start is disable. SCANMD 0: Multi-cycle scan mode ADIE 1: Output of the SG4 end interrupt signal ADI04 is enabled. TRGMD 0x1: A/D conversion start trigger input of SG4 is enabled.
ADCK0SGSTPCR4	0x01	Controls the stop of A / D conversion for scan group 4. SGSTP 1: Stop A / D conversion
AIRISELR0	0x00000000	This register selects interrupt resources. ISEL[8] 0：Select INTADCK0I4
ADCK0THSMPSTCR	0x01	This register controls sampling start of all T&H circuits. SMPST 1: Sampling start

Lists of functions, variables, and constants used in this operation example are provided in Table 2-20 to Table 2-22.

Table 2-20 List of Functions

Function Name	Description
main0	Calls each function.
tsg30_init	Makes initial settings for TSG30.
tsg30_init_duty	Makes initial settings for TSG30.
adck0_init	Makes initial settings for ADCK0.
pic_set_adtrg	Makes initial settings for PIC2.
set_p2	Makes initial settings for ports (P2_5 to P2_10).
set_p11	Makes initial settings for the port (P11_0).
int_init	Makes initial settings for the interrupt feature.
tsg30_enable	Sets TSG30 to operation start.
adck0_enable	Sets ADCK0 to operation start.
int_tsg_dutychange	This function is an interrupt function that updates the duty of the U, V, and W phases.
int_adck0sg4_finish	This function is an interrupt function that outputs a pulse (for operation check) from the P11_0 pin at the end of A/D conversion.

Table 2-21 List of Variables

Variable Name	Description
u4_duty	Used to update the duty
u2_count_i	Used for wait processing

Table 2-22 List of Constants

Constant Name	Description
NUM_TSGCARR	PWM cycle set value
NUM_TSGDT_IP	Dead time value (between negative-phase inactive and positive-phase active)
NUM_TSGDT_PI	Dead time value (between positive-phase inactive and negative-phase active)
MAX_DUTY	Maximum duty value

2.2.5 Operation Flow

The flowchart of this operation example is shown below.

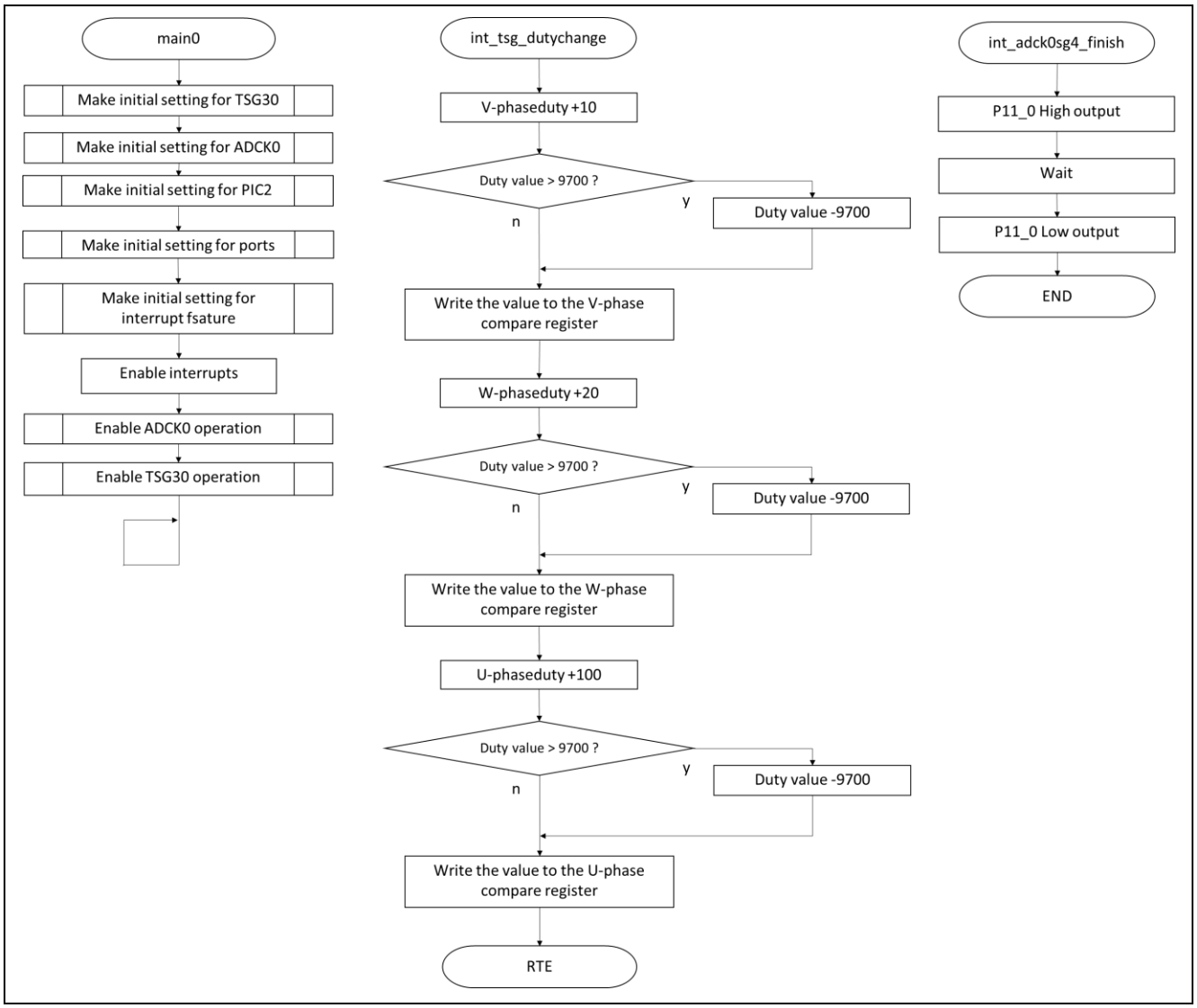


Figure 2-6 Operation Flow

2.3 Compare Match Interrupt in HT-PWM Mode

2.3.1 Overview of Specifications

In this operation example, a compare match interrupt is added to the operation described in section 2.1.

A compare match interrupt (INTTSG3nIm) is generated when the TSG3nCMPmE buffer register value matches the 18-bit counter value. A compare match interrupt is generated depending on the compare register used in operating mode.

In this operation example, a compare match interrupt (INTTSG30I3) is used.

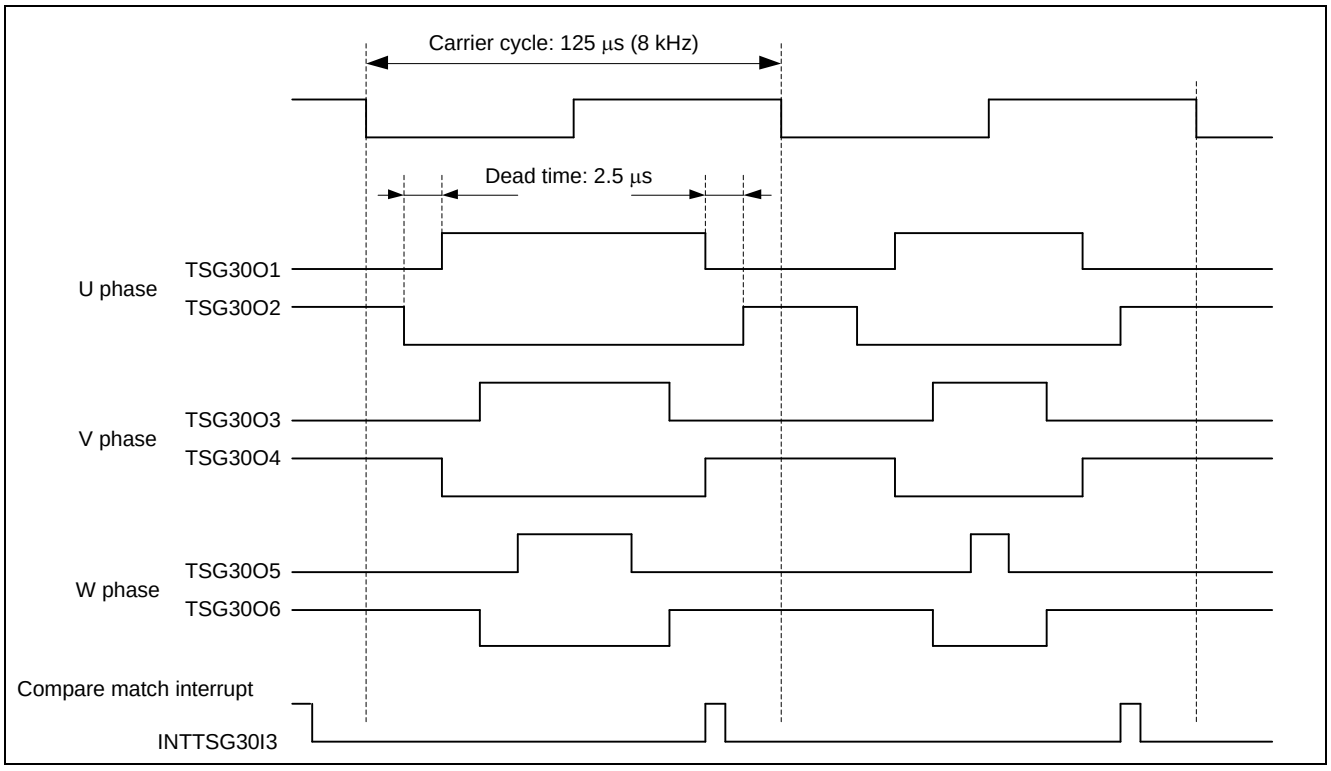


Figure 2-7 Schematic

2.3.2 Operating Conditions of Features Used

Operating conditions of features used in this operation example are shown below.

Table 2-23 Port Settings

Item	Description
Ports to be used	P2_5: TSG30O1 P2_6: TSG30O2 P2_7: TSG30O3 P2_8: TSG30O4 P2_9: TSG30O5 P2_10: TSG30O6 P11_0: Output port

Table 2-24 TSG3 Settings

Item	Description
Clock supplied to TSG3	CLKC_HSB (unmodulated high-speed peripheral clock): 80 MHz
Feature to be used	HT-PWM mode
Carrier cycle	125 μs (8 kHz)
Dead time	2.5 μs
Compare register transfer timing	Reload mode (simultaneous rewrite mode)
Reload timing	Reload operation at the valley timing enabled
Interrupt	Generation of valley interrupt enabled
Skipping rate	1/32
Compare value	3000

Table 2-25 Interrupt Feature Settings

Item	Description
TSG30 valley interrupt (INTTSG30IVLY)	Table reference method, Priority 1
Compare match interrupt (INTTSG30I3)	Table reference method, Priority 1

2.3.3 Operation

In this operation example, a compare match interrupt is added to the operation described in section 2.1.

A compare match interrupt (INTTSG30I3) is used. To check interrupt operation, the P11_0 pin is set as an output port and a pulse is output by the interrupt function.

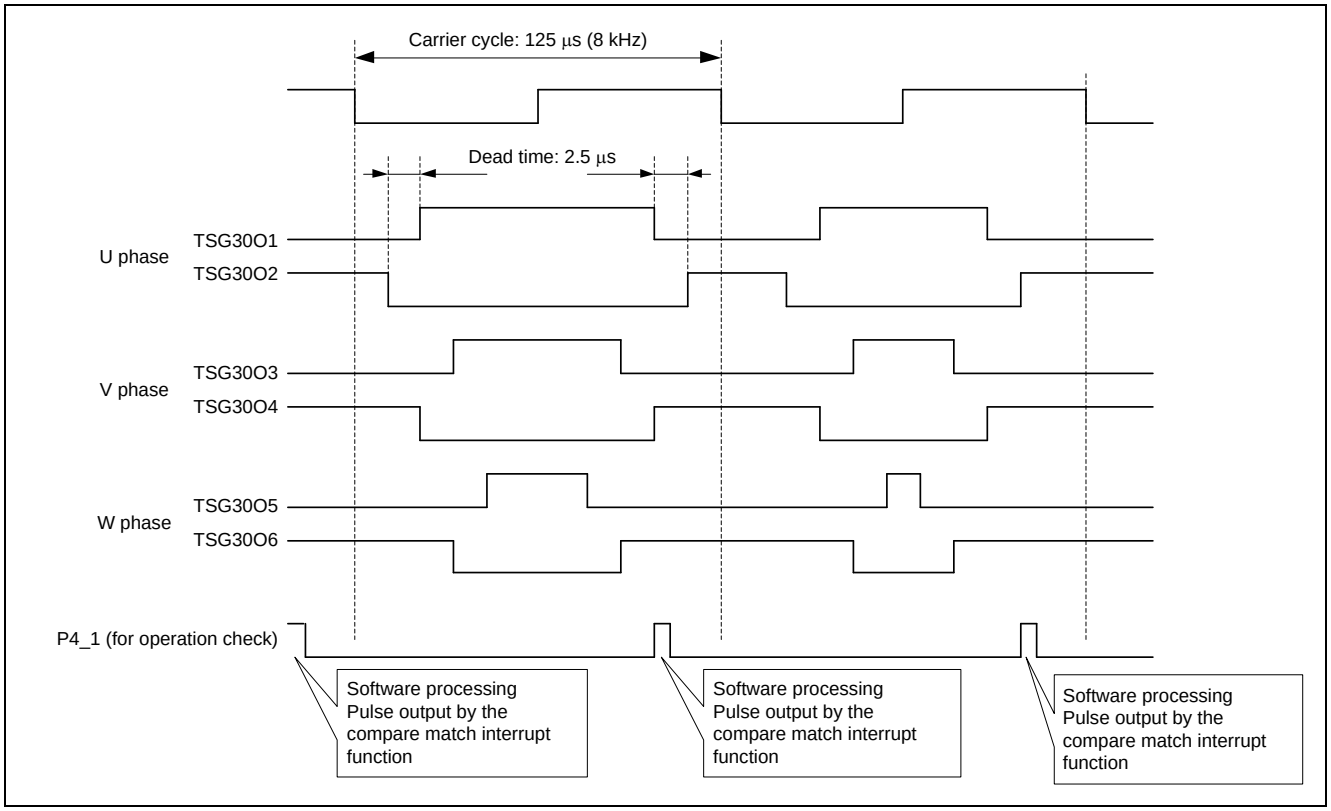


Figure 2-8 Description of Operations Used

2.3.4 Description of Software

Examples of settings of each register used in this operation example are provided in Table 2-26 to Table 2-28.

Table 2-26 Example of TSG3 Register Settings

Register Name	Set Value	Description
TSG30TRG1	0x01	This is a trigger bit that controls the stop of the timer. TSG3nTT 1: The timer is stopped.
TSG30CTL0	0x01	This register sets operating mode of TSG30. TSG30MD[2:0] 0x1: HT-PWM mode (HT-PWM)
TSG30CTL3	0x00	This register sets the compare register rewrite method. TSG30RIA 0: The reload timing occurs at the peak reload timing (set by TSG3nCTL4.TSG3nPRE) and the valley reload timing (set by TSG3nCTL4.TSG3nVRE). TSG30RMC 0: Reload mode (simultaneous rewrite mode)
TSG30CTL4	0x000000BF	This register controls peak interrupt, valley interrupt, and reload timing. TSG30PRE 0: Reload operation at the peak timing disabled TSG30VRE 1: Reload operation at the valley timing enabled TSG30PIE 0: Peak interrupt at the peak timing disabled TSG30VIE 1: Valley interrupt at the valley timing enabled TSG30RCC[04:00] 0x1F: Interrupt and reload skipping rate = 1/32
TSG30CMP0	10000	This register sets the PWM cycle. 1/80 MHz × 10000 = 125 μs (8 kHz)
TSG30TRG0	0x01	This register controls timer start. TSG30TS 1: Timer operation start
TSG30DTC0W	200	This register sets the dead time value (between negative-phase inactive and positive-phase active). TSG30DTC0 200: 1/80 MHz × 200 = 2.5 μs
TSG30DTC1W	200	This register sets the dead time value (between positive-phase inactive and negative-phase active). TSG30DTC1 200: 1/80 MHz × 200 = 2.5 μs
TSG30CMPU	-	This register sets the compare value for the U phase. (U-phase duty setting)
TSG30CMPV	-	This register sets the compare value for the V phase. (V-phase duty setting)
TSG30CMPW	-	This register sets the compare value for the W phase. (W-phase duty setting)
TSG30CMP3	3000	This register sets the compare value.

Table 2-27 Example of Interrupt Control Register Settings

Register Name	Set Value	Description
EIC376 TSG30 valley interrupt (INTTSG30IVLY)	0x0041	This register is provided for each EI-level interrupt source to set interrupt control conditions of each source. EIMKn 0: Interrupt processing enabled EITBn 1: Table reference method EIPn 0x1: Priority 1
EIC365 compare match interrupt (INTTSG30I3)	0x0041	This register is provided for each EI-level interrupt source to set interrupt control conditions of each source. EIMKn 0: Interrupt processing enabled EITBn 1: Table reference method EIPn 0x1: Priority 1

Table 2-28 Example of Port Register Setting

Register Name	Set Value	Description	Selection
PCR2_5	0x00000048	PUCC, PDSC 0x0: Drive intensity low PBDC 0x0: Bidirectional mode disabled PIBC 0x0: Input buffer disabled PMC 0x1: Alternative mode PIPC 0x0: Software input/output control PM 0x0: Output mode (output enabled)	PFCEAE, PFCAE, PFCE, PFC 0x8: Alternative output mode 9 (ALT-OUT9)
PCR2_6	0x00000048		PFCEAE, PFCAE, PFCE, PFC 0x8: Alternative output mode 9 (ALT-OUT9)
PCR2_7	0x00000040		PFCEAE, PFCAE, PFCE, PFC 0x0: Alternative output mode 1 (ALT-OUT1)
PCR2_8	0x00000040		PFCEAE, PFCAE, PFCE, PFC 0x0: Alternative output mode 1 (ALT-OUT1)
PCR2_9	0x0000004C		PFCEAE, PFCAE, PFCE, PFC 0xC: Alternative output mode 13 (ALT-OUT13)
PCR2_10	0x0000004C		PFCEAE, PFCAE, PFCE, PFC 0xC: Alternative output mode 13 (ALT-OUT13)
PCR11_0	0x00000000	Out put (for operation check)	-

Lists of functions, variables, and constants used in this operation example are provided in Table 2-29 to Table 2-31.

Table 2-29 List of Functions

Function Name	Description
main0	Calls each function.
tsg30_init	Makes initial settings for TSG30.
tsg30_init_duty	Makes initial settings for TSG30.
tsg30_setcomp3	Sets the compare value.
set_p2	Makes initial settings for ports (P2_5 to P2_10).
set_p11	Makes initial settings for the port (P11_0).
int_init	Makes initial settings for the interrupt feature.
tsg30_enable	Sets TSG30 to operation start.
int_tsg_dutychange	This function is an interrupt function that updates the duty of the U, V, and W phases.
int_tsg30_cmp	This function is an interrupt function that stores the 18-bit counter value in variables at a compare match interrupt, and outputs a pulse (for checking operation) from the P4_0 pin.

Table 2-30 List of Variables

Variable Name	Description
u4_duty	Used to update the duty
u2_count_i	Used for wait processing
u4_countTSG_pm0_g	Stores the 18-bit counter value when a compare match interrupt occurs.

Table 2-31 List of Constants

Constant Name	Description
NUM_TSGCARR	PWM cycle set value
NUM_TSGDT_IP	Dead time value (between negative-phase inactive and positive-phase active)
NUM_TSGDT_PI	Dead time value (between positive-phase inactive and negative-phase active)
MAX_DUTY	Maximum duty value
NUM_COMP	Compare value

2.3.5 Operation Flow

The flowchart of this operation example is shown below.

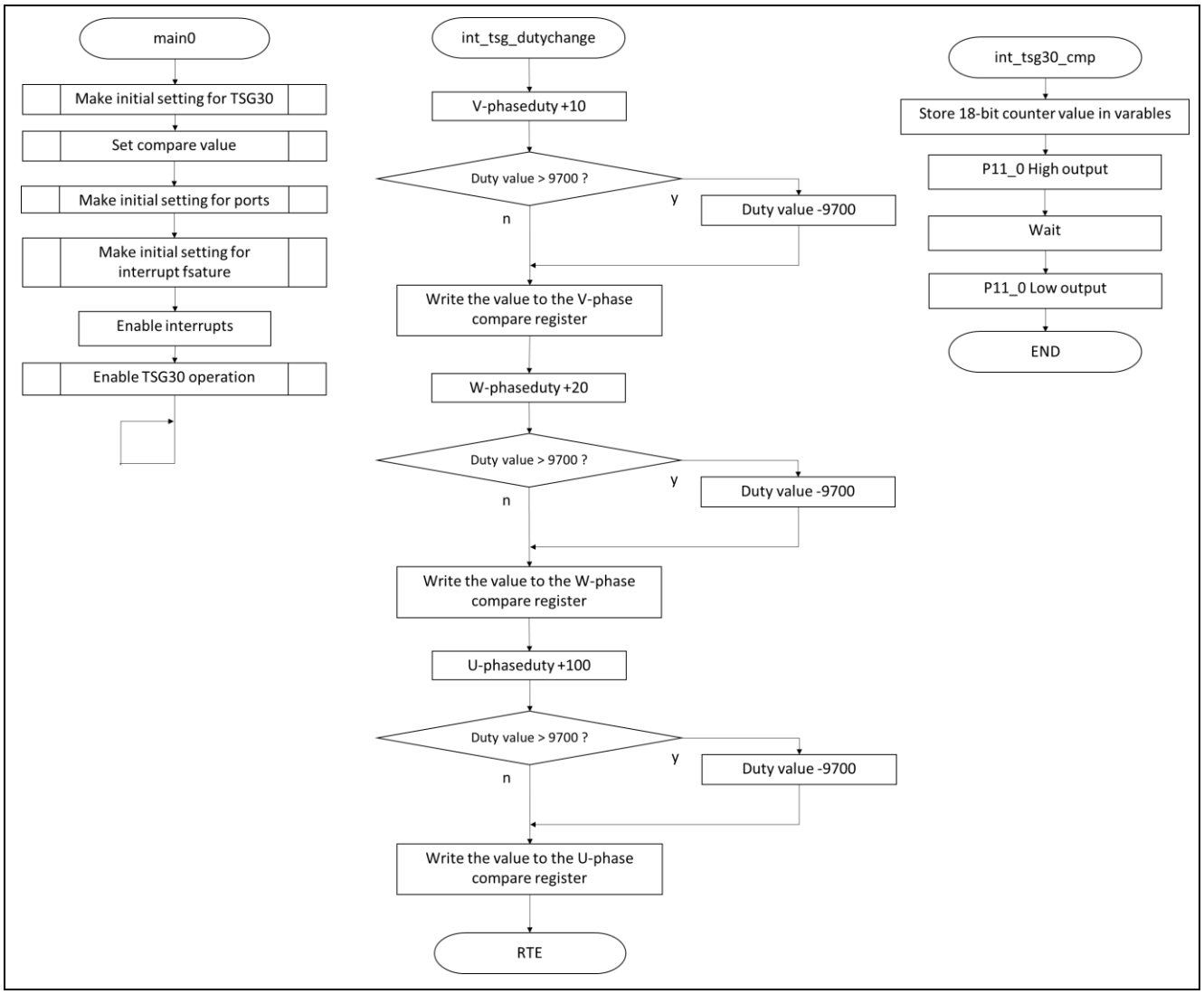
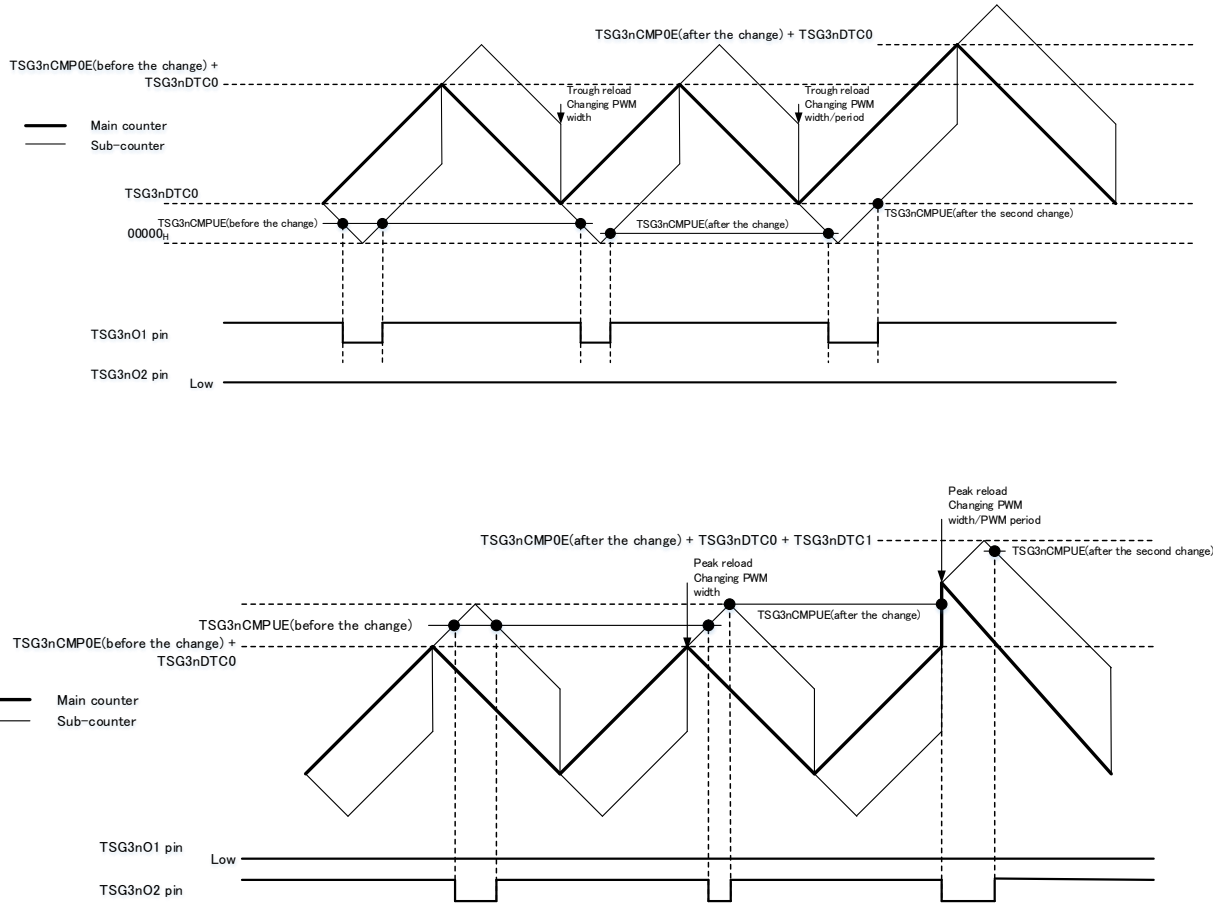


Figure 2-9 Operation Flow

2.4 Notes

PWN output waveform is generated upon a compare match with the sub-counter (not the main counter) when the TSG3nCMPmE has values less than or equal to that of TSG3nDTC0 or more than or equal to that of TSG3nCMP0E+TSG3nDTC0 in HT-PWM mode.



Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2022.06.30	-	First edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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