

RH850/U2Bx High-Resolution PWM (HRPWM)

Summary

This application note describes how to use the HRPWM of RH850/U2B6. The operation examples shown in this application note have been confirmed to work, but please be sure to check the operating environment before using the product.

Operation confirmation device

RH850/U2B6-FCC (R7F702Z22EDBB)

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1. Introduction

This application note describes that how to add a delay to the PWM signal using the HRPWM of RH850/U2B6-FCC.

1.1 Functions

The hardware functions of RH850/U2B6 used in this application note are shown below.

- High-Resolution PWM (HRPWM)
- TSG3 (Motor Control Timer)
- PIC (Peripheral Interconnect)

2. HRPWM output

The HRPWM can be added some delay to a complementary PWM waves generated by GTM or TSG3. The delay can be set individually to each phase. In this application note, it shows the example of the adding a delay to PWM waves by HRPWM. The PWM waves are generated by the HT-PWM mode of TSG3.

Please set the Option Byte shown in Table **2-1** when using this function.

Table 2-1 Option Byte setting

Register name	Value	Operations
OPBT8.CKSEL_HRPWM	11b	Clock source select for HR-PWM : Set when HRPWM is used with TSG3

2.1 Operation overview

The HRPWM can be output the PWM wave with delay according to the setting value of it. The PWM waves are generated by TSG3.

The TSG31 and TSG32 can be used in conjunction with the HRPWM. In this application note, the TSG31 is used. The operation overview is shown in Figure **2-1**.

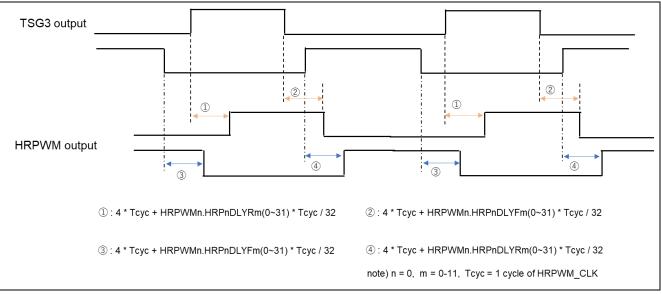


Figure 2-1 Operation overview of outputting the PWM waves with delay



2.2 Flowchart

The flowcharts are shown in Figure 2-2.

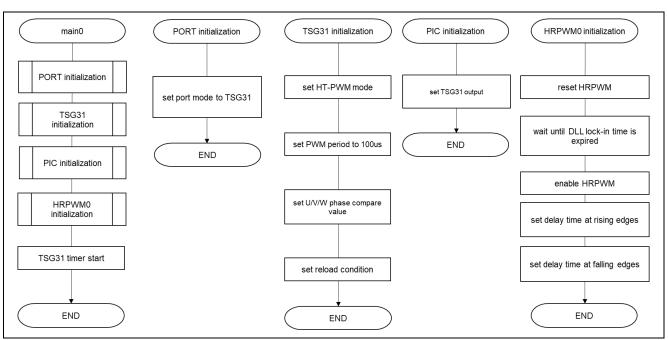


Figure 2-2 Flowchart of operation of PWM waves



2.3 Software operation

This chapter describes the software setting of this example. The Register settings are shown at Table **2-2**, Table **2-3**, Table **2-4**, Table **2-5**.

Register name	Set value	Operations
HRP0DLYCTR	0x03 -> 0x01	PWM Delay Circuit Reset, and DLL Operation is enabled.
HRP0DLYEN	0x0003F	PWM Delay Circuit Channel 0 to 5 are enabled.
HRP0DLYR0-5	0x10	PWM delay value setting which will be appended to rising edges. 0x10 = 16/32 of HRPWM_CLK
HRP0DLYF0-5	0x10	PWM delay value setting which will be appended to falling edges. 0x10 = 16/32 of HRPWM_CLK

Table 2-2	Register setting (HRPWM0)

Table 2-3	Register setting	(TSG31)
	regiotor botting	(10001)

Register name	Set value	Operations
TSG31CTL0	0x01	Select timer mode to T-PWM mode.
TSG31CTL4	0x0000080	Enables reload operation at the peak timing of the 18-bit counter.
TSG31CMP0E	0x00001F40	Set the PWM cycle as 100 usec.
TSG31CMPUE	0x00000FA0	Set the U-phase compare value (50% duty ratio).
TSG31CMPVE	0x00000FA0	Set the V-phase compare value (50% duty ratio).
TSG31CMPWE	0x00000FA0	Set the W-phase compare value (50% duty ratio).
TSG31TRG0	0x01	The TSG31 timer is started.

Table 2-4Register setting (PIC1)

Register name	Set value	Operations
PIC1LHSEL1	0x00	Selects low/high level output of the TSG31 output.
PIC1TSGOUTCTR1	0x00	Set output low/high level as TSG31 output is available.

Table 2-5	Register setting	(PORT)
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Register name	Set value	Operations
PORT0.PCR00_6	0x0000060	Set port output mode as TSG31O1_H.
PORT0.PCR02_0	0x0000069	Set port output mode as TSG31O2_H.
PORT0.PCR02_1	0x0000063	Set port output mode as TSG31O3_H.
PORT0.PCR02_2	0x0000069	Set port output mode as TSG31O4_H.
PORT0.PCR02_3	0x0000068	Set port output mode as TSG31O5_H.
PORT0.PCR02_4	0x0000067	Set port output mode as TSG31O6_H.



The software functions are shown in Table 2-6.

Function name	Overview		
main0	Main application		
hrpwm_init	HRPWM initialization		
tsg3_init TSG31 initialization			
pic_init PIC1 initialization			
port_init PORT initialization			



Revised record

		Revised contents		
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1.00	2022.06.30	-	First edition issued	



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Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

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5. Clock signals

6.

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable. Voltage application waveform at input pin

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