RH850/U2Bx

R01AN6834EJ0100
Rev.1.00

1-bit digital data stream conversion using DSMIF module

Introduction

This application note describes examples of operation using the Delta-Sigma Modulator Interface (DSMIF) of RH850/U2Bx.

Examples of tasks and applications described in this application note are verified. However, before using this example, be sure to check operating environment.

Target Device

This application note applies to RH850/U2B10.

Contents

1. Introduction

This application note describes how to use the overview and the usage of the Delta-Sigma Modulator Interface (DSMIF) and the designation of the software in RH850/U2B10.

1.1 Feature Used

RH850/U2B10 hardware features used in this application note are listed below.

- Delta-Sigma Modulator Interface (DSMIF,DSMOP)
- ADC Interrupt Router (AIR)
- ADC Boundary Flag Generator (ABFG)

2. Outline and function of DSMIF

2.1 Outline

The DSMIF module filters Δ-Σ-modulated 1-bit digital data streams with a high sampling rate and converts into 16-bit digital data with a low sampling rate.

Functions supported by DSMIF are listed below.

- Reception of 1-bit data stream and conversion to 16-bit digital data with SINC filter
- Bandwidth adjustment with built-in FIR filter
- Master and slave operation (input/ output of the delta-sigma clock signal)
- Error signal output by upper and lower limit detection
- Interrupt generation (Via AIR of ADCK)
- Data transfer with DMA
- Data output to DFE.GTM

The DSMIF module is designed to receive the output of an externally mounted Δ-Σ ADC IC, so the interrupt output path and data transfer to the DFE are corresponded to other ADCs.

2.2 Receiving data stream and conversion to 16-bit digital data

Δ-Σ modulation converts analog data into PDM (Pulse Density Modulation) signal represented by a 1-bit (0,1) digital stream. The input signal modulated by PDM represented a 1-bit (0,1) pulse array. If the input signal is close to the minimum limit of determination, the percentage of 0 is high, and if it is close to the maximum limit of determination, the percentage of 1 is high. The voltage is expressed as a ratio of ones and zeros. The following shows how an analog signal is converted to a PDM signal.

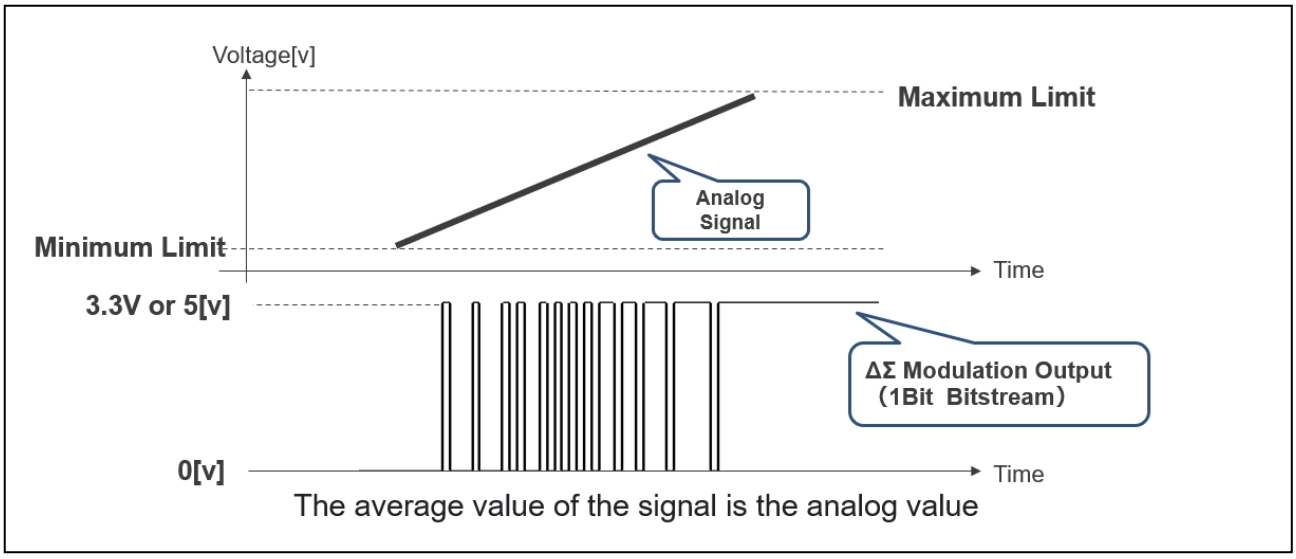


Figure 2-1 Analog Signal and PDM-Converted Signal

The DSMIF module receives this PDM signal (1-bit digital stream signal) generated by an external Δ-Σ ADC IC and converts it into 16-bit digital data. The signal is received synchronously to the clock. Signals can be acquired on either the rising edge, falling edge, or both edges of the clock. It can be performed at up to 20 MHz on the rising or falling edges, and 10 MHz on both edges.

The received PDM signal is converted (demodulated) into 16-bit length digital data and decimated by a cardinal sine function filter (SINC filter). The signal demodulated by the SINC filter has a high-frequency component.

This high-frequency component can be removed by bandwidth adjustment by the FIR filter (DSMOP) in the subsequent stage.

The following is an example of the concept and frequency response of the SINC (SINC3) filter.

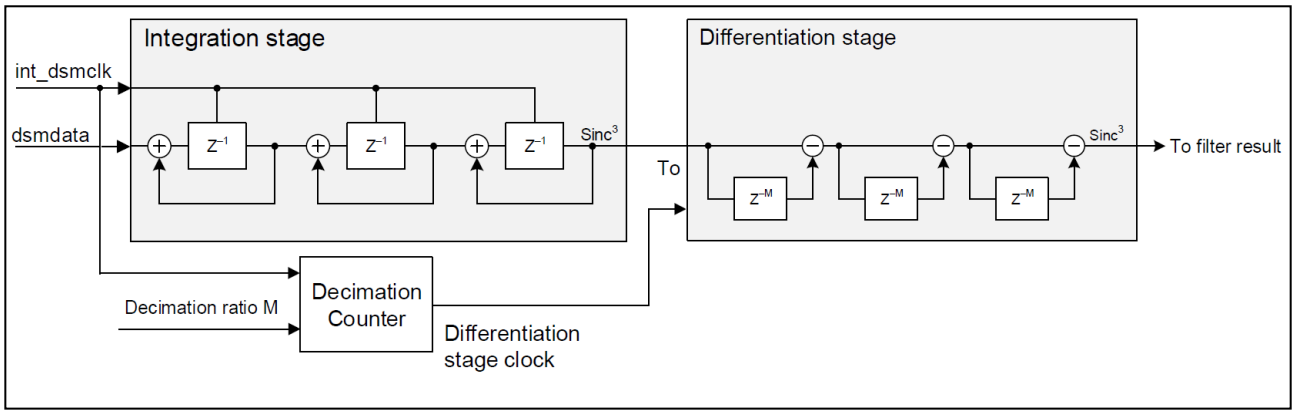


Figure 2-2 Concept SINC(SINC3)Filter

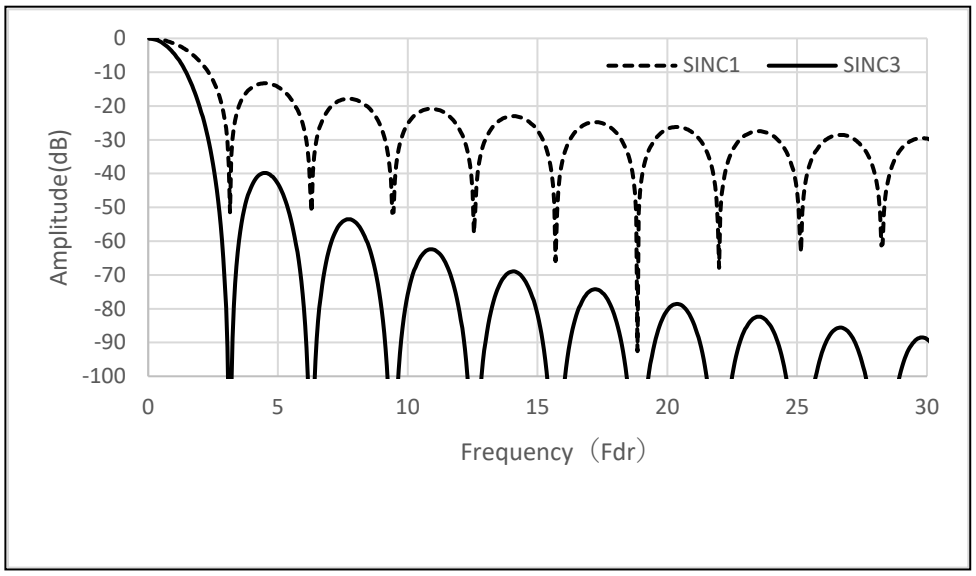


Figure 2-3 Frequency Response of SINC (SINC3) Filter

2.3 Bandwidth adjustment

To remove high-frequency components from signals demodulated by the SINC filter, DSMIF mounts a two-stage FIR filter (DSMOP) in the subsequent stage to SINC filter.
The following is the configuration of DSMOP.

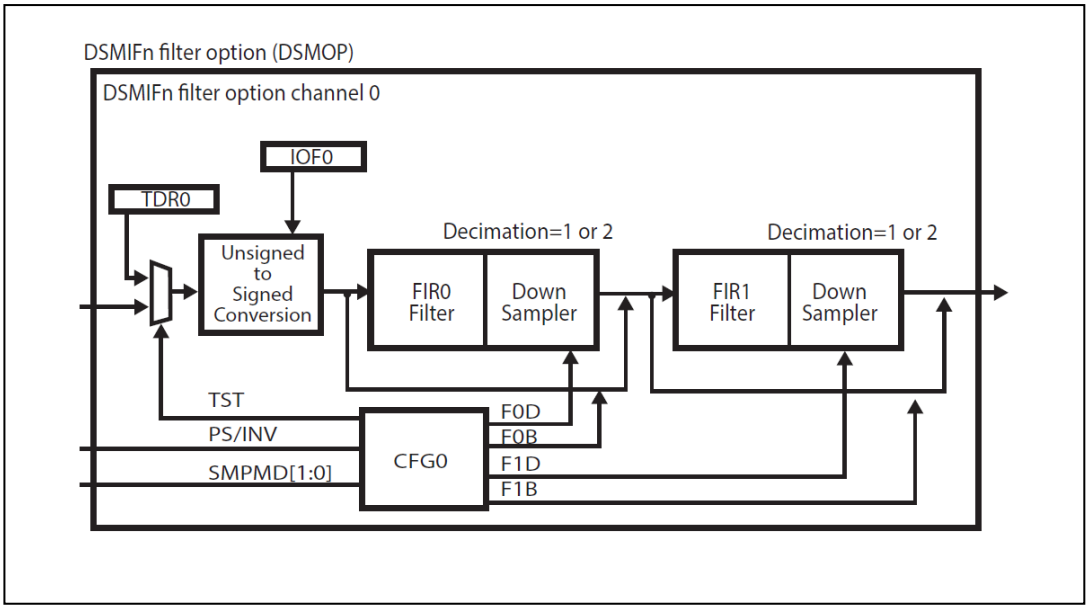
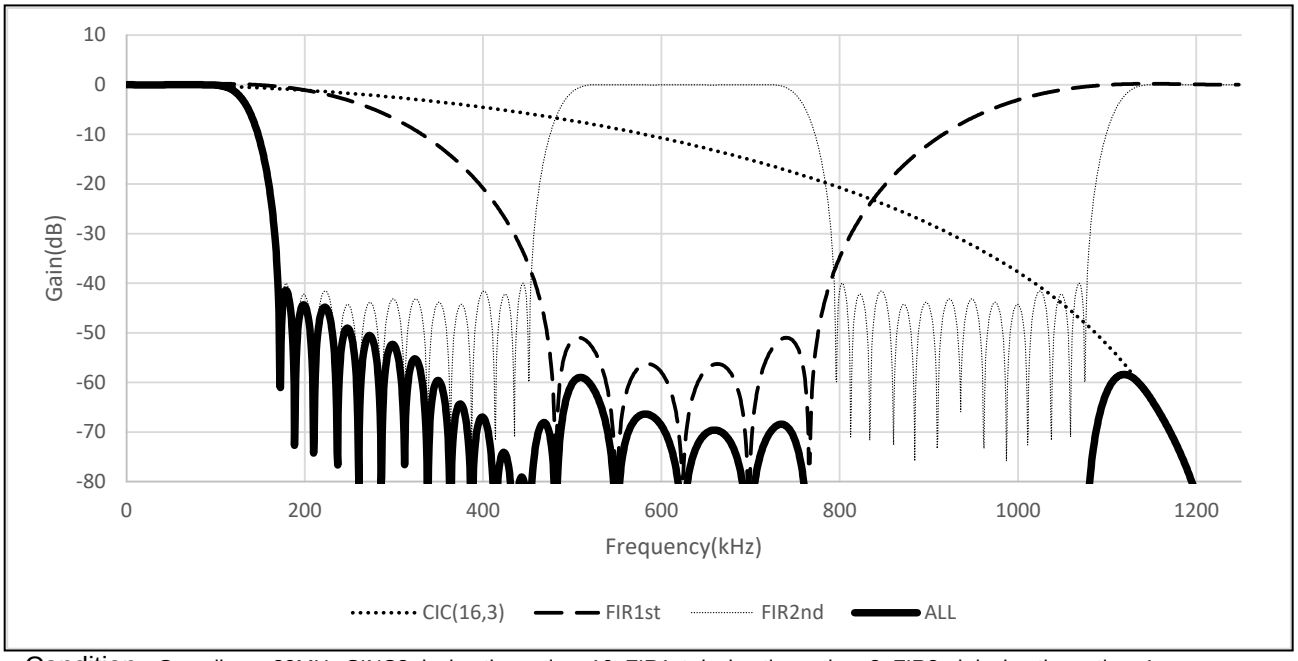


Figure 2-4 Cconfiguration of DSMOP

Each FIR filter in DSMOP can change the capable of usage and the output decimation ratio. The coefficients cannot be changed.
The following is the frequency response of SINC3 filter and filters in DSMOP.



Condition : Sampling = 20MHz,SINC3 decimation ratio = 16, FIR1st decimation ratio = 2, FIR2nd decimation ratio = 1

Figure 2-5 Frequency Response of SINC3 and filters in DSMOP

2.4 Clock signal for receiving (Master operation / Slave operation)

PDM signals (1-bit digital stream signals) are received synchronously to the clock. The DSMIF module has two modes of operation: master mode which outputs a clock, and slave mode which operates synchronously to an external clock.

2.5 Detection upper/lower limit and output interrupts

The DSMIF module can set upper and lower limits for the output of the SINC filter and generate an interrupt when the output exceeds these values. In addition, it has another SINC filter for upper and lower limit detection separated from the data filter, and by setting the response faster than the SINC filter for data, it is possible to detect errors earlier than the data output. The following is an overview of the detection of upper and lower limits.

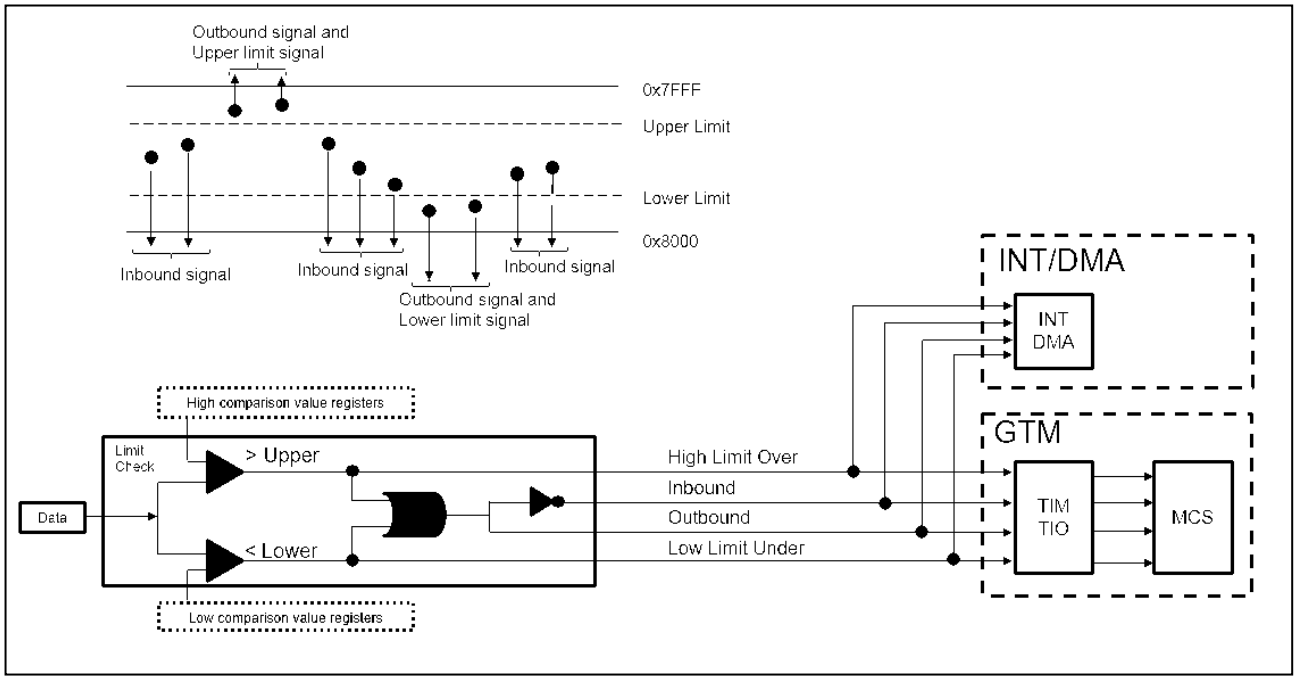


Figure 2-6 Detection Upper / Lower Limit

2.6 Interrupt generation

The DSMIF module can generate interrupts for data updates, high limit over and low limit under, and inbound and outbound. The interrupt is output via AIR in ADCK module.
Therefore, the output of the interrupt to INTC2 requires not only the DSMIF setting, but also the AIR setting. In addition, it is necessary to release the standby mode for using AIR.

2.7 Exceeding upper/lower limit detection, within/outside range detection

The DSMIF module can set upper and lower limits and generate interrupts for outputs that exceed or within the upper and lower limits. To determine whether the output exceeds the upper and lower limits or within the limits, ABFG in ADCK is used. Therefore, to use this function, not only DSMIF settings but also ABFG settings are required. In addition, it is necessary to release the standby mode for using ABFG.

3. Outline of Sample Software

3.1 Basic Operation(Master Mode)

In this example, how to reception the data stream, bandwidth adjustment, interrupt output is described with sample software.

Sample software Project :CSP_U2B10_Sample_DSMIF_M

3.1.1 Specification and outline of operation

In this example, channel 0 of DSMIF0 is used with master mode. It receives the data stream, adjust the bandwidth by DSMOP, and notifies the conversion completion by interrupt.
The specifications of this example are as follows.

Setting of DSMIF

- Channel and Port group for reception of DSMOP : Port group 0 of Channel 0
- Reception mode, sampling clock frequency, edge setting : Master mode, 20MHz, Use negative edge.
- SINC Setting :SINC3,Decimation ratio= 16
- The upper and lower limit detection function works, but the interrupts are not generated.

DSMOP Setting

- Use FIR0 Decimation ratio 2
- Use FIR1 Decimation ratio 1 (No decimation)

Frequency of output data from DSMIF

Setting: Sampling frequency of bit stream: 20MHz
SINC Setting: SINC3, Decimation ratio = 16
Decimation ratio: FIR0= 2 , FIR1= 1

Frequency of output data from DSMIF = Sampling frequency of bit stream / SINC Decimation ratio / FIR0 Decimation ratio / FIR1 Decimation ratio
=20MHz / 16 / 2/ 1 = 625kHz (period 1.6 μ s)

An interrupt generates in the data output cycle. Conversion results are overwritten when that were not read.

3.1.2 Used Functions

The hardware functions used in this operation example are shown below.

- Delta-Sigma Modulator Interface(DSMIF,DSMOP)
- ADC Interrupt Router (AIR)
- ABFG
- INTC2
- PORT

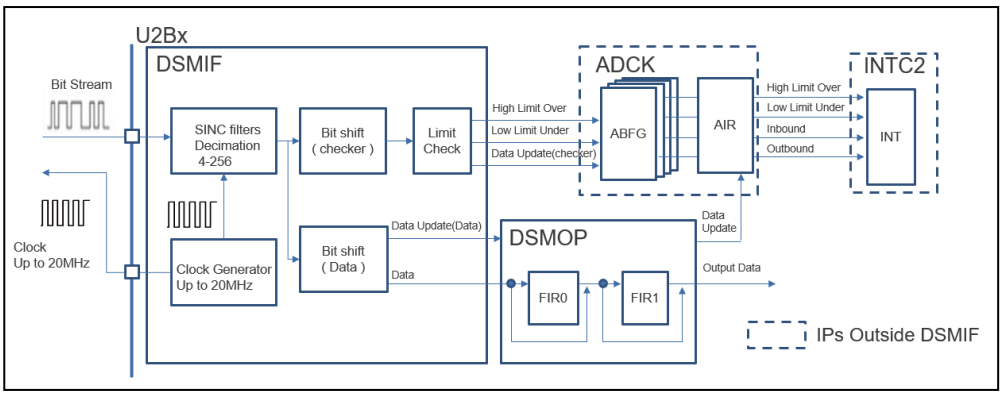


Figure 3-1 Hardware Configuration (Master mode)

3.1.3 Explain of sample software

This sample software performs the reception of data stream by using channel 0 of the DSMIF0 module, filtering, and generation interrupt to notify the conversion completion of the operation.

Initial setting of DSMIF

Release standby of DSMIF0, AIR and ABFG in ADCK.
Disable the detection upper / lower limit of DSMIF0.
Set DSMOP of DSMIF0.
Enable FIR filters in DSMOP.
Set channel 0 of DSMIF0.
Set offset of channel 0 of DSMIF0.
Enable DSMIF with DSMIFnCMON.

Initial setting of interrupt

Set AIR, INTC2 configuration.
Use INT_DSMIF0UPDATE0 (INTAIRINTREQ59(EIC496)Resource 0)

PORT setting

PORT setting for clock output and data stream input.

ABFG setting

Set ABFG configuration.

DSMIF start

Enable interrupt.
After enable the interrupt, output data is collected in every interrupt for data updates by CPU.

Data read

In INT_DSMIF0UPDATE0interrupt , CPU reads DSMIFnMONm register.

Operation flow

The flowchart of this operation example is shown below.

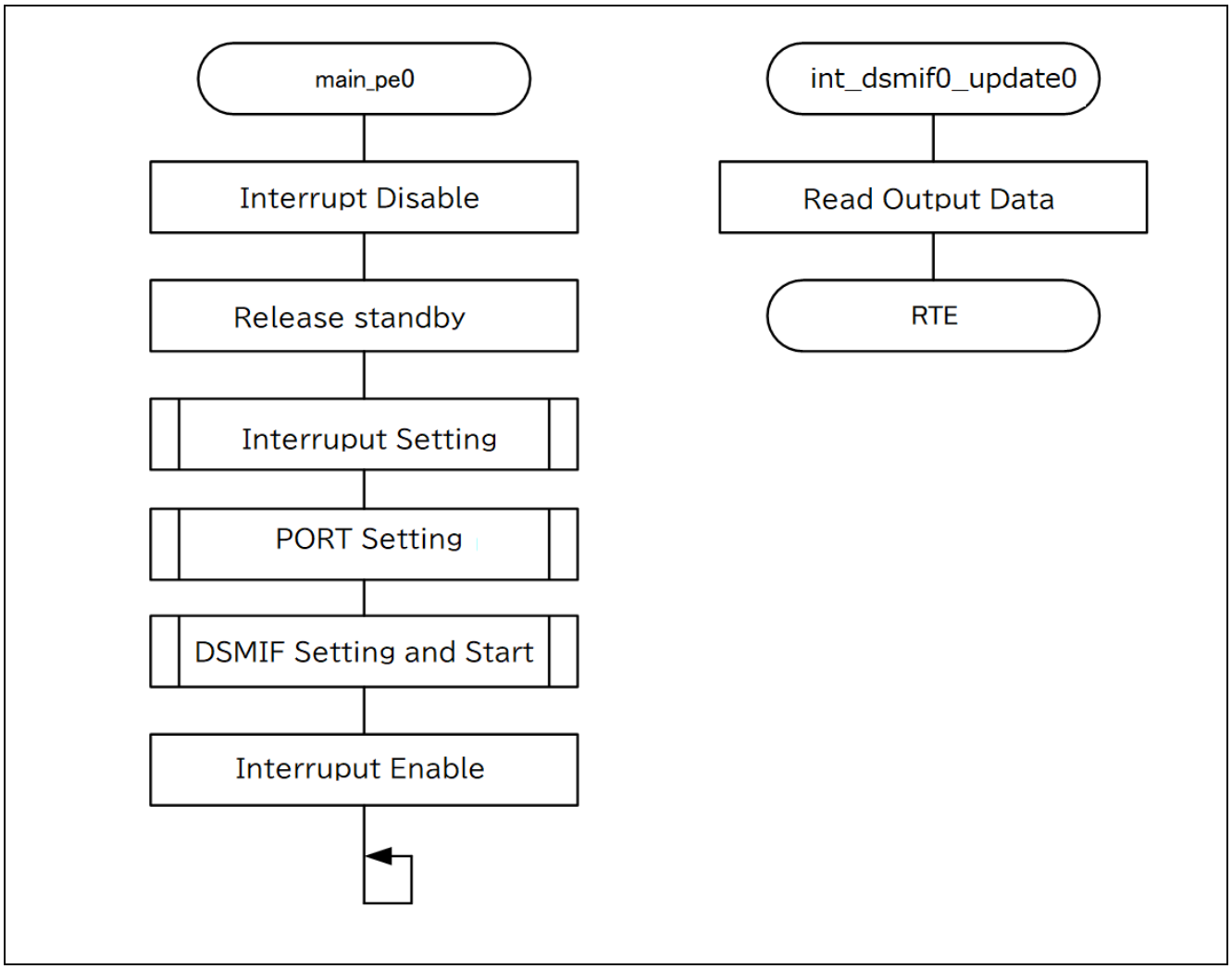


Figure 3-2 Operation Flow

3.1.4 Output of DSMIF

Output of DSMOP (Output of FIR filters) can be monitored with DSMIFnMONm register.

The output value of DSMIFnMONm register is taken from -32768(0x8000)to 32767(0x7FFF) value in setting decimation ratio of SINC3=16, offset =0x8000. The relation between input duty to value in DSMIFnMONm register is shown below.

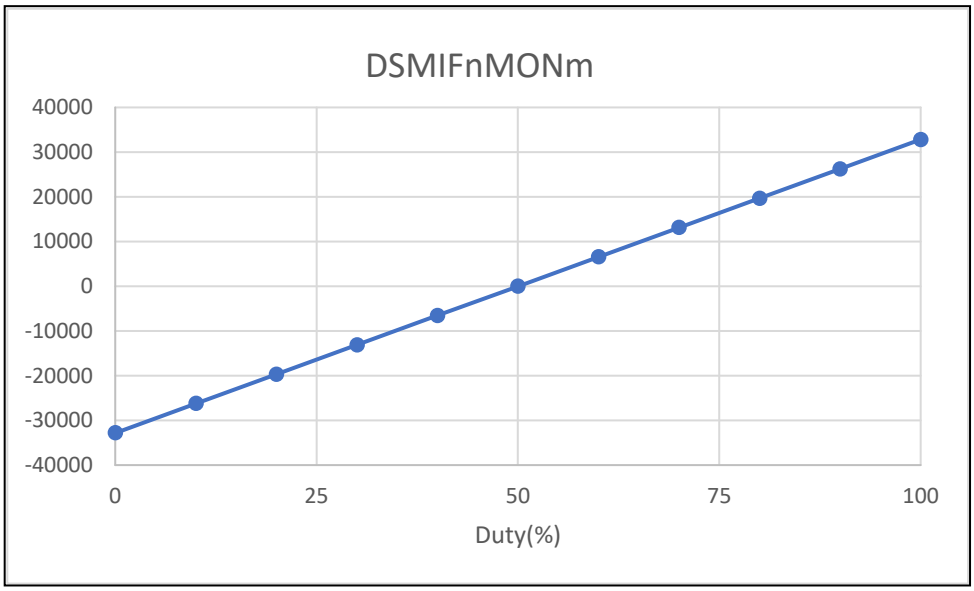


Figure 3-3 Output Value of DSMIFnMONm

Output of SINC filter of DSMIF can be monitored with DSMIFnDSCDRCHm register. DSMIFnDSCDRCHm register is taken value from 0 to 65520(0xFFF0) value in setting decimation ratio of SINC3=16. Since it does not go through the FIR filter, the delay is small, but the values have high-frequency components. The relation between input duty to data in DSMIFnDSCDRCHm register is shown below.

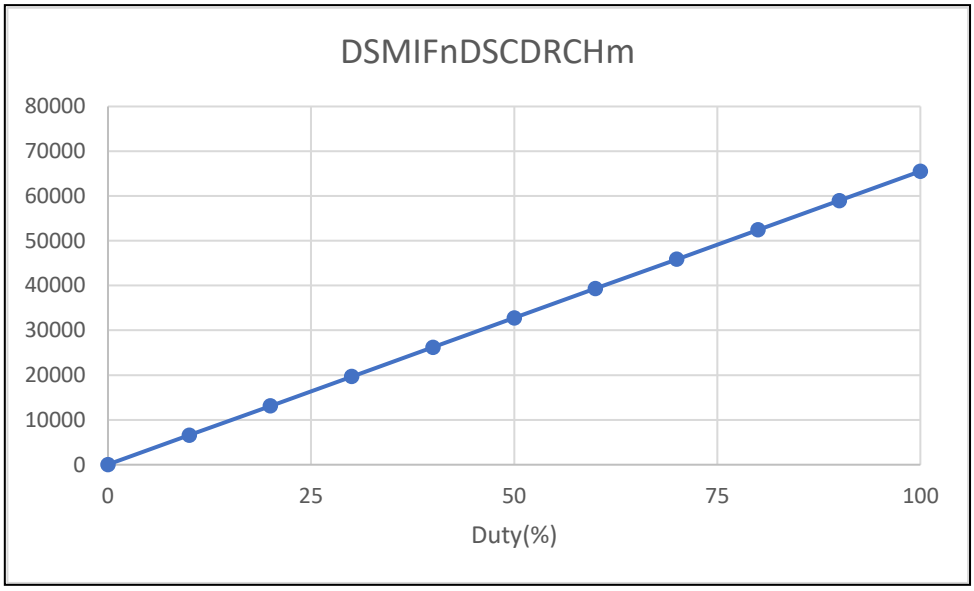


Figure 3-4 Output Value of DSMIFnDSCDRCHm

3.1.5 Description of sample software

- Description of modules in sample software

Below is a list of modules for this operation example.

Table 3-1 List of Modules

Module name	Label	Function
Main	main_pe0	Main function of application. Call functions for setting and run the application.
DSMIF Initialize	dsmif0_init	Initialize the DSMIF0.
Interrupt Initialize	intc_init	Initialize the interrupt of DSMIF0.
ABFG Initialize	dsmif0_abfg_init	Initialize ABFG related to DSMIF0.
DSMIF interrupt service function	int_dsmif0_update0	Read output data in INT_DSMIF0UPDATE0 interrupt.
PORT Initialize	port_init	Initialize PORT.

- Register setting

Settings for each register used in this operation example are shown in Table 3-2 Example of DSMIF0 Register Settingsto Table 3-5 Example of PORT Register Settings.

Table 3-2 Example of DSMIF0 Register Settings

Register Name	Set Value	Description
DSMIF0CCFG	0x00000000	Disable Comparator function
DSMIF0CFG0	0x00010100	SMPMD :0 Normal mode
		INV :0 Not invert
		PS :0 Port group 0 select
		F1D :0 Filter 1 output decimation is 1:1
		F0D :1 Filter 2 output decimation is 2:1
		RSEL[1:0]:01B DFE request masked. Interrupt generates
		F1B, F0B: 0,0 FIR1,FIR0 enable
DSMIF0FER0	0x00000001	EN:1 Postfilter enable
DSMIF0DSOCLTRCH0	0x00000100	Overcurrent detection lower limit
DSMIF0DSOCHTRCH0	0x0000FEFF	Overcurrent detection upper limit
DSMIF0.DSCMCCRCH0	0x00000401	CKDIV[5:0] : 0x04 20MHz
		SEDGE :0 Capture at the negative edge
		CKDIR :1 Master mode
DSMIF0DSCMFCRCH0	0x000C0F00	CMSH :Data shift setting 0xC: [11:0]<<4
		CMDEC : 0x0F Decimation ratio for current measurement = 16
		CMSINC[1:0]: 00B: Sinc3 (3rd order)
DSMIF0.DSOCFCRCH0	0x000C0F00	Same with DSCMFCRCH0 Setting (Not used)
DSMIF0IOF0	0x00008000	Offset 0x8000 (Range of DSMIFnMONm is -32768～32767)
DSMIF0DSCSTRTR	0x00000001	CH0 Enable
DSMIF0DSODCRCH0	0x00000003	Upper/Lower limit detection enable
DSMIF0CMON	0x00000000	Clear CMON
DSMIF0CIEN	0x00000000	Interrupts of comparator disabled

Table 3-3 Example of ABFG Register Settings

Register Name	Set Value	Description
ABFG.BFGCR0	0x020100DC	CHS 220 Upper limit
		BTGC 10B
		BPGC 01B
ABFG.CNTCR0	0x10000101	ABFGENB 1
		NRMCNT 1
		ERRCNT 1
ABFG.BFGCR1	0x030100DE	ABFGCHS 222 inbound
		BTGC 11B inverted
		BPGC 01B
ABFG.CNTCR1	0x10000101	Same to ABFG.CNTCR0
ABFG.BFGCR2	0x020100DE	ABFGCHS 222 outbound
		BTGC 10B
		BPGC 01B
ABFG.CNTCR2	0x10000101	Same to ABFG.CNTCR0
ABFG.BFGCR3	0x020100DE	CHS 221 Lower limit
		BTGC 10B
		BPGC 01B
ABFG.CNTCR3	0x10000101	Same to ABFG.CNTCR0

Table 3-4 Example of Interrupt Register Settings

Register Name	Set Value	Description
EIBD496	0x00000000	Bind the interrupt to PE0 (CPU0)
EIC496	0x0040	Use Table reference method, Priority 0
AIRISELR1	0xF7800000	Select Resource 0 at INTAIRINTREQ59

Table 3-5 Example of PORT Register Settings

Register Name	Set Value	Description
PORT0.PCR22_7	0x00000040	Alternative output mode 1 (ALT-OUT1) *Need to release protection to set
PORT0.PCR22_8	0x0000005A	Alternative input mode 11 (ALT-IN11) *Need to release protection to set

3.2 Basic Operation(Slave Mode)

In this example, how to reception the data stream, bandwidth adjustment, interrupt output is described with sample software.

Sample software Project :CSP_U2B10_Sample_DSMIF_S

3.2.1 Specification and outline of operation

In this example, channel 0 of DSMIF0 is used with slave mode. It receives the data stream, adjust the bandwidth by DSMOP, and notifies the conversion completion by interrupt.

The specifications of this example are as follows.

Setting of DSMIF

- Channel and Port group for reception of DSMOP : Port group 0 of Channel 0
- Reception mode, sampling clock frequency, edge setting : Slave mode, 20MHz, Use negative edge.
- SINC Setting :SINC3. Decimation ratio = 16
- The upper and lower limit detection function works, but the interrupts are not generated.

DSMOP Setting

- Use FIR0 Decimation ratio 2
- Use FIR1 Decimation ratio 1 (No decimation)

Frequency of output data from DSMIF

Setting: Sampling frequency of bit stream: 20MHz
SINC Setting: SINC3, Decimation ratio= 16
Decimation ratio: FIR0= 2 , FIR1= 1

Frequency of output data from DSMIF = Sampling frequency of bit stream / SINC Decimation ratio / FIR0 Decimation ratio / FIR1 Decimation ratio
=20MHz / 16 / 2/ 1 = 625kHz (period 1.6 μ s)

An interrupt generates in the data output cycle. Conversion results are overwritten when that were not read.

3.2.2 Used Functions

The hardware functions used in this operation example are shown below.

- Delta-Sigma Modulator Interface(DSMIF,DSMOP)
- ADC Interrupt Router (AIR)
- ABFG
- INTC2

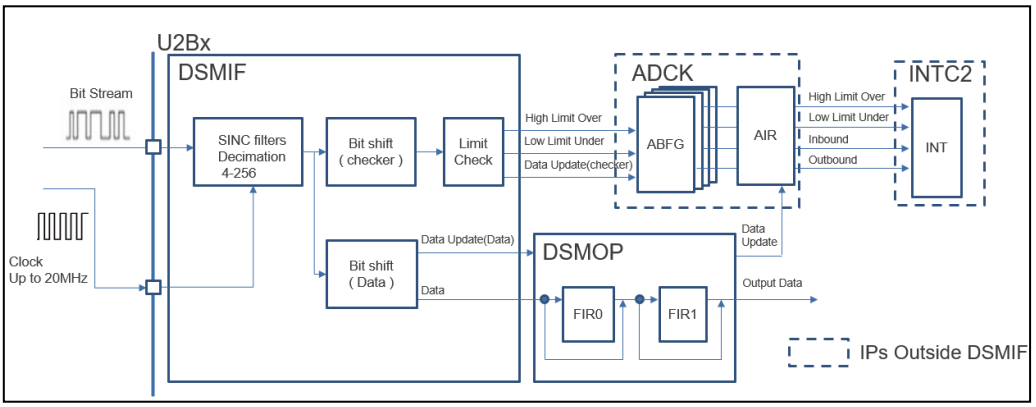


Figure 3-5 Hardware Configuration (Slave mode)

3.2.3 Explain of sample software

The Slave mode operation is almost same with Master mode operation. This sample software performs the reception of data stream by using channel 0 of the DSMIF0 module, filtering, and generation interrupt to notify the conversion completion of the operation.

Initial setting of DSMIF

Release standby of DSMIF0, AIR and ABFG in ADCK.
Disable the detection upper / lower limit of DSMIF0.
Set DSMOP of DSMIF0.
Enable FIR filters in DSMOP.
Set channel 0 of DSMIF0.
Set offset of channel 0 of DSMIF0.
Enable DSMIF with DSMIFnCMON.

Initial setting of interrupt

Set AIR, INTC2 configuration.
Use INT_DSMIF0UPDATE0 (INTAIRINTREQ59(EIC496)Resource 0)

PORT setting

PORT setting for clock and data stream input.

ABFG setting

Set ABFG configuration.

DSMIF start

Enable interrupt.
After enable the interrupt, output data is collected in every interrupt for data updates by CPU.

Data read

In INT_DSMIF0UPDATE0interrupt , CPU reads DSMIFnMONm register.

Operation flow

The flowchart is same as Master mode.

3.2.4 Description of sample software

- Description of modules in sample software

Below is a list of modules for this operation example.

Table 3-6 List of Modules

Module name	Label	Function
Main	main_pe0	Main function of application. Call functions for setting and run the application.
DSMIF Initialize	dsmif0_init	Initialize the DSMIF0.
Interrupt Initialize	intc_init	Initialize the interrupt of DSMIF0.
ABFG Initialize	dsmif0_abfg_init	Initialize ABFG related to DSMIF0.
DSMIF interrupt service function	int_dsmif0_update0	Read output data in INT_DSMIF0UPDATE0 interrupt.
PORT Initialize	port_init	Initialize PORT.

- Register setting

Settings for each register used in this operation example are shown in Table 3-7 to Table 3-10.

Table 3-7 Example of DSMIF0 Register Settings

Register Name	Set Value	Description
DSMIF0CCFG	0x00000000	Disable Comparator function
DSMIF0CFG0	0x00010100	SMPMD :0 Normal mode
		INV :0 Not invert
		PS :0 Port group 0 select
		F1D :0 Filter 1 output decimation is 1:1
		F0D :1 Filter 2 output decimation is 2:1
		RSEL[1:0]:01B DFE request masked. Interrupt generates
		F1B, F0B: 0,0 FIR1,FIR0 enable
DSMIF0FER0	0x00000001	EN:1 Postfilter enable
DSMIF0DSOCLTRCH0	0x00000100	Overcurrent detection lower limit
DSMIF0DSOCHTRCH0	0x0000FEFF	Overcurrent detection upper limit
DSMIF0.DSCMCCRCH0	0x00000400	CKDIV[5:0] : 0x04 20MHz
		SEDGE :0 Capture at the negative edge
		CKDIR :0 Slave mode
DSMIF0DSCMFCRCH0	0x000C0F00	CMSH :Data shift setting 0xC: [11:0]<<4
		CMDEC : 0x0F Decimation ratio for current measurement = 16
		CMSINC[1:0]: 00B: Sinc3 (3rd order)
DSMIF0.DSOCFCRCH0	0x000C0F00	Same with DSCMFCRCH0 Setting (Not used)
DSMIF0IOF0	0x00008000	Offset 0x8000 (Range of DSMIFnMONm is -32768～32767)
DSMIF0DSCSTRTR	0x00000001	CH0 Enable
DSMIF0DSODCRCH0	0x00000003	Upper/Lower limit detection enable
DSMIF0CMON	0x00000000	Clear CMON
DSMIF0CIEN	0x00000000	Interrupts of comparator disabled

Table 3-8 Example of ABFG Register Settings

Register Name	Set Value	Description
ABFG.BFGCR0	0x020100DC	CHS 220 Upper limit
		BTGC 10B
		BPGC 01B
ABFG.CNTCR0	0x10000101	ABFGENB 1
		NRMCNT 1
		ERRCNT 1
ABFG.BFGCR1	0x030100DE	ABFGCHS 222 inbound
		BTGC 11B inverted
		BPGC 01B
ABFG.CNTCR1	0x10000101	Same to ABFG.CNTCR0
ABFG.BFGCR2	0x020100DE	ABFGCHS 222 outbound
		BTGC 10B
		BPGC 01B
ABFG.CNTCR2	0x10000101	Same to ABFG.CNTCR0
ABFG.BFGCR3	0x020100DE	CHS 221 Lower limit
		BTGC 10B
		BPGC 01B
ABFG.CNTCR3	0x10000101	Same to ABFG.CNTCR0

Table 3-9 Example of Interrupt Register Settings

Register Name	Set Value	Description
EIBD496	0x00000000	Bind the interrupt to PE0 (CPU0)
EIC496	0x0040	Use table reference method, Priority 0
AIRISELR1	0xF7800000	Select Resource 0 at INTAIRINTREQ59

Table 3-10 Example of PORT Register Settings

Register Name	Set Value	Description
PORT0.PCR22_7	0x00000050	Alternative input mode 1 (ALT-IN1) *Need to release protection to set
PORT0.PCR22_8	0x0000005A	Alternative input mode 11 (ALT-IN11) *Need to release protection to set

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2023.XX.XX	-	First edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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