RH850/U2B6

TAUD Operation Examples

Introduction

This application note describes examples of PWM waveform outputs (including standard PWM, complementary PWM, push-pull PWM, variable phase PWM, and multi-phase PWM) using the timer array unit D (TAUD) of RH850/U2B6 and examples of input pulse width measurement. The following describes the overview of PWM waveforms.

- Standard PWM (standard PWM waveform)
- Complementary PWM (Complementary PWM waveform with dead time)
- Push-Pull PWM (Same as complementary PWM, except that the waveform is changed by using dead time)
- Variable phase PWM (Output of waveforms shifted from the reference PWM waveform)
- Multi-phase PWM (Three-phase PWM waveforms of U, V, and W phases)

Examples of tasks and applications described in this application note have been verified. However, before using this timer array unit D, be sure to check operating environment.

Target Device

This application note applies to RH850/U2B6

Contents

1. Standard PWM

1.1 Overview

This section describes how to output the standard PWM waveform using the PWM output feature (one of TAUD's synchronous channel operation features). The PWM output feature can generate multiple PWM outputs by using a master channel and slave channels. The PWM cycle is set by the master channel. The duty is set by slave channels.

In this operation example, two channels (master channel and one slave channel) of the TAUD are used and the PWM waveform is output from a single pin. This section also describes how to continuously change the PWM waveform cycle and duty by using interrupts.

Figure 1-1 shows the schematic of the standard PWM output.

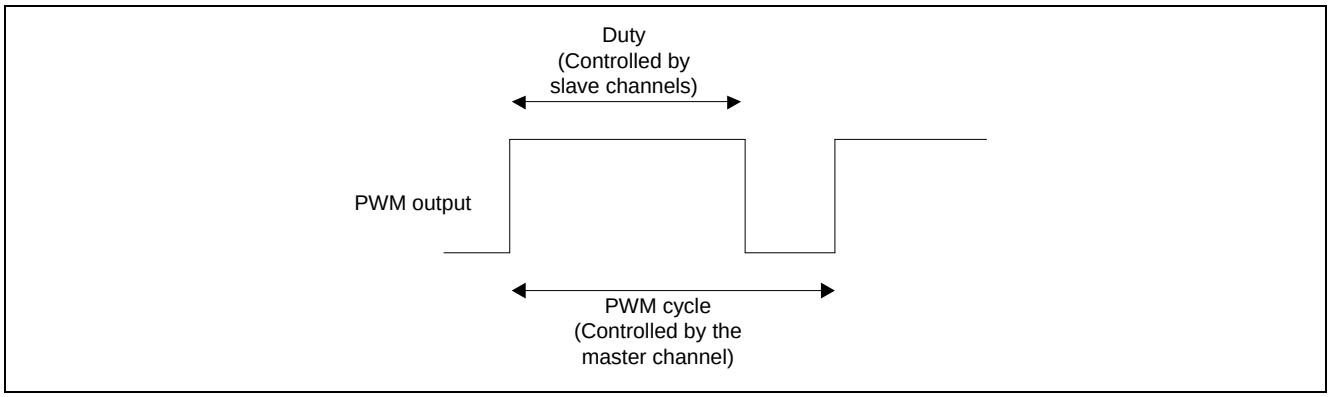


Figure 1-1 Schematic

1.2 Operating Conditions for Features Used

Operating conditions for features used in this operation example are provided below.

Table 1-1 Port Settings

Item	Description
Port to be used	P0_1: TAUD0O1

Table 1-2 Timer TAUD Settings

Item	Description
Feature to be used	PWM output feature of synchronous channel operation features
Clock supplied to TAUD	PLL output clock (80 MHz)
Master channel	Timer channel 0: PWM cycle control
Slave channel	Timer channel 1: Duty control
Timer operation clock	Prescaler output CK0 = (80 MHz) / 1

Table 1-3 Interrupt Settings

Item	Description
Interrupt method	Table reference method
INTTAUD0I0 interrupt	Enabled (Priority 7)

1.3 Operation

A method of how to change the PWM waveform cycle and duty continuously is shown in this operation example.

Table 1-4 lists output waveform patterns used in this operation example. Figure 1-2 shows the output waveform.

Table 1-4 PWM Output Waveform Patterns

Pattern No.	Cycle	Duty
1	50 us	12.5 us
2	50 us	18.75 us
3	50 us	25 us
4	75 us	12.5 us
5	75 us	25 us

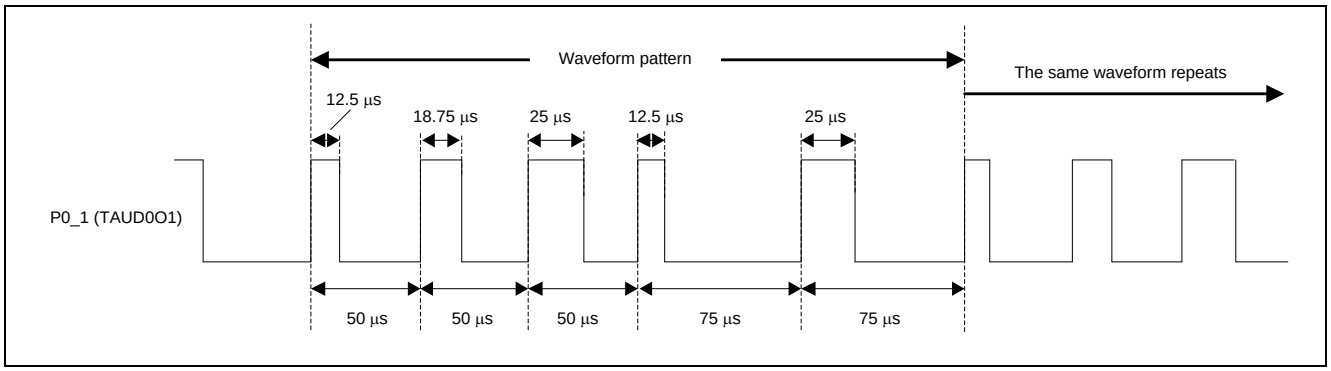


Figure 1-2 Output Waveform

The operation in Figure 1-2 is performed by the software which changes the PWM waveform cycle and duty of the next cycle at an interrupt generated at the beginning of the PWM cycle. Figure 1-3 illustrates hardware processing and software processing in an example that changes the PWM waveform output from "cycle T_a and duty D_a" to "cycle T_b and duty D_b" to ---.

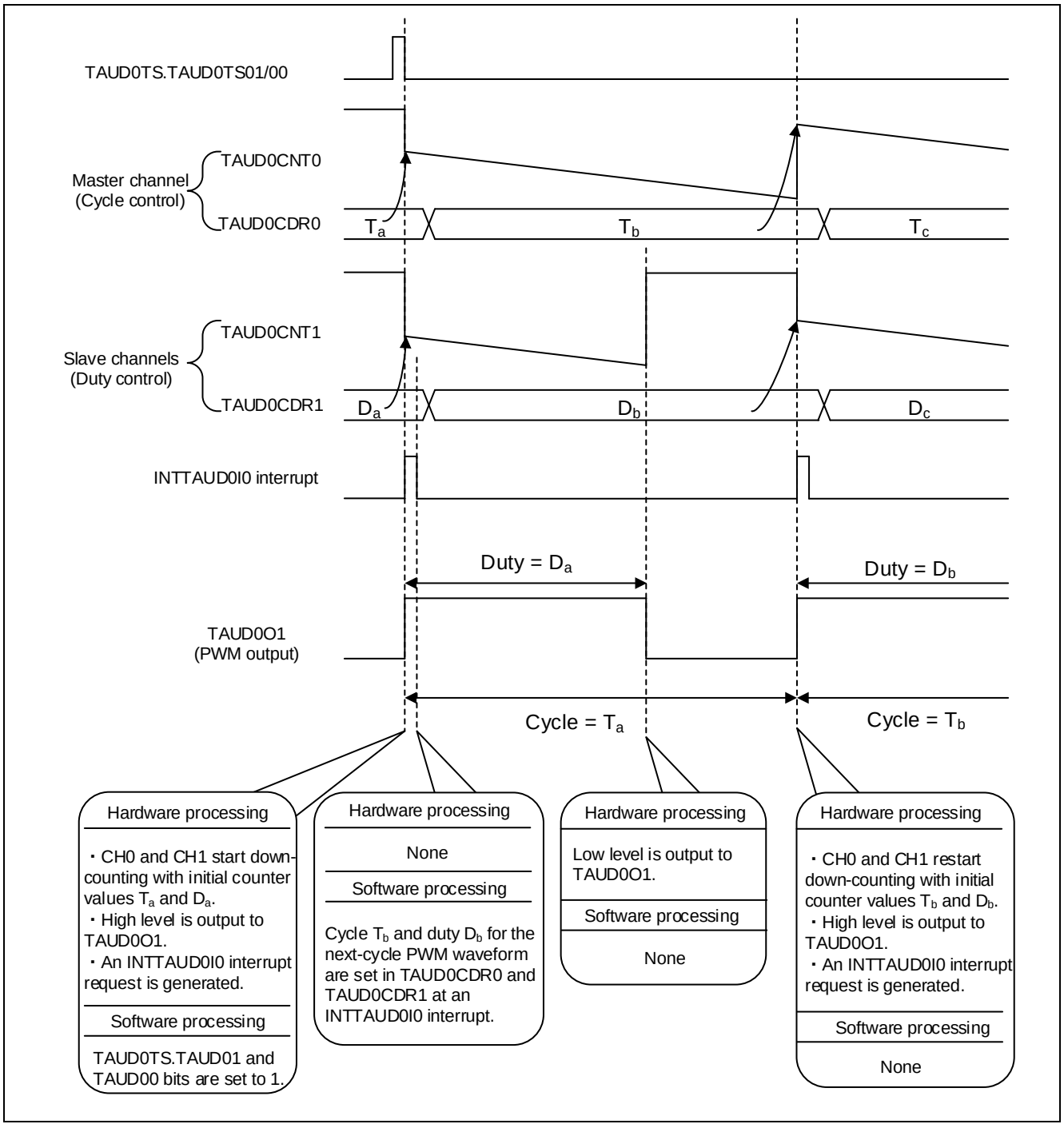


Figure 1-3 Description of Operations Used

1.1 Description of Software

Examples of settings for each register used in this operation example are provided in Table 1-5 to Table 1-7.

Table 1-5 Example of TAUD Register Settings

Register Name	Address	Set Value	Description
TAUD0 channel stop trigger register (TAUD0TT)	0xFFBF01C8	0x0003	This register stops counter operation of each channel. TAUD0TT15-02 0x0: No operation TAUD0TT01-00 0x1: Counter operation is stopped.
TAUD0 prescaler clock select register (TAUD0TPS)	0xFFBF0240	0x0000	This register specifies CK0, CK1, CK2, and CK3_PRE clocks of all channels of the PCLK prescaler. TAUD0PRS3-0[3:0] 0x0: PCLK/2^0
TAUD0 prescaler baud rate setting register (TAUD0BRS)	0xFFBF0244	0x00	This register specifies the division factor of the prescaler clock CK3. TAUD0BRS[7:0] 0x0: CK3_PRE/1
TAUD0 channel mode OS register (TAUD0CMOR0)	0xFFBF0200	0x0801	This register controls operation of Channel 0. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x1: Master channel TAUD0STS[2:0] 0x0: Software trigger TAUD0MD[4:0] 0x1: Interval timer mode INTTAUDnIm is output when count operation starts.
TAUD0 channel mode user register (TAUD0CMUR0)	0xFFBF00C0	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR0)	0xFFBF0000	0x0F9F 0x176F	Initial down-count value of TAUD0CNT0
TAUD0 channel mode OS register (TAUD0CMOR1)	0xFFBF0204	0x0409	This register controls operation of Channel 1. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x0: Slave channel TAUD0STS[2:0] 0x4: INTTAUDnIm of the master channel is a start trigger. TAUD0MD[4:0] 0x9: One-count mode Start trigger detection during counting is enabled.
TAUD0 channel mode user register (TAUD0CMUR1)	0xFFBF00C4	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge

TAUD0 channel data register (TAUD0CDR1)	0xFFBF0004	0x03E7 0x05DB 0x07CF	Initial down-count value of TAUD0CNT1
TAUD0 channel output enable register (TAUD0TOE)	0xFFBF005C	0x0000	Enables or disables independent channel output mode of software control. * Disable channel output before setting channel output setting. TAUD0TOE15-00 0x0: Independent timer output mode disabled
		0x0002	Enables or disables independent channel output mode of software control. * After the channel output setting is completed, necessary channel output is enabled. TAUD0TOE15-02/00 0x0: Independent timer output mode disabled TAUD0TOE01 0x1: Independent timer output mode enabled
TAUD0 channel output register (TAUD0TO)	0xFFBF0058	0x0000	This register specifies and reads the TAUDTTOUTm level. TAUD0TO15-00 0x0: Low level
TAUD0 channel output mode register (TAUD0TOM)	0xFFBF0248	0x0002	This register specifies output mode of each channel. TAUD0TOM01 0x1: Synchronous channel operation TAUD0TOM15-02/00 0x0: Independent channel operation
TAUD0 channel output configuration register (TAUD0TOC)	0xFFBF024C	0x0000	This register specifies output mode of each channel together with TAUDnTOMm. TAUD0TOC15-00 0x0: Operating mode 1
TAUD0 channel output level register (TAUD0TOL)	0xFFBF0040	0x0000	This register specifies the output logic of the channel output bits (TAUDnTO.TAUDnTOm). TAUD0TOL15-00 0x0: Positive logic (active high)
TAUD0 channel dead-time output enable register (TAUD0TDE)	0xFFBF0250	0x0000	This register enables or disables dead-time operation of all channels. TAUD0TDE15-00 0x0: Dead-time operation disabled
TAUDn channel dead-time output mode register (TAUD0TDM)	0xFFBF0254	0x0000	This register specifies the timing at which dead time is to be added during dead time output. TAUD0TDM15-00 0x0: When duty cycle of upper even channels is detected (duty dead time output)
TAUD0 channel dead-time output level register (TAUD0TDL)	0xFFBF0054	0x0000	This register selects a phase to which dead time is to be added. TAUD0TDL15-00 0x0: Positive phase
TAUD0 channel real-time output enable register (TAUD0TRE)	0xFFBF0258	0x0000	This register enables or disables real-time output. TAUD0TRE15-00 0x0: Real-time output disabled

TAUD0 channel real-time output register (TAUD0TRO)	0xFFBF004C	0x0000	This register sets the value to be output to TAUDTTOUTm. TAUD0TRO15-00 0x0: Low level
TAUD0 channel real-time output control register (TAUD0TRC)	0xFFBF025C	0x0000	This register controls real-time output triggers of each channel. TAUD0TRC15-00 0x0: The next upper channel of the channel for which this bit is set to 1
TAUD0 channel modulation output enable register (TAUD0TME)	0xFFBF0050	0x0000	This register enables or disables modulation of timer output and real-time output. TAUD0TME15-00 0x0: Modulation disabled
TAUD0 channel reload data enable register (TAUD0RDE)	0xFFBF0260	0x0003	This register enables or disables simultaneous rewriting of data registers TAUDnCDRm and TAUDnTOLm. TAUD0RDE15-02 0x0: Simultaneous rewriting disabled TAUD0RDE01-00 0x1: Simultaneous rewriting enabled
TAUD0 channel reload data control channel select register (TAUD0RDS)	0xFFBF0268	0x0000	This register selects a channel that controls simultaneous rewriting. TAUD0RDS15-00 0x0: Master channel
TAUD0 channel reload data mode register (TAUD0RDM)	0xFFBF0264	0x0000	This register selects the timing that generates the simultaneous rewriting control signal. TAUD0RDM15-00 0x0: When the counter of the master channel starts counting
TAUD0 channel reload data control register (TAUD0RDC)	0xFFBF026C	0x0000	This register specifies the channel that generates the INTTAUDnIm signal to trigger simultaneous rewriting. TAUD0RDC15-00 0x0: Not used as a simultaneous rewriting trigger channel
TAUD0 channel start trigger register (TAUD0TS)	0xFFBF01C4	0x0003	This register enables counter operation of each channel. TAUD0TS15-02 0x0: No operation TAUD0TS01-00 0x1: Counter operation is enabled and TAUDnTEm in TAUDnTE is set to 1.
TAUDn channel reload data trigger register (TAUD0RDT)	0xFFBF0044	0x0003	This register triggers the simultaneous rewriting enable state. TAUD0RDT15-02 0x0: No operation TAUD0RDT01-00 0x1: The simultaneous rewriting enable flag (TAUDnRSFm) is set to 1 and the simultaneous rewriting trigger wait state is entered.

Table 1-6 Example of Port Register Settings

Register Name	Address	Set Value	Description
Port control register (PCR00_1)	0xFFD92004	0x00000045	This register enables all settings of a pin. PUCC, PDSC 0x0: Drive intensity low PBDC 0x0: Bidirectional mode disabled PIBC 0x0: Input buffer disabled PMC 0x1: Alternative mode PIPC 0x0: Software input/output control PM 0x0: Output mode (output enabled) PFCEAE, PFCAE, PFCE, PFC 0x5: Alternative output mode 6 (ALT-OUT6)

Table 1-7 Example of Interrupt Control Register Settings

Register Name	Address	Set Value	Description
EI level interrupt control register 10 (EIC10)	0xFFFC4014	0x0047	This register is provided for each EI level interrupt source to set interrupt control conditions for each source. EIMKn 0x0: Interrupt processing enabled EITBn 0x4: Table reference method EIPn 0x7: Priority 7

Lists of functions, variables, and constants used in this operation example are provided in Table 1-8 to Table 1-10.

Table 1-8 List of Functions

Function Name	Description
main0	Calls each function.
port_init	Sets the P0_1 pin to TAUD0O1 feature.
pwm_init	Makes initial settings for TAUD0.
pwm_start	Starts timers TAUD0 CH0 and CH1 for PWM output.
pwm_update_duty	Interrupt processing that takes place at each count start (start of PWM cycle) of TAUD0 CH0. This function modifies the PWM cycle and duty.

Table 1-9 List of Variables

Variable name	Description
mode	Index for reading the cnt_table array

Table 1-10 List of Constants

Constant Name	Description
cnt_table [5][2]	Array of specified PWM cycle and duty values

1.2 Operation Flow

Figure 1-4 shows the operation flow of this operation example.

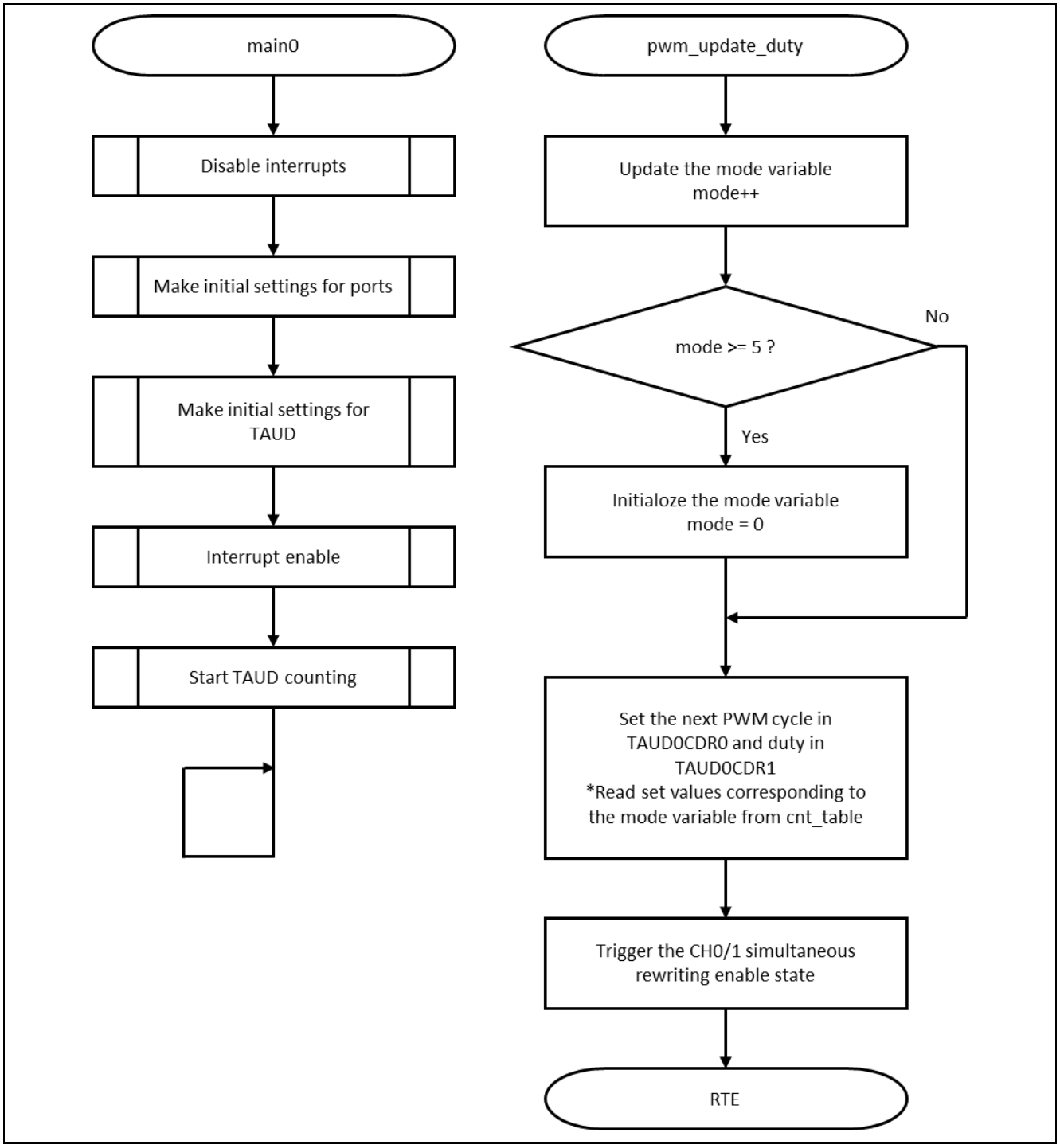


Figure 1-4 Operation Flow

2. Complementary PWM

2.1 Overview

This section describes how to output the complementary PWM by using the triangle PWM output feature with dead time (one of TAUD's synchronous channel operation features). The complementary PWM feature outputs PWM waveforms (positive phase and negative phase) from a pair of pins. The complementary PWM feature can insert dead time so that positive phase and negative phase do not become high level at the same time when output is inverted.

The carrier cycle is set by the master channel, the duty is set by combination of set values of the master channel and slave channels 2 and 3, and the dead time is set by slave channel 3.

In this operation example, three channels (master channel and two slave channels) of the TAUD are used and a pair of complementary PWM waveforms is output. This section also describes how to continuously change the carrier cycle, duty, and dead time by using interrupts.

Figure 2-1 shows the schematic of the complementary PWM output.

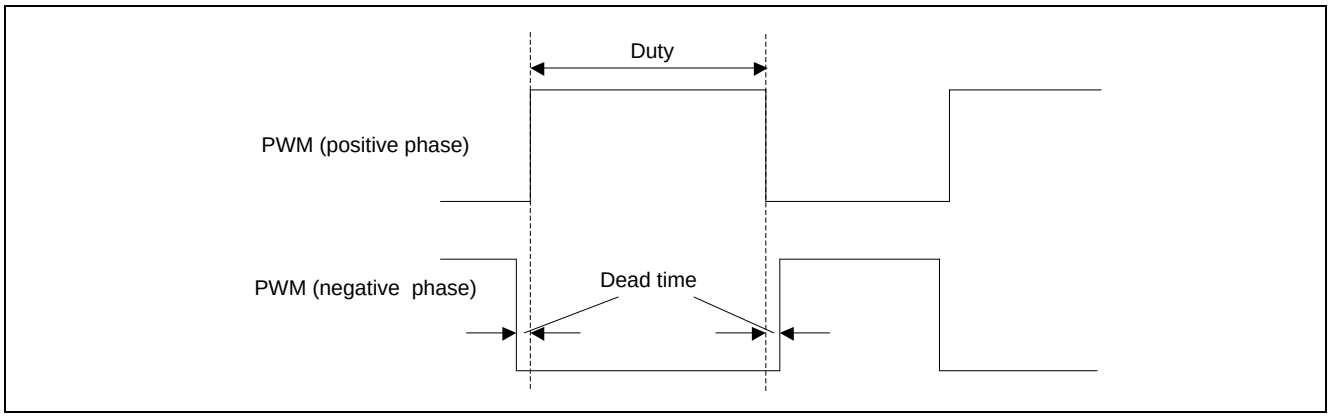


Figure 2-1 Schematic

2.2 Operating Conditions for Features Used

Operating conditions for features used in this operation example are provided below.

Table 2-1 Port Settings

Item	Description
Port to be used	P0_2: TAUD0O2 (positive phase) P0_3: TAUD0O3 (negative phase)

Table 2-2 Timer TAUD Settings

Item	Description
Feature to be used	Triangle PWM output feature with dead time (one of synchronous channel operation features)
Clock supplied to TAUD	PLL output clock (80 MHz)
Master channel	Timer channel 0: Controls the carrier cycle and duty.
Slave channel	Timer channel 2: Controls the duty.
	Timer channel 3: Controls the duty and dead time.
Timer operation clock	Prescaler output CK0 = (80 MHz) / 1

Table 2-3 Interrupt Settings

Item	Description
Interrupt method	Table reference method
INTTAUD0I0 interrupt	Enabled (Priority 7)

2.3 Operation

A method of how to change the PWM waveform carrier cycle, duty, and dead time continuously is shown in this operation example.

Table 2-4 lists output waveform patterns used in this operation example. Figure 2-2 shows output waveforms. The reason why the waveforms are not bilaterally symmetric in the carrier cycle is because the rise of the waveform is delayed by dead time (shift to the right side).

Table 2-4 Output Waveform Patterns

Pattern No.	Carrier Cycle	Duty	Dead Time
1	50 us	17.5 us	2.5 us
2	50 us	22.5 us	2.5 us
3	50 us	27.5 us	2.5 us
4	75 us	35 us	2.5 us
5	75 us	27.5 us	10 us

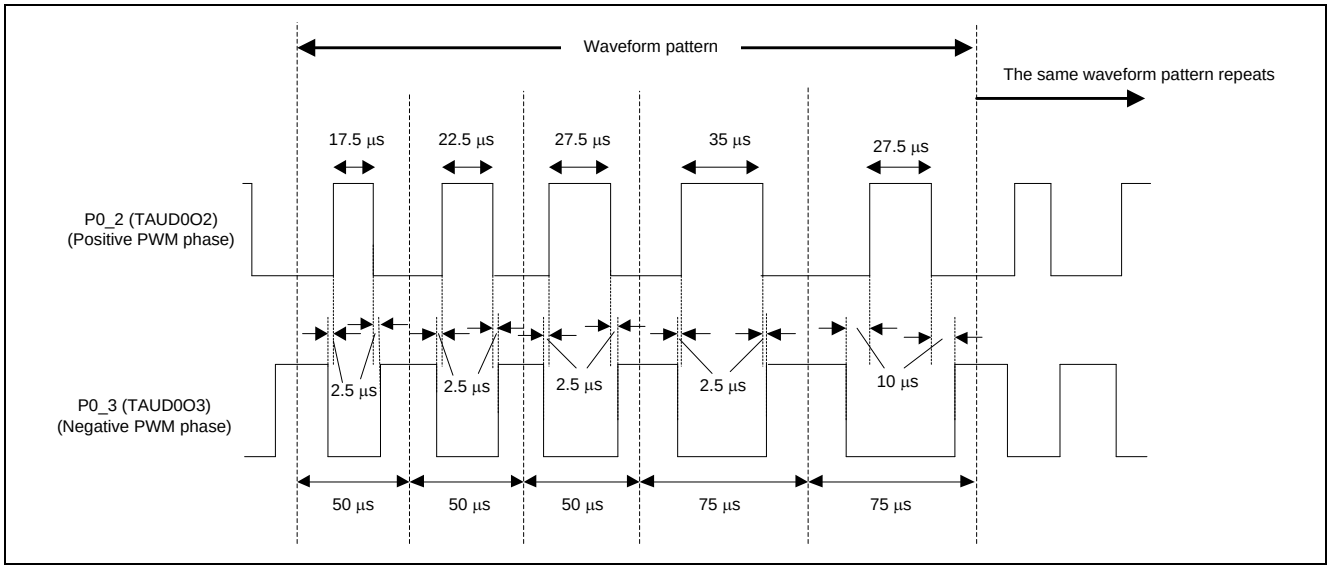


Figure 2-2 Output Waveforms

The operation in Figure 2-2 is performed by the software which changes the carrier cycle, duty, and dead time of the next cycle at an interrupt generated at the beginning of the PWM carrier cycle. Figure 2-3 illustrates hardware processing and software processing in an example that changes the PWM waveform output from "cycle T_a, duty D_a, and dead time DT_a" to "cycle T_b, duty D_b, and dead time DT_b" to ---.

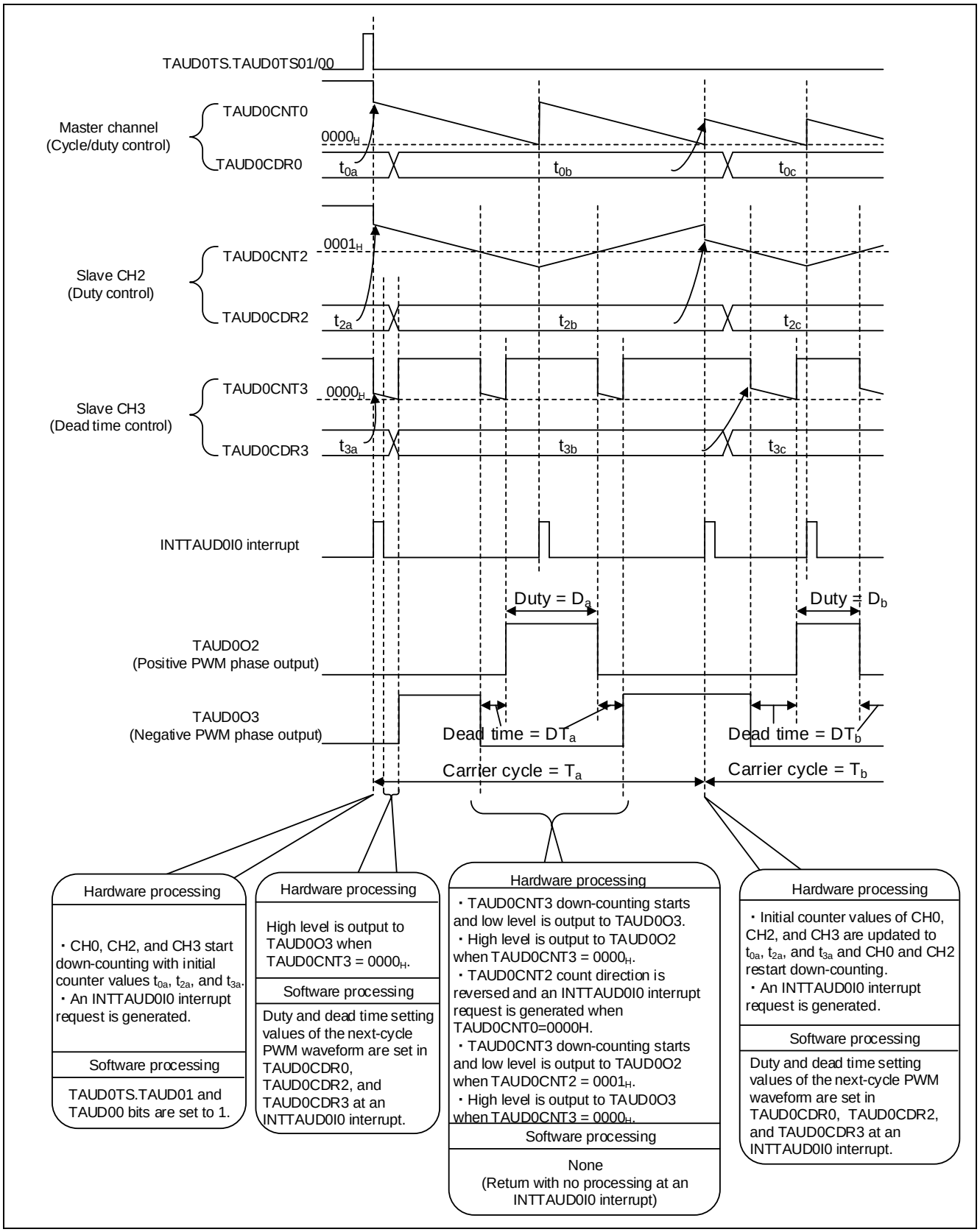


Figure 2-3 Description of Operations Used

2.4 Description of Software

Examples of settings for each register used in this operation example are provided in Table 2-5 to Table **2-7**.

Table 2-5 Example of TAUD Register Settings

Register Name	Address	Set Value	Description
TAUD0 channel stop trigger register (TAUD0TT)	0xFFBF01C8	0x000D	This register stops counter operation of each channel. TAUD0TT15-04, 01 0x0: No operation TAUD0TT03-02, 00 0x1: Counter operation is stopped.
TAUD0 prescaler clock select register (TAUD0TPS)	0xFFBF0240	0x0000	This register specifies CK0, CK1, CK2, and CK3_PRE clocks of all channels of the PCLK prescaler. TAUD0PRS3-0[3:0] 0x0: PCLK/2^0
TAUD0 prescaler baud rate setting register (TAUD0BRS)	0xFFBF0244	0x00	This register specifies the frequency division factor of prescaler clock CK3. TAUD0BRS[7:0] 0x0: CK3_PRE/1
TAUD0 channel mode OS register (TAUD0CMOR0)	0xFFBF0200	0x0801	This register controls operation of Channel 0. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x1: Master channel TAUD0STS[2:0] 0x0: Software trigger TAUD0MD[4:0] 0x1: Interval timer mode NTTAUDnIm is output when count operation starts.
TAUD0 channel mode user register (TAUD0CMUR0)	0xFFBF00C0	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR0)	0xFFBF0000	0x07CF 0x0BB7	Initial down-count value of TAUD0CNT0
TAUD0 channel mode OS register (TAUD0CMOR2)	0xFFBF0208	0x0712	This register controls operation of Channel 2. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x0: Slave channel TAUD0STS[2:0] 0x7: Up/down output trigger signal of the master channel TAUD0MD[4:0] 0x12: Up/down count mode The INTTAUDnIm signal is not output when count operation starts.
TAUD0 channel mode user register (TAUD0CMUR2)	0xFFBF0008	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR2)	0xFFBF020C	0x04AF 0x03E7 0x031F 0x05DB	Initial down-count value of TAUD0CNT2

TAUD0 channel mode OS register (TAUD0CMOR3)	0xFFBF00CC	0x0609	This register controls operation of Channel 3. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x0: Slave channel TAUD0STS[2:0] 0x6: Dead time output signal of the TAUDTTOUTm generation unit TAUD0MD[4:0] 0x9: One-count mode Start trigger detection during counting is enabled.
TAUD0 channel mode user register (TAUD0CMUR3)	0xFFBF000C	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR3)	0xFFBF005C	0x00C7 0x031F	Initial down-count value of TAUD0CNT3
TAUD0 channel output enable register (TAUD0TOE)	0xFFBF0058	0x0000	This register enables or disables independent channel output mode of software control. * Disable channel output before setting channel output setting. TAUD0TOE15-00 0x0: Independent timer output mode disabled
		0x000C	This register enables or disables independent channel output mode of software control. * After the channel output setting is completed, necessary channel output is enabled. TAUD0TOE15-04/01-00 0x0: Independent timer output mode disabled TAUD0TOE03-02 0x1: Independent timer output mode enabled
TAUD0 channel output register (TAUD0TO)	0xFFBF0248	0x0000	This register specifies and reads the TAUDTTOUTm level. TAUD0TO15-00 0x0: Low level
TAUD0 channel output mode register (TAUD0TOM)	0xFFBF024C	0x000C	This register specifies output mode of each channel. TAUD0TOM02-03 0x1: Synchronous channel operation TAUD0TOM15-04/01 0x0: Independent channel operation
TAUD0 channel output configuration register (TAUD0TOC)	0xFFBF0040	0x000C	This register specifies output mode of each channel together with TAUDnTOMm. TAUD0TOC15-00 0x0: Operating mode 1
TAUD0 channel output level register (TAUD0TOL)	0xFFBF00CC	0x0000	This register specifies the output logic of the channel output bits (TAUDnTO.TAUDnTOm). TAUD0TOL15-00 0x0: Positive logic (active high)
TAUD0 channel dead-time output enable register (TAUD0TDE)	0xFFBF0250	0x000C	This register enables or disables dead-time operation of all channels. TAUD0TDE02-03 0x1: Dead-time operation enabled TAUD0TDE15-04/01 0x0: Dead-time operation disabled
TAUDn channel dead-time output mode register (TAUD0TDM)	0xFFBF0254	0x0000	This register specifies the timing at which dead time is to be added during dead time output. TAUD0TDM15-00 0x0: When duty cycle of upper even channels is detected (duty dead time output)

TAUD0 channel dead-time output level register (TAUD0TDL)	0xFFBF0054	0x0008	This register selects a phase to which dead time is to be added. TAUD0TDL15-04/02-00 0x0: Positive phase TAUD0TDL03 0x1: Negative phase
TAUD0 channel real-time output enable register (TAUD0TRE)	0xFFBF0258	0x0000	This register enables or disables real-time output. TAUD0TRE15-00 0x0: Real-time output disabled
TAUD0 channel real-time output register (TAUD0TRO)	0xFFBF004C	0x0000	This register sets the value to be output to TAUDTTOUTm. TAUD0TRO15-00 0x0: Low level
TAUD0 channel real-time output control register (TAUD0TRC)	0xFFBF025C	0x0000	This register controls real-time output triggers of each channel. TAUD0TRC15-00 0x0: The next upper channel of the channel for which this bit is set to 1
TAUD0 channel modulation output enable register (TAUD0TME)	0xFFBF0050	0x0000	This register enables or disables modulation of timer output and real-time output. TAUD0TME15-00 0x0: Modulation disabled
TAUD0 channel reload data enable register (TAUD0RDE)	0xFFBF0260	0x000D	This register enables or disables simultaneous rewriting of data registers TAUDnCDRm and TAUDnTOLm. TAUD0RDE15-04/01 0x0: Simultaneous rewriting disabled TAUD0RDE03-02/00 0x1: Simultaneous rewriting enabled
TAUD0 channel reload data control channel select register (TAUD0RDS)	0xFFBF0268	0x0000	This register selects a channel that controls simultaneous rewriting. TAUD0RDS15-00 0x0: Master channel
TAUD0 channel reload data mode register (TAUD0RDM)	0xFFBF0264	0x000D	This register selects the timing that generates the simultaneous rewriting control signal. TAUD0RDM15-04/01 0x0: When the counter of the master channel starts counting TAUD0RDM03-02/00 0x1: At the peak of triangular wave cycle
TAUD0 channel reload data control register (TAUD0RDC)	0xFFBF026C	0x0000	This register specifies the channel that generates the INTTAUDnIm signal to trigger simultaneous rewriting. TAUD0RDC15-00 0x0: Not used as a simultaneous rewriting trigger channel
TAUD0 channel start trigger register (TAUD0TS)	0xFFBF01C4	0x000D	This register enables counter operation of each channel. TAUD0TS15-04/01 0x0: No operation TAUD0TS03-02/00 0x1: Counter operation is enabled and TAUDnTEm in TAUDnTE is set to 1.
TAUDn channel reload data trigger register (TAUD0RDT)	0xFFBF0044	0x000D	This register triggers the simultaneous rewriting enable state. TAUD0RDT15-04/01 0x0: No operation TAUD0RDT03-02/00 0x1: The simultaneous rewriting enable flag (TAUDnRSFm) is set to 1 and the simultaneous rewriting trigger wait state is entered.

Table 2-6 Example of Port Register Settings

Register Name	Address	Set Value	Description
Port control register (PCR0_2)	0xFFD92008	0x00000045	This register enables all settings of a pin. PUCC, PDSC 0x0: Drive intensity low PBDC 0x0: Bidirectional mode disabled PIBC 0x0: Input buffer disabled PMC 0x1: Alternative mode PIPC 0x0: Software input/output control PM 0x0: Output mode (output enabled) PFCEAE, PFCAE, PFCE, PFC 0x5: Alternative output mode 6 (ALT-OUT6)
Port control register (PCR0_3)	0xFFD9200C	0x00000045	This register enables all settings of a pin. PUCC, PDSC 0x0: Drive intensity low PBDC 0x0: Bidirectional mode disabled PIBC 0x0: Input buffer disabled PMC 0x1: Alternative mode PIPC 0x0: Software input/output control PM 0x0: Output mode (output enabled) PFCEAE, PFCAE, PFCE, PFC 0x0: Alternative output mode 6 (ALT-OUT6)

Table 2-7 Example of Interrupt Control Register Settings

Register Name	Address	Set Value	Description
EI level interrupt control register 10 (EIC10)	0xFFFC4014	0x0047	This register is provided for each EI level interrupt source to set interrupt control conditions for each source. EIMKn 0x0: Interrupt processing enabled EITBn 0x4: Table reference method EIPn 0x7: Priority 7

Lists of functions, variables, and constants used in this operation example are provided in Table 2-8 to Table 2-10.

Table 2-8 List of Functions

Function Name	Description
main0	Calls each function.
port_init	Sets P0_2 and P0_3 pins to TAUD0O2 feature and TAUD0O3 feature respectively.
pwm_init	Makes initial settings for TAUD0.
pwm_start	Starts timers TAUD0 CH0, CH2, and CH3 for PWM output.
pwm_update_duty	Interrupt processing that takes place at each count start (half carrier cycle) of TAUD0 CH0 This function modifies the PWM carrier cycle, duty, and dead time.

Table 2-9 List of Variables

Variable Name	Description
mode	Index for reading the cnt_table array

Table 2-10 List of Constants

Constant Name	Description
cnt_table[5][3]	Array of specified PWM carrier cycle, duty, and dead time values

2.5 Operation Flow

Figure 2-4 shows the operation flow of this operation example.

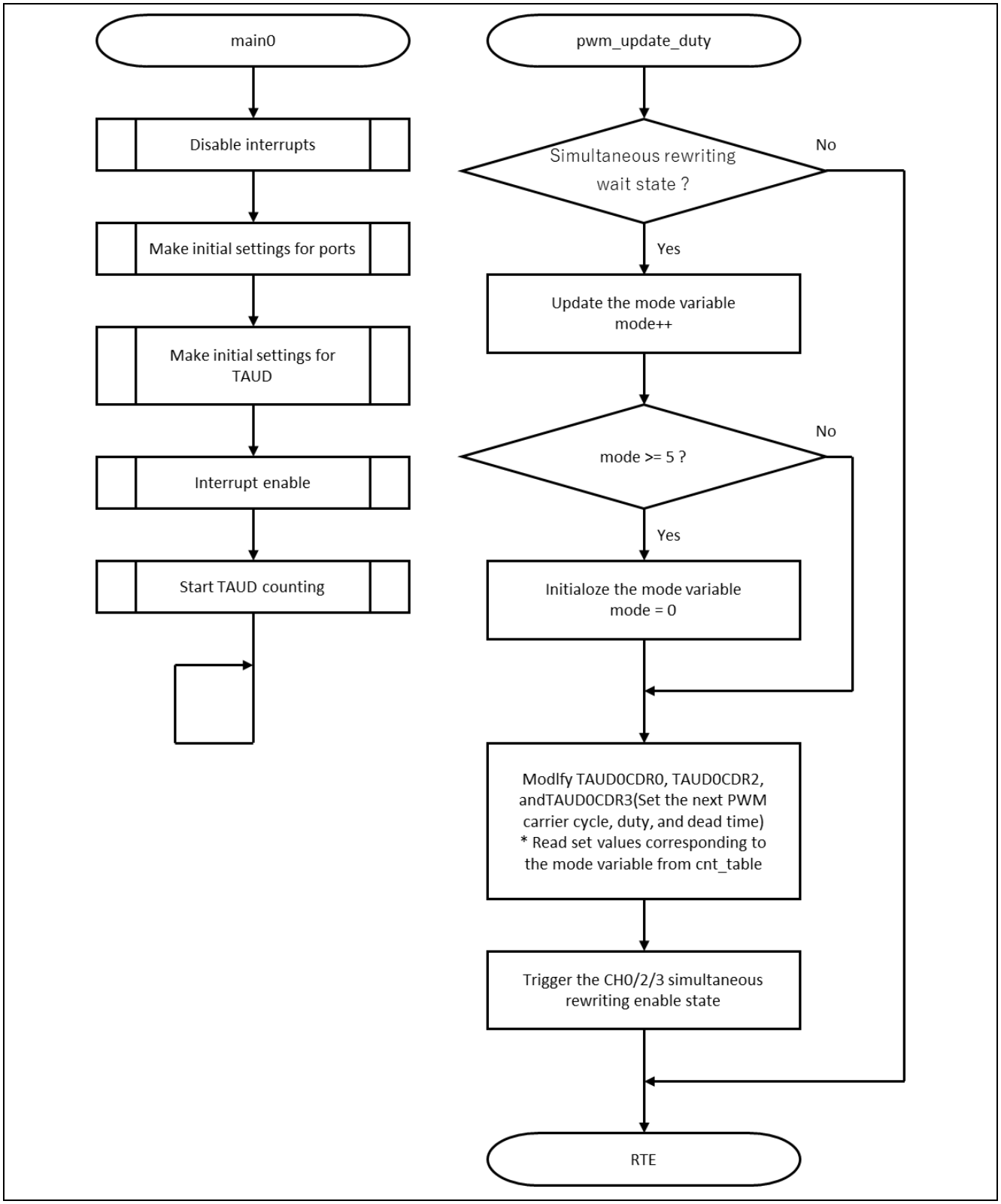


Figure 2-4 Operation Flow

3. Push-Pull PWM

3.1 Overview

Push-pull PWM waveforms can be output in the same way as Section 2, Complementary PWM.

Only set values of carrier cycle, duty, and dead time are different from those of the complementary PWM. In push-pull PWM waveforms, dead time is used to prevent simultaneous high level of positive phase and negative phase and also to ensure the simultaneous low level period of positive phase and negative phase.

Figure 3-1 shows the difference in the simultaneous low level period due to dead time.

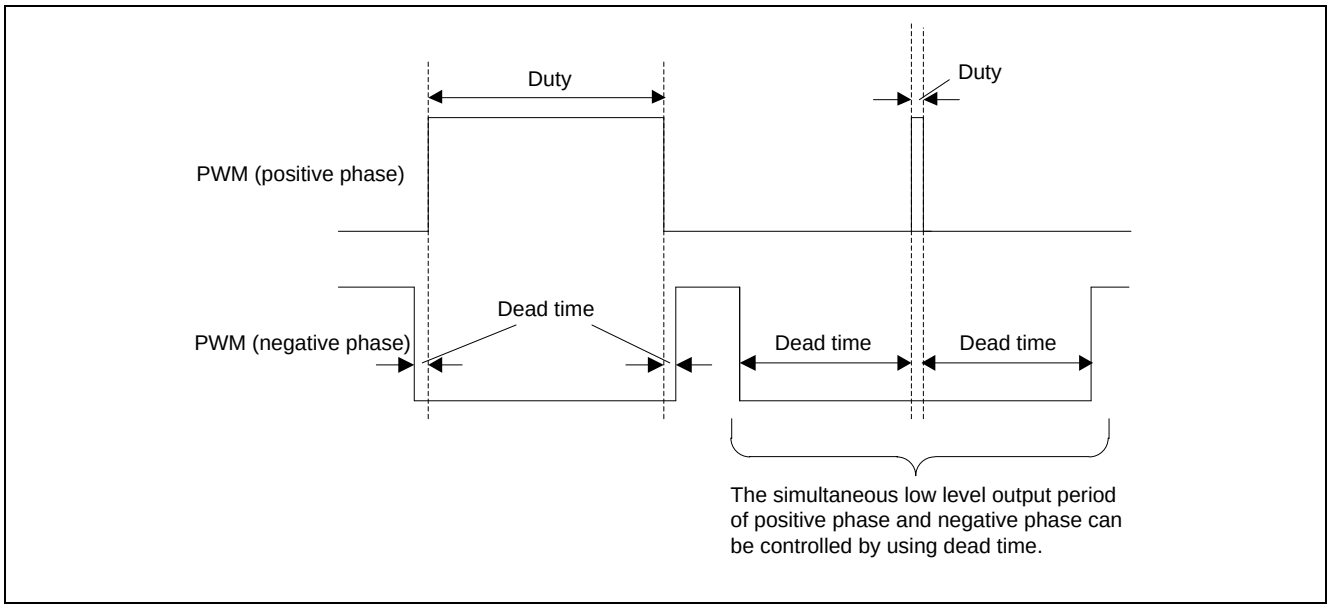


Figure 3-1 Schematic

3.2 Operating Conditions for Features Used

Operating conditions are the same as those for Section 2, Complementary PWM. See Section 2.2, Operating Conditions for Features Used.

3.3 Operation

Table 3-1 lists output waveform patterns used in this operation example. Figure 3-2 shows output waveforms.

Table 3-1 Output Waveform Patterns

Pattern No.	Carrier Cycle	Duty	Dead Time
1	50 us	22.5 us	2.5 us
2	50 us	12.5 us	12.5 us
3	50 us	2.5 us	22.5 us
4	75 us	2.5 us	35 us
5	75 us	22.5 us	15 us

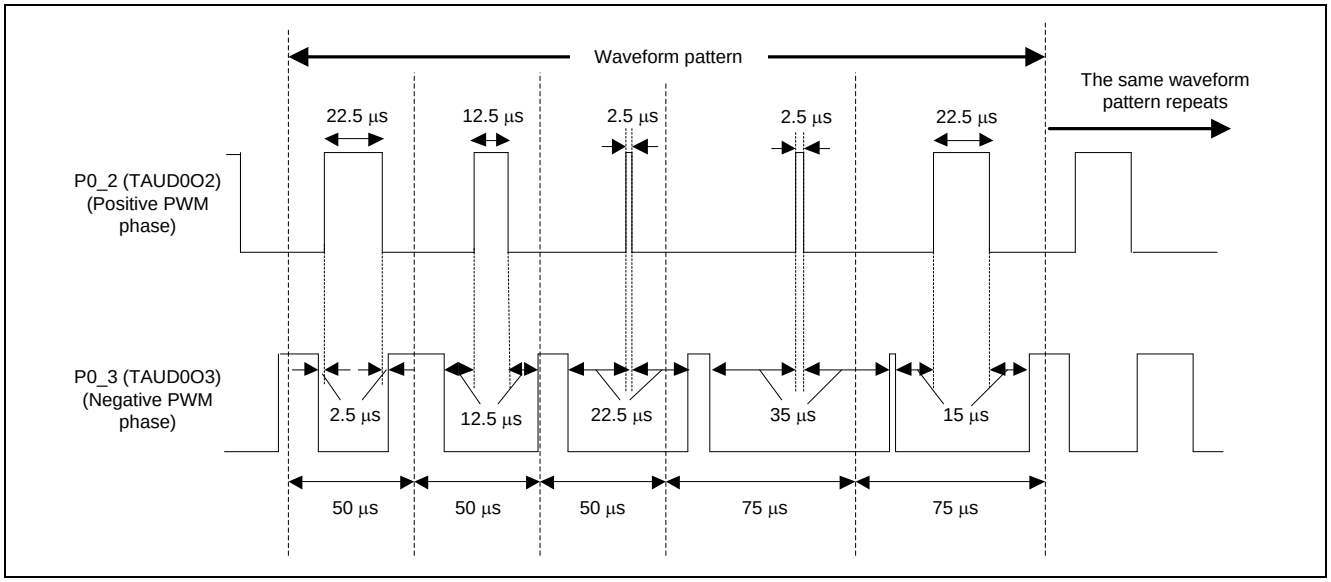


Figure 3-2 Output Waveforms

Operations used are the same as those of the complementary PWM. See Section 2.3, Operation.

3.4 Description of Software

The specified values of the push-pull PWM and the complementary PWM are the same except that the values of the TAUD0CDRm registers (Table 2-5 to

Table **2-7**). Table 3-2 lists only the set values of the TAUD0CDRm register. For set values of other registers, see Table 2-5 to

Table **2-7**.

Table 3-2 Example of TAUD Register Settings

Register Name	Address	Set Value	Description
TAUD0 channel data register (TAUD0CDR0)	0xFFBF0000	0x07CF 0x0BB7	Initial down-count value of TAUD0CNT0
TAUD0 channel data register (TAUD0CDR2)	0xFFBF0008	0x03E7 0x05DB	Initial down-count value of TAUD0CNT2
TAUD0 channel data register (TAUD0CDR3)	0xFFBF000C	0x00C7 0x03E7 0x0707 0x0AEF 0x04AF	Initial down-count value of TAUD0CNT3

Description of functions, variables, and constants used in the push-pull PWM operation example is the same as that in the complementary PWM operation example. For lists of functions, variables, and constants, see Table 2-8 to Table 2-10.

3.5 Operation Flow

The operation flow of the push-pull PWM is the same as that of the complementary PWM. See Section 2.5, Operation Flow.

4. Variable-Phase PWM

4.1 Overview

This section describes how to output the variable-phase PWM by using the delay pulse output feature (one of TAUD's synchronous channel operation features). In the variable-phase PWM, waveforms shifted from the reference PWM waveform phase can be output. The cycle is set by the master channel and the duty is set by odd slave channels. The shift time is set by even slave channels. Figure 4-1 shows the schematic of variable-phase PWM output.

In this operation example, eight channels (master channel and seven slave channels) of the TAUD are used and variable-phase PWM waveforms are output from four pins. This section also describes how to continuously change the cycle, duty, and shift time by using interrupts.

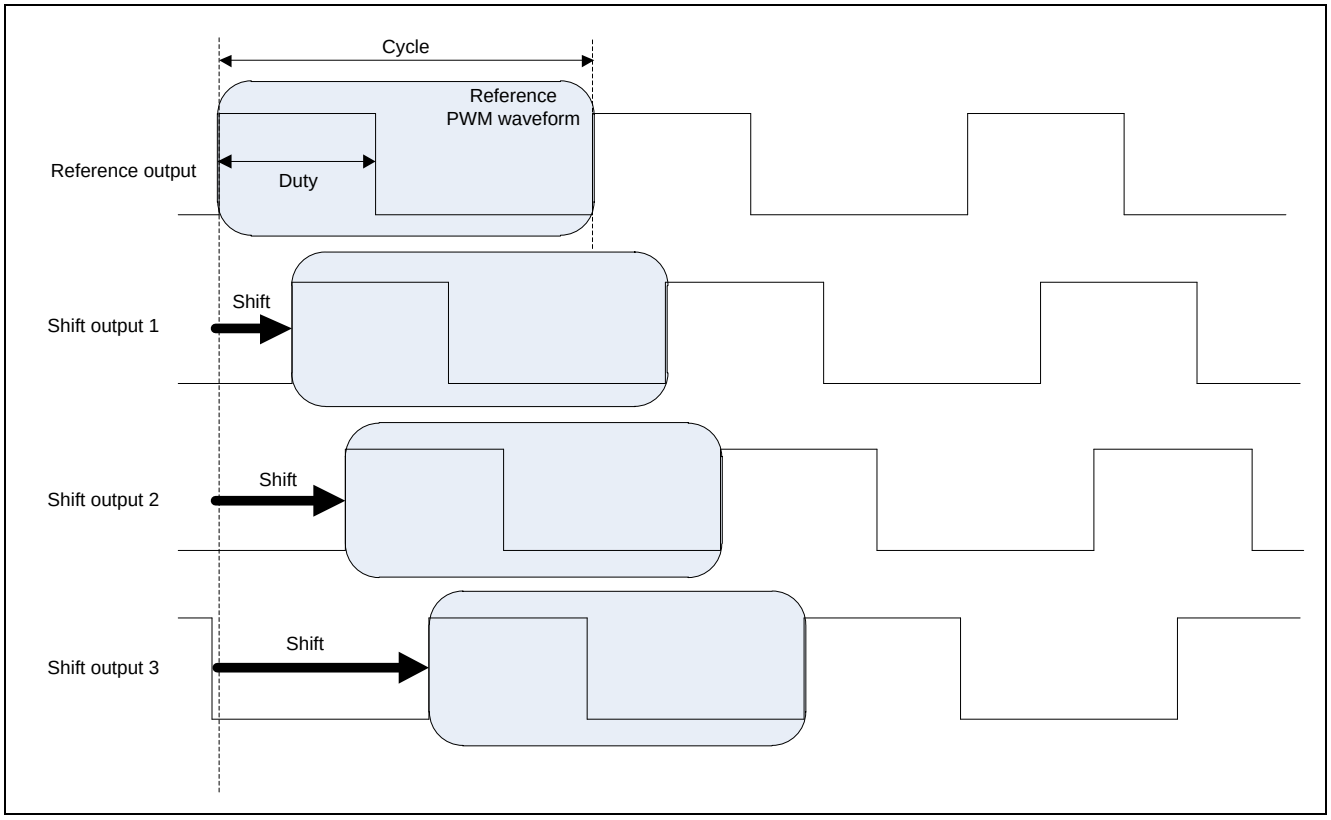


Figure 4-1 Schematic

4.2 Operating Conditions for Features Used

Operating conditions for features used in this operation example are provided below.

Table 4-1 Port Settings

Item	Description
Port to be used	P0_1: TAUD0O1 (Reference output) P0_3: TAUD0O3 (Shift output 1) P0_5: TAUD0O5 (Shift output 2) P0_7: TAUD0O7 (Shift output 3)

Table 4-2 Timer TAUD Settings

Item	Description
Function to be used	Delay pulse output feature of synchronous channel operation features
Clock supplied to TAUD	PLL output clock (80 MHz)
Master channel	Timer channel 0: Controls the cycle.
Slave channel	Timer channels 1, 3, 5, and 7: Control the duty.
	Timer channels 2, 4, and 6: Control the shift time.
Timer operation clock	Prescaler output CK0 = (80 MHz) / 1

Table 4-3 Interrupt Settings

Item	Description
Interrupt method	Table reference method
INTTAUD0I0 interrupt	Enabled (Priority 7)

4.3 Operation

A method of how to change the cycle, duty, and shift time of variable-phase PWM waveforms continuously is shown in this operation example.

Table 4-4 lists output waveform patterns used in this operation example. Figure 4-2 shows output waveforms.

Table 4-4 Output Waveform Patterns

Pattern No.	Cycle	Duty	Shift Time
1	50 us	22.5 us	Shift output 1: 5.6 us Shift output 2: 25 us Shift output 3: 30.6 us
2	50 us	22.5 us	Shift output 1: 11.3 us Shift output 2: 25 us Shift output 3: 36.3 us
3	50 us	22.5 us	Shift output 1: 16.9 us Shift output 2: 25 us Shift output 3: 41.9 us
4	50 us	20 us	Shift output 1: 10 us Shift output 2: 25 us Shift output 3: 35 us
5	75 us	32.5 us	Shift output 1: 16.3 us Shift output 2: 37.5 us Shift output 3: 53.8 us

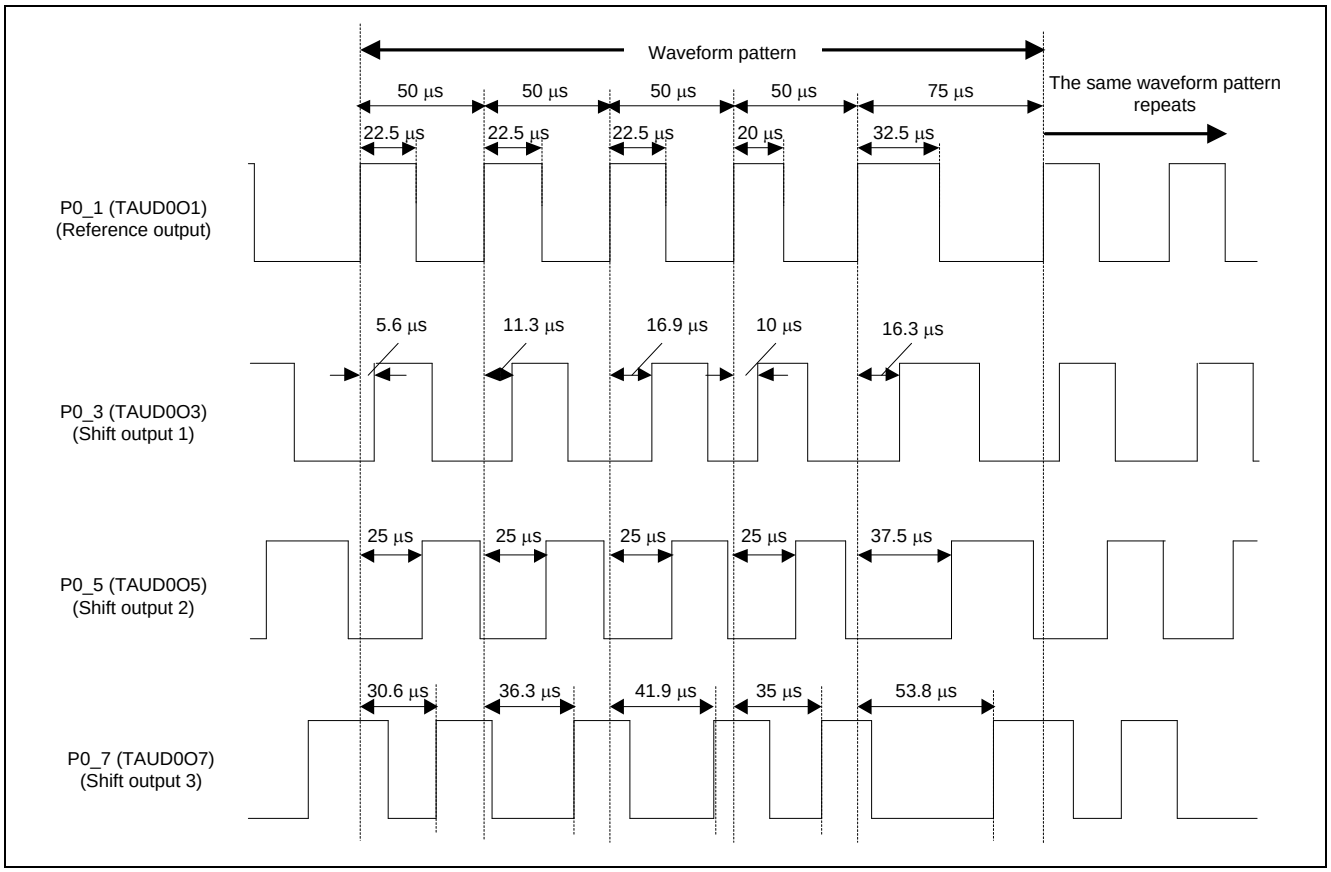


Figure 4-2 Output Waveforms

The operation in Figure 4-2 is performed by the software which changes the cycle, duty, and shift time of the next cycle at an interrupt generated at the beginning of the PWM cycle. Figure 4-3 illustrates hardware processing and software processing in an example that changes the PWM's reference output and shift output 1 from "cycle T_a, duty D_a, and shift time S_a" to "cycle T_b, duty D_b, and shift time S_b" to ---.

In this operation example, shift output 2 and shift output 3 are also generated in addition to shift output 1, which is achieved by increasing the number of slave channels to be used with the method shown in Figure 4-3.

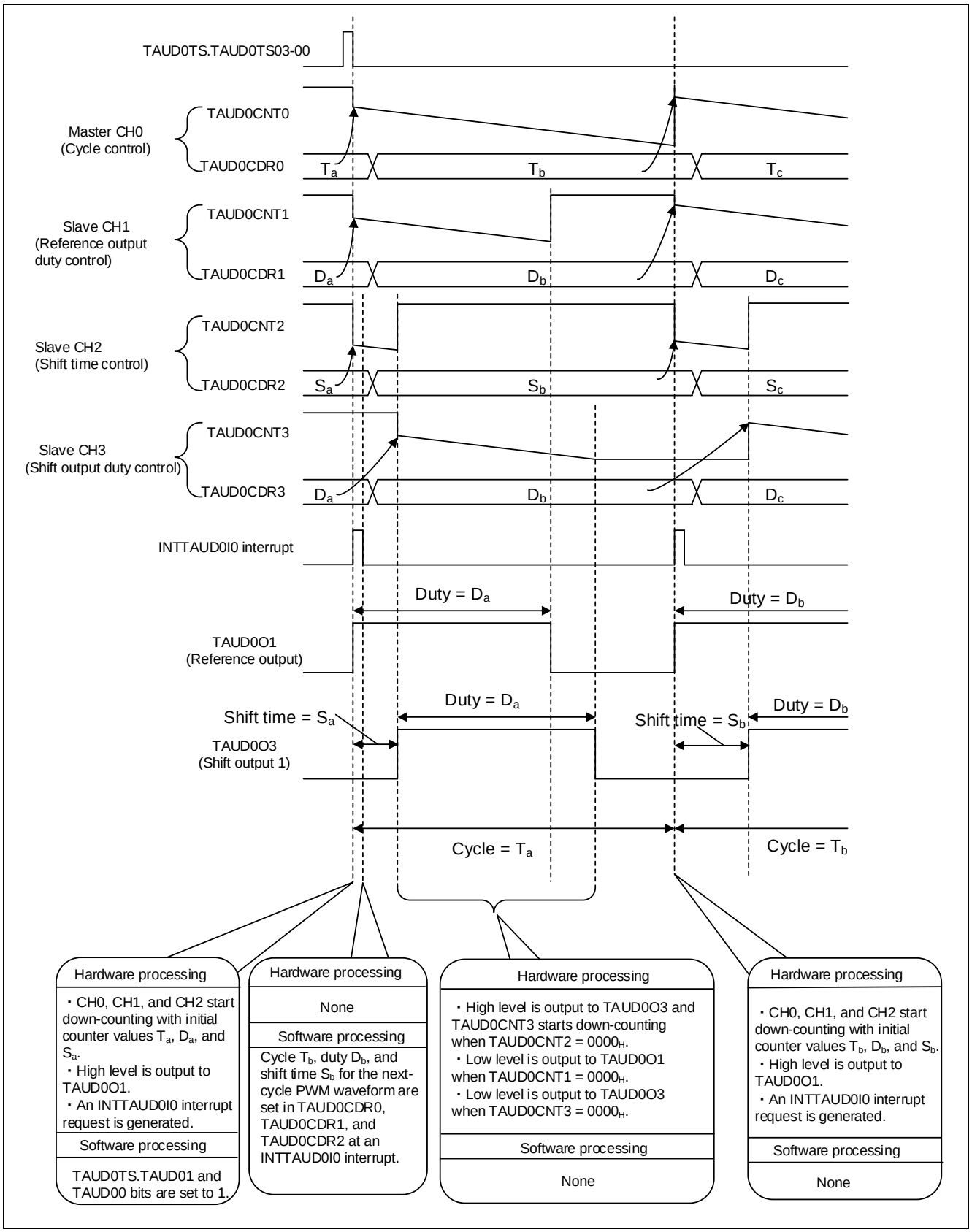


Figure 4-3 Description of Operations Used

4.4 Description of Software

Examples of settings for each register used in this operation example are provided in Table 4-5 to Table 4-7.

Table 4-5 Example of TAUD Register Settings

Register Name	Address	Set Value	Description
TAUD0 channel stop trigger register (TAUD0TT)	0xFFBF01C8	0x00FF	This register stops counter operation of each channel. TAUD0TT15-08 0x0: No operation TAUD0TT07-00 0x1: Counter operation is stopped.
TAUD0 prescaler clock select register (TAUD0TPS)	0xFFBF0240	0x0000	This register specifies CK0, CK1, CK2, and CK3_PRE clocks of all channels of the PCLK prescaler. TAUD0PRS3-0[3:0] 0x0: PCLK/2^0
TAUD0 prescaler baud rate setting register (TAUD0BRS)	0xFFBF0244	0x00	This register specifies the frequency division factor of the prescaler clock CK3. TAUD0BRS[7:0] 0x0: CK3_PRE/1
TAUD0 channel mode OS register (TAUD0CMOR0)	0xFFBF0200	0x0801	This register controls operation of Channel 0. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x1: Master channel TAUD0STS[2:0] 0x0: Software trigger TAUD0MD[4:0] 0x1: Interval timer mode INTTAUDnIm is output when count operation starts.
TAUD0 channel mode user register (TAUD0CMUR0)	0xFFBF00C0	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR0)	0xFFBF0000	0x0F9F 0x176F	Initial down-count value of TAUD0CNT0
TAUD0 channel mode OS register (TAUD0CMOR1)	0xFFBF0204	0x0409	This register controls operation of Channel 1. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x0: Slave channel TAUD0STS[2:0] 0x4: INTTAUDnIm of the master channel is a start trigger. TAUD0MD[4:0] 0x9: One-count mode Start trigger detection during counting is enabled.
TAUD0 channel mode user register (TAUD0CMUR1)	0xFFBF00C4	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR1)	0xFFBF0004	0x0707 0x063F 0x0A27	Initial down-count value of TAUD0CNT1

TAUD0 channel mode OS register (TAUD0CMOR2)	0xFFBF0208	0x0409	This register controls operation of Channel 1. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x0: Slave channel TAUD0STS[2:0] 0x4: INTTAUDnIm of the master channel is a start trigger. TAUD0MD[4:0] 0x9: One-count mode Start trigger detection during counting is enabled.
TAUD0 channel mode user register (TAUD0CMUR2)	0xFFBF00C8	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR2)	0xFFBF0008	0x01BF 0x0387 0x0547 0x031F 0x0517	Initial down-count value of TAUD0CNT2
TAUD0 channel mode OS register (TAUD0CMOR3)	0xFFBF020C	0x0515	This register controls operation of Channel 3. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x0: Slave channel TAUD0STS[2:0] 0x5: INTTAUDnIm of upper channel (m-1) is a start trigger regardless of master settings. TAUD0MD[4:0] 0x15: Pulse one-count mode Start trigger detection during counting is enabled.
TAUD0 channel mode user register (TAUD0CMUR3)	0xFFBF00CC	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR3)	0xFFBF000C	0x0707 0x063F 0x0A27	Initial down-count value of TAUD0CNT3
TAUD0 channel mode OS register (TAUD0CMOR4)	0xFFBF0210	0x0409	This register controls operation of Channel 4. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x0: Slave channel TAUD0STS[2:0] 0x4: INTTAUDnIm of the master channel is a start trigger. TAUD0MD[4:0] 0x9: One-count mode Start trigger detection during counting is enabled.
TAUD0 channel mode user register (TAUD0CMUR4)	0xFFBF00D0	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR4)	0xFFBF0010	0x07CF 0x0BB7	Initial down-count value of TAUD0CNT4

TAUD0 channel mode OS register (TAUD0CMOR5)	0xFFBF0214	0x0515	This register controls operation of Channel 5. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x0: Slave channel TAUD0STS[2:0] 0x5: INTTAUDnIm of upper channel (m-1) is a start trigger regardless of master settings. TAUD0MD[4:0] 0x15: Pulse one-count mode Start trigger detection during counting is enabled.
TAUD0 channel mode user register (TAUD0CMUR5)	0xFFBF00D4	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR5)	0xFFBF0014	0x0707 0x063F 0x0A27	Initial down-count value of TAUD0CNT5
TAUD0 channel mode OS register (TAUD0CMOR6)	0xFFBF0218	0x0409	This register controls operation of Channel 6. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x0: Slave channel TAUD0STS[2:0] 0x4: INTTAUDnIm of the master channel is a start trigger. TAUD0MD[4:0] 0x9: One-count mode Start trigger detection during counting is enabled.
TAUD0 channel mode user register (TAUD0CMUR6)	0xFFBF00D8	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR6)	0xFFBF0018	0x098F 0x0B57 0x0D17 0x0AEF 0x10CF	Initial down-count value of TAUD0CNT6
TAUD0 channel mode OS register (TAUD0CMOR7)	0xFFBF021C	0x0515	This register controls operation of Channel 7. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x0: Slave channel TAUD0STS[2:0] 0x5: INTTAUDnIm of upper channel (m-1) is a start trigger regardless of master settings. TAUD0MD[4:0] 0x15: Pulse one-count mode Start trigger detection during counting is enabled.
TAUD0 channel mode user register (TAUD0CMUR7)	0xFFBF00DC	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR7)	0xFFBF001C	0x0707 0x063F 0x0A27	Initial down-count value of TAUD0CNT7

TAUD0 channel output enable register (TAUD0TOE)	0xFFBF005C	0x0000	This register enables or disables independent channel output mode of software control. * Disable channel output before setting channel output setting. TAUD0TOE15-00 0x0: Independent timer output mode disabled
		0x00AA	This register enables or disables independent channel output mode of software control. * After the channel output setting is completed, necessary channel output is enabled. TAUD0TOE15-8/6/4/2/0 0x0: Independent timer output mode disabled TAUD0TOE7/5/3/1 0x1: Independent timer output mode enabled
TAUD0 channel output register (TAUD0TO)	0xFFBF0058	0x0000	This register specifies and reads the TAUDTTOUTm level. TAUD0TO15-00 0x0: Low level
TAUD0 channel output mode register (TAUD0TOM)	0xFFBF0248	0x0002	This register specifies output mode of each channel. TAUD0TOM01 0x1: Synchronous channel operation TAUD0TOM15-02/00 0x0: Independent channel operation
TAUD0 channel output configuration register (TAUD0TOC)	0xFFBF024C	0x00A8	This register specifies output mode of each channel together with TAUDnTOMm. TAUD0TOC7/5/3 0x1: Operating mode 2 TAUD0TOC15-8/6/4/2-0 0x0: Operating mode 1
TAUD0 channel output level register (TAUD0TOL)	0xFFBF0040	0x0000	This register specifies the output logic of the channel output bits (TAUDnTO.TAUDnTOm). TAUD0TOL15-00 0x0: Positive logic (active high)
TAUD0 channel dead-time output enable register (TAUD0TDE)	0xFFBF0250	0x0000	This register enables or disables dead-time operation of all channels. TAUD0TDE15-00 0x0: Dead-time operation disabled
TAUDn channel dead-time output mode register (TAUD0TDM)	0xFFBF0254	0x0000	This register specifies the timing at which dead time is to be added during dead-time output. TAUD0TDM15-00 0x0: When duty cycle of upper even channels is detected (duty dead time output)
TAUD0 channel dead-time output level register (TAUD0TDL)	0xFFBF0054	0x0000	This register selects a phase to which dead time is to be added. TAUD0TDL15-00 0x0: Positive phase
TAUD0 channel real-time output enable register (TAUD0TRE)	0xFFBF0258	0x0000	This register enables or disables real-time output. TAUD0TRE15-00 0x0: Real-time output disabled
TAUD0 channel real-time output register (TAUD0TRO)	0xFFBF004C	0x0000	This register sets the value to be output to TAUDTTOUTm. TAUD0TRO15-00 0x0: Low level
TAUD0 channel real-time output control register (TAUD0TRC)	0xFFBF025C	0x0000	This register controls real-time output triggers of each channel. TAUD0TRC15-00 0x0: The next upper channel of the channel for which this bit is set to 1

TAUD0 channel modulation output enable register (TAUD0TME)	0xFFBF0050	0x0000	This register enables or disables modulation output of timer output and real-time output. TAUD0TME15-00 0x0: Modulation disabled
TAUD0 channel reload data enable register (TAUD0RDE)	0xFFBF0260	0x00FF	This register enables or disables simultaneous rewriting of data registers TAUDnCDRm and TAUDnTOLm. TAUD0RDE15-08 0x0: Simultaneous rewriting disabled TAUD0RDE07-00 0x1: Simultaneous rewriting enabled
TAUD0 channel reload data control channel select register (TAUD0RDS)	0xFFBF0268	0x0000	This register selects a channel that controls simultaneous rewriting. TAUD0RDS15-00 0x0: Master channel
TAUD0 channel reload data mode register (TAUD0RDM)	0xFFBF0264	0x0000	This register selects the timing that generates the simultaneous rewriting control signal. TAUD0RDM15-00 0x0: When the counter of the master channel starts counting
TAUD0 channel reload data control register (TAUD0RDC)	0xFFBF026C	0x0000	This register specifies the channel that generates the INTTAUDnIm signal to trigger simultaneous rewriting. TAUD0RDC15-00 0x0: Not used as a simultaneous rewriting trigger channel
TAUD0 channel start trigger register (TAUD0TS)	0xFFBF01C4	0x00FF	This register enables counter operation of each channel. TAUD0TS15-08 0x0: No operation TAUD0TS07-00 0x1: Counter operation is enabled and TAUDnTEm in TAUDnTE is set to 1.
TAUDn channel reload data trigger register (TAUD0RDT)	0xFFBF0044	0x00FF	This register triggers the simultaneous rewriting enable state. TAUD0RDT15-08 0x0: No operation TAUD0RDT07-00 0x1: The simultaneous rewriting enable flag (TAUDnRSFm) is set to 1 and the simultaneous rewriting trigger wait state is entered.

Table 4-6 Example of Port Register Settings

Register Name	Address	Set Value	Description
Port control register (PCR0_1)	0xFFD92008	0x00000045	This register enables all settings of a pin. PUCC, PDSC 0x0: Drive intensity low PBDC 0x0: Bidirectional mode disabled PIBC 0x0: Input buffer disabled PMC 0x1: Alternative mode PIPC 0x0: Software input/output control PM 0x0: Output mode (output enabled) PFCEAE, PFCAE, PFCE, PFC 0x0: Alternative output mode 6 (ALT-OUT6)
Port control register (PCR0_3)	0xFFD9200C	0x00000045	This register enables all settings of a pin. PUCC, PDSC 0x0: Drive intensity low PBDC 0x0: Bidirectional mode disabled PIBC 0x0: Input buffer disabled PMC 0x1: Alternative mode PIPC 0x0: Software input/output control PM 0x0: Output mode (output enabled) PFCEAE, PFCAE, PFCE, PFC 0x0: Alternative output mode 6 (ALT-OUT6)
Port control register (PCR0_5)	0xFFD92014	0x00000045	This register enables all settings of a pin. PUCC, PDSC 0x0: Drive intensity low PBDC 0x0: Bidirectional mode disabled PIBC 0x0: Input buffer disabled PMC 0x1: Alternative mode PIPC 0x0: Software input/output control PM 0x0: Output mode (output enabled) PFCEAE, PFCAE, PFCE, PFC 0x0: Alternative output mode 6 (ALT-OUT6)
Port control register (PCR0_7)	0xFFD9201C	0x00000045	This register enables all settings of a pin. PUCC, PDSC 0x0: Drive intensity low PBDC 0x0: Bidirectional mode disabled PIBC 0x0: Input buffer disabled PMC 0x1: Alternative mode PIPC 0x0: Software input/output control PM 0x0: Output mode (output enabled) PFCEAE, PFCAE, PFCE, PFC 0x0: Alternative output mode 6 (ALT-OUT6)

Table 4-7 Example of Interrupt Control Register Settings

Register Name	Address	Set Value	Description
EI level interrupt control register 10 (EIC10)	0xFFFC4014	0x0047	This register is provided for each EI level interrupt source to set interrupt control conditions for each source. EIMKn 0x0: Interrupt processing enabled EITBn 0x4: Table reference method EIPn 0x7: Priority 7

Lists of functions, variables, and constants used in this operation example are provided in Table 4-8 to Table 4-10.

Table 4-8 List of Functions

Function Name	Description
main0	Calls each function.
port_init	Sets P0_1, P0_3, P0_5, and P0_7 pins to TAUD0O1, TAUD0O3, TAUD0O5, and TAUD0O7 features respectively.
pwm_init	Makes initial settings for TAUD0.
pwm_start	Starts timers TAUD0 CH0 to CH7 for PWM output.
pwm_update_duty	Interrupt processing that takes place at each count start (carrier cycle) of TAUD0 CH0. This function modifies the PWM carrier cycle, duty, and shift time.

Table 4-9 List of Variables

Variable Name	Description
mode	Index for reading the cnt_table array

Table 4-10 List of Constants

Constant Name	Description
cnt_table[5][8]	Array of specified values of PWM cycle, duty, and shift time

4.5 Operation Flow

Figure 4-4 shows the operation flow of this operation example.

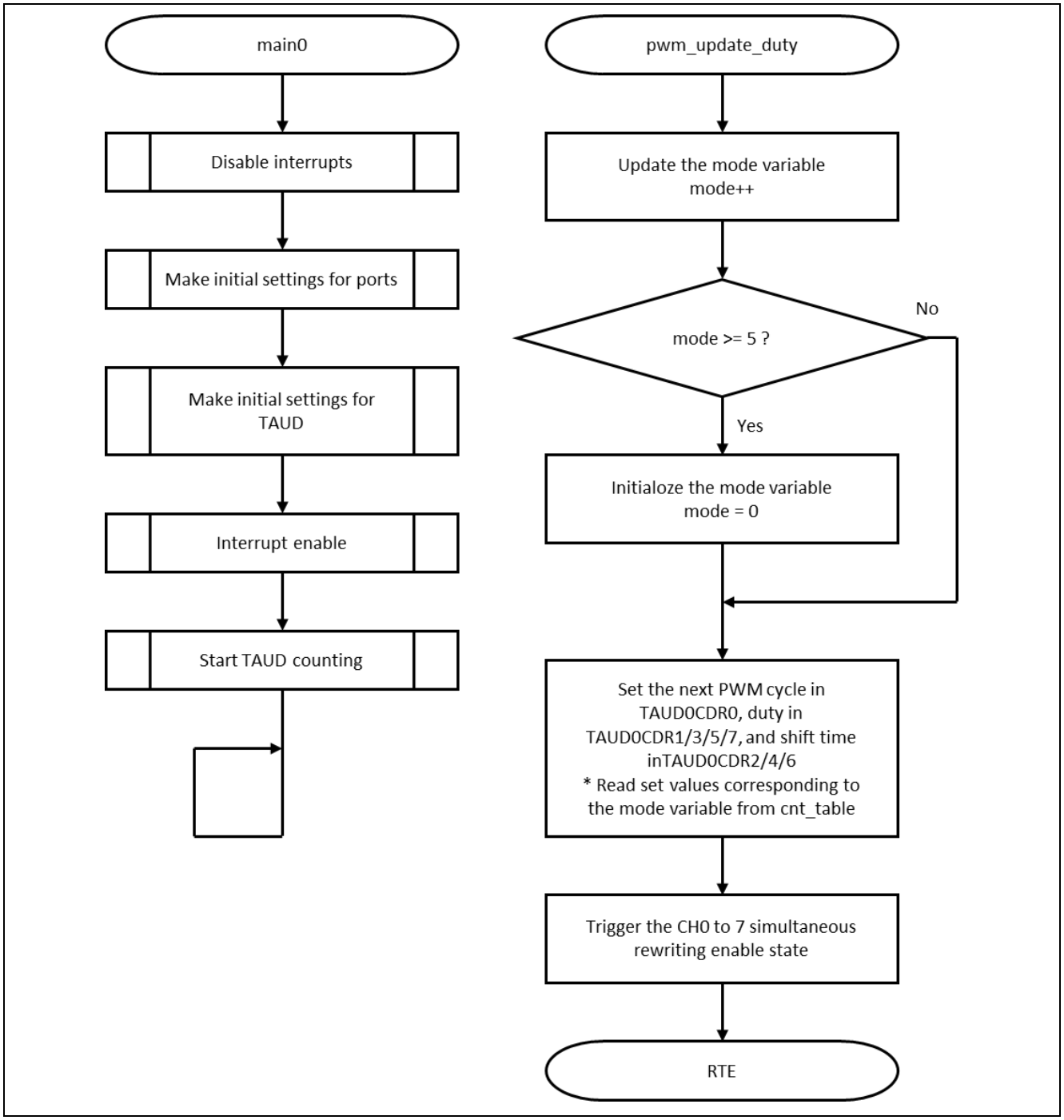


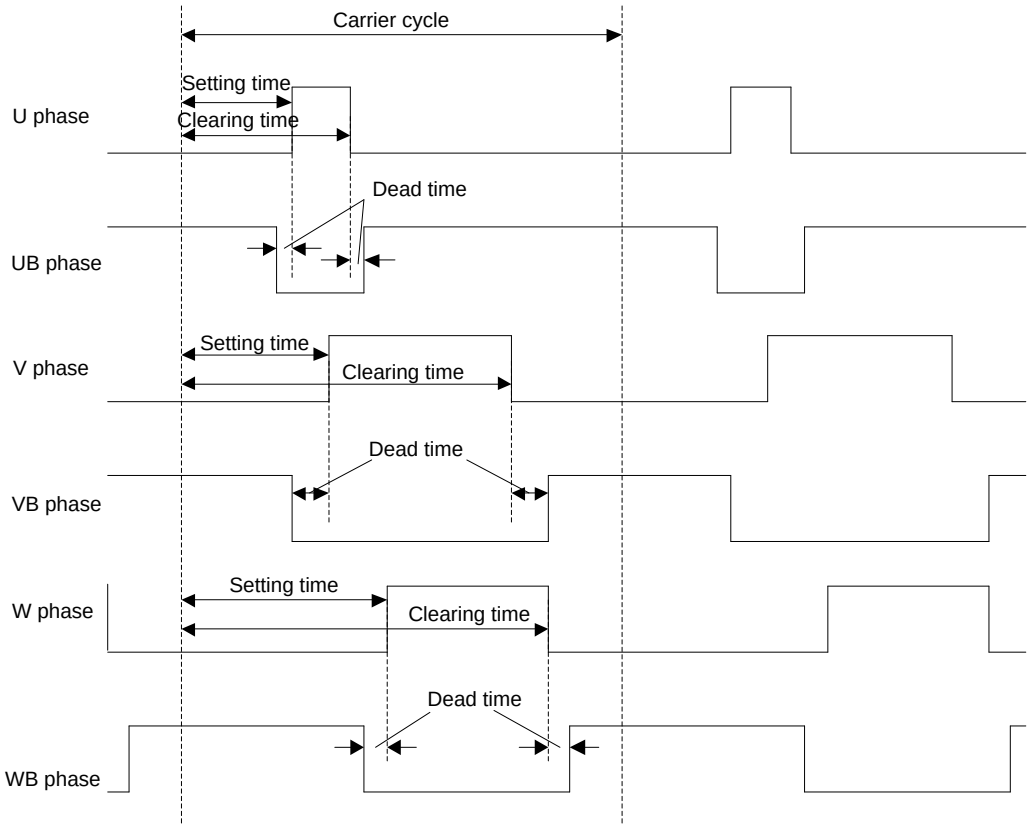
Figure 4-4 Operation Flow

5. Multi-Phase PWM

5.1 Overview

This section describes how to output the multi-phase PWM by using the PWM output feature (with dead time) for which the TAUD's PWM output feature is interlocked with the single-phase PWM output feature by the PIC1. The multi-phase PWM can control the setting timing, clearing timing, and dead time of single-phase to 3-phase (U phase, V phase, and W phase) PWM output. The use of each TAUD channel has been determined for each channel number in this feature. Figure 5-1 shows the schematic of multi-phase PWM output.

In this operation example, 13 channels (master channel and 12 slave channels) of the TAUD are used and 3-phase PWM waveforms are output. This section also describes how to continuously change the setting timing and clearing timing of each phase in each carrier cycle by using interrupts.



The following shows TAUD channel numbers for setting each parameter.
[All phases]
Carrier cycle: Set by master CH2

[U phase]
Setting time: Set by slave CH4
Clearing time: Set by slave CH5
Dead time: Set by slave CH11

[V phase]
Setting time: Set by slave CH6
Clearing time: Set by slave CH7
Dead time: Set by slave CH13

[W phase]
Setting time: Set by slave CH8
Clearing time: Set by slave CH9
Dead time: Set by slave CH15

Figure 5-1 Schematic

5.2 Operating Conditions for Features Used

Operating conditions for features used in this operation example are provided below.

Table 5-1 Port Settings

Item	Description
Port to be used	P12_5: TAPA0UP (U phase) P12_3: TAPA0UN (UB phase) P12_0: TAPA0VP (V phase) P12_1: TAPA0VN (VB phase) P12_2: TAPA0WP (W phase) P12_6: TAPA0WN (WB phase)

Table 5-2 Timer TAUD Settings

Item	Description
Feature to be used	PWM output feature with dead time (PWM output feature is interlocked with single-phase PWM output feature by the PIC1)
Clock supplied to TAUD	PLL output clock (80 MHz)
Master channel	Timer channel 2: Controls the carrier cycle.
Slave channels	Timer channel 4: Controls the U-phase setting time.
	Timer channel 5: Controls the U-phase clearing time.
	Timer channel 6: Controls the V-phase setting time
	Timer channel 7: Controls the V-phase clearing time.
	Timer channel 8: Controls the W-phase setting time
	Timer channel 9: Controls the W-phase clearing time.
	Timer channel 10: Controls the U-phase output.
	Timer channel 11: Controls the UB-phase output and dead time.
	Timer channel 12: Controls the V-phase output.
	Timer channel 13: Controls the VB-phase output and dead time.
	Timer channel 14: Controls the W-phase output.
	Timer channel 15: Controls the WB-phase output and dead time.
Timer operation clock	Prescaler output CK0 = (80 MHz) / 1

Table 5-3 Interrupt Settings

Item	Description
Interrupt method	Table reference method
INTTAUD0I2 interrupt	Enabled (Priority 7)

5.3 Operation

A method of how to change the carrier cycle, setting time, and clearing time of multi-phase PWN waveforms continuously is shown in this operation example.

Table 5-4 lists output waveform patterns used in this operation example. Figure 5-2 shows output waveforms.

Table 5-4 Output Waveform Patterns

Pattern No.	Phase	Carrier Cycle	Setting Time Note	Clearing Time Note	Dead Time
1	U phase	50 us	20 us	30 us	2.5 us
	V phase				
	W phase				
2	U phase	50 us	15 us	35 us	2.5 us
	V phase				
	W phase				
3	U phase	50 us	10 us	40 us	2.5 us
	V phase				
	W phase				
4	U phase	50 us	20 us	30 us	2.5 us
	V phase		15 us	35 us	
	W phase		10 us	40 us	
5	U phase	60 us	25 us	35 us	2.5 us
	V phase		20 us	40 us	
	W phase		15 us	45 us	

Note: Specified values of the timer for setting and clearing are provided. As shown in Figure 5-2, there is a delay by dead time in the actual setting timing and clearing timing of output waveforms.

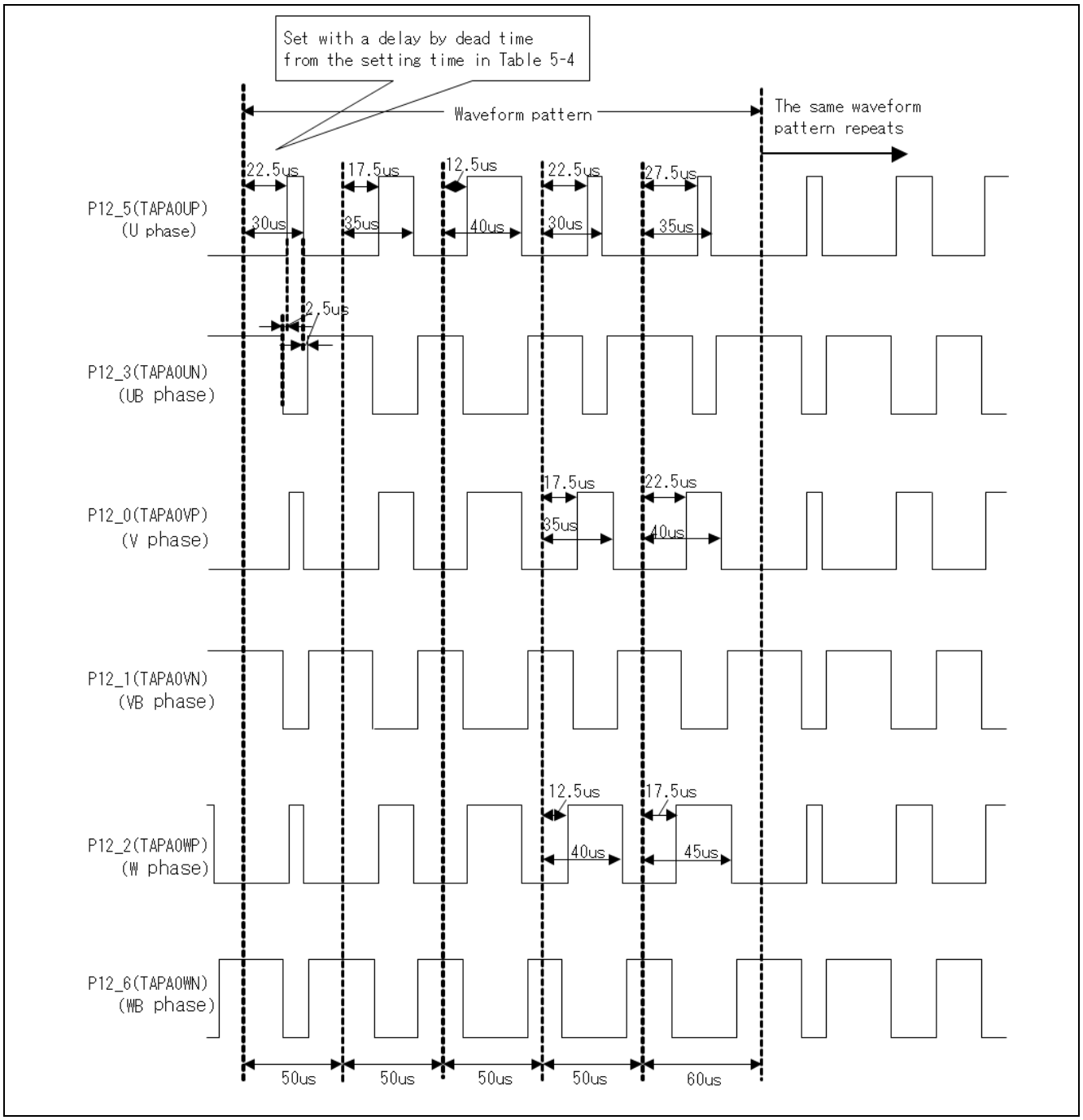


Figure 5-2 Output Waveforms

The operation in Figure 5-2 is performed by the software which changes the carrier cycle, setting time, and clearing time of the next cycle at an interrupt generated at the beginning of the carrier cycle. Figure 5-3 illustrates hardware processing and software processing of a method of changing the U-phase carrier cycle, setting time, and clearing time from "carrier cycle T_a, setting time S_a, and clearing time C_a" to "carrier cycle T_b, setting time S_b, and clearing time C_b" to ---. The same control method also applies to the V phase and W phase.

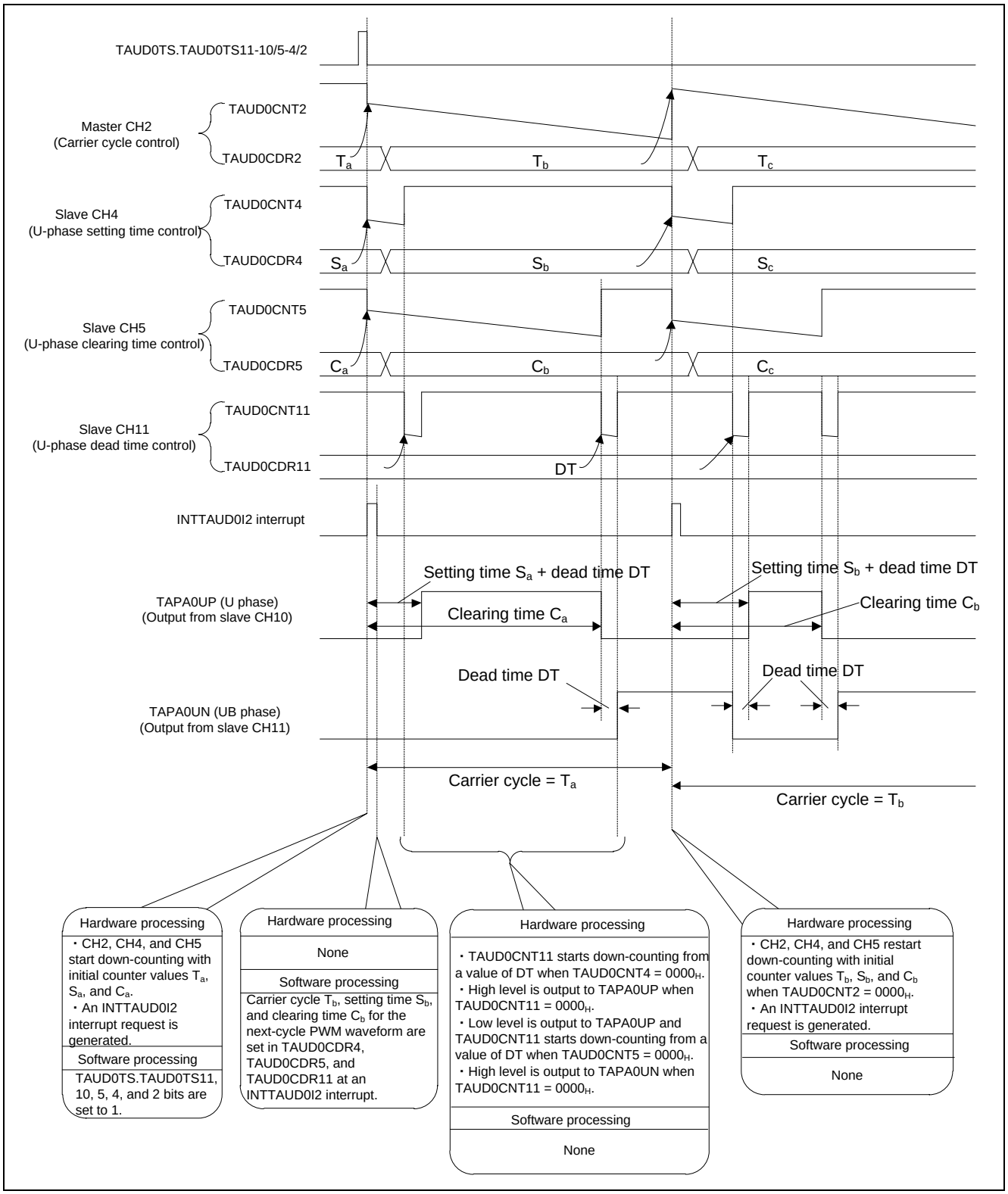


Figure 5-3 Description of Operations Used

5.4 Description of Software

Examples of settings for each register used in this operation example are provided in Table 5-5 to Table **5-8**.

Table 5-5 Example of TAUD Register Settings

Register Name	Address	Set Value	Description
TAUD0 channel stop trigger register (TAUD0TT)	0xFFBF01C8	0xFFF4	This register stops counter operation of each channel. TAUD0TT3/1-0 0x0: No operation TAUD0TT15-4/2 0x1: Counter operation is stopped.
TAUD0 prescaler clock select register (TAUD0TPS)	0xFFBF0240	0x0000	This register specifies CK0, CK1, CK2, and CK3_PRE clocks of all channels of the PCLK prescaler. TAUD0PRS3-0[3:0] 0x0: PCLK/2^0
TAUD0 prescaler baud rate setting register (TAUD0BRS)	0xFFBF0244	0x00	This register specifies the division factor of the prescaler clock CK3. TAUD0BRS[7:0] 0x0: CK3_PRE/1
TAUD0 channel mode OS register (TAUD0CMOR2)	0xFFBF0208	0x0801	This register controls operation of Channel 2. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x1: Master channel TAUD0STS[2:0] 0x0: Software trigger TAUD0MD[4:0] 0x1: Interval timer mode INTTAUDnIm is output when count operation starts.
TAUD0 channel mode user register (TAUD0CMUR2)	0xFFBF00C8	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR2)	0xFFBF0008	0x0F9F 0x12BF	Initial down-count value of TAUD0CNT2
TAUD0 channel mode OS register (TAUD0CMOR4)	0xFFBF0210	0x0409	This register controls operation of Channel 4. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x0: Slave channel TAUD0STS[2:0] 0x4: INTTAUDnIm of the master channel is a start trigger. TAUD0MD[4:0] 0x9: One-count mode Start trigger detection during counting is enabled.
TAUD0 channel mode user register (TAUD0CMUR4)	0xFFBF00D0	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR4)	0xFFBF0010	0x063F 0x04AF 0x031F 0x07CF	Initial down-count value of TAUD0CNT4

TAUD0 channel mode OS register (TAUD0CMOR5)	0xFFBF0214	0x0409	This register controls operation of Channel 5. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x0: Slave channel TAUD0STS[2:0] 0x4: INTTAUDnIm of the master channel is a start trigger. TAUD0MD[4:0] 0x9: One-count mode Start trigger detection during counting is enabled.
TAUD0 channel mode user register (TAUD0CMUR5)	0xFFBF00D4	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR5)	0xFFBF0014	0x0C7F 0x095F 0x0AEF	Initial down-count value of TAUD0CNT5
TAUD0 channel mode OS register (TAUD0CMOR6)	0xFFBF0218	0x0409	This register controls operation of Channel 6. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x0: Slave channel TAUD0STS[2:0] 0x4: INTTAUDnIm of the master channel is a start trigger. TAUD0MD[4:0] 0x9: One-count mode Start trigger detection during counting is enabled.
TAUD0 channel mode user register (TAUD0CMUR6)	0xFFBF00D8	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR6)	0xFFBF0018	0x063F 0x04AF 0x031F	Initial down-count value of TAUD0CNT6
TAUD0 channel mode OS register (TAUD0CMOR7)	0xFFBF021C	0x0409	This register controls operation of Channel 7. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x0: Slave channel TAUD0STS[2:0] 0x4: INTTAUDnIm of the master channel is a start trigger. TAUD0MD[4:0] 0x9: One-count mode Start trigger detection during counting is enabled.
TAUD0 channel mode user register (TAUD0CMUR7)	0xFFBF00DC	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR7)	0xFFBF001C	0x095F 0x0AEF 0x0C7F	Initial down-count value of TAUD0CNT7

TAUD0 channel mode OS register (TAUD0CMOR8)	0xFFBF0220	0x0409	This register controls operation of Channel 8. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x0: Slave channel TAUD0STS[2:0] 0x4: INTTAUDnIm of the master channel is a start trigger. TAUD0MD[4:0] 0x9: One-count mode Start trigger detection during counting is enabled.
TAUD0 channel mode user register (TAUD0CMUR8)	0xFFBF00E0	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR8)	0xFFBF0020	0x063F 0x04AF 0x031F	Initial down-count value of TAUD0CNT8
TAUD0 channel mode OS register (TAUD0CMOR9)	0xFFBF0224	0x0409	This register controls operation of Channel 9. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x0: Slave channel TAUD0STS[2:0] 0x4: INTTAUDnIm of the master channel is a start trigger. TAUD0MD[4:0] 0x9: One-count mode Start trigger detection during counting is enabled.
TAUD0 channel mode user register (TAUD0CMUR9)	0xFFBF00E4	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR9)	0xFFBF0024	0x095F 0x0AEF 0x0C7F 0x0E0F	Initial down-count value of TAUD0CNT9
TAUD0 channel mode OS register (TAUD0CMOR10)	0xFFBF0228	0x0000	This register controls operation of Channel 10. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x0: Slave channel TAUD0STS[2:0] 0x0: Software trigger TAUD0MD[4:0] 0x0: Interval timer mode INTTAUDnIm is not output when count operation starts.
TAUD0 channel mode user register (TAUD0CMUR10)	0xFFBF00E8	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR10)	0xFFBF0028	0x0000	Initial down-count value of TAUD0CNT10

TAUD0 channel mode OS register (TAUD0CMOR11)	0xFFBF022C	0x0109	This register controls operation of Channel 11. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x0: Slave channel TAUD0STS[2:0] 0x0: Valid edge of the TAUDTTINm input signal TAUD0MD[4:0] 0x9: One-count mode Start trigger detection during counting is enabled.
TAUD0 channel mode user register (TAUD0CMUR11)	0xFFBF00EC	0x03	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x3: Both edges detected (high-level width measurement selected)
TAUD0 channel data register (TAUD0CDR11)	0xFFBF002C	0x00C7	Initial down-count value of TAUD0CNT11
TAUD0 channel mode OS register (TAUD0CMOR12)	0xFFBF0230	0x0000	This register controls operation of Channel 12. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x0: Slave channel TAUD0STS[2:0] 0x0: Software trigger TAUD0MD[4:0] 0x0: Interval timer mode INTTAUDnIm is output when count operation starts.
TAUD0 channel mode user register (TAUD0CMUR12)	0xFFBF00F0	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR12)	0xFFBF0030	0x0000	Initial down-count value of TAUD0CNT12
TAUD0 channel mode OS register (TAUD0CMOR13)	0xFFBF0234	0x0109	This register controls operation of Channel 13. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x0: Slave channel TAUD0STS[2:0] 0x0: Valid edge of the TAUDTTINm input signal TAUD0MD[4:0] 0x9: One-count mode Start trigger detection during counting is enabled.
TAUD0 channel mode user register (TAUD0CMUR13)	0xFFBF00F4	0x03	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x3: Both edges detected (high-level width measurement selected)
TAUD0 channel data register (TAUD0CDR13)	0xFFBF0034	0x00C7	Initial down-count value of TAUD0CNT13

TAUD0 channel mode OS register (TAUD0CMOR14)	0xFFBF0238	0x0000	This register controls operation of Channel 14. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x0: Slave channel TAUD0STS[2:0] 0x0: Software trigger TAUD0MD[4:0] 0x0: Interval timer mode INTTAUDnIm is output when count operation starts.
TAUD0 channel mode user register (TAUD0CMUR14)	0xFFBF00F8	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR14)	0xFFBF0038	0x0000	Initial down-count value of TAUD0CNT14
TAUD0 channel mode OS register (TAUD0CMOR15)	0xFFBF023C	0x0109	This register controls operation of Channel 15. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0MAS 0x0: Slave channel TAUD0STS[2:0] 0x0: Valid edge of the TAUDTTINm input signal TAUD0MD[4:0] 0x9: One-count mode Start trigger detection during counting is enabled.
TAUD0 channel mode user register (TAUD0CMUR15)	0xFFBF00FC	0x03	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x3: Both edges detected (high-level width measurement selected)
TAUD0 channel data register (TAUD0CDR15)	0xFFBF003C	0x00C7	Initial down-count value of TAUD0CNT15
TAUD0 channel output enable register (TAUD0TOE)	0xFFBF005C	0x0000	Enables or disables independent channel output mode of software control. * Disable channel output before setting channel output setting. TAUD0TOE15-00 0x0: Independent timer output mode disabled
		0xFC00	Enables or disables independent channel output mode of software control. * After the channel output setting is completed, necessary channel output is enabled. TAUD0TOE9-0 0x0: Independent timer output mode disabled TAUD0TOE15-10 0x1: Independent timer output mode enabled
TAUD0 channel output register (TAUD0TO)	0xFFBF0058	0x0000	This register specifies and reads the TAUDTTOUTm level. TAUD0TO15-00 0x0: Low level
TAUD0 channel output mode register (TAUD0TOM)	0xFFBF0248	0xFFF0	This register specifies output mode of each channel. TAUD0TOM15-04 0x1: Synchronous channel operation TAUD0TOM03-00 0x0: Independent channel operation

TAUD0 channel output configuration register (TAUD0TOC)	0xFFBF024C	0xFC00	This register specifies output mode of each channel together with TAUDnTOMm. TAUD0TOC15-10 0x1: Operating mode 2 TAUD0TOC9-0 0x0: Operating mode 1
TAUD0 channel output level register (TAUD0TOL)	0xFFBF0040	0x0000	This register specifies the output logic of the channel output bits (TAUDnTO.TAUDnTOm). TAUD0TOL15-00 0x0: Positive logic (active high)
TAUD0 channel dead-time output enable register (TAUD0TDE)	0xFFBF0250	0xFC00	This register enables or disables dead-time operation of all channels. TAUD0TDE15-10 0x1: Dead-time operation enabled TAUD0TDE9-0 0x0: Dead-time operation disabled
TAUDn channel dead-time output mode register (TAUD0TDM)	0xFFBF0254	0xFC00	This register specifies the timing at which dead time is to be added during dead time output. TAUD0TDM15-10 0x1: When the TIN input edge of a lower odd channel is detected (single-phase dead-time output) TAUD0TDM9-0 0x0: When the duty cycle of an upper even channel is detected (duty dead-time output)
TAUD0 channel dead-time output level register (TAUD0TDL)	0xFFBF0054	0xA800	This register selects a phase to which dead time is to be added. TAUD0TDL15/13/11 0x1: Negative phase TAUD0TDL14/12/10-0 0x0: Positive phase
TAUD0 channel real-time output enable register (TAUD0TRE)	0xFFBF0258	0x0000	This register enables or disables real-time output. TAUD0TRE15-00 0x0: Real-time output disabled
TAUD0 channel real-time output register (TAUD0TRO)	0xFFBF004C	0x0000	This register sets the value to be output to TAUDTTOUTm. TAUD0TRO15-00 0x0: Low level
TAUD0 channel real-time output control register (TAUD0TRC)	0xFFBF025C	0x0000	This register controls real-time output triggers of each channel. TAUD0TRC15-00 0x0: The next upper channel of the channel for which this bit is set to 1
TAUD0 channel modulation output enable register (TAUD0TME)	0xFFBF0050	0x0000	This register enables or disables modulation output of timer output and real-time output. TAUD0TME15-00 0x0: Modulation disabled
TAUD0 channel reload data enable register (TAUD0RDE)	0xFFBF0260	0x03F4	This register enables or disables simultaneous rewriting of data registers TAUDnCDRm and TAUDnTOLm. TAUD0RDE15-10/3/1-0 0x0: Simultaneous rewriting disabled TAUD0RDE9-4/2 0x1: Simultaneous rewriting enabled
TAUD0 channel reload data control channel select register (TAUD0RDS)	0xFFBF0268	0x0000	This register selects a channel that controls simultaneous rewriting. TAUD0RDS15-00 0x0: Master channel

TAUD0 channel reload data mode register (TAUD0RDM)	0xFFBF0264	0x0000	This register selects the timing that generates the simultaneous rewriting control signal. TAUD0RDM15-00 0x0: When the counter of the master channel starts counting
TAUD0 channel reload data control register (TAUD0RDC)	0xFFBF026C	0x0000	This register specifies the channel that generates the INTTAUDnIm signal to trigger simultaneous rewriting. TAUD0RDC15-00 0x0: Not used as a simultaneous rewriting trigger channel
TAUD0 channel start trigger register (TAUD0TS)	0xFFBF01C4	0xFFF4	This register enables counter operation of each channel. TAUD0TS3/1-0 0x0: No operation TAUD0TS15-4/2 0x1: Counter operation is enabled and TAUDnTEm in TAUDnTE is set to 1.
TAUDn channel reload data trigger register (TAUD0RDT)	0xFFBF0044	0x03F4	This register triggers the simultaneous rewriting enable state. TAUD0RDT15-10/3/1-0 0x0: No operation TAUD0RDT9-4/2 0x1: The simultaneous rewriting enable flag (TAUDnRSFm) is set to 1 and the simultaneous rewriting trigger wait state is entered.

Table 5-6 Example of PIC1 Register Settings

Register Name	Address	Set Value	Description
Timer input/output control register 202 (PIC1REG202)	0xFFBFAFC8	0x0888001C	This register selects an input signal of TAUD0 CHm. PIC1REG20227/226 0x2: Signal selected by PIC1REG20204 bit is selected as TIN signal of CH15. PIC1REG20225/224 0x0: TIN pin input is selected as TIN input signal of CH14. PIC1REG20223/222 0x2: Signal selected by PIC1REG20203 bit is selected as TIN signal of CH13. PIC1REG20221/220 0x0: TIN pin input is selected as TIN input signal of CH12. PIC1REG20219/218 0x2: Signal selected by PIC1REG20202 bit is selected as TIN signal of CH11. PIC1REG20217/216 0x0: TIN pin input is selected as TIN input signal of CH10. PIC1REG20204 0x1: Set/clear signals output by TAUD0INT08 and INT09 are selected to be supplied to TIN of CH15. PIC1REG20203 0x1: Set/clear signals output by TAUD0INT06 and INT07 are selected to be supplied to TIN of CH13. PIC1REG20202 0x1: Set/clear signals output by TAUD0INT04 and INT05 are selected to be supplied to TIN of CH11.
TAUD0 input select register (PIC1TAUD0SEL)	0xFFBFAF78	0x00000000	This 32-bit register selects a TAUD0I input signal. PIC1TAUD0INm3-2 0x0: TAUD0TIN (m+1) selected PIC1TAUD0INm1-0 0x0: TAUD0TIN (m) selected
Timer input/output control register 201 (PIC1REG201)	0xFFBFAFC4	0x00000000	This register selects the logic of combination circuit PFN0xx. PIC1REG20127-126 0x0: * PIC1REG20125-124 0x0: * PIC1REG20123-122 0x0: * PIC1REG20121-120 0x0: * PIC1REG20119-118 0x0: * PIC1REG20117-116 0x0: * * This register is fixed to these values for the PWM output feature with dead time.
Timer input/output control register 203 (PIC1REG203)	0xFFBFAFCC	0x00000000	This register selects the logic of combination circuit FN0i. PIC1REG20322-320 0x0: A PIC1REG20318-316 0x0: A PIC1REG20314-312 0x0: A PIC1REG20310-308 0x0: A PIC1REG20306-304 0x0: A PIC1REG20302-300 0x0: A

Table 5-7 Example of Port Register Settings

Register Name	Address	Set Value	Description
Port control register (PCR12_5)	0xFFD92314	0x00000079	This register enables all settings of a pin. PUCC, PDSC 0x0: Drive intensity low PBDC 0x0: Bidirectional mode disabled PIBC 0x0: Input buffer disabled PMC 0x1: Alternative mode PIPC 0x1: Direct input/output control PM 0x1: Disabled because of direct input/output control PFCEAE,PFCAE, PFCE,PFC 0x9: Alternative output mode 10 (ALT-OUT10)
Port control register (PCR12_3)	0xFFD9230C	0x0000007A	This register enables all settings of a pin. PUCC, PDSC 0x0: Drive intensity low PBDC 0x0: Bidirectional mode disabled PIBC 0x0: Input buffer disabled PMC 0x1: Alternative mode PIPC 0x1: Direct input/output control PM 0x1: Disabled because of direct input/output control PFCEAE,PFCAE, PFCE,PFC 0xA: Alternative output mode 11 (ALT-OUT11)
Port control register (PCR12_0)	0xFFD92300	0x0000007A	This register enables all settings of a pin. PUCC, PDSC 0x0: Drive intensity low PBDC 0x0: Bidirectional mode disabled PIBC 0x0: Input buffer disabled PMC 0x1: Alternative mode PIPC 0x1: Direct input/output control PM 0x1: Disabled because of direct input/output control PFCEAE,PFCAE, PFCE,PFC 0xA: Alternative output mode 11 (ALT-OUT11)
Port control register (PCR12_1)	0xFFD92304	0x0000007A	This register enables all settings of a pin. PUCC, PDSC 0x0: Drive intensity low PBDC 0x0: Bidirectional mode disabled PIBC 0x0: Input buffer disabled PMC 0x1: Alternative mode PIPC 0x1: Direct input/output control PM 0x1: Disabled because of direct input/output control PFCEAE,PFCAE, PFCE,PFC 0xA: Alternative output mode 11 (ALT-OUT11)
Port control register (PCR12_2)	0xFFD92308	0x0000007A	This register enables all settings of a pin. PUCC, PDSC 0x0: Drive intensity low PBDC 0x0: Bidirectional mode disabled PIBC 0x0: Input buffer disabled PMC 0x1: Alternative mode PIPC 0x1: Direct input/output control PM 0x1: Disabled because of direct input/output control PFCEAE,PFCAE, PFCE,PFC 0xA: Alternative output mode 11 (ALT-OUT11)

Port control register (PCR12_6)	0xFFD92318	0x00000070	This register enables all settings of a pin. PUCC, PDSC 0x0: Drive intensity low PBDC 0x0: Bidirectional mode disabled PIBC 0x0: Input buffer disabled PMC 0x1: Alternative mode PIPC 0x1: Direct input/output control PM 0x1: Disabled because of direct input/output control PFCEAE,PFCAE, PFCE, PFC 0x0: Alternative output mode 1 (ALT-OUT1)

Table 5-8 Example of Interrupt Control Register Settings

Register Name	Address	Set Value	Description
EI level interrupt control register 11 (EIC11)	0xFFFC4016	0x0047	This register is provided for each EI level interrupt source to set interrupt control conditions for each source. EIMKn 0x0: Interrupt processing enabled EITBn 0x4: Table reference method EIPn 0x7: Priority 7

Lists of functions, variables, and constants used in this operation example are provided in Table 5-9 to Table 5-11.

Table 5-9 List of Functions

Function Name	Description
main0	Calls each function.
port_init	Sets P12_5 to TAPA0UP, P12_3 to TAPA0UN, P12_0 to TAPA0VP, P12_1 to TAPA0VN, P12_2 to TAPA0WP, P12_6 to TAPA0WN features respectively.
pwm_init	Makes initial settings for TAUD0 and PIC1.
pwm_start	Starts timers TAUD0 CH2 and CH4 to CH15 for PWM output.
pwm_update_duty	Interrupt processing that takes place at each count start (carrier cycle) of TAUD0 CH2 This function modifies the PWM carrier cycle and setting time and clearing time of each phase.

Table 5-10 List of Variables

Variable Name	Description
mode	Index for reading the cnt_table array

Table 5-11 List of Constants

Constant Name	Description
cnt_table[5][10]	Array of specified values of the PWM carrier cycle, setting/clearing time of each phase, and dead time

5.5 Operation Flow

Figure 5-4 shows the operation flow of this operation example.

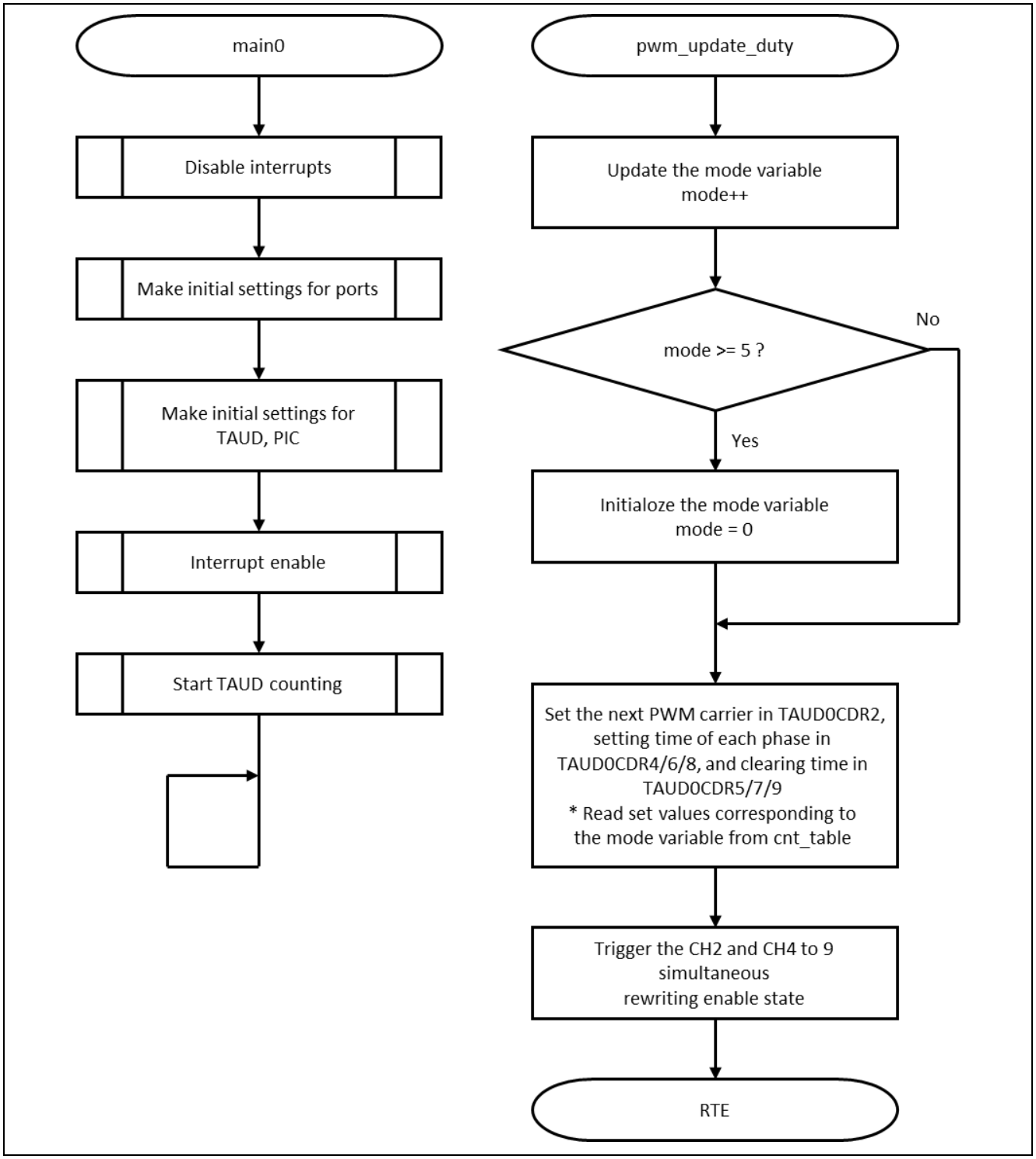


Figure 5-4 Operation Flow

6. Generation of a Pulse Signal and Measurement of High-Level Width

6.1 Overview

This section describes generation of a pulse signal using the interval timer feature that is a TAUD's independent channel operation feature, as well as describes measurement of the high-level pulse width using the TAUDTTINm input signal width measurement feature.

Figure 6-1 shows the schematic of this operation example.

In this operation example, a pulse signal to be measured is generated by the TAUD's interval timer feature and the generated pulse signal is output from the TAUD0O0 pin. This pulse signal is input to the TAUD0I6 pin and its high-level width is measured by using the TAUDTTINm input interval timer feature.

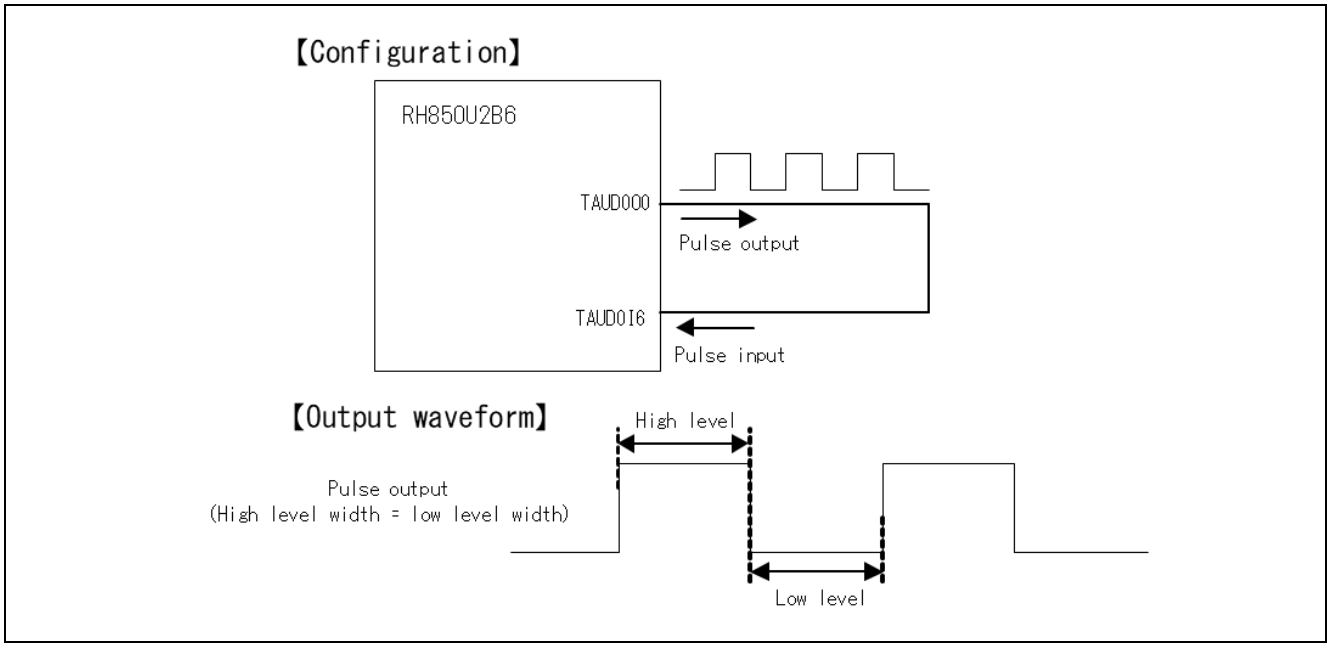


Figure 6-1 Schematic

6.2 Operating Conditions for Features Used

Operating conditions for features used in this operation example are provided below.

Table 6-1 Port Settings

Item	Description
Port to be used	P0_0: TAUD0O0 P10_6: TAUD0I6

Table 6-2 Timer TAUD Settings

Item	Description
Feature to be used	Timer channel 0: Interval timer feature (pulse signal generation) Timer channel 6: TAUDTTINm input signal width measurement feature
Clock supplied to TAUD	PLL output clock (80 MHz)
Timer operation clock	Prescaler output CK0 = (80 MHz) / 1

Table 6-3 Interrupt Settings

Item	Description
Interrupt method	Table reference method
INTTAUD0I6 interrupt	Enabled (Priority 15)

6.3 Operation

The interval timer feature toggles the TAUDTTOUTm signal at constant intervals to generate a pulse signal.

The TAUDTTINm input signal width measurement feature starts counting at the TAUDTTINm rising edge and captures the count value at the TAUDTTINm falling edge to measure the TAUDTTINm signal width.

Figure 6-2 illustrates hardware processing and software processing of the pulse signal generation operation and the high-level width measurement operation. (In this operation example, a pulse signal with a high-level width of 205 us is generated and its high-level time is measured.)

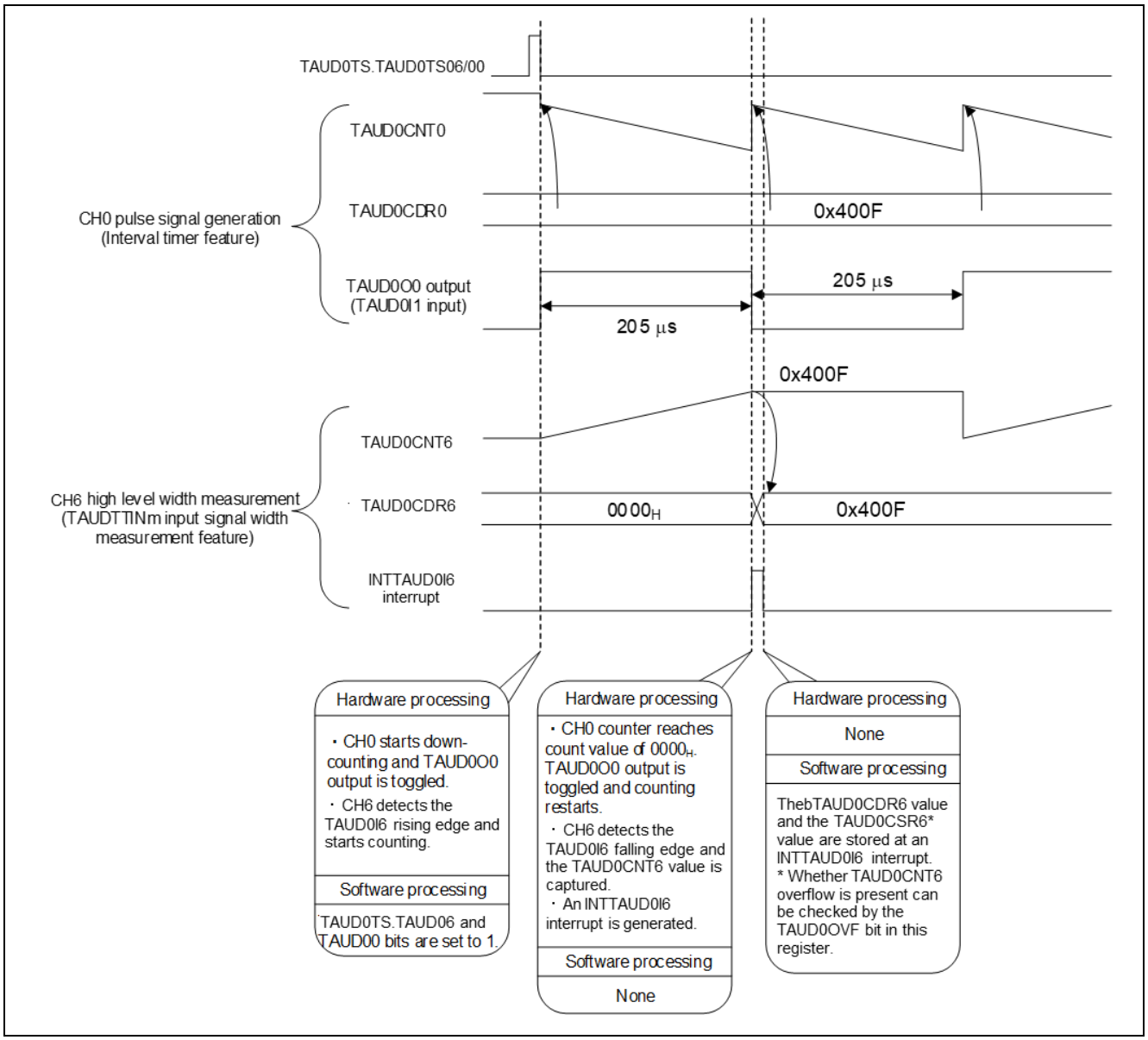


Figure 6-2 Description of Operations Used

6.4 Description of Software

Examples of settings for each register used in this operation example are provided in Table 6-4 to Table 6-6.

Table 6-4 Example of TAUD Register Settings

Register Name	Address	Set Value	Description
TAUD0 channel stop trigger register (TAUD0TT)	0xFFBF01C8	0x0041	This register stops counter operation of each channel. TAUD0TT15-07,05-01 0x0: No operation TAUD0TT06,00 0x1: Counter operation is stopped.
TAUD0 prescaler clock select register (TAUD0TPS)	0xFFBF0240	0x0000	This register specifies CK0, CK1, CK2, and CK3_PRE clocks of all channels of the PCLK prescaler. TAUD0PRS3-0[3:0] 0x0: PCLK/2^0
TAUD0 prescaler baud rate setting register (TAUD0BRS)	0xFFBF0244	0x00	This register specifies the frequency division factor of the prescaler clock CK3. TAUD0BRS[7:0] 0x0: CK3_PRE/1
TAUD0 channel mode OS register (TAUD0CMOR0)	0xFFBF0200	0x0001	This register controls operation of Channel 0. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0STS[2:0] 0x0: Software trigger TAUD0MD[4:0] 0x1: Interval timer mode NTTAUDnIm is output when count operation starts.
TAUD0 channel mode user register (TAUD0CMUR0)	0xFFBF00C0	0x00	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x0: Falling edge
TAUD0 channel data register (TAUD0CDR0)	0xFFBF0000	0x400F	Initial down-count value of TAUD0CNT0
TAUD0 channel mode OS register (TAUD0CMOR1)	0xFFBF0204	0x020C	This register controls operation of Channel 1. TAUD0CKS[1:0] 0x0: Operation clock CK0 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm TAUD0STS[2:0] 0x2: The valid trigger of the TAUDTTINm input signal is used as a start trigger and the opposite edge is used as a stop trigger. TAUD0COS[1:0] 0x0: TAUDnCDRm is updated when a valid edge of the TAUDTTINm input is detected. The TAUDnOVF bit in TAUDnCSRm is updated (cleared or set) when a valid edge of the TAUDTTINm input is detected. TAUD0MD[4:0] 0xC: Capture and one-count mode
TAUD0 channel mode user register (TAUD0CMUR1)	0xFFBF00C4	0x03	This register specifies the valid-edge detection type used for TAUDTTINm input. TAUD0TIS[1:0] 0x3: Both edges detected (high-level width measurement selected)

TAUD0 channel output enable register (TAUD0TOE)	0xFFBF005C	0x0000	Enables or disables independent channel output mode of software control. * Disable channel output before setting channel output setting. TAUD0TOE15-00 0x0: Independent timer output mode disabled
		0x0001	Enables or disables independent channel output mode of software control. * After the channel output setting is completed, necessary channel output is enabled. TAUD0TOE15-01 0x0: Independent timer output mode disabled TAUD0TOE00 0x1: Independent timer output mode enabled
TAUD0 channel output mode register (TAUD0TOM)	0xFFBF0248	0x0000	This register specifies output mode of each channel. TAUD0TOM15-00 0x0: Independent channel operation
TAUD0 channel output configuration register (TAUD0TOC)	0xFFBF024C	0x0000	This register specifies output mode of each channel together with TAUDnTOMm. TAUD0TOC15-00 0x0: Operating mode 1
TAUD0 channel start trigger register (TAUD0TS)	0xFFBF01C4	0x0041	This register enables counter operation of each channel. TAUD0TS15-07,05-01 0x0: No operation TAUD0TS06,00 0x1: Counter operation is enabled and TAUDnTEm in TAUDnTE is set to 1.

Table 6-5 Example of Port Register Settings

Register Name	Address	Set Value	Description
Digital noise elimination control register (DNFACTL_TAUD0)	0xFFED0E00	0x00	This register sets conditions for eliminating noise of channel number m in DNF group number n. NFSTS[2:0] 0x0: Number of digital noise elimination sampling times: Twice PRS[3:0] 0x0: DNF input clock/ 1
Digital noise elimination enable register (DNFAen_TAUD0L)	0xFFED0E04	0x40	NFENL6 0x1: Digital noise eliminated
Port control register (PCR0_0)	0xFFD92000	0x00000045	This register enables all settings of a pin. PUCC, PDSC 0x0: Drive intensity low PBDC 0x0: Bidirectional mode disabled PIBC 0x0: Input buffer disabled PMC 0x1: Alternative mode PIPC 0x0: Software input/output control PM 0x0: Output mode (output enabled) PFCEAE, PFCAE, PFCE, PFC 0x5: Alternative output mode 6 (ALT-OUT6)
Port control register (PCR10_1)	0xFFD92284	0x0000005A	This register enables all settings of a pin. PUCC, PDSC 0x0: Drive intensity low PBDC 0x0: Bidirectional mode disabled PIBC 0x0: Input buffer disabled PMC 0x1: Alternative mode PIPC 0x0: Software input/output control PM 0x1: Input mode (output disabled) PFCEAE, PFCAE, PFCE, PFC 0xA: Alternative input mode 11 (ALT-IN11)

Table 6-6 Example of Interrupt Control Register Settings

Register Name	Address	Set Value	Description
EI level interrupt control register 320 (EIC320)	0xFFF80280	0x004F	This register is provided for each EI level interrupt source to set interrupt control conditions for each source. EIMKn 0x0: Interrupt processing enabled EITBn 0x4: Table reference method EIPn 0xF: Priority 15

Lists of functions and variables used in this operation example are provided in Table 6-7 and Table 6-8.

Table 6-7 List of Functions

Function Name	Description
main0	Calls each function.
port_init	Sets P0_0, P10_6 pins to TAUD0O0, TAUD0I6 features respectively.
pulse_init	Makes initial settings for TAUD0.
pulse_start	Starts the timer TAUD0 CH0 for pulse waveform output and CH6 for pulse width measurement.
pulse_measure	Interrupt processing that takes place when TAUD0 CH6 captures the pulse width. This function stores the pulse width and occurrence of an overflow.

Table 6-8 List of Variables

Variable Name	Description
pulsewidth	Stores the high-level width of a measured pulse signal.
overflow	Stores occurrence of counter overflow when the high-level width is measured.

6.5 Operation Flow

Figure 6-3 shows the operation flow of this operation example.

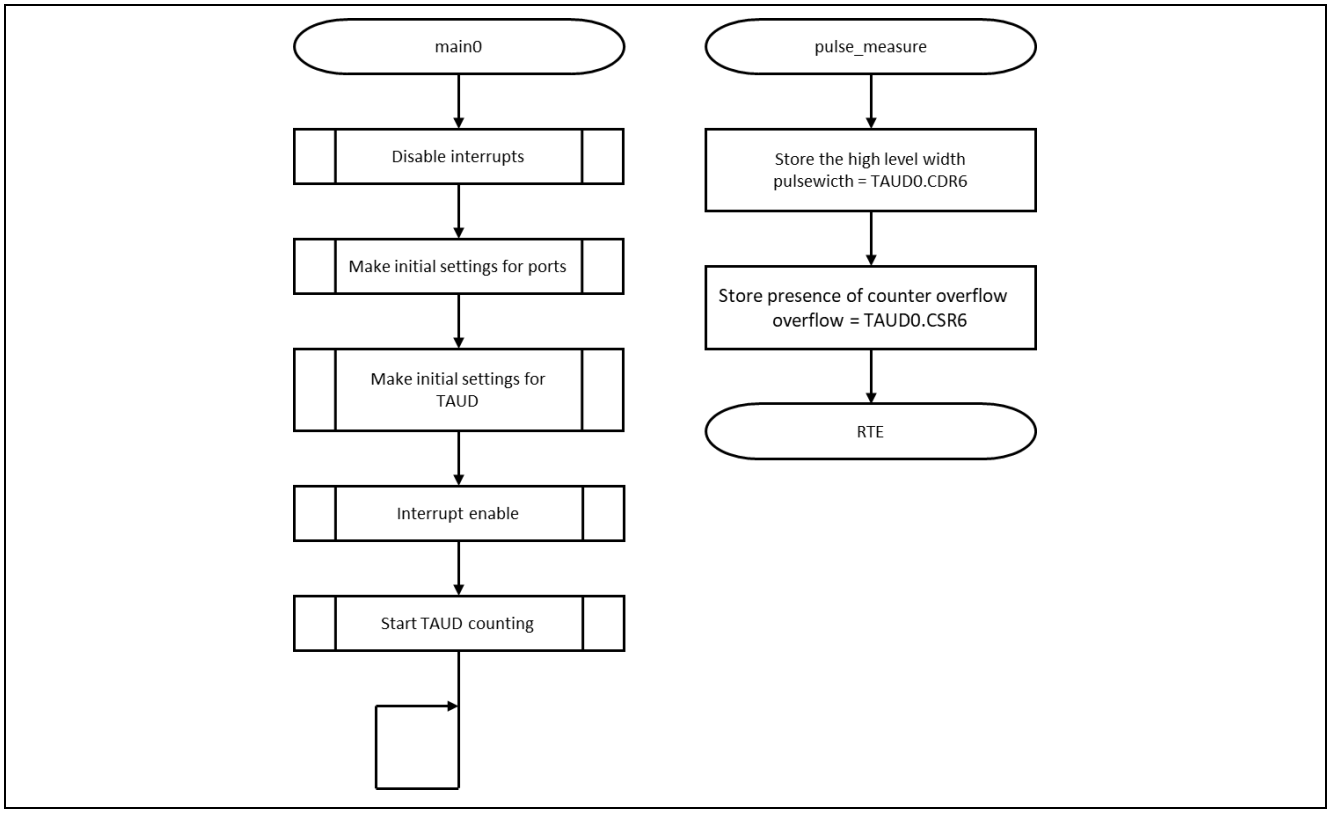


Figure 6-3 Operation Flow

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2023.09.22	-	First edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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