# RH850/U2B6

## sDMAC usage example

### Introduction

This application note describes a setting example of the sDMAC (Direct Memory Access) function of the RH850 / U2B6.

Although the task examples and application examples described in this application note have been confirmed to work, please be sure to check the operating environment before using them.

### Target Device

This application note applies to RH850/U2B6

### Contents

# 1. Introduction

This application note describes how to use the sDMAC function of the RH850 and an example of creating firmware.

The following usage is explained.

-DMA transfer using sDMAC (Auto request mode)

-DMA transfer using sDMAC (Hardware request mode using descriptor)

# 2. DMA transfer (sDMAC, Auto reqest mode)

## 2.1 Operating Conditions for Features Used

The operating conditions of the functions used in this operation example are shown below.

Table 2-1 sDMAC settings

| Item | Description |
|---|---|
| Channel | sDMAC0 CH0 |
| Transfer mode | Auto reqest mode |
| Transfer cycle | 50 cycles |
| Function used | Slow speed mode |

Table 2-2 TAUD settings

| Item | Description |
|---|---|
| Channel | TAUD0 CH0 |
| Feature to be used | Interval timer |
| Clock supplied to TAUD | PLL output clock (80MHz) |
| Timer operation clock | Prescaler output CK0 = (80MHz)/ 1 |
| Timer counter | 0xFFFF |

Table 2-3 Interrupt settings

| Item | Description |
|---|---|
| Interrupt method | Table reference method |
| INTSDMAC0CH0 interrupt | Enabled (Priority 0) |

## 2.2 Operation

This operation example shows how to perform DMA transfer in the low-speed mode of the auto request mode.

In this operation example, the timer count value of TAUD0CNT0 is read in the main processing loop, and the timer count value read by the automatic request is transferred to another RAM.

When the number of transfers n (50 in this operation example) is reached, the automatic request is cleared after that.

Figure 2-1 shows an operation example.

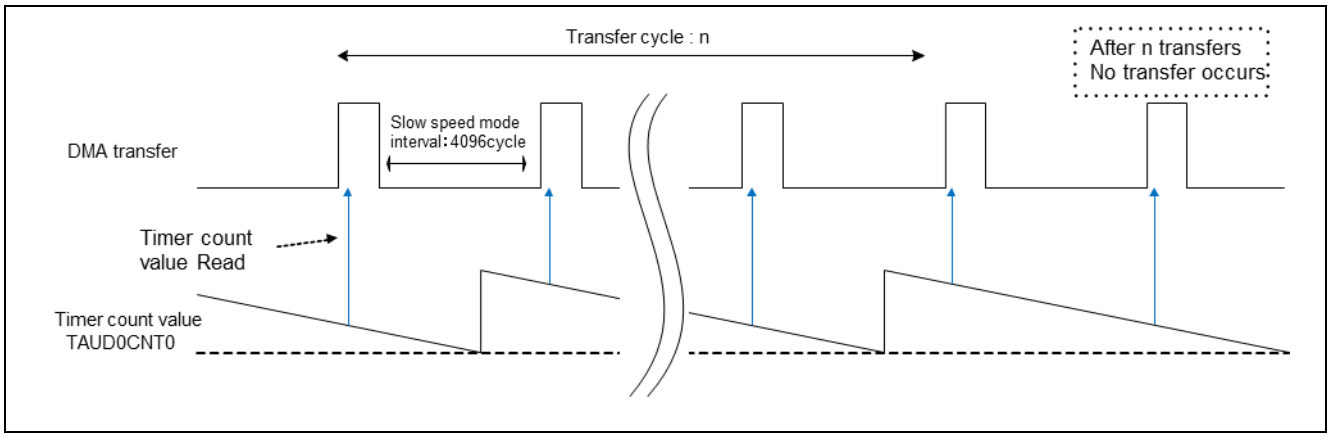


Figure 2-1 Example of Operation

## 2.3 Description of Software

Table 2-4 to Table 2-6 show setting examples of each register used in this operation example.

Table 2-4 Example of DMA register settings

| Register Name | Address | Set Value | Description |
|---|---|---|---|
| DMA Channel Master Setting Register (DMA0CM_0) | 0xFFF90100 | 0x00000000 | Configures the DMA master information.<br>SPID[1:0] 0x1: SPID=1<br>UM 0x0: Supervisor mode |
| DMA Source Address Regisuter (DMA0SAR_0) | 0xFFF98400 | &TAUD0.CNT0 | Set the DMA transfer source address. |
| DMA Destination Address Regisuter (DMA0DAR_0) | 0xFFF92004 | &dest_data[0] | Set the DMA transfer destination address. |
| DMA Transfer Size Register (DMA0TSR_0) | 0xFFF92008 | 0x00000064 | Specifies the DMA transfer size.<br>TSR[31:0] 0x0064: 100Byte (2Byte x 50 times) transfer |
| DMA Transfer Mode Register (DMA0TMR_0) | 0xFFF92010 | 0x00C00411 | Specifies the DMA transfer mode.<br>SLM 0x7: Slow Speed mode (4096 clock cycles)<br>PRI 0x0: Channel request priority is disabled.<br>TSR 0x0: Auto request<br>DM [1:0] 0x1: Destination address is incremented based on destination transaction size.<br>SM [1:0] 0x0: Fixed source address.<br>DTS 0x1: Destination transaction size 2-byte<br>STS 0x1: Source transaction size 2-byte |
| DMA Channel Flag Clear register (DMA0CHFCR_0) | 0xFFF9201C | 0x0000320F | Clears the DMA channel status flags.<br>OVFC 0x1: Hardware transfer request overflow flag clear.<br>DRQC 0x1: Hardware transfer request clear.<br>DPEC 0x1: Descriptor enable clear.<br>CAEC 0x1: Address error flag clear.<br>DSEC 0x1: Descriptor step end flag clear.<br>TEC 0x1: Transfer end flag clear.<br>DEC 0x1: DMA enable clear. |
| DMA Operation Register (DMA0OR) | 0xFFF90060 | DME: 0x1 | controls master enable and specifies the priority level of all DMA channels.<br>DME 0x1: Enable DMA transtfers on all channels. |
| DMA Channel Control Register (DMA0CHCR_0) | 0xFFF92014 | DE: 0x1<br>DE: 0x0<br>IE: 0x1 | Controls DMA transfer.<br>DE 0x1 : DMA transfer enable.<br>DE 0x0 : DMA transfer disable.<br>IE 0x1 : Transfer end interrupt request is enable. |

Table 2-5 Example of TAUD register settings

| Register Name | Address | Set Value | Description |
|---|---|---|---|
| TAUD0 channel stop trigger register (TAUD0TT) | 0xFFBF01C8 | 0x0001 | This register stops counter operation of each channel.<br>TAUD0TT15-02 0x0: No operation<br>TAUD0TT01-00 0x1: Counter operation is stopped. |
| TAUD0 prescaler clock select register (TAUD0TPS) | 0xFFBF0240 | 0x0000 | This register specifies CK0, CK1, CK2, and CK3_PRE clocks of all channels of the PCLK prescaler.<br>TAUD0PRS3-0[3:0] 0x0: PCLK/$2^0$ |
| TAUD0 channel mode OS register (TAUD0CMOR0) | 0xFFBF0200 | 0x0000 | This register controls operation of Channel 0.<br>TAUD0CKS[1:0] 0x0: Operation clock CK0<br>TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm. TAUD0MAS 0x0: Slave channel<br>TAUD0STS[2:0] 0x0: Software trigger.<br>TAUD0MD[4:0] 0x0: Interval timer mode<br>INTTAUDnIm is not output when count operation starts. |
| TAUD0 Chanel data register (TAUD0CDR0) | 0xFFBF0000 | 0xFFFF | Initial down-count value of TAUD0CNT0 |
| TAUD0 Channel start trigger register (TAUD0TS) | 0xFFBF01C4 | 0x0001 | Enable counter operation of each channels.<br>TAUD0TS15-01 0x0: No operation.<br>TAUD0TS00 0x1: Counter operation is enabled. |

Table 2-6 Example of interrupt control settings

| **Register Name** | **Address** | **Set Value** | **Description** |
|---|---|---|---|
| EI level interrupt control register 70 (EIC70) (INTSDMAC0CH0) | 0xFFF8008C | 0x0040 | This register is provided for each EI level interrupt source to set interrupt control conditions for each source.<br>EIMKn 0x0: Interrupt processing enabled<br>EITBn 0x4: Table reference method<br>EIPn 0x0: Priority 0 |

Table 2-7 to Table 2-8 show a list of functions, variables, and constants used in this operation example.

Table 2-7 List of Functions

| Function Name | Description |
|---|---|
| pe0_main | Calls each function. |
| dmac0_ch0_init | Makes initial settings for sDMAC. |
| dmac0_ch0_start | Enable sDMAC operation. |
| taud0_ch0_init | Makes initial setting for TAUD0. |
| taud0_ch0_start | Start TAUD0 operation. |
| sdmac0_ch0_interrupt | Processes sDMAC0 channel 0 transfer end interrupt. |

Table 2-8 List of Variables

| Variable Name | Description |
|---|---|
| dest_data[50] | RAM area of DMA transfer destination. |

## 2.4 Description of Software

Figure 2-2 shows the operation flow of this operation example.

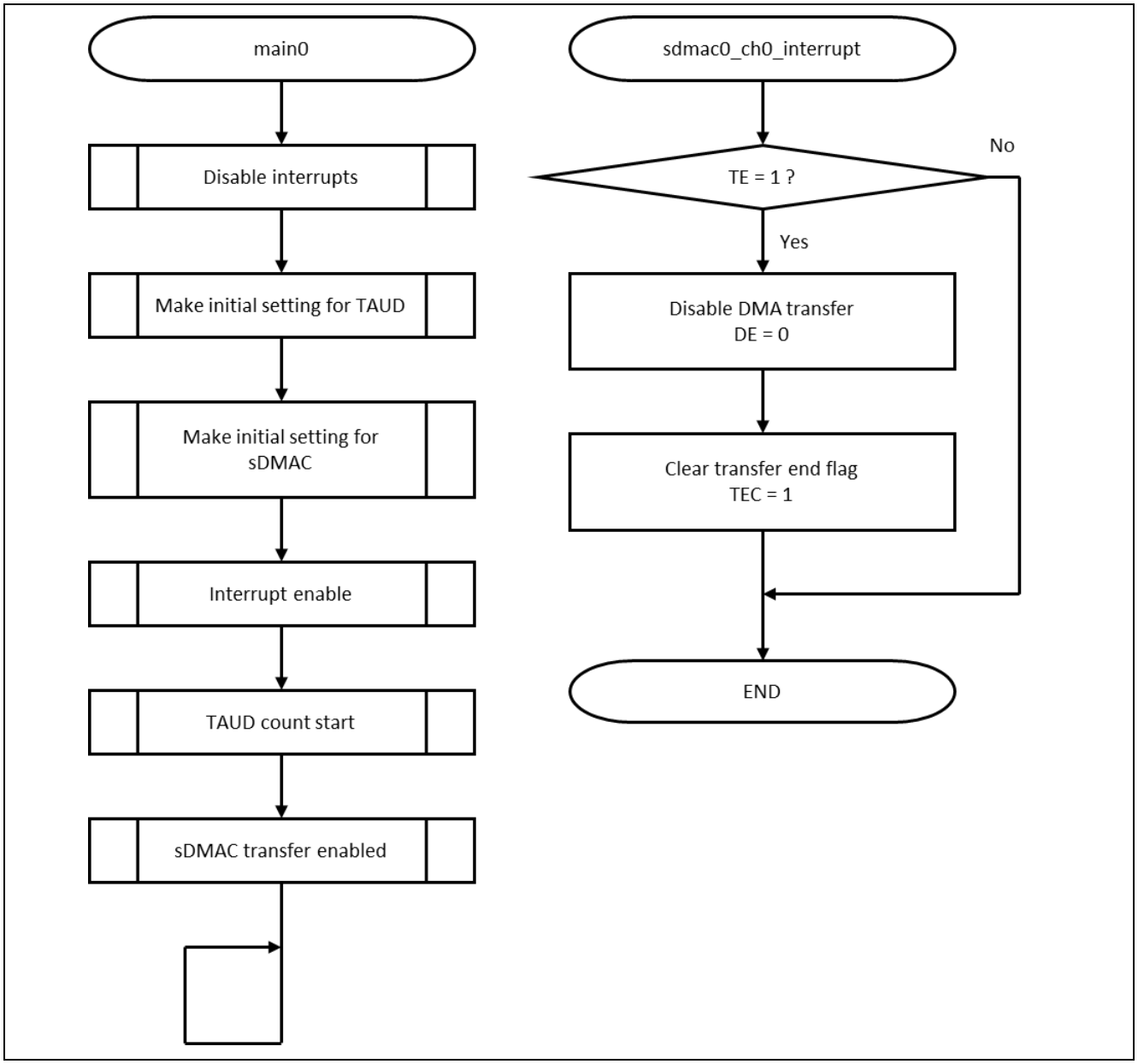


Figure 2-2 Operation Flow

# 3. DMA transfer (sDMAC, Hardware reqest mode)

## 3.1 Overview

This chapter describes how to use sDMAC hardware DMA transfer requests to perform DMA transfers.

In this operation example, INTTAUD0I0 interrupt is used to generate a hardware DMA transfer factor.

In addition, the descriptor function is used to update the transfer information.

## 3.2 Operating Conditions for Features Used

The operating conditions of the functions used in this operation example are shown below.

Table 3-1 DMA settings

| **Item** | **Description** |
|---|---|
| Channel | DMAC0 CH0 |
| Transfer mode | Hardware reqest mode |
| Transfer trigger | INTTAUD0I0 interrupt |
| Function used | Descriptor |

Table 3-2 TAUD setting

| **Item** | **Description** |
|---|---|
| Feature to be used | Interval timer |
| Clock supplied to TAUD | PLL output clock (80MHz) |
| Timer operation clock | Prescaler output CK0 = (80MHz)/ 1 |

Table 3-3 Interrupt of sDMAC settings

| **Item** | **Description** |
|---|---|
| Interrupt method | Table reference method |
| INTSDMAC0CH0 interrupt | Enabled (Priority 0) |

## 3.3 Operation

In this operation example, a hardware DMA transfer request is generated each time the interval timer expires, and the descriptor operation is processed by the occurrence of the transfer request to perform DMA transfer.

Figure 3-1 shows an operation example of a hardware DMA transfer request using the descriptor function.

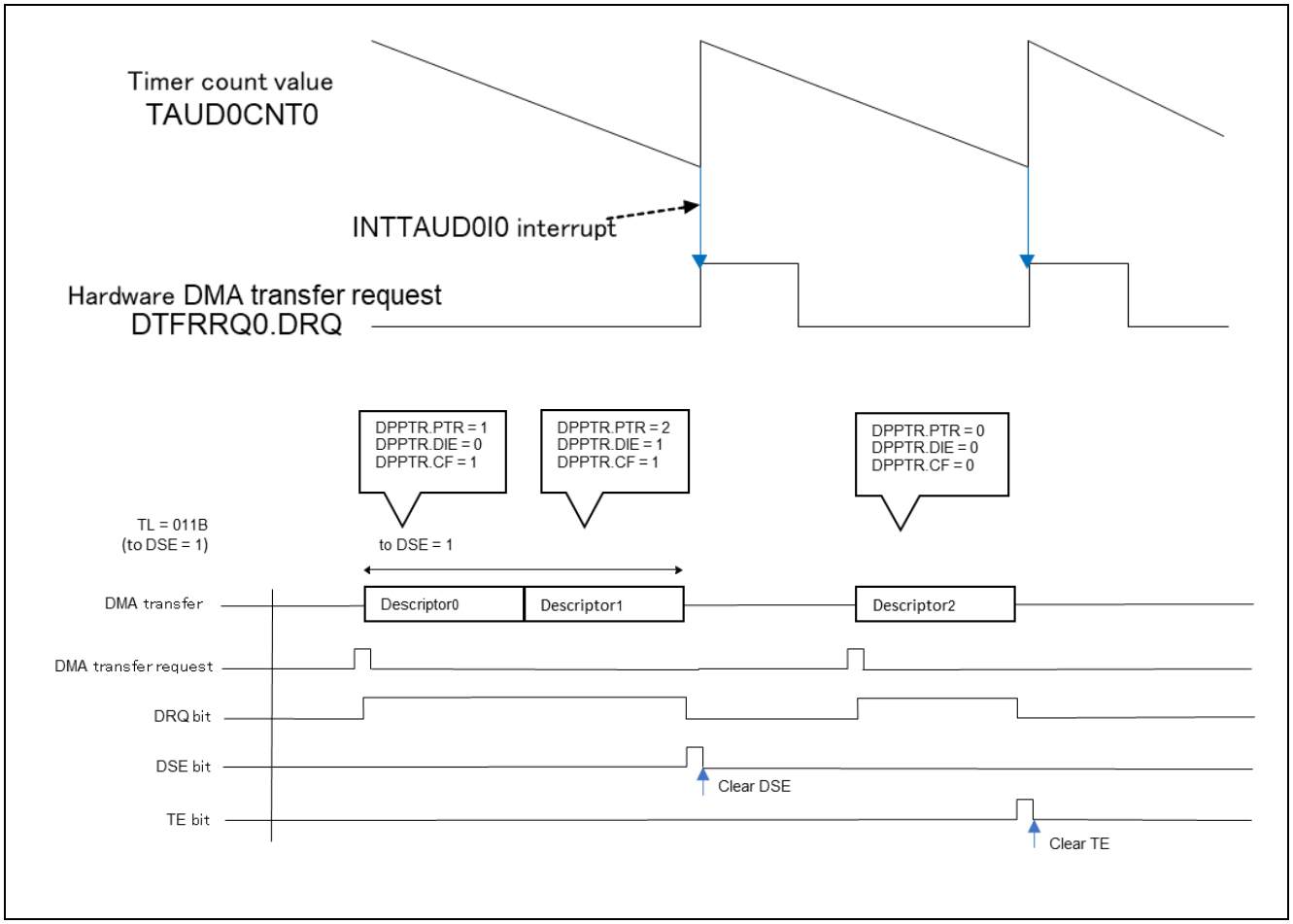


Figure 3-1 Example of Operation

## 3.4 Discription of Software

**Table 3-4 to Table 3-7 the setting example of each register used in this operation example is shown.**

Table 3-4 Example of sDMAC register settings

| Register Name | Address | Set Value | Description |
|---|---|---|---|
| sDMAC0 Transfer Request Group Selection Register (DMACSEL0_13) | 0xFF090434 | 0x00000000 | Specifies the sDMACj transfer request group for each channel.<br>SEL4 [1:0] 0X0: Transfer request group 0 |
| DMA Channel Master Setting Register (DMA0CM_0) | 0xFFF90100 | 0x00000000 | Configures the DMA master information.<br>SPID[1:0] 0x1: SPID=1<br>UM 0x0: Supervisor mode |
| DMA Transfer Mode Register (DMA0TMR_0) | 0xFFF92010 | 0x00001500 | Specifies the DMA transfer mode.<br>SLM 0x0: Normal mode<br>PRI 0x0: Channel request priority is disabled.<br>TSR 0x0: Hardware request<br>DM [1:0] 0x1: Destination address is incremented based on destination transaction size.<br>SM [1:0] 0x0: Source address is incremented based on Source transaction size.<br>DTS 0x1: Destination transaction size 1-byte<br>STS 0x1: Source transaction size 1-byte |
| DMA Descriptor Control Register (DMA0DPCR_0) | 0xFFF92054 | 0x00000007 | Specifies which channel settings will be updated with the contents of the descriptor memory.<br>UPF[0] 1: Enable updating the source address.<br>UPF[1] 1: Enable updating the destination address.<br>UPF[2] 1: Enable updating the transfer size.<br>UPF[3~10] 0: Disabale updating other setting. |
| DMA Descriptor Pointer Register (DMA0DPPTR_0) | 0xFFF92050 | PTR: 0x0000 | Specifies the address of the next register setting in the descriptor memory.<br>PTR 0x0000: Address pointer of descripeor 000 |
| DMA Resorce Select Register (DMA0RS_0) | 0xFFF92040 | 0x000030D4 | Specifies the source and control settings for hardware transfer requests.<br>TL 0x3: Until the DSE flag is asserted.<br>PLE 0x0: Pre-load disable.<br>DRQI 0x0: Disabled DRQ initial when desctiptor settings are loaded.<br>RS 0xD4: Selected DMA request source. |
| DMA Channel Flag Clear register (DMA0CHFCR_0) | 0xFFF9201C | 0x0000320F | Clears the DMA channel status flags.<br>OVFC 0x1: Hardware transfer request overflow flag clear.<br>DRQC 0x1: Hardware transfer request clear.<br>DPEC 0x1: Descriptor enable clear.<br>CAEC 0x1: Address error flag clear.<br>DSEC 0x1: Descriptor step end flag clear.<br>TEC 0x1: Transfer end flag clear.<br>DEC 0x1: DMA enable clear. |

| | | | |
|---|---|---|---|
| DMA Operation Register (DMA0OR) | 0xFFF90060 | DME: 0x1 | controls master enable and specifies the priority level of all DMA channels.<br>DME 0x1: Enable DMA transtfers on all channels. |
| DMA Channel Control Register (DMA0CHCR_0) | 0xFFF92014 | DPE: 0x1<br>DPB: 0x1<br>DSIE: 0x1<br>IE: 0x1<br>DE: 0x1<br>DE: 0x0 | Controls DMA transfer.<br>DPE 0x1: Enable descriptor operation.<br>DPB 0x1: Start DMA transfer after the channel configuration is copied from the descriptor memory.<br>DSIE 0x1: Enable descriptor step end interrupt.<br>IE 0x1: Enable transfer end interrupt.<br>DE 0x1: Enable DNA transfer.<br>DE 0x0: Disable DNA transfer. |
| DMA Source Address Register 0 (DMA0SAR_0) | 0xFFF92000 | &dp0_source_data_table[0]<br>&dp1_source_data_table[0]<br>&dp2_source_data_table[0] | This register specifies the source address for DMA transfer. |
| DMA Destination Address Register 0 (DMA0DAR_0) | 0xFFF92004 | &dp0_dest_data[0]<br>&dp1_dest_data[0]<br>&dp2_dest_data[0] | This register specifies the DMA transfer destination address. |
| DMA Transfer Size Register 0 (DMA0TSR_0) | 0xFFF92008 | 0x00000032 | This register specifies the DMA transfer size.<br>TSR 0x00000032: 50byte |
| DMA Descriptor Pointer Register 0 (DMA0DPPTR_0) | 0xFFF92050 | 0x00000011<br>0x00000023<br>0x00000000 | PTR 0x008: Address pointer of descriptor<br>0x004: Address pointer of descriptor<br>DIE 0x1: Interrupt request is enabled<br>0x0: Interrupt request is disabled<br>CF 0x1: Continuation enabled of descriptor<br>0x0: Continuation disable of descriptor |

Table 3-5 Descriptor memory settings

| APB address | Descriptor pointer | Descriptor memory | | |
|---|---|---|---|---|
| 0x4000 | 0x000 | DMA0SAR_0 | &dp0_source_data_table[0] | Descriptor[0] |
| 0x4004 | 0x001 | DMA0DAR_0 | &dp0_dest_data[0] | |
| 0x4008 | 0x002 | DMA0TSR_0 | 0x00000032: 50byte | |
| 0x400C | 0x003 | DMA0DPPTR_0 | 0x00000011 | |
| | | | 0x4: Descriptor pointer | |
| | | | 0x0: Disable descriptor step end interrupt | |
| | | | 0x1: Enable descriptor continuation | |
| 0x4010 | 0x004 | DMA0SAR_0 | &dp1_source_data_table[0] | Descriptor[1] |
| 0x4014 | 0x005 | DMA0DAR_0 | &dp1_dest_data[0] | |
| 0x4018 | 0x006 | DMA0TSR_0 | 0x00000032: 50byte | |
| 0x401C | 0x007 | DMA0DPPTR_0 | 0x00000023 | |
| | | | 0x8: Descriptor pointer | |
| | | | 0x1: Enable descriptor step end interrupt | |
| | | | 0x1: Enable descriptor continuation | |
| 0x4020 | 0x008 | DMA0SAR_0 | &dp2_source_data_table[0] | Descriptor[2] |
| 0x4024 | 0x009 | DMA0DAR_0 | &dp2_dest_data[0] | |
| 0x4028 | 0x00A | DMA0TSR_0 | 0x00000032: 50byte | |
| 0x402C | 0x00B | DMA0DPPTR_0 | 0x00000000 | |
| | | | 0x0: Descriptor pointer (Arbitrary value) | |
| | | | 0x0: Disable descriptor step end interrupt | |
| | | | 0x0: Disable descriptor continuation | |
| ... | ... | | | |
| 0x4FFC | 0x3FF | | | |

Table 3-6 Example of TAUD register settings

| Register Name | Address | Set Value | Description |
|---|---|---|---|
| TAUD0 channel stop trigger register (TAUD0TT) | 0xFFBF01C8 | 0x0001 | This register stops counter operation of each channel.<br>TAUD0TT15-02 0x0: No operation<br>TAUD0TT01-00 0x1: Counter operation is stopped. |
| TAUD0 prescaler clock select register (TAUD0TPS) | 0xFFBF0240 | 0x0000 | This register specifies CK0, CK1, CK2, and CK3_PRE clocks of all channels of the PCLK prescaler.<br>TAUD0PRS3-0[3:0] 0x0: PCLK/$2^0$ |
| TAUD0 prescaler baud rate settting register (TAUD0BRS) | 0xFFBF0244 | 0x4F | Specifies the division factor of prescaler clock CK3.<br>TAUD0BRS[7:0] 0x50: CK3_PRE/80 |
| TAUD0 channel mode OS register (TAUD0CMOR0) | 0xFFBF0200 | 0xC000 | This register controls operation of Channel 0.<br>TAUD0CKS[1:0] 0x2: Operation clock CK3<br>TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm. TAUD0MAS 0x1: Master channel<br>TAUD0STS[2:0] 0x0: Software trigger.<br>TAUD0MD[4:0] 0x0: Interval timer mode<br>INTTAUDnIm is not output when count operation starts. |
| TAUD0 Chanel data register (TAUD0CDR0) | 0xFFBF0000 | 0x2710 | Initial down-count value of TAUD0CNT0 |
| TAUD0 Channel start trigger register (TAUD0TS) | 0xFFBF01C4 | 0x0001 | Enable counter operation of each channels.<br>TAUD0TS15-01 0x0: No operation.<br>TAUD0TS00 0x1: Counter operation is enabled. |

Table 3-7 Example of interrupt control settings

| Register Name | Address | Set Value | Description |
|---|---|---|---|
| EI level interrupt control register 70 (EIC70) (INTSDMAC0CH0) | 0xFFF8008C | 0x0040 | This register is provided for each EI level interrupt source to set interrupt control conditions for each source.<br>EIMKn 0x0: Interrupt processing enabled<br>EITBn 0x4: Table reference method<br>EIPn 0x0: Priority 0 |

Table 3-8 to Table 3-10 show a list of functions, variables, and constants used in this operation example.

Table 3-8 List of Functions

| Function Name | Description |
|---|---|
| pe0_main | Calls each function. |
| sdmac0_ch0_init | Makes initial settings for sDMAC. |
| sdmac0_ch0_start | Enable sDMAC operation. |
| taud0_ch0_init | Makes initial setting for TAUD0. |
| taud0_ch0_start | Start TAUD0 operation. |
| sdmac0_ch0_interrupt | INTSDMAC0CH0 interrupt processing. |

Table 3-9 List of Variables

| Variable Name | Description |
|---|---|
| dp0_dest_data[50] | RAM area of DMA transfer destination (descriptor0). |
| dp1_dest_data[50] | RAM area of DMA transfer destination (descriptor1). |
| dp2_dest_data[50] | RAM area of DMA transfer destination (descriptor2). |
| *descriptor_ptr | Pointer to descriptor memory |

Table 3-10 List of Constants

| Constants Name | Description |
|---|---|
| dp0_source_data_table[50] | 0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07,<br>0x08, 0x09, 0x0A, 0x0B, 0x0C, 0x0D, 0x0E, 0x0F,<br>0x10, 0x11, 0x12, 0x13, 0x14, 0x15, 0x16, 0x17,<br>0x18, 0x19, 0x1A, 0x1B, 0x1C, 0x1D, 0x1E, 0x1F,<br>0x20, 0x21, 0x22, 0x23, 0x24, 0x25, 0x26, 0x27,<br>0x28, 0x29, 0x2A, 0x2B, 0x2C, 0x2D, 0x2E, 0x2F,<br>0x30, 0x31, |
| dp1_source_data_table[50] | 0x32, 0x33, 0x34, 0x35, 0x36, 0x37, 0x38, 0x39,<br>0x3A, 0x3B, 0x3C, 0x3D, 0x3E, 0x3F,<br>0x40, 0x41, 0x42, 0x43, 0x44, 0x45, 0x46, 0x47,<br>0x48, 0x49, 0x4A, 0x4B, 0x4C, 0x4D, 0x4E, 0x4F,<br>0x50, 0x51, 0x52, 0x53, 0x54, 0x55, 0x56, 0x57,<br>0x58, 0x59, 0x5A, 0x5B, 0x5C, 0x5D, 0x5E, 0x5F,<br>0x60, 0x61, 0x62, 0x63, |
| dp2_source_data_table[50] | 0x64, 0x65, 0x66, 0x67, 0x68, 0x69, 0x6A, 0x6B,<br>0x6C, 0x6D, 0x6E, 0x6F,<br>0x70, 0x71, 0x72, 0x73, 0x74, 0x75, 0x76, 0x77,<br>0x78, 0x79, 0x7A, 0x7B, 0x7C, 0x7D, 0x7E, 0x7F,<br>0x80, 0x81, 0x82, 0x83, 0x84, 0x85, 0x86, 0x87,<br>0x88, 0x89, 0x8A, 0x8B, 0x8C, 0x8D, 0x8E, 0x8F,<br>0x90, 0x91, 0x92, 0x93, 0x94, 0x95, |

## 3.5 Operation Flow

Figure 3-2 shows the operation flow of this operation example.

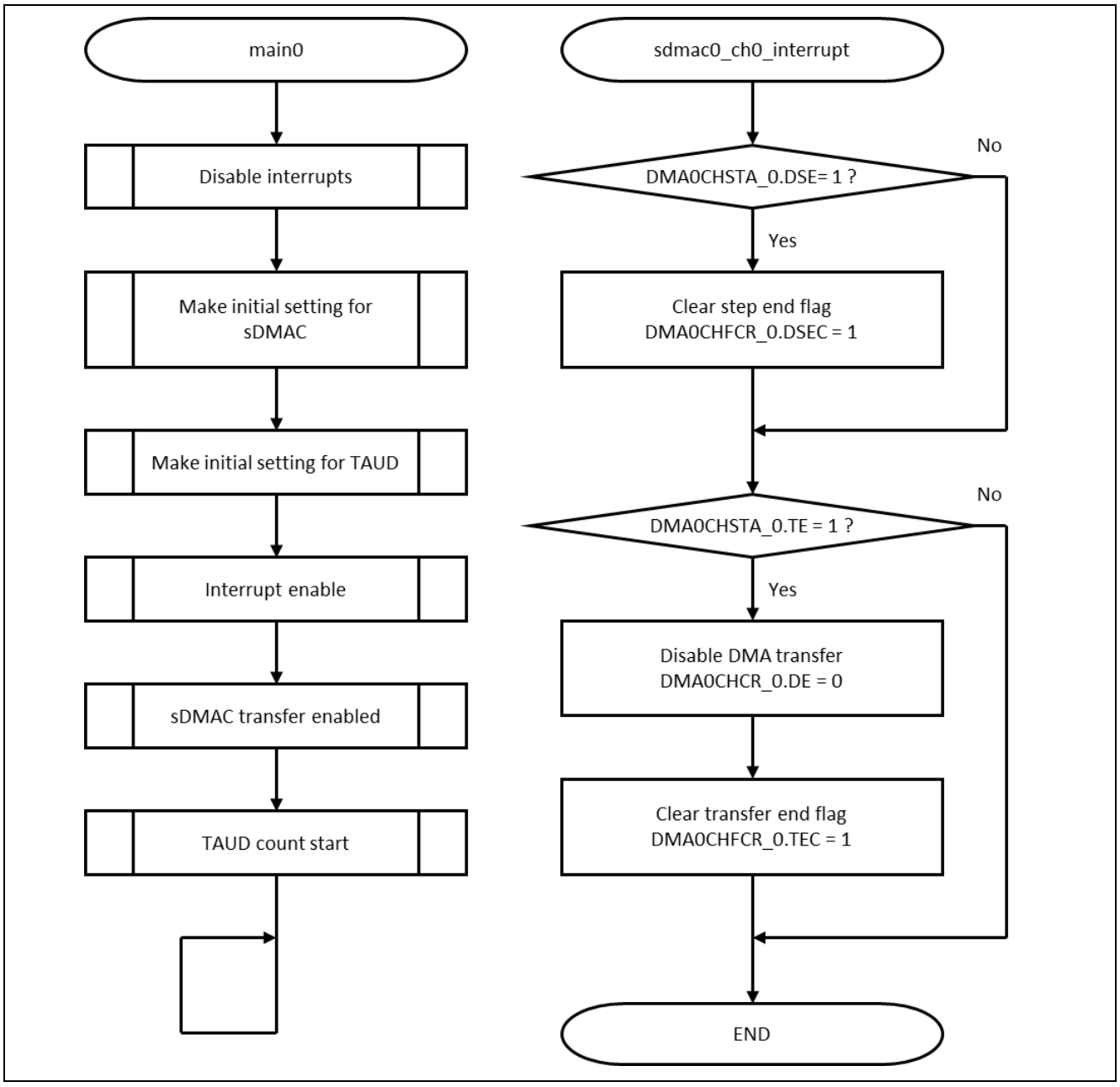


Figure 3-2 Operation Flow

## Revision History

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | 2023.09.22 | - | First edition |
| | | | |
| | | | |

# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

## Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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