RH850/U2B6-FCC

Motor Control Using GTM

Summary

This application note describes methods of the motor control by GTM of the RH850/U2B6.

Although the examples of tasks and applications examples in this application note have been confirmed to work, please be sure to check the operating environment before using the product.

Operation-confirmation device

RH850/U2B6-FCC (R7F702Z22EDBB)

Table of contents

1. Introduction

This application note describes methods of the motor control by GTM of the RH850/U2B6-FCC.

1.1 The function to be used

The RH850/U2B6 hardware functions used in this application note are shown below.

Also, in this application note, each hardware function is controlled from CPU0.

Hardware function name	Symbol
Resolver to Digital Converter (successive-approximation-register analog-to-digital type)	RDC3AL
Analog to Digital Converter	ADCK
Generic Module Timer	GTM
Advanced Routing Unit	ARU
Clock Management Unit	CMU
Cluster Configuration Module	CCU
Time Base Unit	TBU
Timer Input Module	TIM
ARU-connected Timer Output Module	ATOM
Dead Time Module	DTM
Multi Channel Sequencer	MCS
Interrupt Controller	INTC
OS Timer	OSTM
Peripheral Interconnect	PIC
I/O Port	PORT

2. Motor Control Using GTM

This chapter describes how to implement motor control using GTM instead of EMU3S.

This application uses the resolver/digital converter RDC3AL, analog/digital converter ADCK and each sub-module ARU, CCM, CMU, TIM, TBU, ATOM, DTM and MCS installed in the timer module GTM, and selects the input signal to ADCK or TIM with PIC.

2.1 Sample for MCS operation

In this application, we get the angle from the resolver, determine the zone from the compare value stored in RAM, and update the output with the corresponding output value.

This application uses ADCK and RDC3AL installed in U2B6, and ARU, CCM, CMU, TBU, ATOM, DTM, and MCS installed in GTM, and selects the trigger signal to ADCK with PIC.

2.1.1 Operation overview

In this application, the angle information of the resolver is converted to PWM in the following flow.

- Acquire angle information from resolver and output to GTM with angle compare interrupt
- Receive angle information with ADC_CH22_DATA of GTM and transfer to MCS1 and MCS2 via ARU
- MCS0 to MCS2 determine the zone by binary search and determine the PWM output value (MCS0 corresponds to U phase, MCS1 corresponds to V phase, MCS2 corresponds to W phase)
- MCS1 and MCS2 pass the output value to MCS0 via ARU after determining the zone
- MCS0 is the output value for 3 phases, updates the ATOM0 register, and reflects it in the output

Figure 2-1 shows the flow from resolver to PWM output via RDC3AL and GTM in this application.

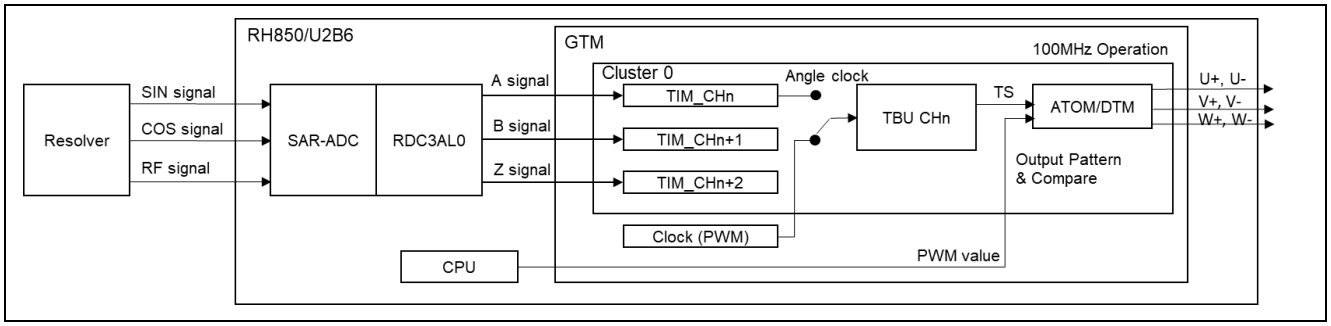
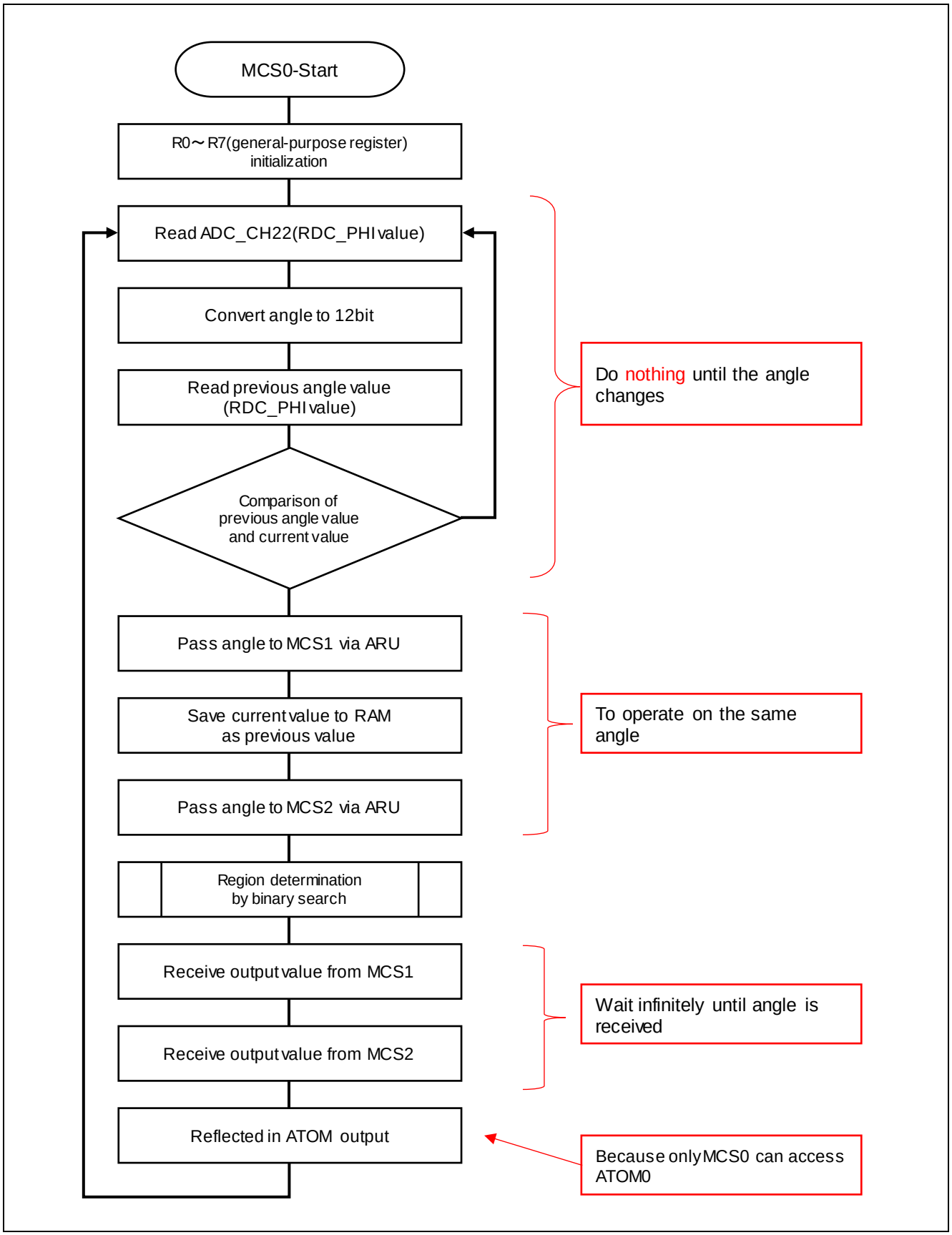


Figure 2-1 Block diagram overview

Figure 2-2 shows the contents of MCS processing in this application.

The following processing programs are copied to MCS-RAM from the mcs0_use.c / mcs0_mem, mcs1_use.c / mcs1_mem, mcs2_use.c / mcm2_mem arrays by the gtm.c / *LoadMcs function.


MCS0-Start
R0～R7(general-purpose register) initialization
Read ADC_CH22(RDC_PHI value)
Convert angle to 12bit
Read previous angle value (RDC_PHI value)
Comparison of previous angle value and current value
Pass angle to MCS1 via ARU
Save current value to RAM as previous value
Pass angle to MCS2 via ARU
Region determination by binary search
Receive output value from MCS1
Receive output value from MCS2
Reflected in ATOM output
Do nothing until the angle changes
To operate on the same angle
Wait infinitely until angle is received
Because only MCS0 can access ATOM0

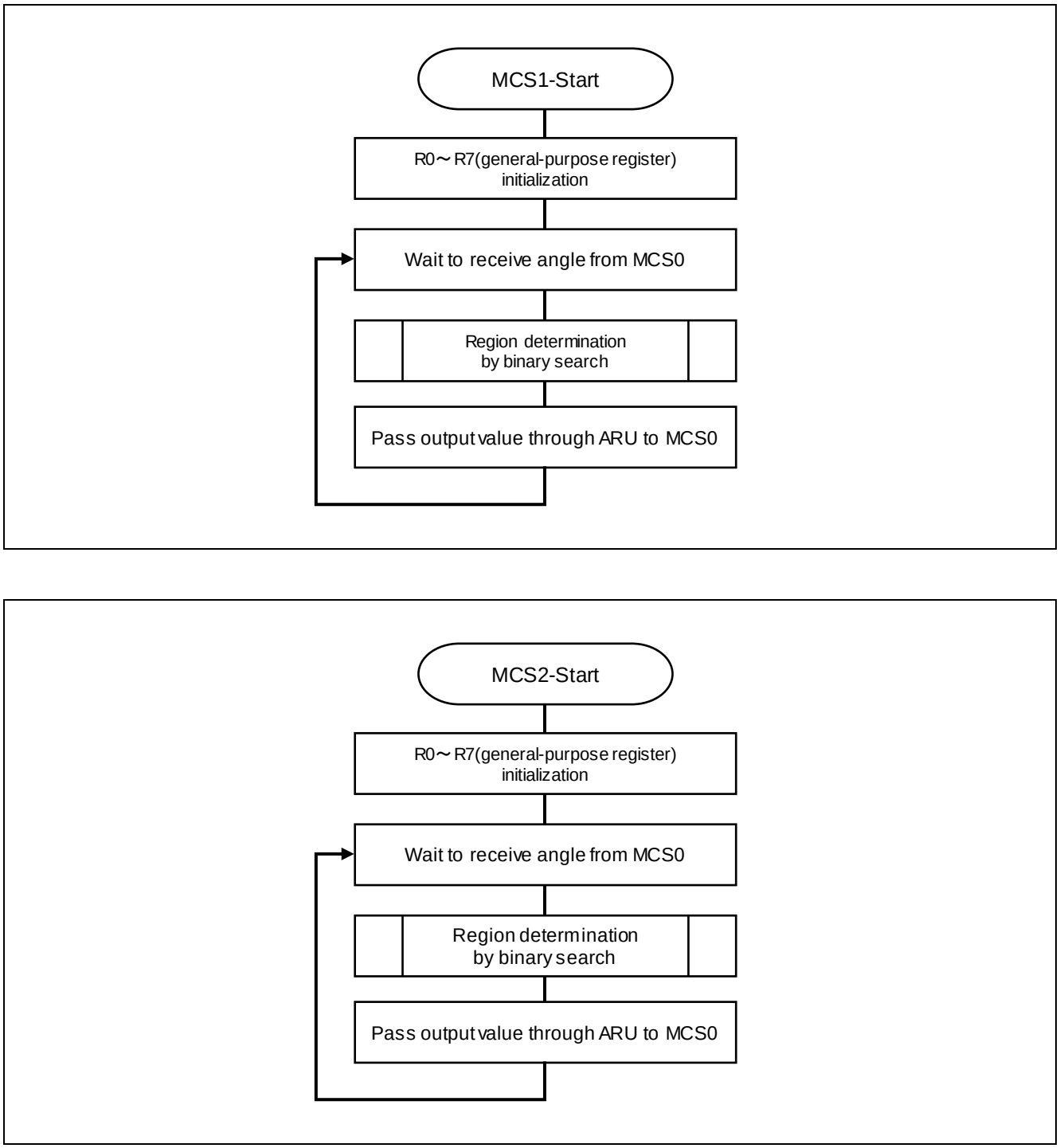


Figure 2-2 MCS processing details

2.1.2 Operation flowchart

Figure 2-3 shows the flow of initialization and startup processing executed when this software is started, and Figure 2.4 shows the processing performed in the main function.

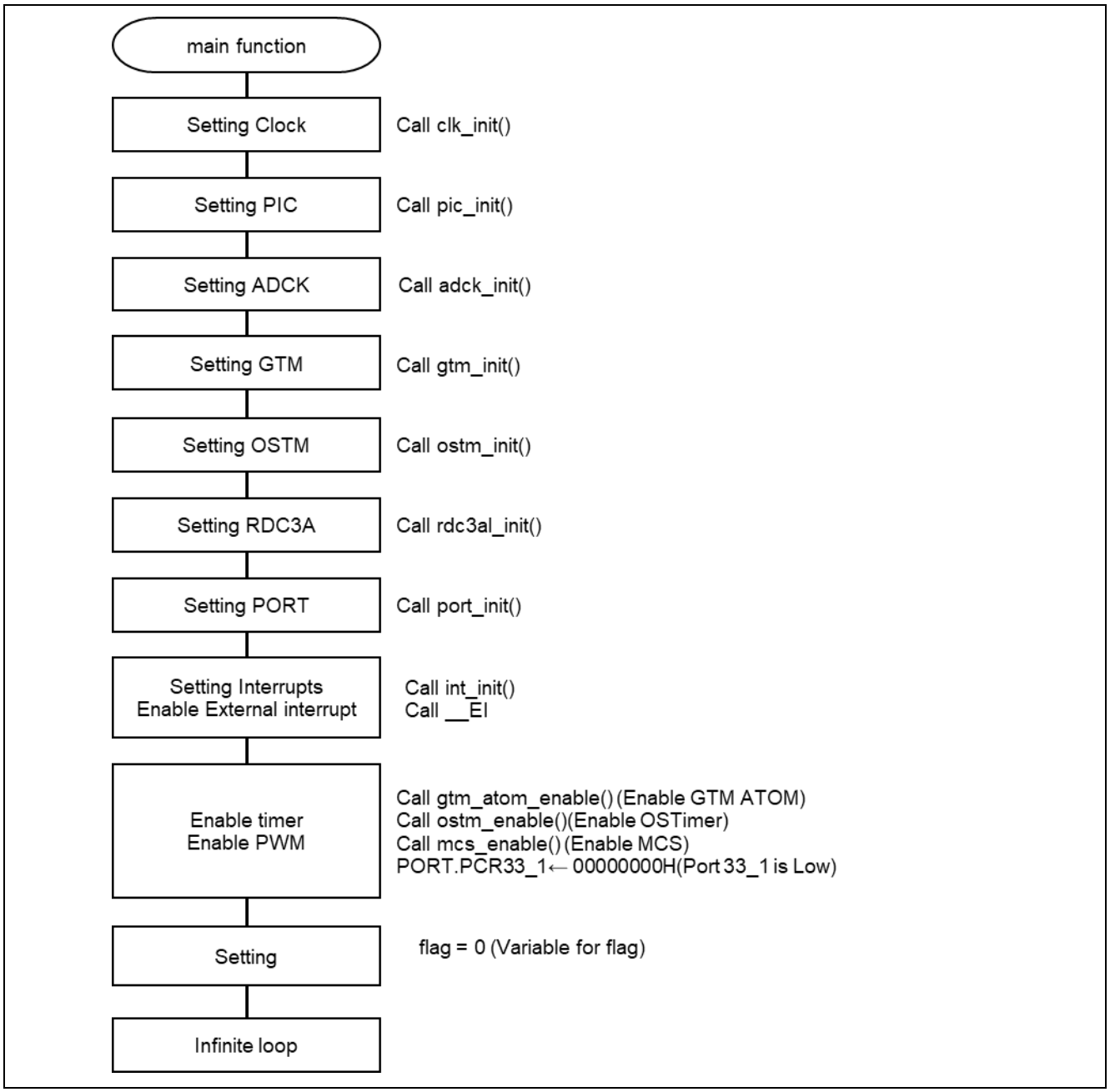


Figure 2-3 Initialization

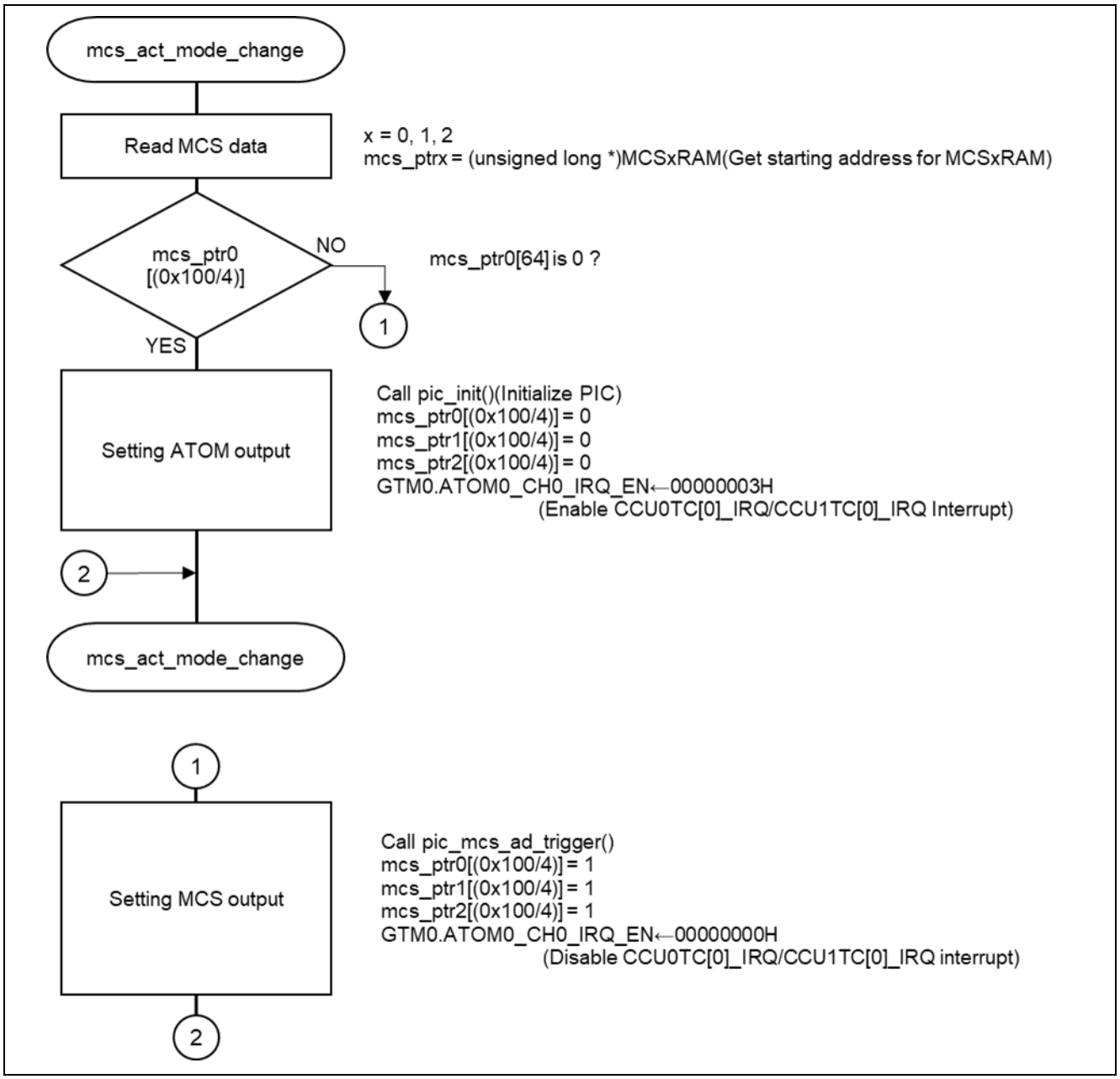


Figure 2-4 MCS operation flag change processing

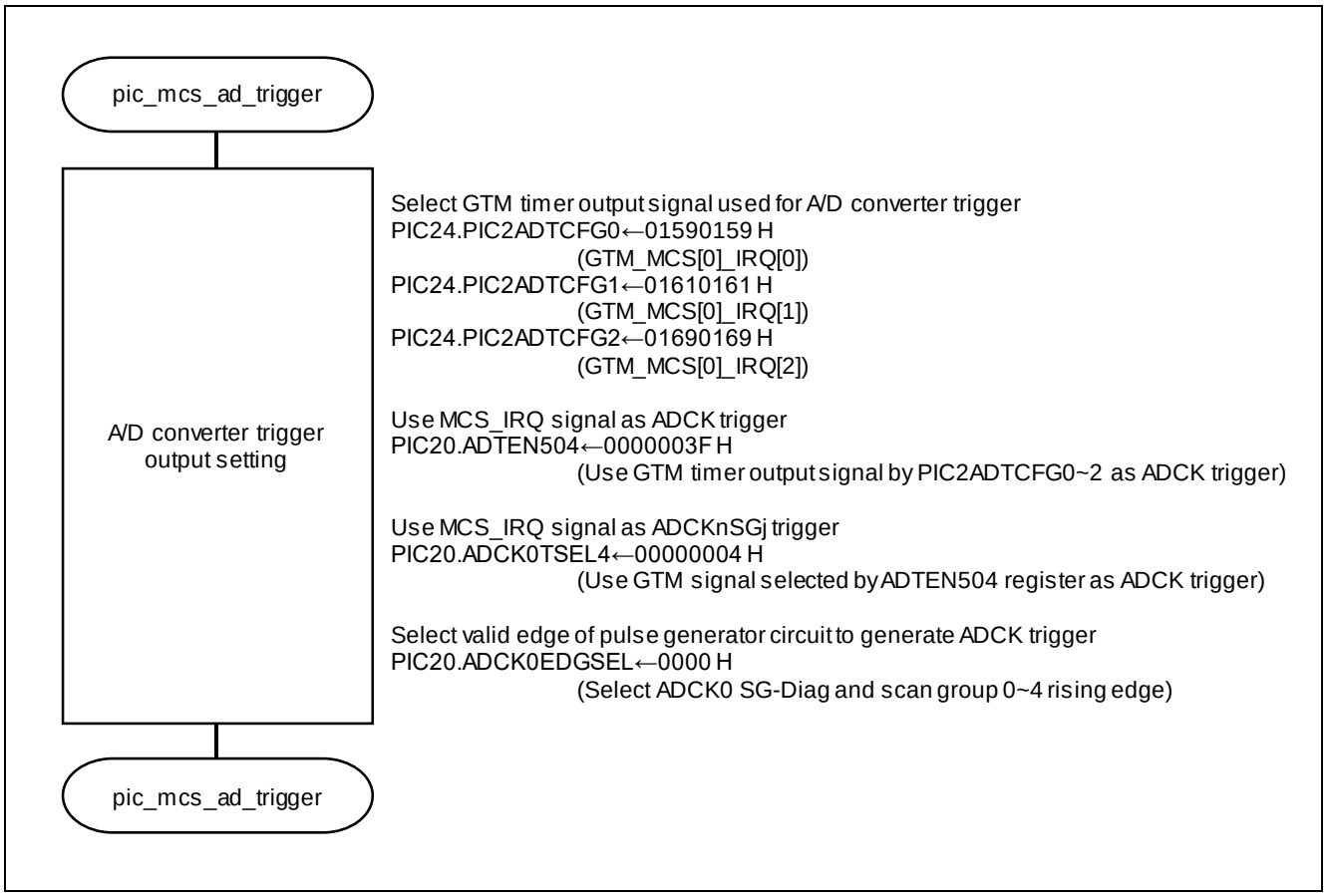


Figure 2-5 PIC setting Process

Figure 2-6 shows the processing contents of the main function running on CPU1 and CPU2 (main1.c / main1, main2.c / main2).

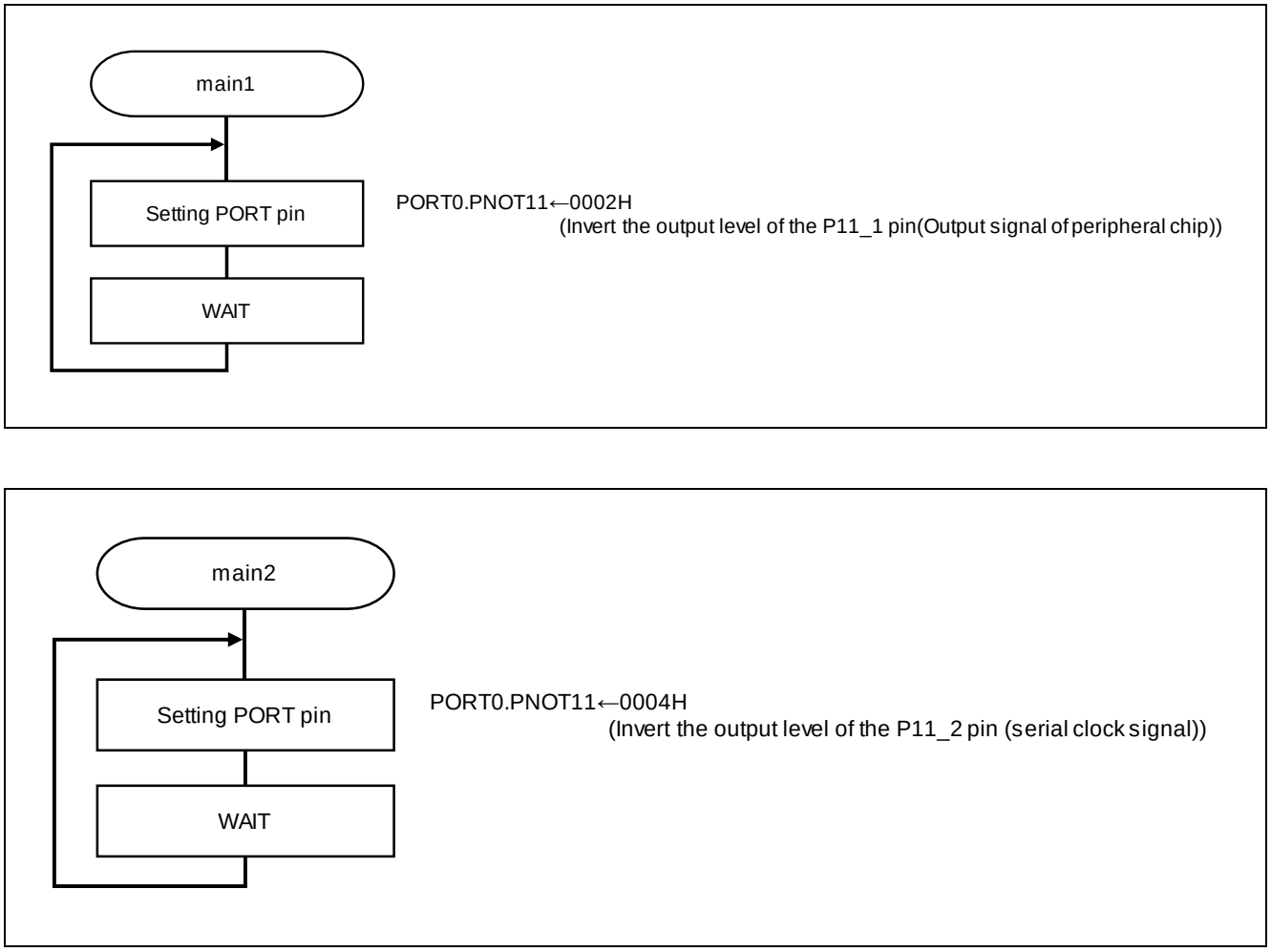


Figure 2-6 Processing content for main1 and main2

Figure 2-7 shows the clock setting flow (main.c / clk_init).

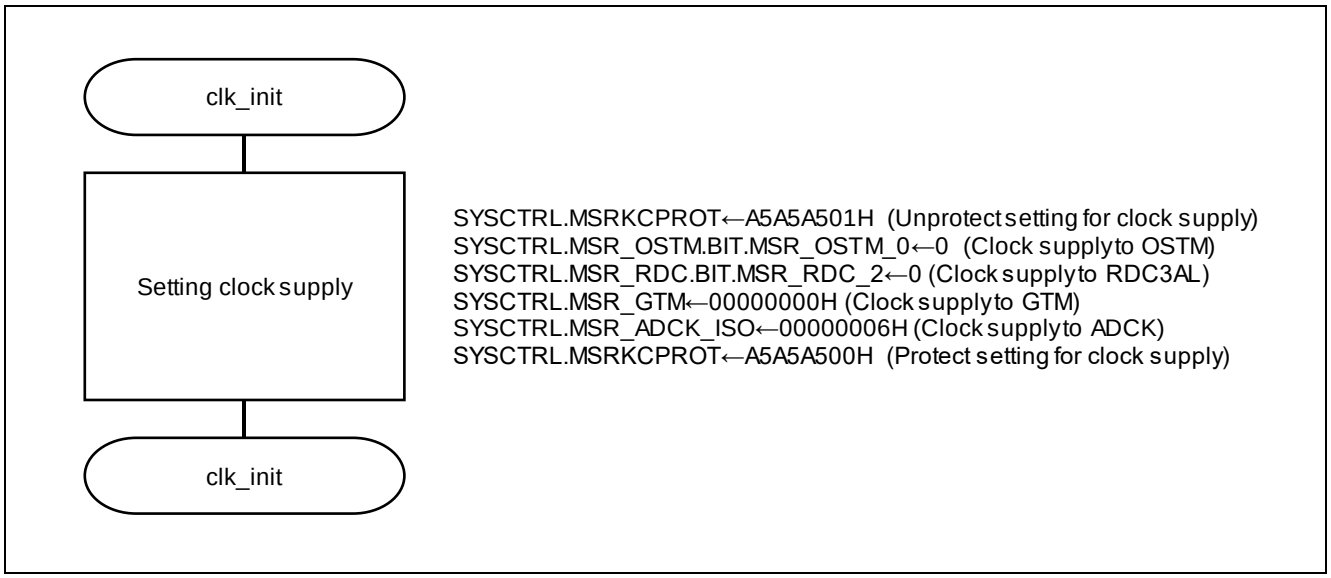


Figure 2-7 Flow of the initial Clock setting

Figure 2-8 shows the PIC setup flow (pic.c/pic_init).

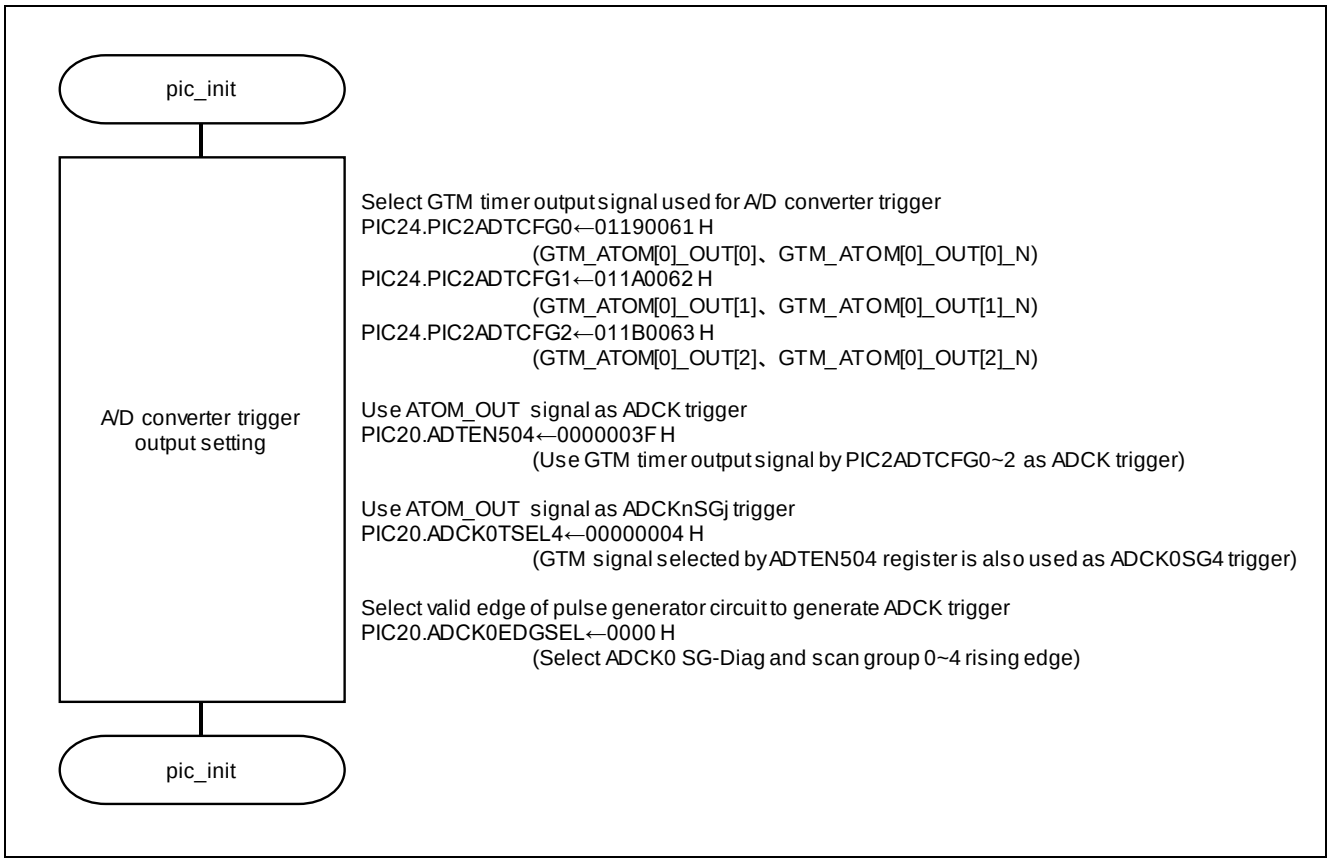


Figure 2-8 Flow of the initial PIC setting

Figure 2-9 shows the ADCK setting flow (adck.c / adck_init).

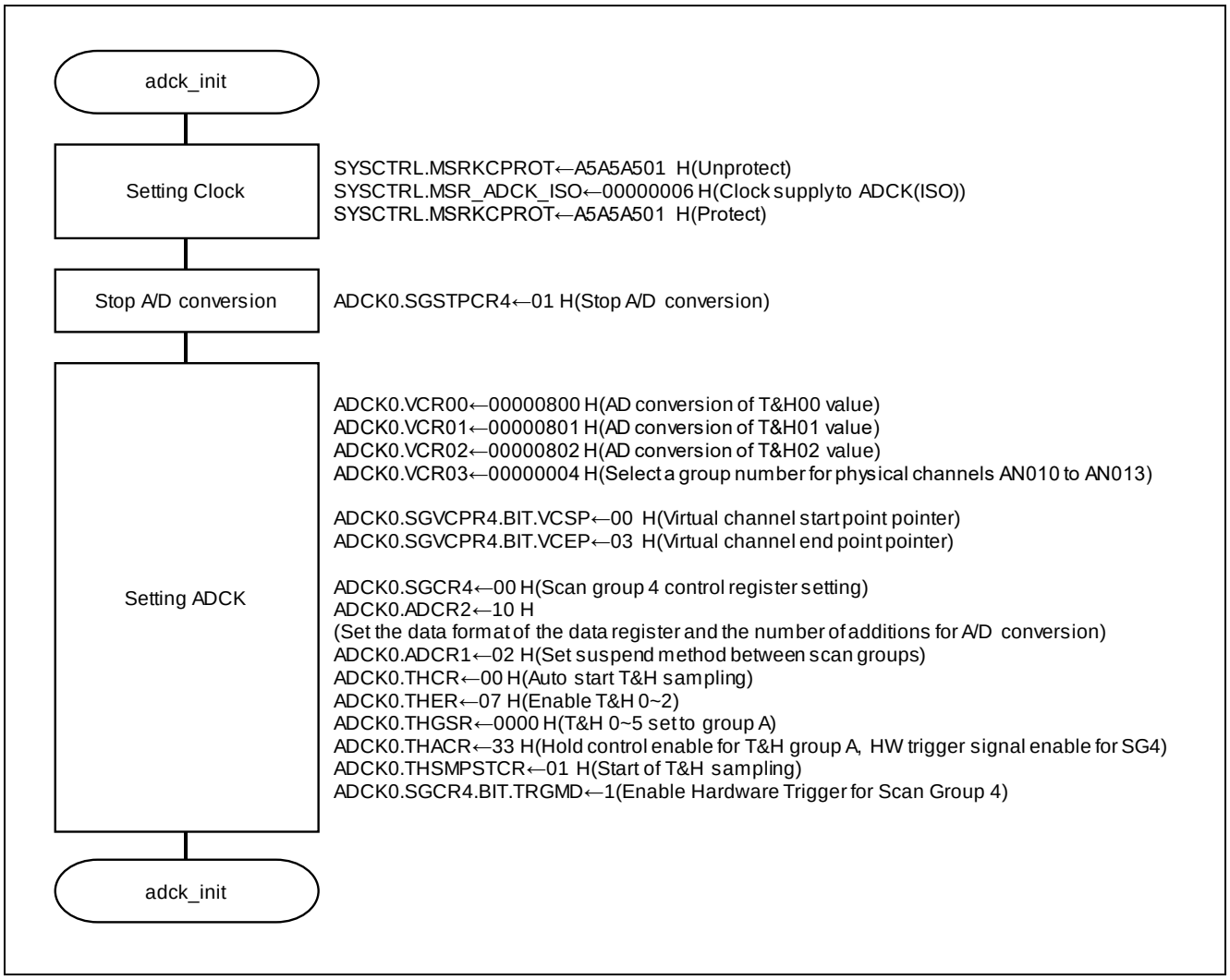
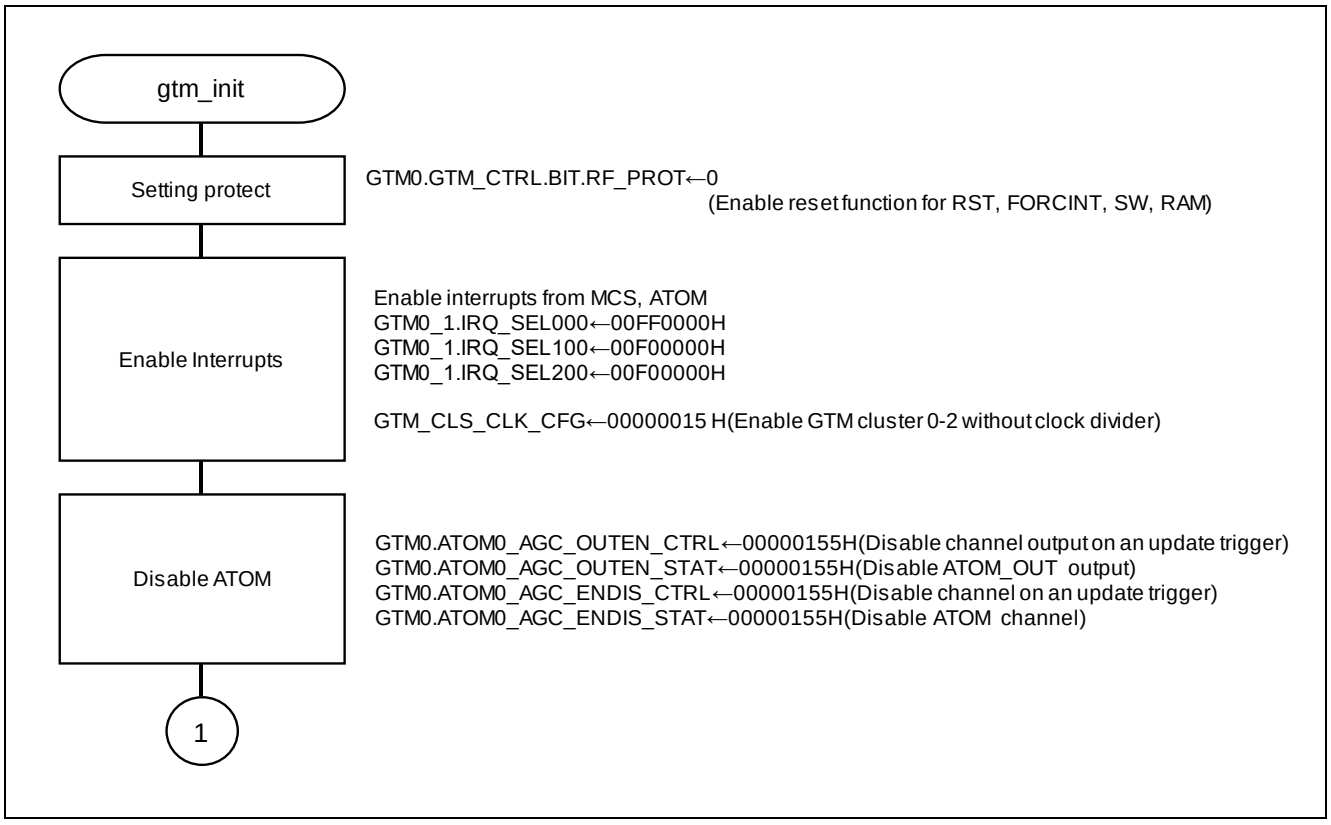
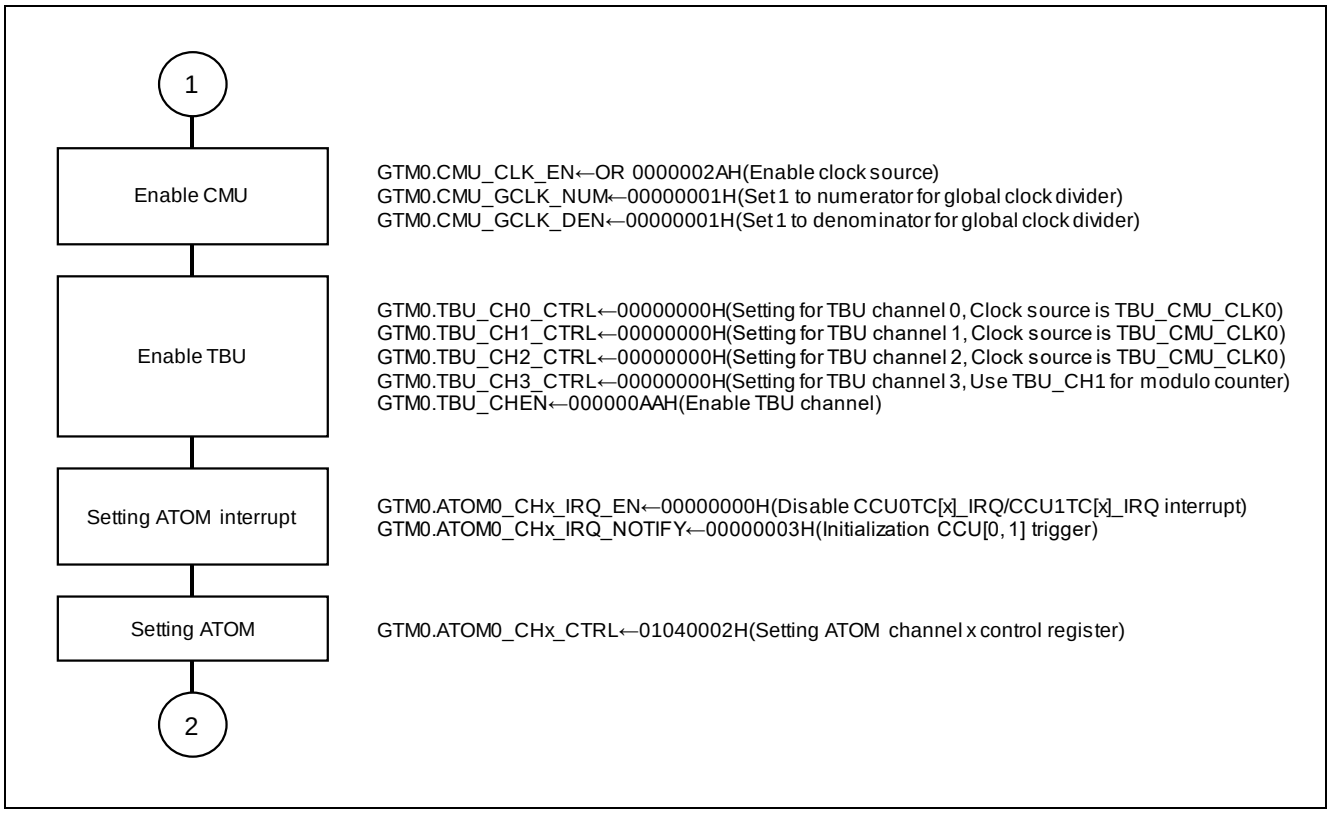
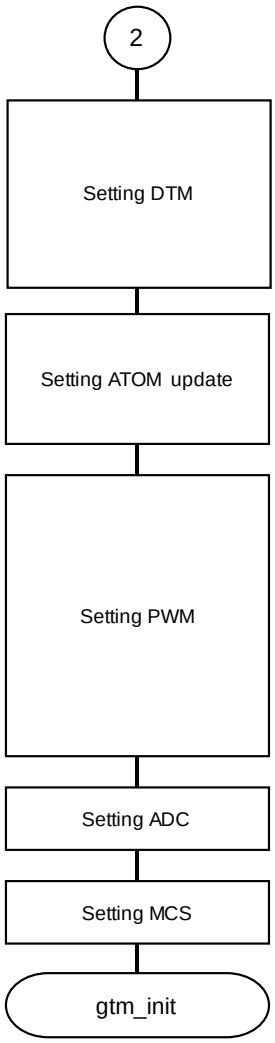


Figure 2-9 Flow of the initial ADCK setting

Figure 2-10 shows the GTM setting flow (gtm.c / gtm_init).







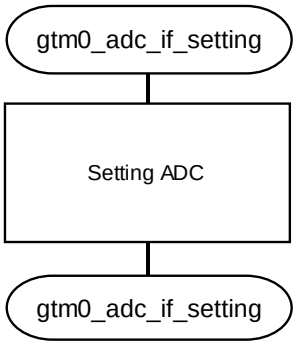
GTM0.CDTM0_DTM4_CTRL←00000001H(DTM configure/control register, define clock source)
GTM0.CDTM0_DTM4_CH_CTRL1←00000000H(DTM control register 1)
GTM0.CDTM0_DTM4_CH_CTRL2←00888888H(DTM control register 2)
GTM0.CDTM0_DTM4_CH_CTRL3←00000000H(DTM control register 3)
GTM0.CDTM0_DTM4_CHx_DTV←DEAD_TIME_COUNT | (DEAD_TIME_COUNT << 16)
(Reload value setting for dead time during measurement)

GTM0.ATOM0_AGC_GLB_CTRL←002A0000H(Setting for ATOM AGC(Grobal control subunit))
GTM0.ATOM0_AGC_FUPD_CTRL←002A002AH(Enable forced update for ATOM channel 0～3)
GTM0.ATOM0_AGC_INT_TRIG←0000002AH(Use internal trigger from channel 0～3(ATOM_TRIGOUT)

GTM0.ATOM0_CHx_SR0(Input value to SR0 for ATOM channel x shadow register)
x = 0 ～ 2 : CARR_COUNT / 2
GTM0.ATOM0_CHx_SR1(Input value to SR1 for ATOM channel x shadow register)
x = 0 ～ 2 : 500
GTM0.ATOM0_CHx_CM0(Input value to ATOM channel x CCU0 compare register)
x = 0 ～ 2 : CARR_COUNT / 2
GTM0.ATOM0_CHx_CM1(Input value to ATOM channel x CCU1 compare register)
x = 0 ～ 2 : 1
GTM0.ATOM0_CHx_CN0(Input value to ATOM channel x CCU0 counter register)
x = 0 ～ 2 : 0

Call gtm0_adc_if_setting() (Setting ADC interface)

Call gtm0_mcs0_ch0_main()(Read MCS data, set MCS interrupt)



GTM0_1.ADCI_STRSEL1←00000000 H
GTM0_1.ADCI_STRSEL.BIT.RDC3A_0_PHI←1(Store value for RDC3A_0_PHI)
GTM0_1.ADCI_RDCSEL←0(Store the RDC3AL value in the bit selected by the above register)

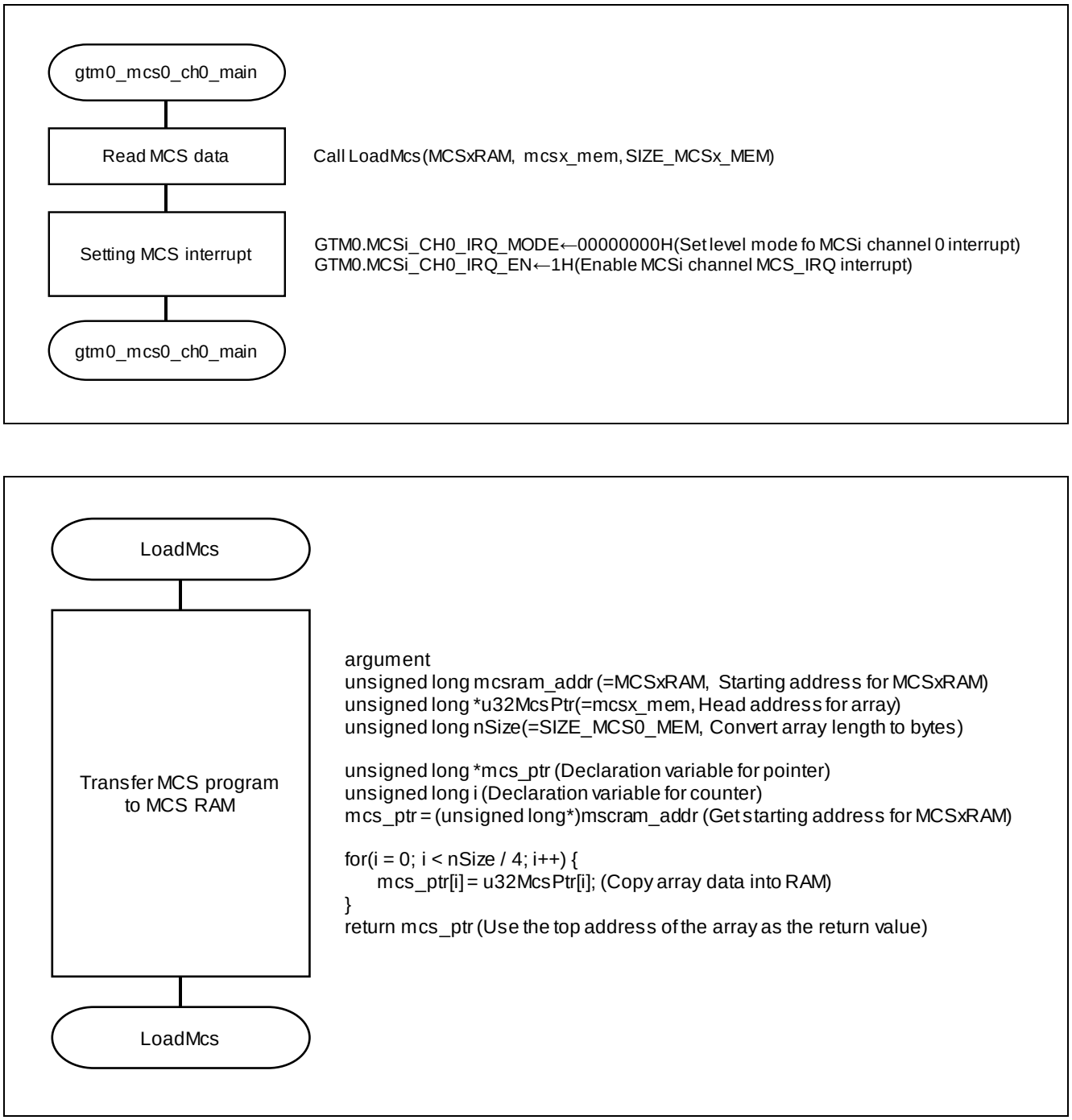


Figure 2-10 Flow of the initial GTM setting
(x = 0 ~ 2、i = 0 ~ 2(exclude those used in loops))

Figure 2-11 shows the OSTM startup setup flow (ostm.c / ostm_init).

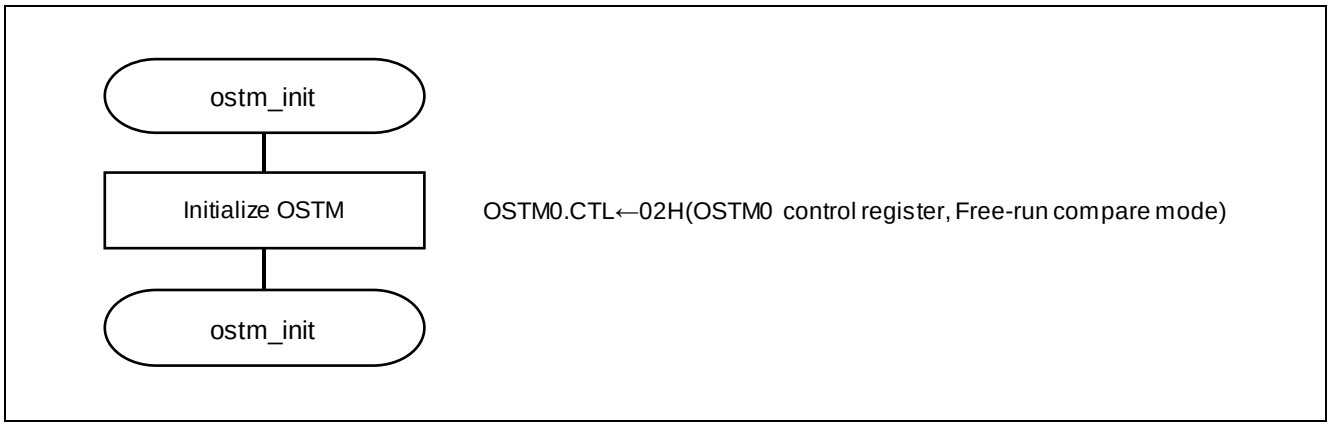


Figure 2-11 Flow of the initial OSTM setting

Figure 2-12 and Figure 2-13 shows the RDC3AL0 initialization and startup setting flow (rdc3al.c / rdc3al_init).

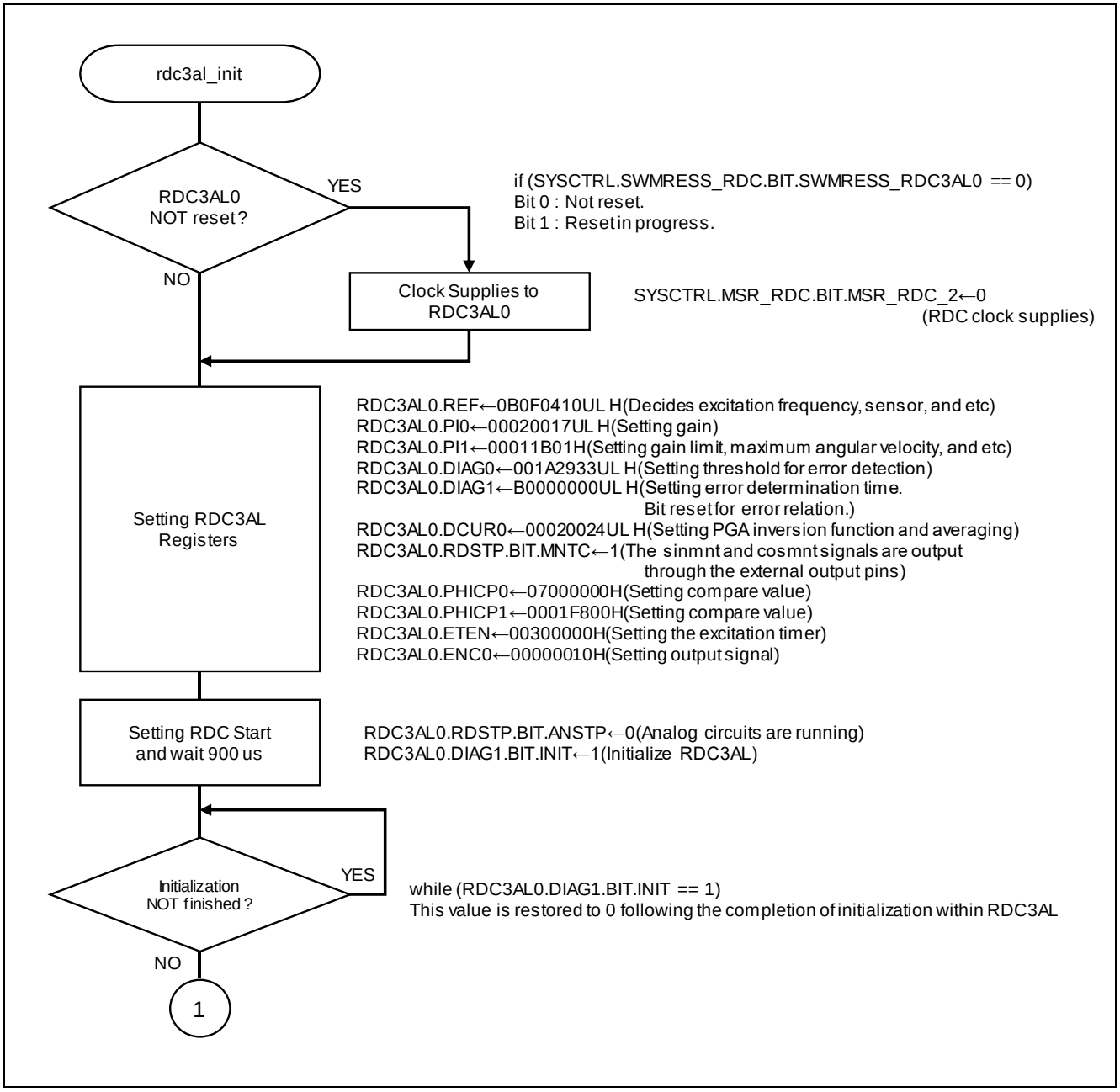


Figure 2-12 Flow of the RDC3AL initialization

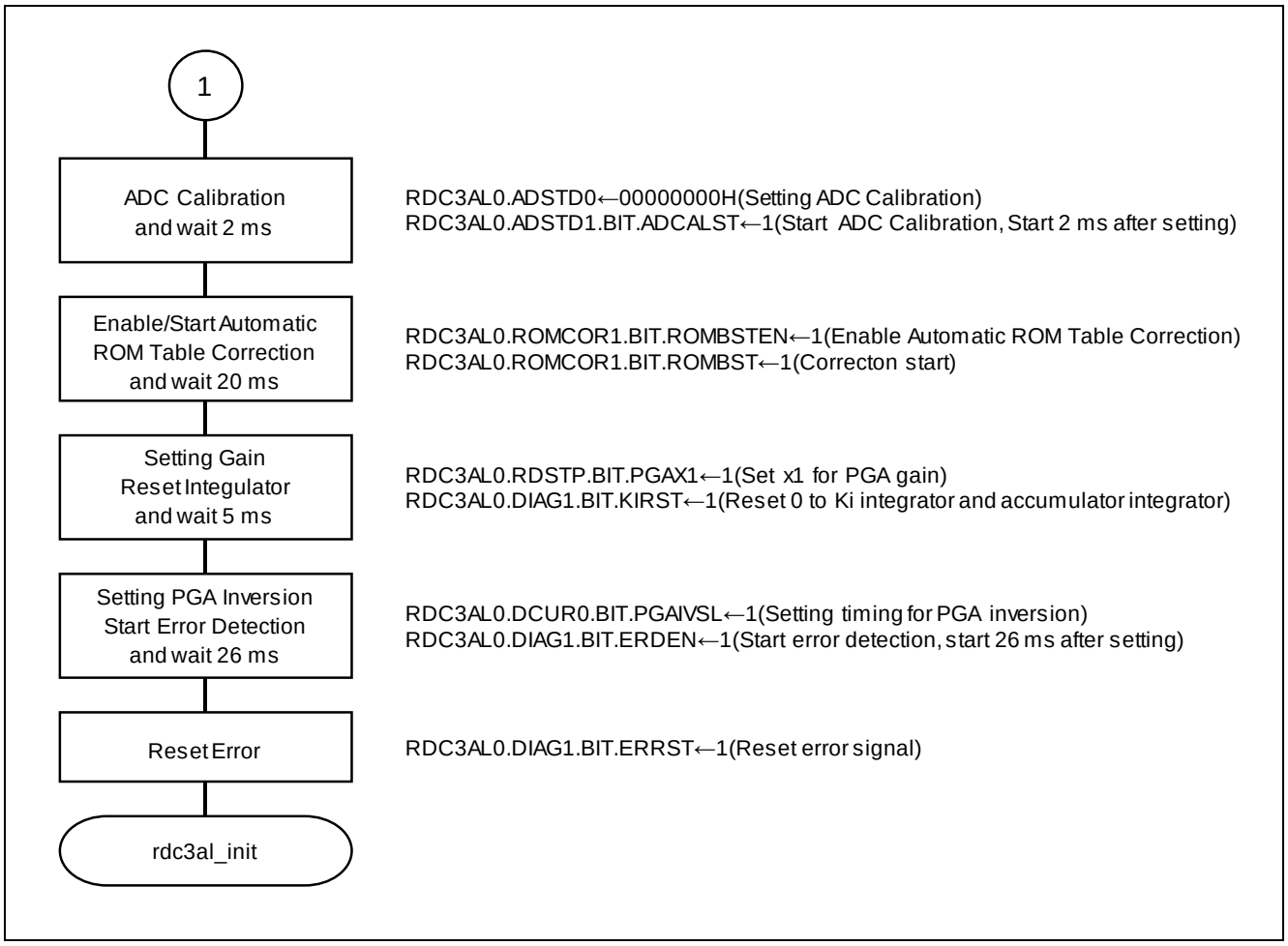


Figure 2-13 Flow of the RDC3AL starting

Figure 2-14 shows the PORT setting flow (port.c / port_init).

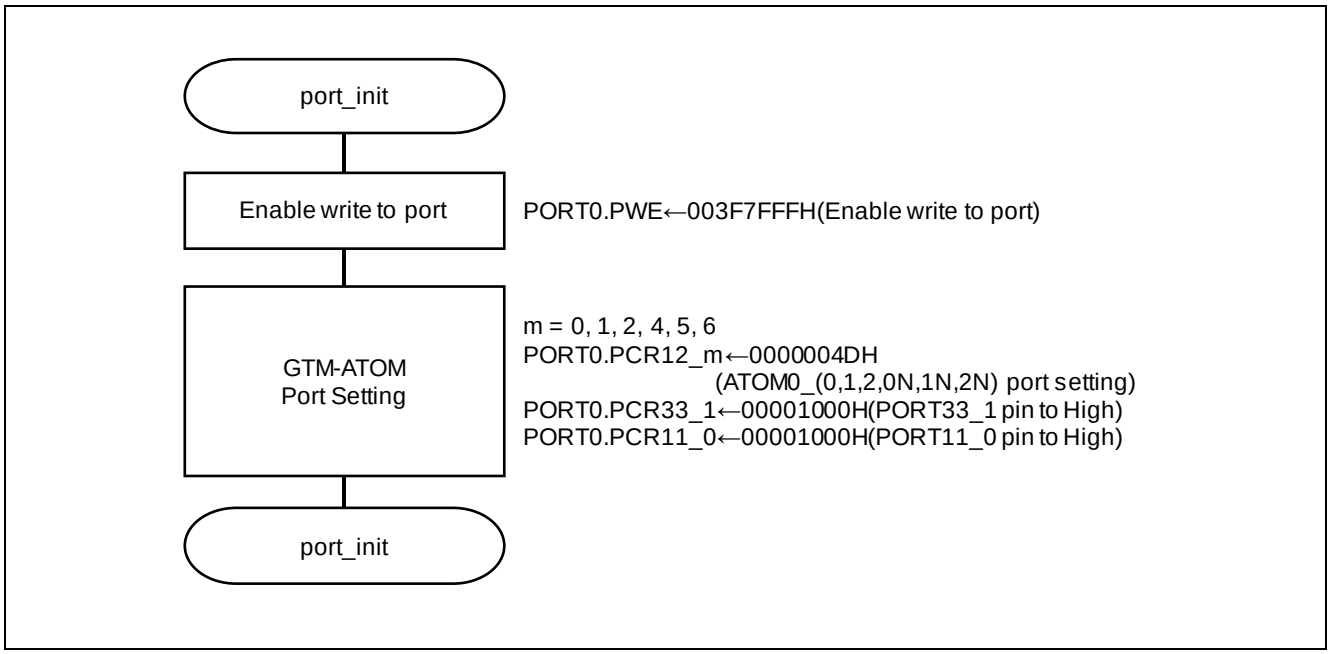


Figure 2-14 Flow of the initial PORT setting

Figure 2-15 shows the interrupt setting flow (user_int_cpu0.c / int_init).

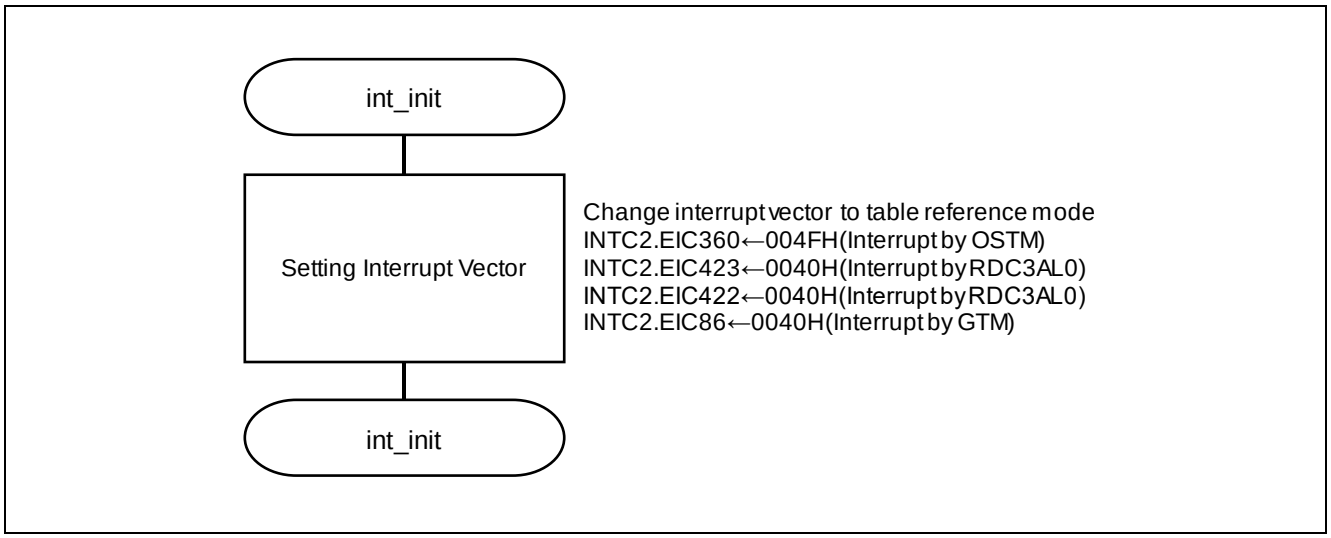


Figure 2-15 Flow of the initial interrupts setting

Figure 2-16 にタイマの有効化フロー(gtm.c / gtm_atom_enable、ostm.c / ostm_enable、gtm.c / mcs_enable)を示します。

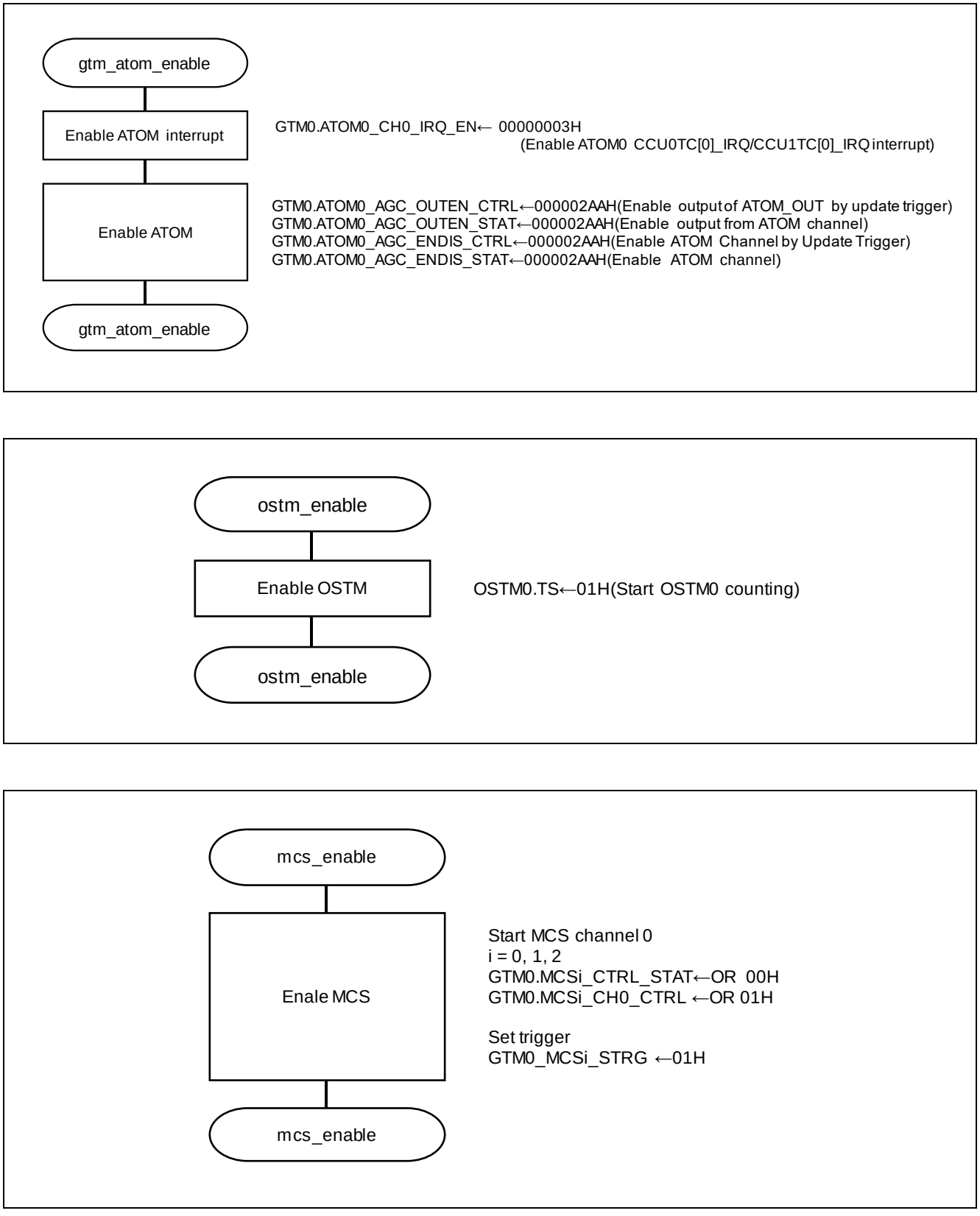


Figure 2-16 Flow of the enabling timers

2.1.3 Software description

Table 2-1 shows the register settings used to set the clock feeding each peripheral.

Table 2-2 and Table 2-3 show the PIC register settings used to trigger ADCK.

Table 2-4 shows the register settings used for ADCK.

Table 2-5 through Table 2-16show the register settings used for GTM activation and interrupts.

Table 2-17 shows the register settings used by the OS Timer (OSTM).

Table 2-18 through Table 2-19 show the register settings used to initialize and start up RDC3AL0.

Table 2-20 shows the register settings used for the input/output port pins (PORT).

Table 2-21 shows the register settings used by the interrupt controller (INTC).

Table 2-22 through Table 2-24 show the register settings used for RDC_CMP0, RDC_CMP1 and GTM0_IRQ interrupts.

Table 2-25 through Table 2-27 show the register settings used to enable ATOM, OSTM and MCS.

Table 2-1 Setting Clock(clk_init)

Resister name	Setting value	Function
Module Standby Register Key Code Protection Register (SYSCTRL.MSRKCPROT)	0xA5A5A501	Unprotect
	0xA5A5A500	Protect
Module Standby Register for OSTM module (SYSCTRL.MSR_OSTM)	MSR.OSTM_0 : 0	Clock supplies to OSTM
Module Standby Register for RDC module (SYSCTRL.MSR_RDC)	MSR_RDC_2 : 0	Clock supplies to RDC
Module Standby Register for GTM module (SYSCTRL.MSR_ GTM)	0x00000000	Clock supplies to GTM
Module Standby Register for ADCK module (SYSCTRL.MSR_ ADCK_ISO)	0x00000006	Clock supplies to ADCK
Port 33_1 Control Register (PORT0.PCR33_1)	0x00000000	Port 33 pin 1 to Low level

Table 2-2 Setting PIC(pic_init)

Resister name	Setting value	Function
A/D Converter Trigger Output Configuration Register 0 (PIC24.PIC2ADTCFG0)	0x01190061	Use GTM_ATOM[0]_OUT[0]、GTM_ATOM[0]_OUT[0]_N for A/D converter trigger
A/D Converter Trigger Output Configuration Register 1 (PIC24.PIC2ADTCFG1)	0x011A0062	Use GTM_ATOM[0]_OUT[1]、GTM_ATOM[0]_OUT[1]_N for A/D converter trigger
A/D Converter Trigger Output Configuration Register 2 (PIC24.PIC2ADTCFG2)	0x011B0063	Use GTM_ATOM[0]_OUT[2]、GTM_ATOM[0]_OUT[2]_N for A/D converter trigger
A/D Converter Trigger Output Control Register 0504 (PIC20.ADTEN504)	0x0000003F	Use GTM timer external output signal selected by PIC2ADTCFG0~2 registers for ADCK trigger
A/D Converter 0 Trigger Selection Control Register 04 (PIC20.ADCK0TSEL4)	0x00000004	Use GTM signal selected by PIC2ADTEN504 register for ADCK0SG4 trigger
A/D Converter 0 Trigger Edge Selection Control Register 0 (PIC20.ADCK0EDGSEL)	0x0000	Select SG-Diag of ADCK0 and the rising edge of scan groups 0 to 4 as the valid edge of the pulse generation circuit that generates the ADCK trigger

Table 2-3 Setting PIC (pic_mcs_ad_trigger)

Resister name	Setting value	Function
A/D Converter Trigger Output Configuration Register 0 (PIC24.PIC2ADTCFG0)	0x01590159	Use GTM_MCS[0]_IRQ[0] for A/D converter trigger
A/D Converter Trigger Output Configuration Register 1 (PIC24.PIC2ADTCFG1)	0x01610161	Use GTM_MCS[0]_IRQ[1] for A/D converter trigger
A/D Converter Trigger Output Configuration Register 2 (PIC24.PIC2ADTCFG2)	0x01690169	Use GTM_MCS[0]_IRQ[2] for A/D converter trigger
A/D Converter Trigger Output Control Register (PIC20.ADTEN504)	0x0000003F	Use GTM timer output signal selected by PIC2ADTCFG0~2 registers for ADCK trigger
A/D Converter 0 Trigger Selection Control Register 04 (PIC20.ADCK0TSEL4)	0x00000004	Use GTM signal selected by PIC2ADTEN504 register for ADCK0SG4 trigger
A/D Converter 0 Trigger Edge Selection Control Register 0 (PIC20.ADCK0EDGSEL)	0x0000	Select SG-Diag of ADCK0 and the rising edge of scan groups 0 to 4 as the valid edge of the pulse generation circuit that generates the ADCK trigger

Table 2-4 Setting ADCK

Resister name	Setting value	Function
Module Standby Register Key Code Protection Register (SYSCTRL.MSRKCPROT)	0xA5A5A501	Unprotect
	0xA5A5A500	Protect
Module Standby Register for ADCK module (SYSCTRL.MSR_ ADCK_ISO)	0x00000006	Clock supplies to ADCK
Scan Group 4 Stop Control Register (ADCK0.SGSTPCR4)	0x01	Stop A/D conversion
Virtual Channel Register 0 (ADCK0.VCR00)	0x00000800	・Hold value A/D conversion ・T&H00 value is A/D converted
Virtual Channel Register 1 (ADCK0.VCR01)	0x00000801	・Hold value A/D conversion ・T&H01 value is A/D converted
Virtual Channel Register 2 (ADCK0.VCR02)	0x00000802	・Hold value A/D conversion ・T&H02 value is A/D converted
Virtual Channel Register 3 (ADCK0.VCR03)	0x00000004	・Normal A/D conversion ・Set group number of physical channels ANn10 to ANn13
Scan Group 4 Virtual Channel Pointer Register (ADCK0.SGVCPR4)	VCSP：0x00	Starting Virtual Channel Pointer
	VCEP：0x03	End Virtual Channel Pointer
Scan Group 4 Control Register (ADCK0.SGCR4)	0x00	Scan group 4 setting ・Disable A/D conversion simultaneous start ・Multicycle scan mode ・Output disabled Scan End Interrupt
	TRGMD：1	Enable HW trigger of Scan Group 4
A/D Control Register 2 (ADCK0.ADCR2)	0x10	・Select 12-bit signed integer format for data registers. ・Addition twice for addition mode A/D conversion
A/D Control Register 1 (ADCK0.ADCR1)	0x02	Select Asynchronous Suspend for suspending method between scan groups
T&H Control Register (ADCK0.THCR)	0x00	Sampling starts automatically
T&H Enable Register (ADCK0.THER)	0x07	Enable T&H0~2
T&H Group Select Register (ADCK0.THGSR)	0x0000	T&H0~5 is selected for group A
T&H Group A Control Register (ADCK0.THACR)	0x33	・Enable Hold control ・Enable HW trigger signal by SG4
T&H Sampling Start Control Register (ADCK0.THSMPSTCR)	0x01	Start T&H sampling

Table 2-5 Setting protect

Resister name	Setting value	Function
GTM Global control register (GTM0.GTM_CTRL)	RF_PROT：0	Enable reset function (RST, FORCINT, SW, RAM)

Table 2-6 Enable Interrupts

Resister name	Setting value	Function
GTM Interrupt Selection Control Register 000 (IRQ_SEL000)	0x00FF0000	Output interrupt requests from MCS0_IRQ[3:0] and ATOM0_IRQ[3:0] to INTC
GTM Interrupt Selection Control Register 100 (IRQ_SEL100)	0x00F00000	Output interrupt request from MCS1_IRQ[3:0] to INTC
GTM Interrupt Selection Control Register 200 (IRQ_SEL200)	0x00F00000	Output interrupt request from MCS2_IRQ[3:0] to INTC
GTM Cluster Clock Configuration (GTM_CLS_CLK_CFG)	0x000000AA	Enable clusters 0-3 with clock divider 2

Table 2-7 Disable ATOM

Resister name	Setting value	Function
ATOM AGC Output Enable Control Register (ATOM0_AGC_OUTEN_CTRL)	0x00000155	Disable ATOM_OUT output by update trigger
ATOM AGC Output Enable Status Register (ATOM0_AGC_OUTEN_STAT)	0x00000155	Disable output from ATOM channel [4:0]
ATOM AGC Enable/Disable Control Register (ATOM0_AGC_ENDIS_CTRL)	0x00000155	Disable ATOM channel by update trigger
ATOM AGC Enable/Disable Status Register (ATOM0_AGC_ENDIS_STAT)	0x00000155	Disable ATOM channel [4:0]

Table 2-8 Setting CMU

Resister name	Setting value	Function
CMU Clock Enable Register (CMU_CLK_EN)	OR 0x0000002A	Enable clock source
CMU Global Clock Control Numerator Register (CMU_GCLK_NUM)	0x00000001	Set 1 to numerator for global clock divider
CMU Global Clock Control Denominator Register (CMU_GCLK_DEN)	0x00000001	Set 1 to denominator for global clock divider

Table 2-9 Setting TBU

Resister name	Setting value	Function
TBU Channel 0 Control Register (TBU_CH0_CTRL)	0x00000000	Select counter bits resolution and clock source (TBU_CMU_CLK0)
TBU Channel 1 Control Register (TBU_CH1_CTRL)	0x00000000	Select channel mode and clock source (TBU_CMU_CLK0)
TBU Channel 2 Control Register (TBU_CH2_CTRL)	0x00000000	Select channel mode and clock source (TBU_CMU_CLK0)
TBU Channel 3 Control Register (TBU_CH3_CTRL)	0x00000000	Select channel mode Use TBU_CH1 for modulo counter
TBU Global Channel Enable Register (TBU_CHEN)	0x000000AA	Enable channel 0~3

Table 2-10 Setting ATOM interrupt

Resister name	Setting value	Function
ATOM0 Channel x Interrupt Enable Register (ATOM0_CHx_IRQ_EN)	0x00000000 (x = 0 ~ 3)	Disable interrupts for ATOM0 channels 0-3
ATOM0 Channel x Interrupt Notification Register (ATOM0_CHx_IRQ_NOTIFY)	0x00000003 (x = 0 ~ 3)	Clear interrupt flag

Table 2-11 Setting ATOM

Resister name	Setting value	Function
ATOM0 Channel [x] Control Register (ATOM0_CHx_CTRL)	0x01040002 (x = 0 ~ 2)	・ATOM Signal Output Mode PWM (SOMP) ・Output TRIG_CCU0 as TRIG_OUT[0:0]

Table 2-12 Setting DTM

Resister name	Setting value	Function
DTM4 Global Configuration and Control Register (CDTM0_DTM4_CTRL)	0x00000001	Set clock source
DTM4 Channel Control Register 1 (CDTM0_DTM4_CH_CTRL1)	0x00000000	Setting about dead time
DTM4 Channel Control Register 2 (CDTM0_DTM4_CH_CTRL2)	0x00888888	Allow dead-time pass for channels 0-2
DTM4 Channel Control Register 3 (CDTM0_DTM4_CH_CTRL3)	0x00000000	Setting about Combinational input
DTM4 Channel [x] Dead Time Reload Values Register (CDTM0_DTM4_CHx_DTV)	DEAD_TIME_COUNT OR (DEAD_TIME_COUNT << 16) (13107400)、(x = 0 ~ 2)	Reload value setting for rising and falling edges dead time

Table 2-13 Setting ATOM update

Resister name	Setting value	Function
ATOM0 AGC Global Control Register (ATOM0_AGC_GLB_CTRL)	0x002A0000	Request trigger for register update
ATOM0 AGC Force Update Control Register (ATOM0_AGC_FUPD_CTRL)	0x002A002A	Forced update enable for channels 0-2, counter register reset on update
ATOM0 AGC Internal Trigger Control Register (ATOM0_AGC_INT_TRIG)	0x0000002A	Use internal trigger from channel as trigger source for ATOM_TRIGOUT

Table 2-14 Setting PWM

Resister name	Setting value	Function
ATOM0 Channel x CCU0 Compare Shadow Register (ATOM0_CHx_SR0)	CARR_COUNT / 2 (x = 0 ~ 2)	Shadow registers for updating compare registers
ATOM0 Channel x CCU1 Compare Shadow Register (ATOM0_CHx_SR1)	500 (x = 0 ~ 2)	Shadow registers for updating compare registers
ATOM0 Channel x CCU0 Compare Register (ATOM0_CHx_CM0)	CARR_COUNT / 2 (x = 0 ~ 2)	Register to store value for comparison
ATOM0 Channel x CCU1 Compare Register (ATOM0_CHx_CM1)	1 (x = 0 ~ 2)	Register to store value for comparison
ATOM0 Channel x CCU0 Counter Register (ATOM0_CHx_CN1)	0 (x = 0 ~ 2)	Counter register

Table 2-15 Setting ADC

Resister name	Setting value	Function
GTM ADCI Storage Data Selection Register 1 (GTM0_1.ADCI_STRSEL1)	0x00000000	Select data to store in ADC_CH[y] _DATA
GTM ADCI Storage Data Selection Register (GTM0_1.ADCI_STRSEL)	RDC3A_0_PHI：1	Store encoder counter value RDC3A_0_PHI in ADC_CH22_DATA register
GTM ADCI RDC3AL/AS Selection Register (GTM0_1.ADCI_RDCSEL)	0	Store the RDC3AL value in the bit selected by the GTM_ADCI_STRSEL register

Table 2-16 Setting MCS

Resister name	Setting value	Function
GTM MCSi Channel 0 IRQ Mode Configuration Register (GTM0.MCSi_CH0_IRQ_MODE)	0x00000000 (i = 0、1、2)	MCSi Set channel 0 interrupt to level mode
GTM MCSi Channel 0 Interrupt Enable Register (GTM0.MCSi_CH0_IRQ_EN)	0x1	Enable MCSi channel 0 MCS_IRQ interrupt

Table 2-17 Setting OSTM

Resister name	Setting value	Function
OSTM0 Control Register (OSTM0.CTL)	0x02	Running by Free-run compare mode

Table 2-18 Initial RDC3AL setting

Resister name	Setting value	Function
Module Standby Register for RDC3 (SYSCTRL.MSR_RDC)	MSR_RDC_2 : 0	Clock supplies to RDC3AL0.
Excitation Setting Register (RDC3AL0.REF)	0x0B0F0410	Decides excitation frequency, sensor, and etc.
Control Gain Select Register 0 (RDC3AL0.PI0)	0x00020017	Setting gain.
Control Gain Select Register 1 (RDC3AL0.PI1)	0x00011B01	Setting gain limit, maximum angular velocity, and etc.
Error Detection Register 0 (RDC3AL0.DIAG0)	0x001A2933	Setting threshold for error detection.
Error Detection Register 1 (RDC3AL0.DIAG1)	0xB0000000	Setting error determination time. Bit reset for error relation.
Digital Operation Register 0 (RDC3AL0.DCUR0)	0x00020024	Setting PGA inversion function and averaging.
RDC Stop Register (RDC3AL0.RDSTP)	MNTC : 1	The sinmnt and cosmnt signals are output through the external output pins.
PHI Compare Setting Register 0 (RDC3AL0.PHICP0)	0x07000000	Setting compare value.
PHI Compare Setting Register 1 (RDC3AL0.PHICP1)	0x00000000	Setting compare value.
ET Control Register (RDC3AL0.ETEN)	0x03000000	Setting the excitation timer
Encoder Register 0 (RDC3AL0.ENC0)	0x00000010	Setting output signal. Enable angle compare match interrupt

Table 2-19 Start RDC3AL setting

Resister name	Setting value	Function
RDC Stop Register (RDC3AL0.RDSTP)	ANSTP：0	Analog circuits are running.
	PGAX1：1	Set x1 for PGA gain.
Error Detection Register 1 (RDC3AL0.DIAG1)	INIT：1	Initialize RDC3AL (This value is restored to 0 following the completion of initialization within RDC3AL.)
	KIRST：1	Reset 0 to Ki integrator and accumulator integrator
	ERDEN：1	Start error detection (Start 26 ms after setting)
	ERRST：1	Reset error signal.
12-Bit SAR-ADC Digital Circuit Block Setting Register 0 (RDC3AL0.ADSTD0)	0x00000000	Setting ADC calibration.
12-Bit SAR-ADC Digital Circuit Block Setting Register 1 (RDC3AL0.ADSTD1)	ADCALST：1	Start ADC calibration. (Start 2 ms after setting)
Automatic ROM Table Correction Register 1 (RDC3AL0.ROMCOR1)	ROMBSTEN：1	Enable Automatic ROM Table Correction
	ROMBST：1	Start Automatic ROM Table Correction
Digital Operation Register 0 (RDC3AL0.DCUR0.BIT)	PGAIVSL：1	Setting timing for PGA inversion

Table 2-20 Setting PORT

Resister name	Setting value	Function
Port Write Enable register (PORT0.PWE)	0x003F7FFF	Enable write to port.
Port 12 Mode Control Register (PORT0.PCR12_m) (m = 0、1、2、4、5、6)	0x0000004D	Enable port output by ATOM0_0, 1, 2, 0N, 1N, 2N
Port 33_1 Mode Control Register (PORT0.PCR33_1)	0x00001000	Port 33 pin 1 to High
Port 11_0 Mode Control Register (PORT0.PCR11_0)	0x00001000	Port 11 pin 0 to High

Table 2-21 Setting INTC

Resister name	Setting value	Function
EI Level Interrupt Control Register 2 (INTC2)	EIC360：0x004F	Interrupt vector to table reference mode OSTM0 Interrupt (priority 15: lowest)
	EIC423：0x0040	RDC3AL0 compare interrupt 0 (priority 0: highest)
	EIC422：0x0040	RDC3AL0 compare interrupt 1 (priority 0: highest)
	EIC86：0x0040	GTM0_ATOM_CH0 Interrupt (priority 0: highest)

Table 2-22 RDC_CMP0 Interrupt

Resister name	Setting value	Function
Port 11_0 Control Register (PORT0.PCR11_0)	0x00001000	Port 11 pin 0 to High
PHI Compare Setting Register 0 (RDC3AL0.PHICP0)	0x07000000	Setting compare value

Table 2-23 RDC_CMP1 Interrupt

Resister name	Setting value	Function
Port 11_0 Control Register (PORT0.PCR11_0)	0x00000000	Port 11 pin 0 to Low
PHI Compare Setting Register 0 (RDC3AL0.PHICP0)	0x07000000	Setting compare value

Table 2-24 GTM0_IRQ Interrupt

Resister name	Setting value	Function
MCSi Channel 0 Interrupt Notification Register (GTM0.MCSi_CH0_IRQ_NOTIFY)	0x00000001 (i = 0、1、2)	Interrupt request by MCS channel 0. Clear after writing.
ATOM0 Channel 0 Interrupt Notification Register (GTM0.ATOM0_CHx_IRQ_NOTIFY)	0x00000003 (x = 0、1、2)	CCU0, CCU1 channel 0 trigger condition interrupt occurs on ATOM channel 0. Clear after writing.

Table 2-25 Enable ATOM(gtm_atom_enable)

Resister name	Setting value	Function
ATOM0 Channel 0 Interrupt Enable Register (ATOM0_CH0_IRQ_EN)	0x00000003	Enable interrupts for ATOM0 channels 0 CCU0TC_IRQ
ATOM AGC Output Enable Control Register (ATOM0_AGC_OUTEN_CTRL)	0x000002AA	Enable channel output on an update trigger
ATOM AGC Output Enable Status Register (ATOM0_AGC_OUTEN_STAT)	0x000002AA	Enable ATOM_OUT output
ATOM Enable/Disable Control Register (ATOM0_AGC_ENDIS_CTRL)	0x000002AA	Enable ATOM channel on an update trigger
ATOM Enable/Disable Status Register (ATOM0_AGC_ENDIS_CTRL)	0x000002AA	Enable ATOM channels

Table 2-26 Enable OSTM (ostm_enable)

Resister name	Setting value	Function
OSTM0 Count Start Trigger Register (OSTM0.TS)	0x01	Start counting and set OSTM0TE.OSTM0TE (count enable state register) to 1

Table 2-27 Enable MCS (mcs_enable)

Resister name	Setting value	Function
MCSi Control and Status Register (GTM0.MCSi_CTRL_STAT)	OR 0x00 (i = 0, 1, 2)	Retain MCS scheduling mode
MCSi Channel 0 Control Register (GTM0.MCSi_CH0_CTRL)	OR 0x1 (I = 0, 1, 2)	MCSi channel 0 activation request
MCSi Set Trigger Control Register (GTM0.MCSi_STRG)	0x01	Set trigger bit

3. Appendix

This section describes how to start MCS based on the edge input to TIM.

This section describes the settings assuming that MCS is started from TIM using sample software.

3.1 Activation using the count start trigger function

3.1.1 Operation overview

When TIM 24-bit counter (TIM0_CH0_CNT) exceeds 0xFFFFFF, an overflow interrupt CNTOFL_IRQ is generated.

Operates the TIM counter (TIM0_CH0_CNT) using the input signal as a start trigger. This application uses the compare interrupt signal output from RDC3AL as the input signal.

Start counting TIM0_CH0_CNT with the falling edge of the signal as a trigger.

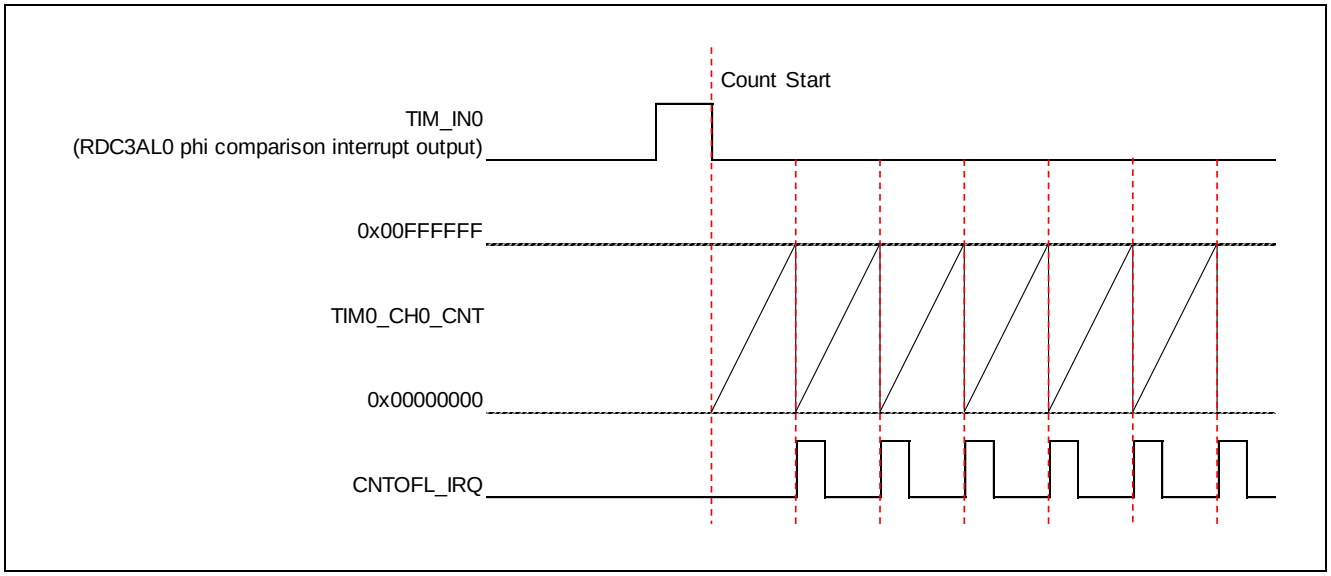


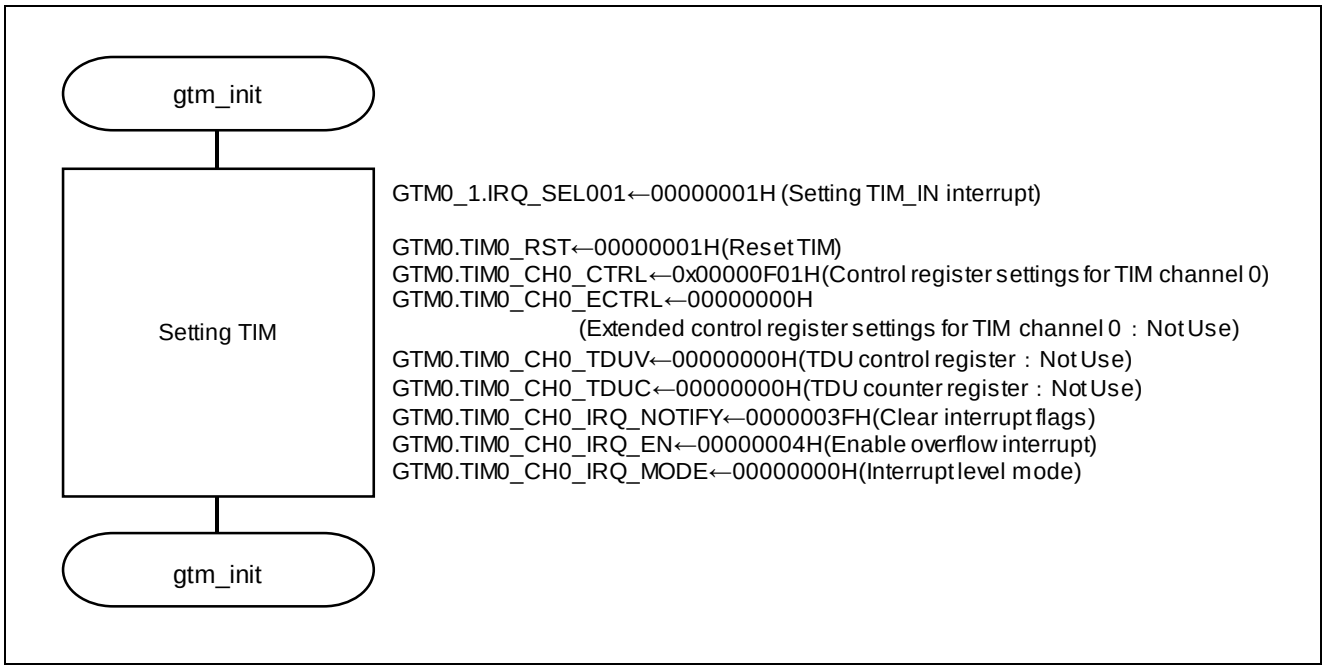
Figure 3-1 Operation overview

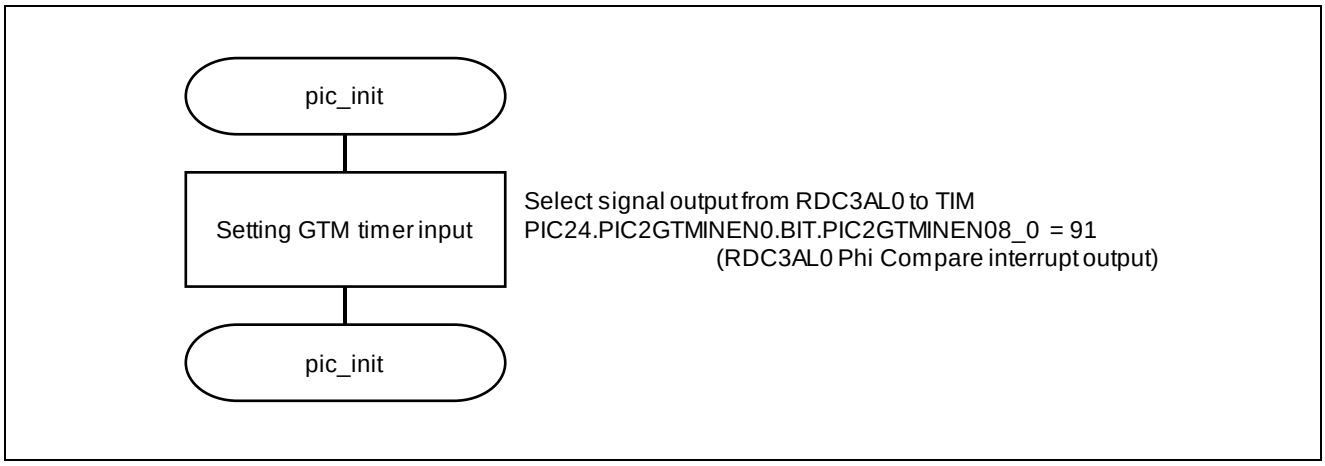
3.1.2 Operation flowchart

Figure 3-2 shows the setting flow for GTM, etc. They are GTM settings, PIC settings, INTC settings, and compare interrupt settings, respectively, and the following settings are added to each function.

Figure 3-3 shows the setting flow of interrupt processing. This will be added directly to user_int_cpu0.c.

Figure 3-4 shows the interrupt vector table setting flow. This takes the form of editing vecttbl0.asm.





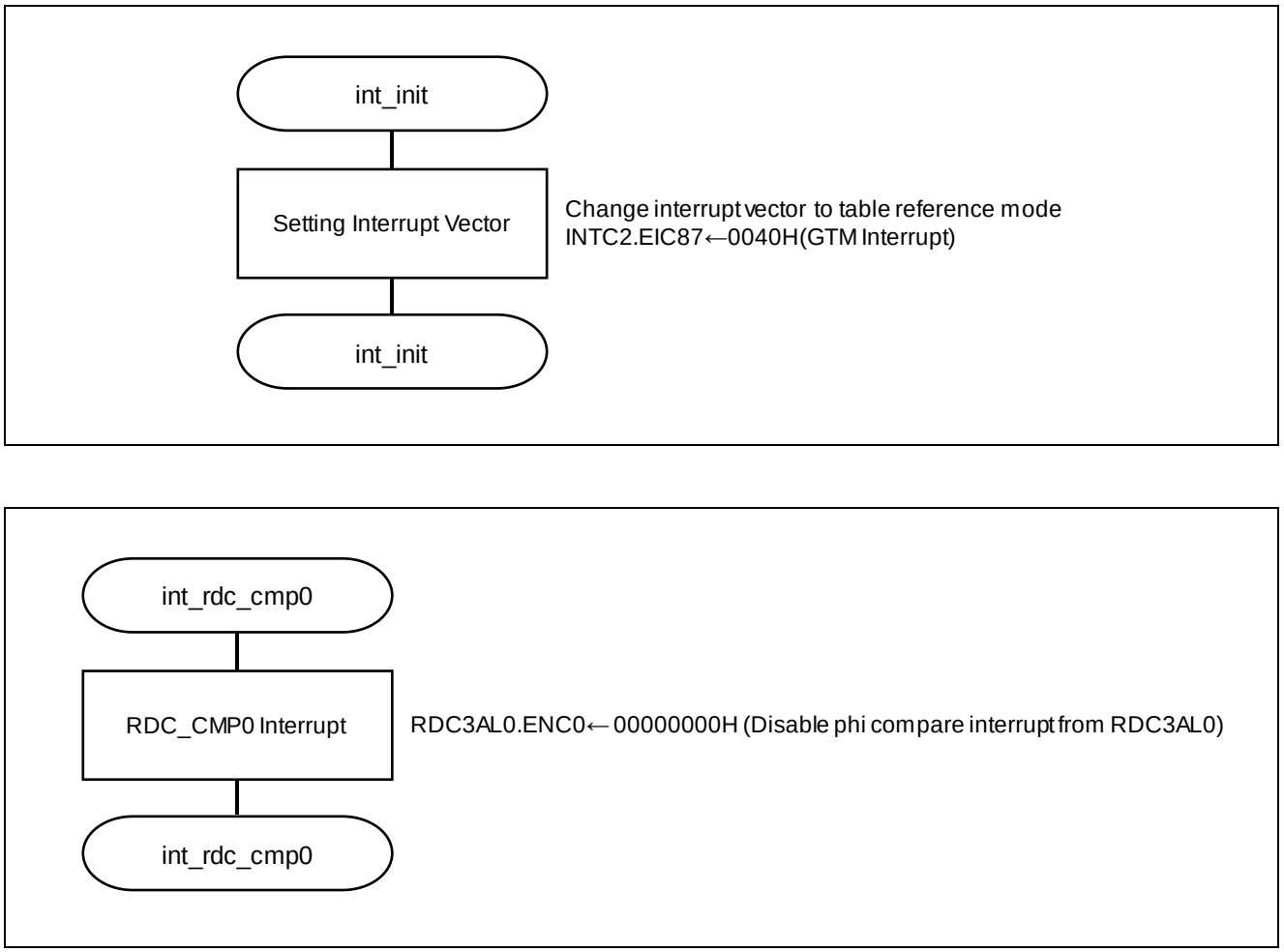


Figure 3-2 Setting registers

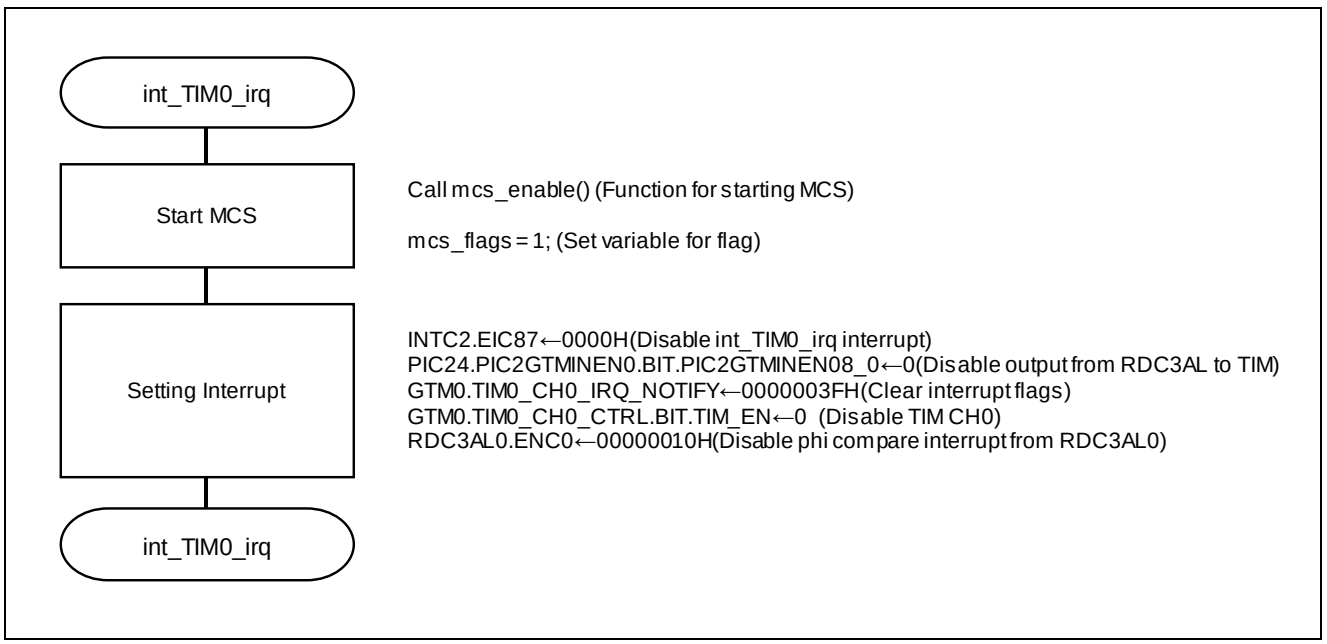


Figure 3-3 Setting overflow interrupt

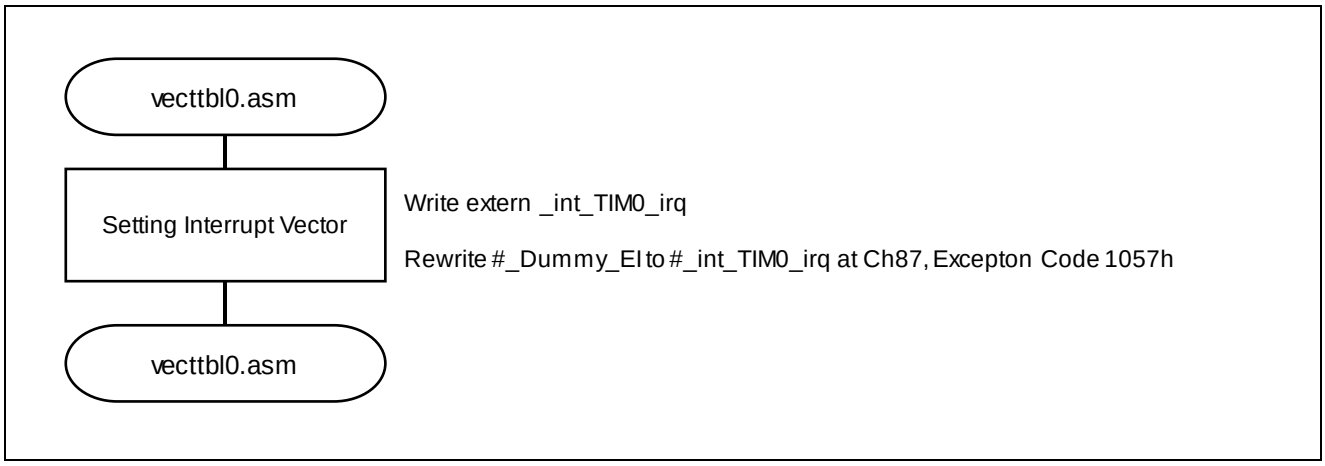


Figure 3-4 Edit vector table

3.1.3 Software description

Table 3-1 through Table 3-4 show the register settings used for the GTM, PIC, INTC and RDC3AL0 compare interrupts.

Table 3-5 shows the register settings used by the overflow interrupt int_TIM0_irq.

Table 3-1 Setting TIM(gtm_init)

Register name	Setting value	Function
GTM Interrupt Selection Control Register 001 (IRQ_SEL001)	0x00000001	Output TIM0 (Ch0) interrupt request to INTC
TIM0 Global Software Reset Register (TIM0_RST)	0x00000001	Reset TIM (Ch0)
TIM0 Channel 0 Control Register (TIM0_CH0_CTRL)	0x00000F01	・Measurement starts from the falling edge ・Continuous operation mode ・PWM measurement mode ・Enable channel
TIM0 Channel 0 Extended Control Register (TIM0_CH0_ECTRL)	0x00000000	Since the extended function is not used, use the reset value of the microcomputer
TIM0 Channel 0 TDU Control Register (TIM0_CH0_TDUV)	0x00000000	Since the TDU is not used, use the reset value of the microcomputer
TIM0 Channel 0 TDU Counter Register (TIM0_CH0_TDUC)	0x00000000	Since the TDU is not used, use the reset value of the microcomputer
TIM0 Channel 0 Interrupt Notification Register (TIM0_CH0_IRQ_NOTIFY)	0x0000003F	Clear interrupt flags
TIM0 Channel 0 Interrupt Enable Register (TIM0_CH0_IRQ_EN)	0x00000004	Enable overflow interrupt
TIM0 Channel 0 Interrupt Mode Configuration Register (TIM0_CH0_IRQ_MODE)	0x00000000	Level interrupt

Table 3-2 Setting PIC(pic_init)

Register name	Setting value	Function
GTM Timer Input Module (TIM) Source Select Register 0 (PIC24.PIC2GTMINEN0)	PIC2GTMINEN0[8:0] ：91	Set RDC3AL0 compare interrupt output to GTM_TIM0_IN0

Table 3-3 Setting interrupt vector(int_init)

Register name	Setting value	Function
EI Level Interrupt Control Register 2 (INTC2)	EIC87：0x0040	Set interrupt vector to table reference mode int_TIM0_irq interrupt(priority 0: highest)

Table 3-4 RDC_CMP0 interrupt(int_rdc_cmp0)

Register name	Setting value	Function
RDC3AL0 Encoder Register (RDC3AL0.ENC0)	0x00000000	Disable phi compare interrupt from RDC3AL0

Table 3-5 Setting interrupt(int_TIM0_irq)

Register name	Setting value	Function
EI Level Interrupt Control Register 2 (INTC2)	EIC87：0x0000	Disable int_TIM0_irq interrupt
GTM Timer Input Module (TIM) Source Select Register 0 (PIC24.PIC2GTMINEN0)	PIC2GTMINEN08_0：0	Disable output from RDC3AL0 to TIM
TIM0 Channel 0 Interrupt Notification Register (TIM0_CH0_IRQ_NOTIFY)	0x0000003F	Clear interrupt flags
TIM0 Channel 0 Control Register (TIM0_CH0_CTRL)	TIM_EN：0	Disable TIM_CH0
RDC3AL0 Encoder Register 0 (RDC3AL0.ENC0)	0x00000010	Enable phi compare interrupt from RDC3AL0

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2023/9/29		First-edition issued

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   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
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(Rev.5.0-1 October 2020)

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