RH850/U2B6-FCC

Angle synchronized PWM output in GTM

Summary

This application note describes methods of the angle synchronized PWM output by GTM of the RH850/U2B6.

Although the examples of tasks and applications examples in this application note have been confirmed to work, please be sure to check the operating environment before using the product.

Operation confirmation device

RH850/U2B6-FCC (R7F702Z22EDBB).

Table of contents

1. Introduction

This application note describes methods of the angle synchronized PWM output by GTM of the RH850/U2B6-FCC.

The functions described in this application note are shown below.

1.1 The function to be used

The RH850/U2B6 hardware functions used in this application note are shown below.

Also, in this application note, each hardware function is controlled from CPU0.

Hardware function name	Symbol
Clock Management Unit	CMU
Cluster Configuration Module	CCU
Time Base Unit	TBU
Timer Input Module	TIM
ARU-connected Timer Output Module	ATOM
Dead Time Module	DTM
Interrupt Controller	INTC
Peripheral Interconnect	PIC
I/O Port	PORT

2. Motor Control Using GTM

This chapter describes how to implement the angle synchronized PWM output using GTM instead of EMU3S.

2.1 Angle Count Using Encoder Signal (AB Signal) and Angle Period PWM Output

This application uses the digital converter RDC3AL and each sub-module CCM, CMU, TIM, TBU, and ATOM installed in the timer module GTM, and selects the input signal to TIM with PIC.

The clock created by TIM is counted by TBU, the counted value is passed to ATOM from TBU in the form of a timestamp, and ATOM compares the timestamp and the compare value to control the output.

2.1.1 Operation overview

In this application, the angle information of the resolver is converted to PWM in the following flow.

- Acquire angle information from resolver and encode to AB signal with RDC3AL
- Receive AB signal in TIM subunit of GTM and count as clock in TBU after filtering
- Input timestamp from TBU to ATOM and generate PWM with ATOM based on timestamp
- Output the generated PWM with dead time applied by DTM

Figure 2-1 shows the flow from resolver to PWM output via RDC3AL and GTM in this application.

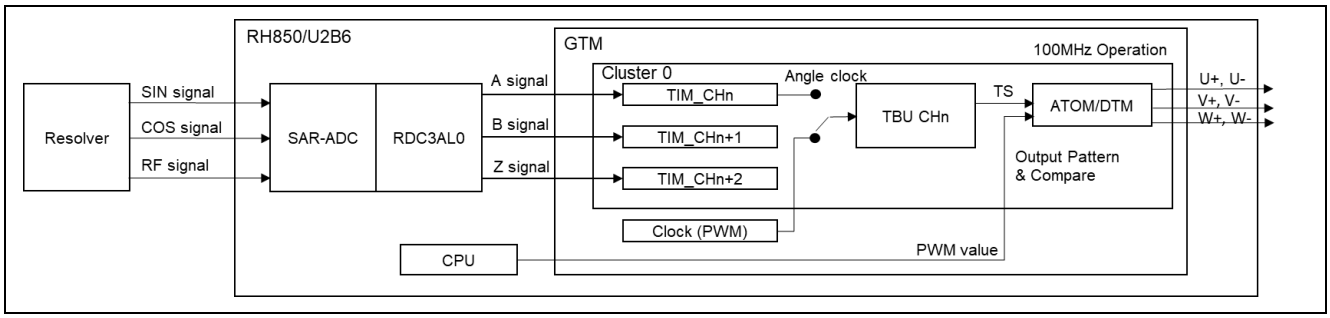


Figure 2-1 Block diagram overview

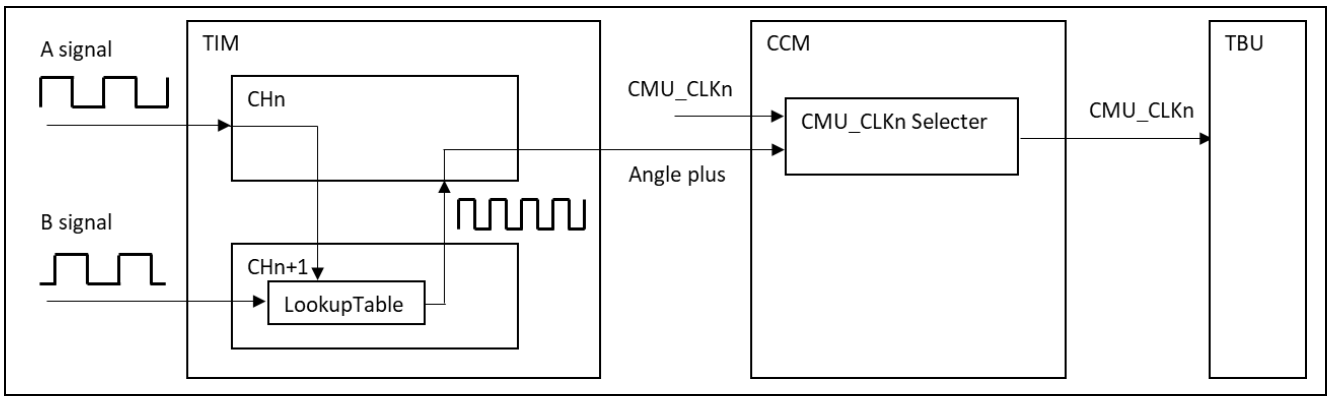


Figure 2-2 Clock flow within GTM

2.1.2 Operation flowchart

Figure 2-3 shows the flow of initialization and startup processing executed when this software is started.

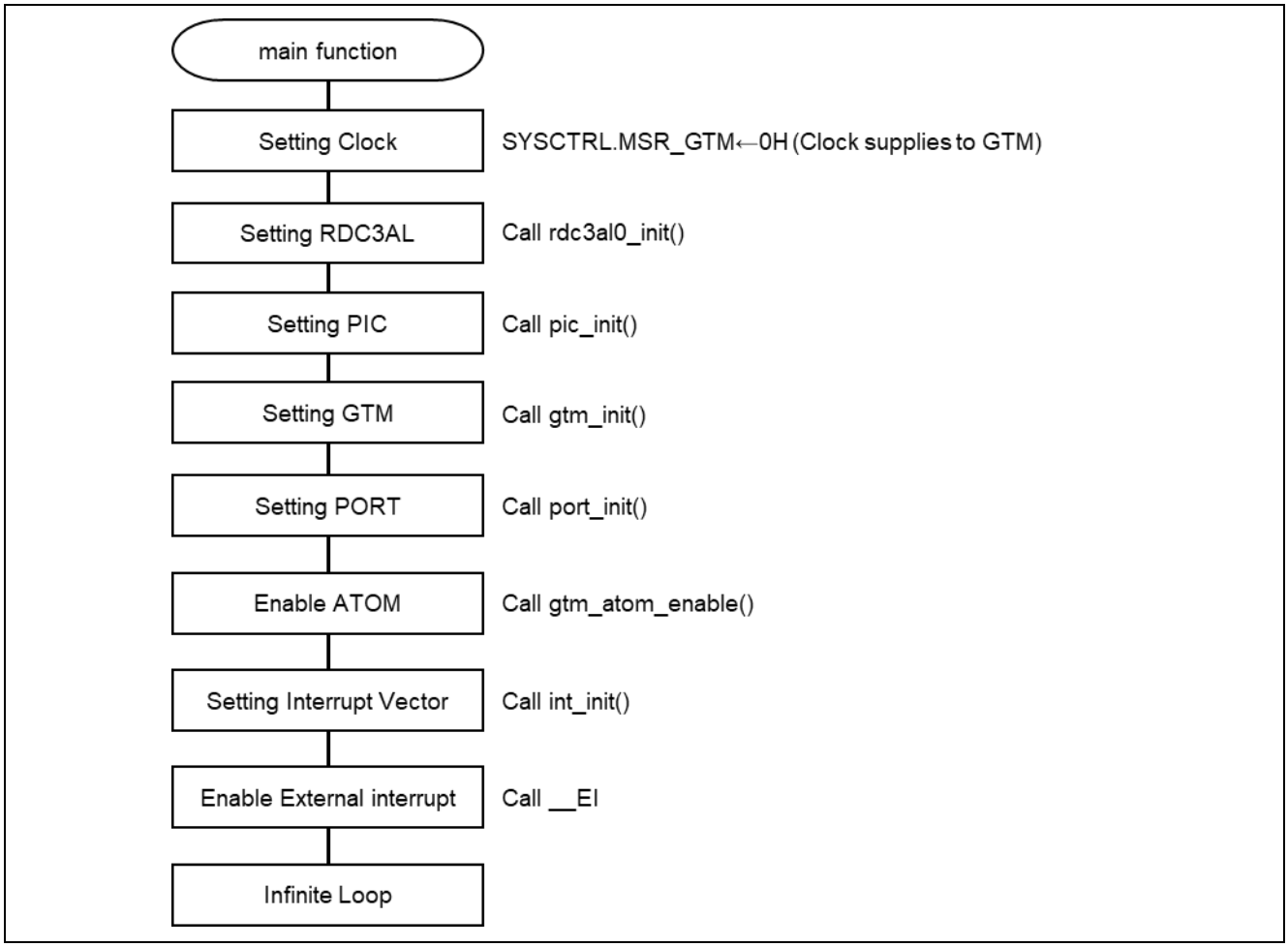
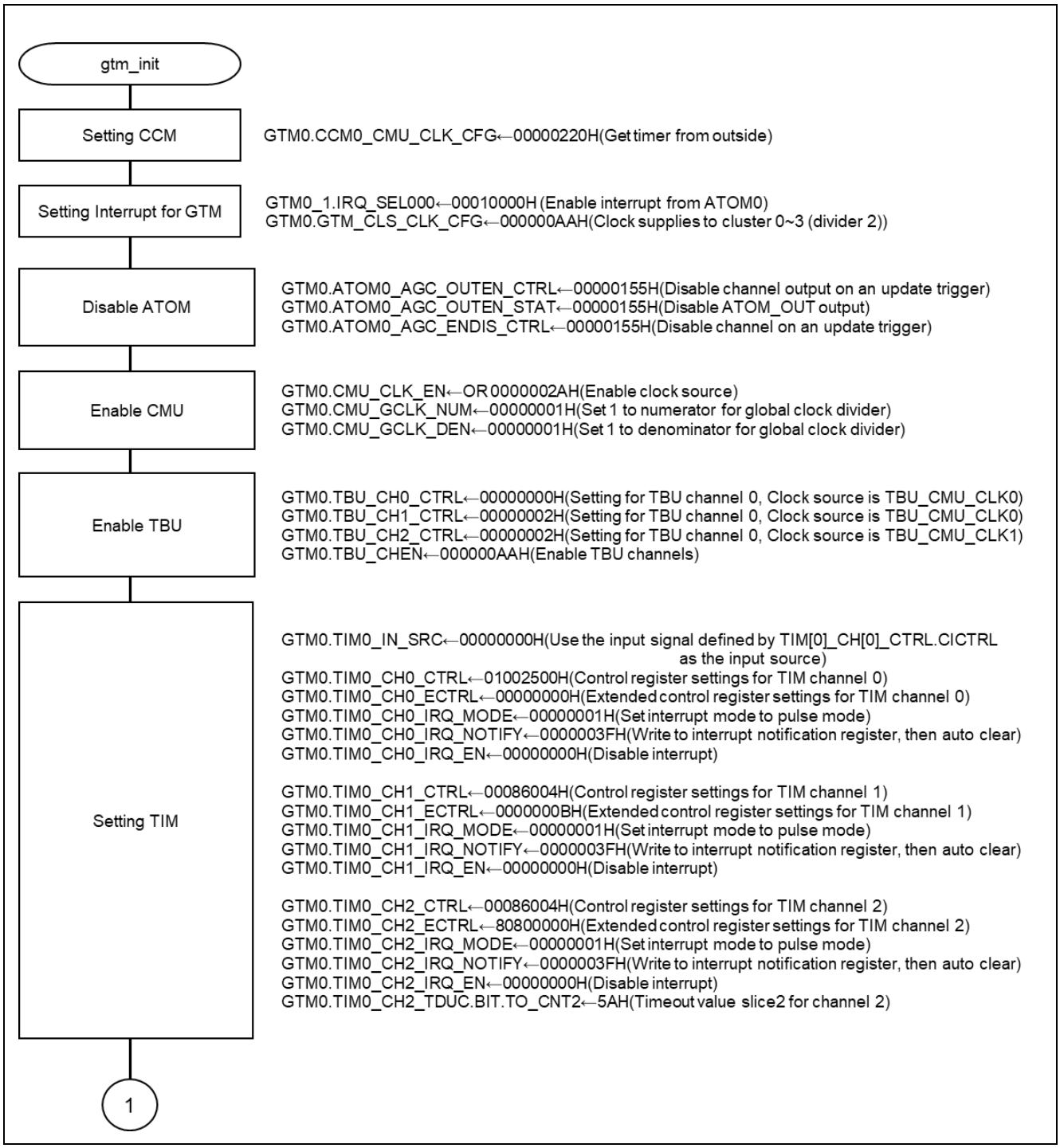


Figure 2-3 Initializing process of software for Angle Count Using Encoder Signal.

Figure 2-4 shows the GTM initialization flow.



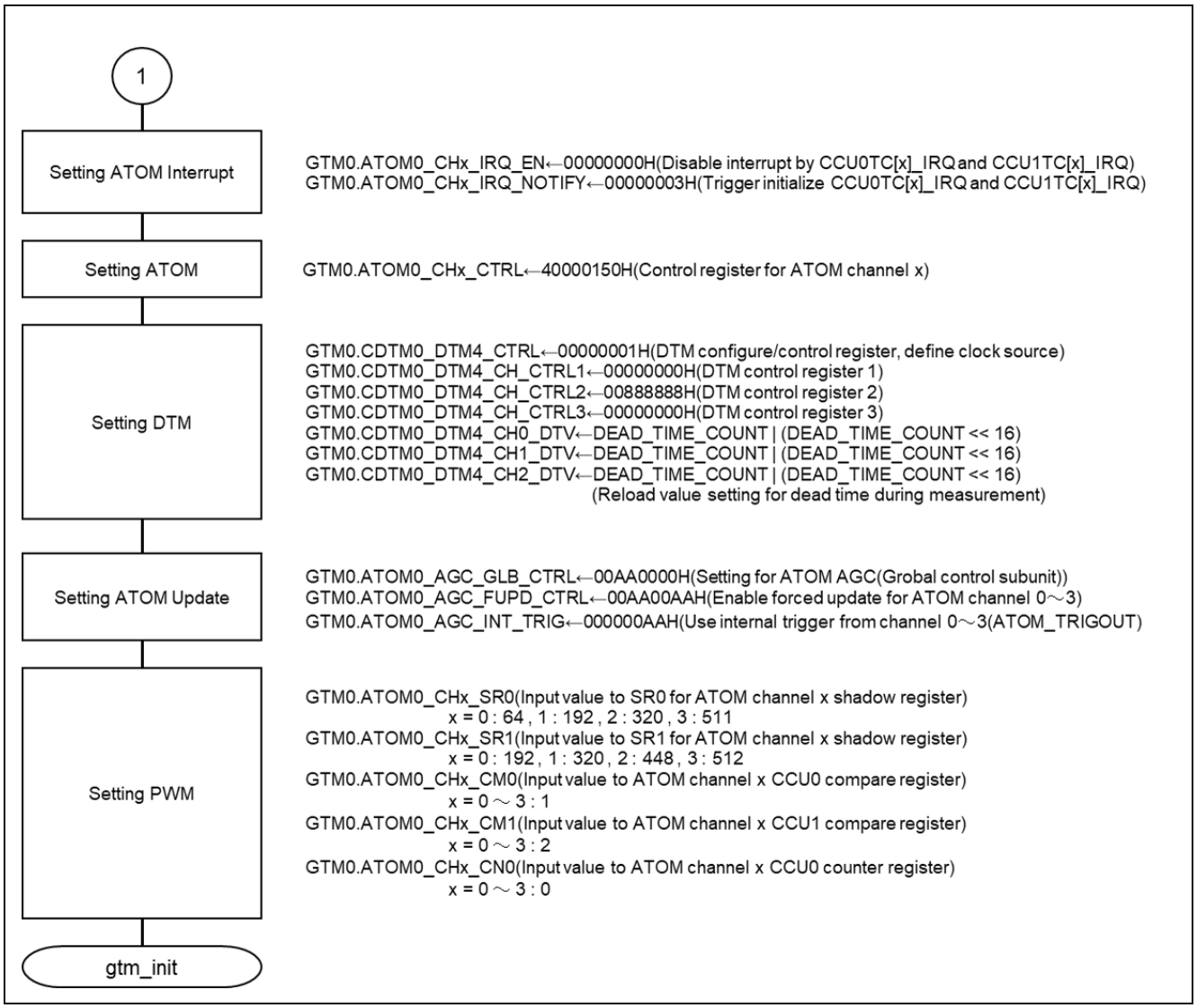


Figure 2-4 Flow of the GTM initial setting (x = 0 ~ 3)

Figure 2-5 shows the ATOM startup setting flow

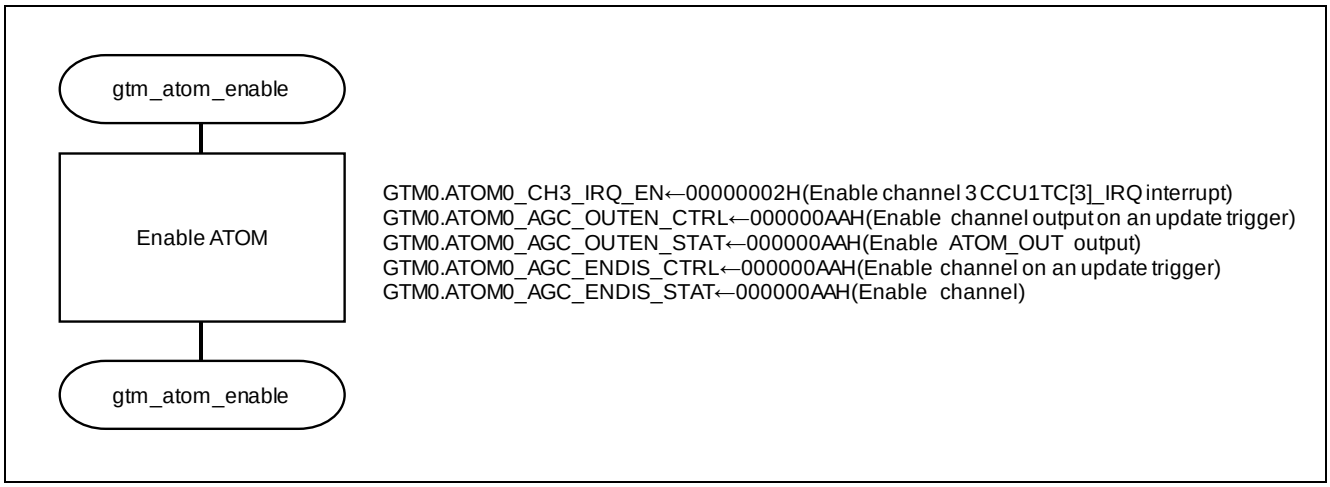


Figure 2-5 Flow of the ATOM startup setting

Figure 2-6 shows the flow when an ATOM0 interrupt occurs.

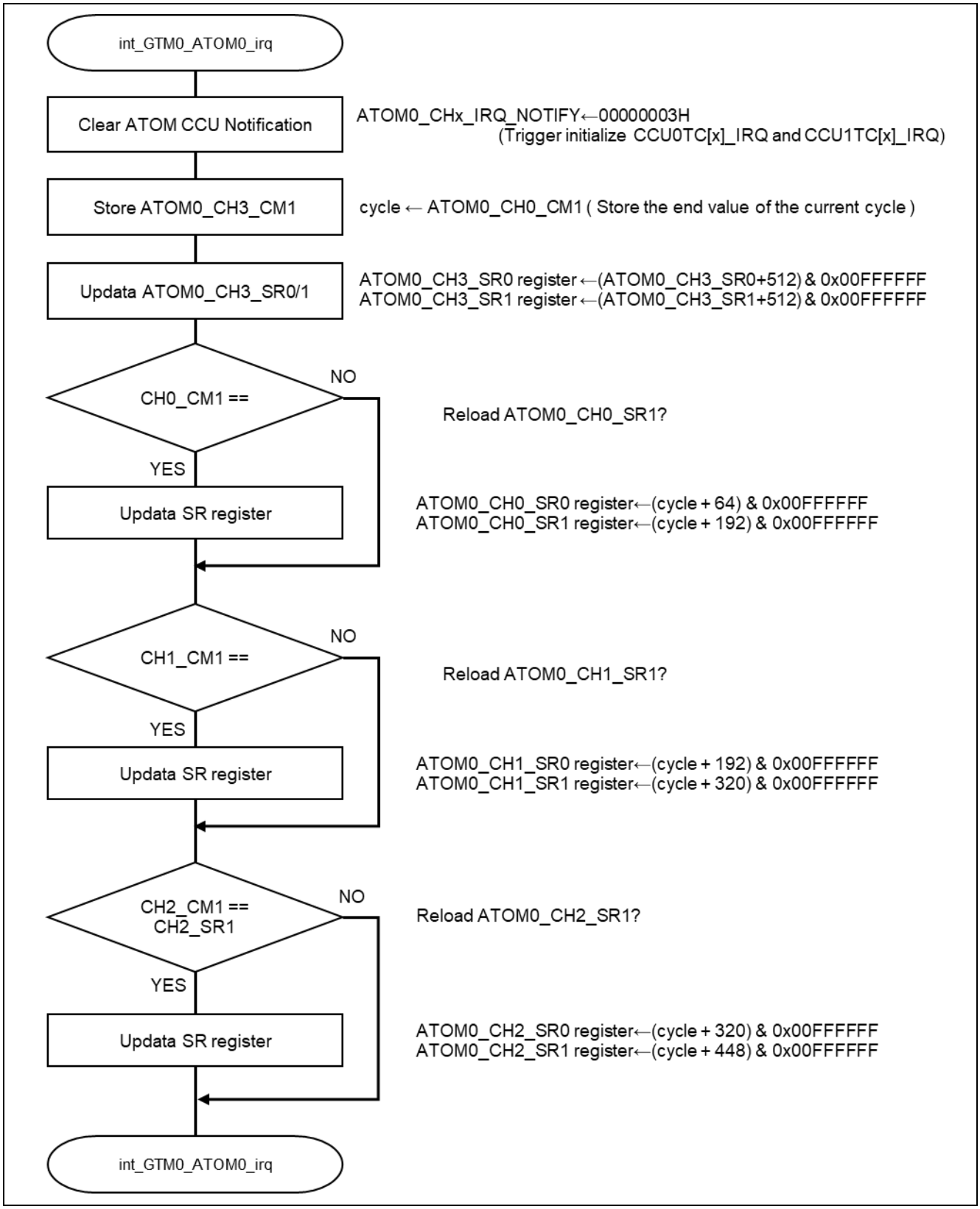


Figure 2-6 Flow of the ATOM_CH3 interrupt

Figure 2-7 shows the INTC initialization flow.

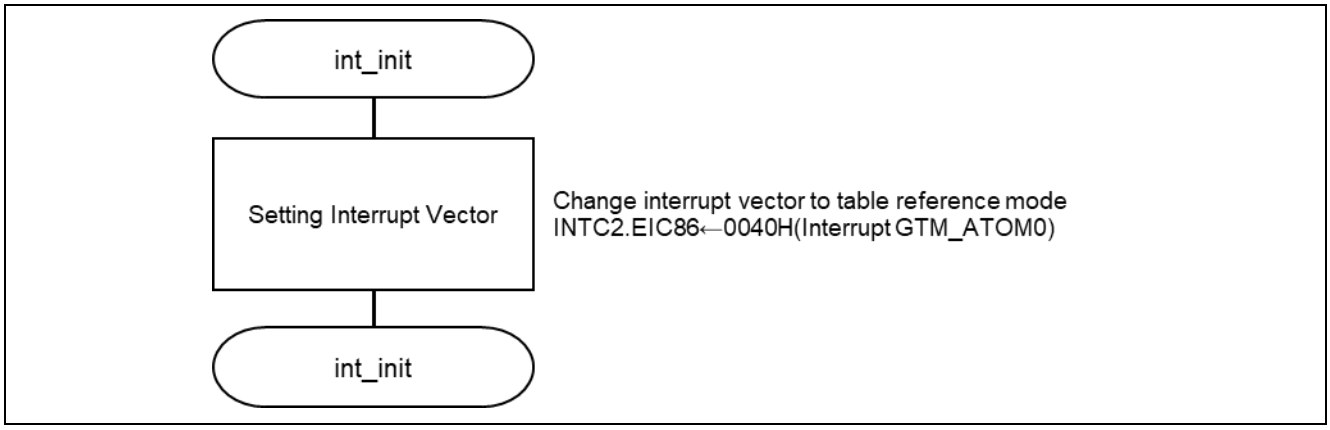


Figure 2-7 Flow of the INTC setting

Figure 2-8 shows the operation flow of initialization of RDC3AL, Figure 2-9 shows the operation flow of starting of RDC3AL.

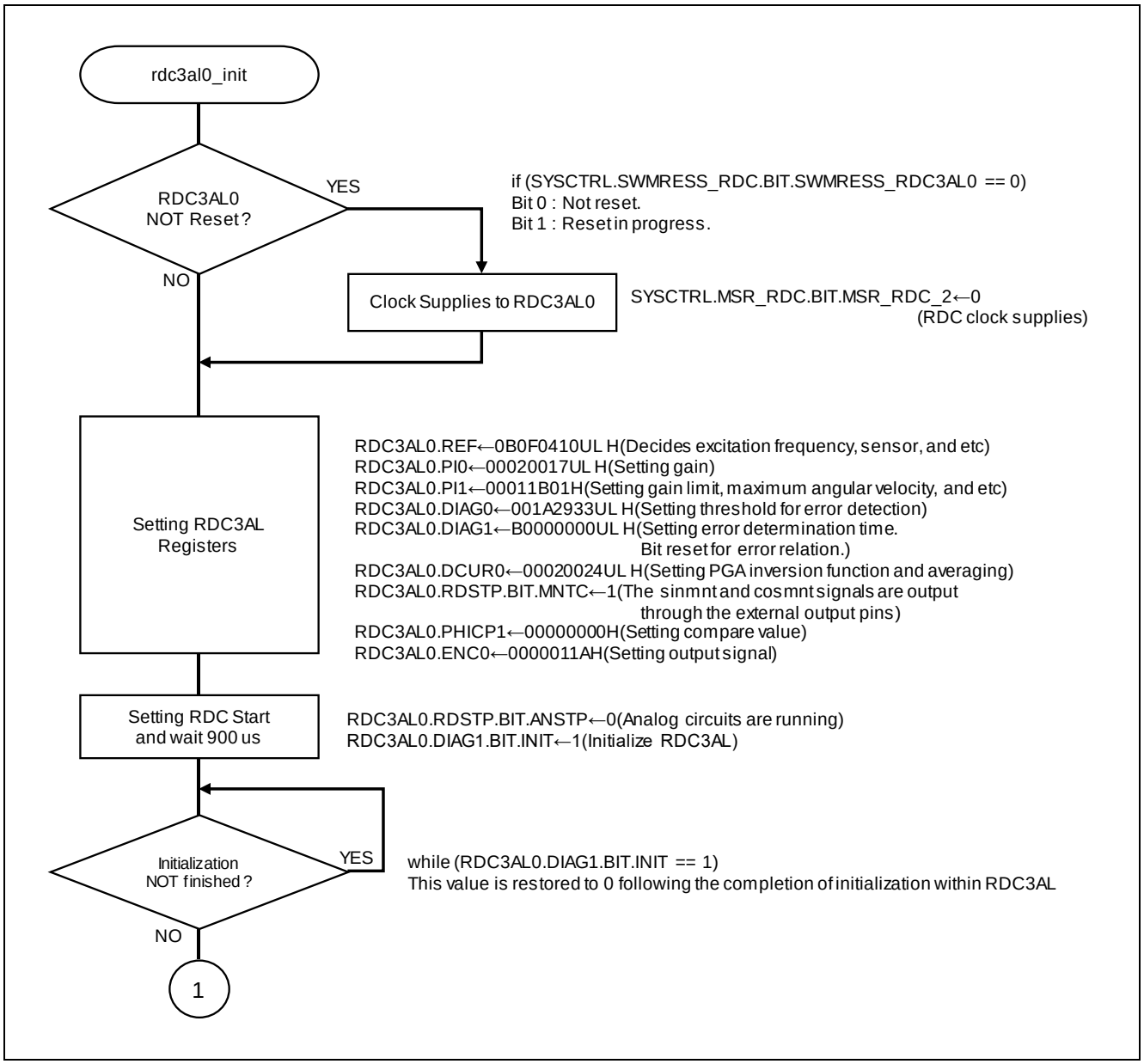


Figure 2-8 Flow of the RDC3AL initialization

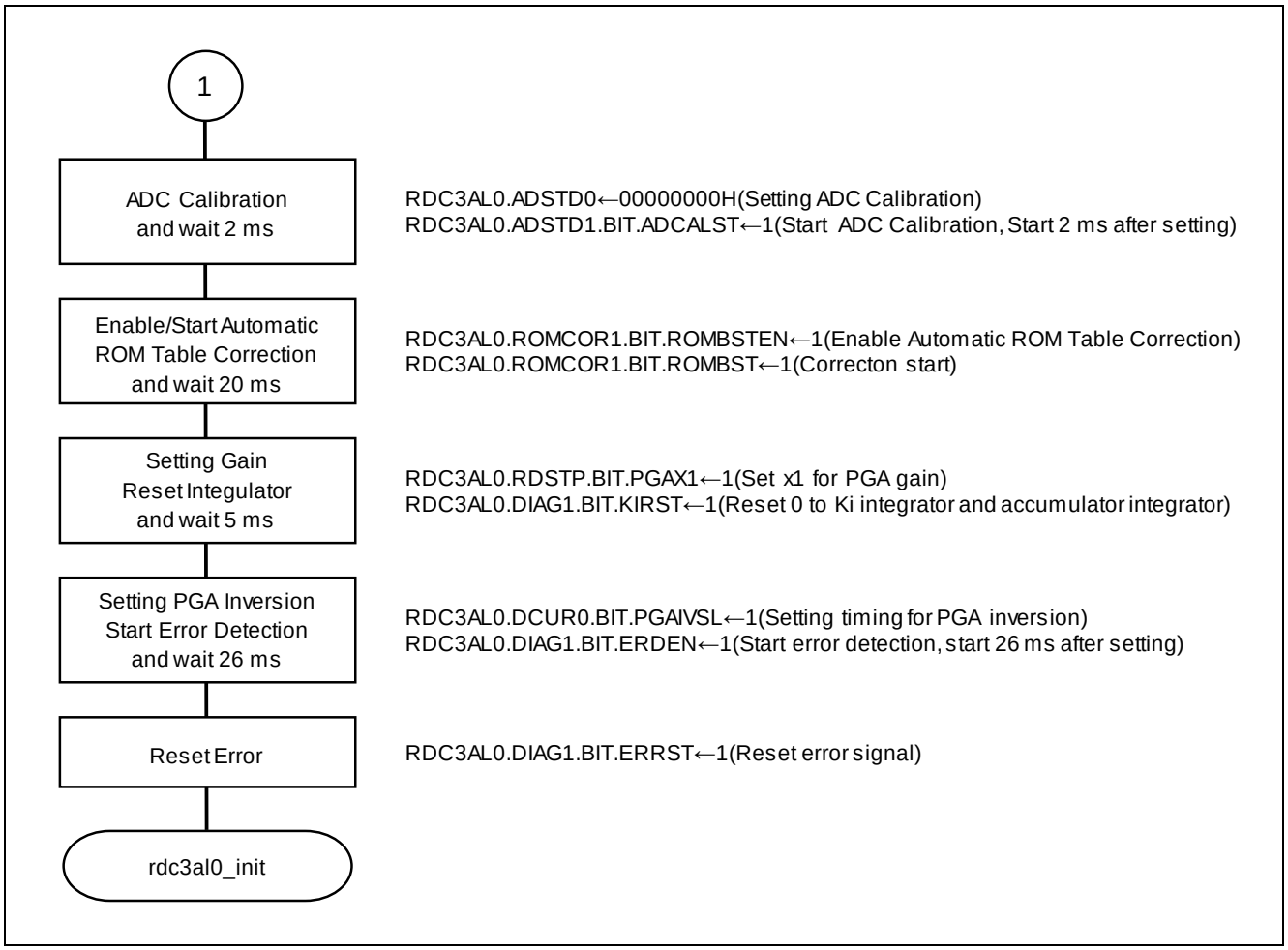


Figure 2-9 Flow of the RDC3AL starting

PIC selects the input signal to the TIM. In this application, select and use the RDC3AL encoder pulse output Z phase / A phase / B phase for GTM_TIM0_IN0 / 1 / 2 respectively.

Figure 2-10 shows the operation flow of the initial settings.

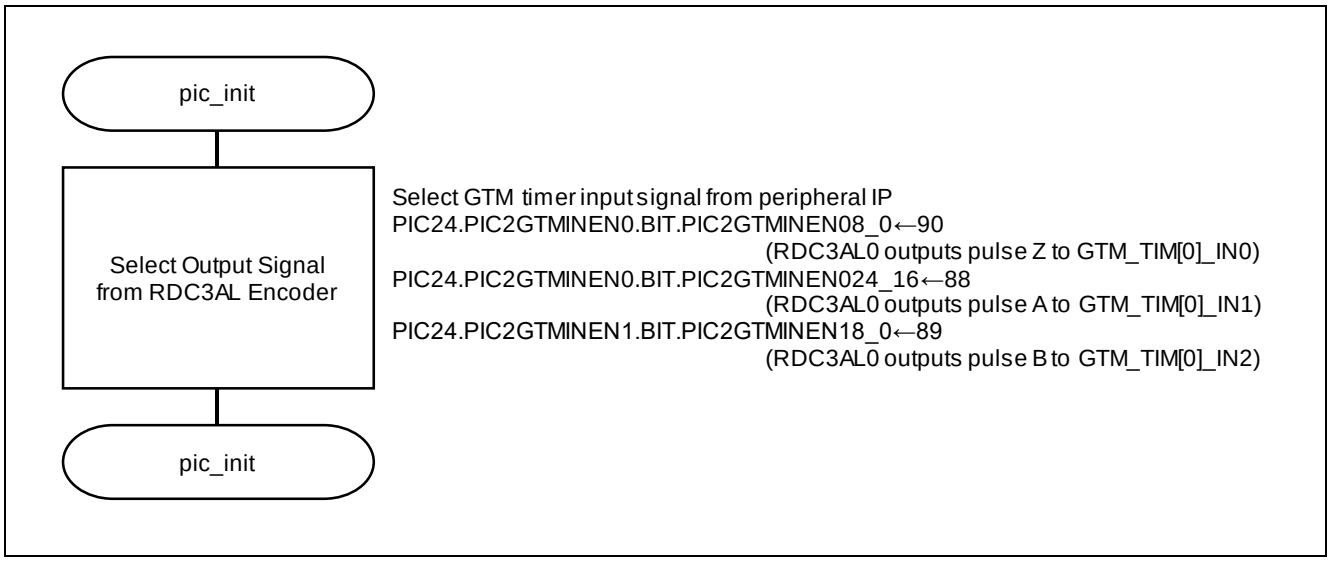


Figure 2-10 Flow of the PIC initial setting

Figure 2-11 shows the initial setting operation flow.

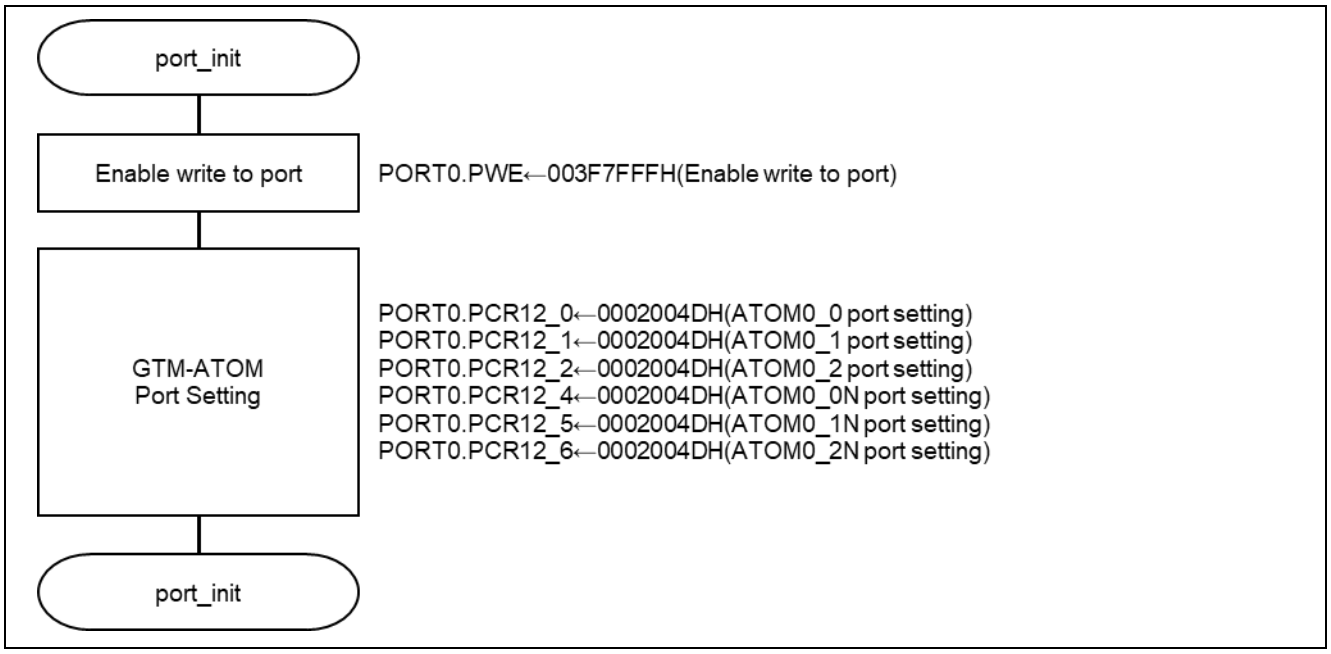


Figure 2-11 Flow of the PORT initial setting

2.1.3 Software description

Table 2-1 to Table 2-13 show the register settings used for GTM activation and interrupts.

Table 2-14 to Table 2-15 show the register settings used for the ATOM0 interrupt.

Table 2-16 shows the register settings used by the interrupt controller (INTC).

Table 2-17 shows the initialization of RDC3AL and Table 2-18 shows the register settings used when starting RDC3AL.

Table 2-19 shows the register settings used for the initial settings of the PIC.

Table 2-20 shows the register settings used for port initial settings.

Table 2-1 Setting Interrupt for GTM

Register name	Setting value	Function
GTM Interrupt Selection Control Register 000 (IRQ_SEL000)	0x00010000	Output only interrupt requests from ATOM0 to INTC

Table 2-2 Setting CCM

Register name	Setting value	Function
GTM Interrupt Selection Control Register 000 (IRQ_SEL000)	0x00010000	Output only interrupt requests from ATOM0 to INTC
CCM0 CMU Clock Configuration Register (CCM0_CMU_CLK_CFG)	0x00000220	In-cluster clocks obtained externally

Table 2-3 Setting clock for GTM

Register name	Setting value	Function
CCM0 CMU Clock Configuration Register (GTM_CLS_CLK_CFG)	0x000000AA	Enable clusters 0-3 with clock divider 2

Table 2-4 Disable ATOM

Register name	Setting value	Function
ATOM AGC Output Enable Control Register (ATOM0_AGC_OUTEN_CTRL)	0x00000155	Disable channel output on an update trigger
ATOM AGC Output Enable Status Register (ATOM0_AGC_OUTEN_STAT)	0x00000155	Disable ATOM_OUT output
ATOM Enable/Disable Status Register (ATOM0_AGC_ENDIS_CTRL)	0x00000155	Disable channel on an update trigger

Table 2-5 Enable CMU

Register name	Setting value	Function
CMU Clock Enable Register (CMU_CLK_EN)	OR 0x0000002A	Enable clock source
CMU Global Clock Control Numerator Register (CMU_GCLK_NUM)	0x00000001	Set 1 to numerator for global clock divider
CMU Global Clock Control Denominator Register (CMU_GCLK_DEN)	0x00000001	Set 1 to denominator for global clock divider

Table 2-6 Enable TBU

Register name	Setting value	Function
TBU Channel 0 Control Register (TBU_CH0_CTRL)	0x00000000	Select counter bits resolution and clock source (TBU_CMU_CLK0)
TBU Channel 1 Control Register (TBU_CH1_CTRL)	0x00000002	Select channel mode and clock source (TBU_CMU_CLK1)
TBU Channel 2 Control Register (TBU_CH2_CTRL)	0x00000002	Select channel mode and clock source (TBU_CMU_CLK1)
TBU Global Channel Enable Register (TBU_CHEN)	0x000000AA	Enable channel 0~3

Table 2-7 Setting TIM

Register name	Setting value	Function
TIM0 AUX IN Source Selection Register (TIM0_IN_SRC)	0x00000000	Using input signal as input source
TIM0 Channel 0 Control Register (TIM0_CH0_CTRL)	0x01002500	・Use CCM_CLK_RES[1:1] as clock source ・Measurement starts from the rising edge ・TIM PWM measurement mode (TPWM)
TIM0 Channel 0 Extended Control Register (TIM0_CH0_ECTRL)	0x00000000	Since the extended function is not used, use the reset value of the microcomputer
TIM0 Channel 0 Interrupt Mode Configuration Register (TIM0_CH0_IRQ_MODE)	0x00000001	Set interrupt to pulse mode
TIM0 channel 0 Interrupt Notification Register (TIM0_CH0_IRQ_NOTIFY)	0x0000003F	Clear interrupt flags
TIM0 Channel 0 Interrupt Enable Register (TIM0_CH0_IRQ_EN)	0x00000000	Interrupt disable
TIM0 Channel 1 Control Register (TIM0_CH1_CTRL)	0x00086004	・Enable external capture mode ・Measurement starts at both rising and falling edges ・TIM Input event mode (TIEM)
TIM0 Channel 1 Extended Control Register (TIM0_CH1_ECTRL)	0x0000000B	Select trigger source for EXT_CAPTURE function
TIM0 Channel 1 Interrupt Mode Configuration Register (TIM0_CH1_IRQ_MODE)	0x00000001	Set interrupt to pulse mode
TIM0 channel 1 Interrupt Notification Register (TIM0_CH1_IRQ_NOTIFY)	0x0000003F	Clear interrupt flags
TIM0 Channel 1 Interrupt Enable Register (TIM0_CH1_IRQ_EN)	0x00000000	Interrupt disable
TIM0 Channel 2 Control Register (TIM0_CH2_CTRL)	0x00086004	・Enable external capture mode ・Measurement starts at both rising and falling edges ・TIM Input event mode (TIEM)
TIM0 Channel 2 Extended Control Register (TIM0_CH2_ECTRL)	0x80800000	Select data for channel measurements and filters
TIM0 Channel 2 Interrupt Mode Configuration Register (TIM0_CH2_IRQ_MODE)	0x00000001	Set interrupt to pulse mode
TIM0 channel 2 Interrupt Notification Register (TIM0_CH2_IRQ_NOTIFY)	0x0000003F	Clear interrupt flags
TIM0 Channel 2 Interrupt Enable Register (TIM0_CH2_IRQ_EN)	0x00000000	Interrupt disable
TIM0 Channel 2 TDU Counter Register (TIM0_CH2_TDUC)	TO_CNT2 : 0x5A	Current timeout slice value setting for channel 2

Table 2-8 Setting ATOM Interrupt

Register name	Setting value	Function
ATOM0 Channel x Interrupt Enable Register (ATOM0_CHx_IRQ_EN)	0x00000000 (x = 0 ~ 3)	Disable interrupts for ATOM0 channels 0-3
ATOM0 Channel x Interrupt Notification Register (ATOM0_CHx_IRQ_NOTIFY)	0x00000003 (x = 0 ~ 3)	Clear interrupt flags

Table 2-9 Setting ATOM

Register name	Setting value	Function
ATOM0 Channel x Control Register (ATOM0_CHx_CTRL)	0x40000150 (x = 0 ~ 3)	・ATOM Signal Output Mode Buffered Compare (SOMB) ・Use time stamp signal (ATOM_TBU_TS1) for compare

Table 2-10 Setting DTM

Register name	Setting value	Function
DTM4 Global Configuration and Control Register (CDTM0_DTM4_CTRL)	0x00000001	Shut-off reset and clock source setting
DTM4 Channel Control Register 1 (CDTM0_DTM4_CH_CTRL1)	0x00000000	Dead time setting
DTM4 Channel Control Register 2 (CDTM0_DTM4_CH_CTRL2)	0x00888888	Allow dead-time pass for channels 0-2
DTM4 Channel Control Register 3 (CDTM0_DTM4_CH_CTRL3)	0x00000000	Settings related to combination input
DTM4 Channel x Dead Time Reload Values (CDTM0_DTM4_CHx_DTV)	DEAD_TIME_COUNT OR (DEAD_TIME_COUNT << 16) (13107400), (x = 0 ~ 3)	Setting reload value for rising edge dead time and falling edge dead time

Table 2-11 Setting ATOM Update

Register name	Setting value	Function
ATOM0 AGC Global Control Register (ATOM0_AGC_GLB_CTRL)	0x00550000	Settings that do not update or reset channels from internal registers
ATOM0 AGC Force Update Control Register (ATOM0_AGC_FUPD_CTRL)	0x00AA00AA	Reset counter register and enable forced update of channel
ATOM0 AGC Internal Trigger Control Register (ATOM0_AGC_INT_TRIG)	0x000000AA	Use internal trigger from channel as trigger source for ATOM_TRIGOUT

Table 2-12 Setting PWM(for Test)

Register name	Setting value	Function
ATOM0 Channel x CCU0 Compare Shadow Register (ATOM0_CHx_SR0)	x = 0 : 64 x = 1 : 192 x = 2 : 320 x = 3 : 511	Shadow registers for updating compare registers
ATOM0 Channel x CCU1 Compare Shadow Register (ATOM0_CHx_SR1)	x = 0 : 192 x = 1 : 320 x = 2 : 448 x = 3 : 512	Shadow registers for updating compare registers
ATOM0 Channel x CCU0 Compare Register (ATOM0_CHx_CM0)	1 (x = 0 ~ 3)	Register to store value for comparison
ATOM0 Channel x CCU1 Compare Register (ATOM0_CHx_CM1)	2 (x = 0 ~ 3)	Register to store value for comparison
ATOM0 Channel x CCU0 Counter Register (ATOM0_CHx_CN0)	0 (x = 0 ~ 3)	Counter register

Table 2-13 Setting Enable ATOM

Register name	Setting value	Function
ATOM0 Channel 3 Interrupt Enable Register (ATOM0_CH3_IRQ_EN)	0x00000002	Enable interrupts for ATOM0 channels 3 CCU1TC_IRQ
ATOM AGC Output Enable Control Register (ATOM0_AGC_OUTEN_CTRL)	0x000000AA	Enable channel output on an update trigger
ATOM AGC Output Enable Status Register (ATOM0_AGC_OUTEN_STAT)	0x000000AA	Enable ATOM_OUT output
ATOM Enable/Disable Control Register (ATOM0_AGC_ENDIS_CTRL)	0x000000AA	Enable ATOM channel on an update trigger
ATOM Enable/Disable Status Register (ATOM0_AGC_ENDIS_CTRL)	0x000000AA	Enable ATOM channels

Table 2-14 ATOM0 Interrupt: Clear ATOM CCU Notification

Register name	Setting value	Function
ATOM0 Channel x Interrupt Notification Register (ATOM0_CHx_IRQ_NOTIFY)	0x00000003 (x = 0 ~ 3)	Clear interrupt flags

Table 2-15 ATOM0 Interrupt: Update Compare Registers

Register name	Setting value	Function
ATOM0 Channel x CCU0 Compare Shadow Register (ATOM0_CHx_SR0)	x = 0 : cycle + 64 x = 1 : cycle + 192 x = 2 : cycle + 320 x = 3 : SR0 + 512 (cycle = ATOM0_CH3_CM1)	Shadow registers for updating compare registers
ATOM0 Channel x CCU1 Compare Shadow Register (ATOM0_CHx_SR1)	x = 0 : cycle + 192 x = 1 : cycle + 320 x = 2 : cycle + 448 x = 3 : SR1 + 512 (cycle = ATOM0_CH3_CM1)	Shadow registers for updating compare registers

Table 2-16 INTC Setting

Register name	Setting value	Function
EI level Interrupt Control Register 2 (INTC2)	EIC86 : 0x004F	Change interrupt vector to Table reference mode GTM0_ATOM0 interrupt (priority: 0, lowest)

Table 2-17 RDC3AL registers initial setting

Register name	Setting value	Function
Module Standby Register for RDC3 (SYSCTRL.MSR_RDC)	MSR_RDC_2 : 0	Clock supplies to RDC3AL0.
Excitation Setting Register (RDC3AL0.REF)	0x0B0F0410	Decides excitation frequency, sensor, and etc.
Control Gain Select Register 0 (RDC3AL0.PI0)	0x00020017	Setting gain.
Control Gain Select Register 1 (RDC3AL0.PI1)	0x00011B01	Setting gain limit, maximum angular velocity, and etc.
Error Detection Register 0 (RDC3AL0.DIAG0)	0x001A2933	Setting threshold for error detection.
Error Detection Register 1 (RDC3AL0.DIAG1)	0xB0000000	Setting error determination time. Bit reset for error relation.
Digital Operation Register 0 (RDC3AL0.DCUR0)	0x00020024	Setting PGA inversion function and averaging.
RDC Stop Register (RDC3AL0.RDSTP)	MNTC : 1	The sinmnt and cosmnt signals are output through the external output pins.
PHI Compare Setting Register 1 (RDC3AL0.PHICP1)	0x00000000	Setting compare value.
Encoder Register 0 (RDC3AL0.ENC0)	0x0000011A	Setting output signal.

Table 2-18 RDC3AL registers start setting

Register name	Setting value	Function
RDC Stop Register (RDC3AL0.RDSTP)	ANSTP : 0	Analog circuits are running.
	PGAX1 : 1	Set x1 for PGA gain.
Error Detection Register 1 (RDC3AL0.DIAG1)	INIT : 1	Initialize RDC3AL (This value is restored to 0 following the completion of initialization within RDC3AL.)
	KIRST : 1	Reset 0 to Ki integrator and accumulator integrator
	ERDEN : 1	Start error detection (Start 26 ms after setting)
	ERRST : 1	Reset error signal.
12-Bit SAR-ADC Digital Circuit Block Setting Register 0 (RDC3AL0.ADSTD0)	0x00000000	Setting ADC calibration.
12-Bit SAR-ADC Digital Circuit Block Setting Register 1 (RDC3AL0.ADSTD1)	ADCALST : 1	Start ADC calibration. (Start 2 ms after setting)
Automatic ROM Table Correction Register 1 (RDC3AL0.ROMCOR1)	ROMBSTEN : 1	Enable Automatic ROM Table Correction
	ROMBST : 1	Start Automatic ROM Table Correction
Digital Operation Register 0 (RDC3AL0.DCUR0.BIT)	PGAIVSL : 1	Setting timing for PGA inversion

Table 2-19 PIC registers initial setting

Register name	Setting value	Function
GTM Timer Input Module (TIM) Source Select Register 0 (PIC2GTMINEN0)	PIC2GTMINEN0[8:0] : 90	Select encoder pulse output (Z phase) for GTM_TIM0_IN0
	PIC2GTMINEN0[24:16] : 88	Select encoder pulse output (A phase) for GTM_TIM0_IN1
GTM Timer Input Module (TIM) Source Select Register 1 (PIC2GTMINEN1)	PIC2GTMINEN1[8:0] : 89	Select encoder pulse output (B phase) for GTM_TIM0_IN2

Table 2-20 PORT registers initial setting

Register name	Setting value	Function
Port Write Enable register (PORT0.PWE)	0x003F7FFF	Enable write to port.
Port Mode Control Register (PORT0.PCR12_m) (m = 0, 1, 2, 4, 5, 6)	0x0002004D	Enable port output ATOM0_0, 1, 2, 0N, 1N, 2N

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2023.9.29		First edition issued

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   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
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