RH850/U2B6

EMU3S (AD Trigger)

Summary

This application note describes how to use each of EMU3S features in RH850/U2B6. Although the examples of tasks and applications listed in this application note have been tested, please be sure to check the operating environment before actually using them.

Operation confirmation device

RH850/U2B6-FCC (R7F702Z22EDBB)

Table of contents

1. Introduction

This application note describes the operation of various EMU3S functions in RH850/U2B6-FCC.

The functions described in this application note are listed below.

- A/D trigger generation using TSG3 sub-counters
- Delay time setting to angle latch and current value latch of EMU3S
- Multiple A/D conversion trigger generation and batch value acquisition in a carrier half cycle
- Interrupt thinning function for peak and valley and setting the number of thinnings

1.1 The function to be used

RH850/U2B6 hardware features used in this application note are listed below.

In addition, this application note controls each hardware function from CPU0.

Table 1-1 Hardware functions used

Hardware function name	Symbol
Enhanced Motor control Unit 3 S	EMU3S
Motor Control Timer	TSG3
Peripheral Interconnect	PIC
Resolver to Digital Converter	RDC3AL
Analog to Digital Converter	ADCK

2. Motor control operation by EMU3S

First, motor control operation using EMU3S is described. EMU3S performs vector control and generates PWM compare values based on the motor current value and angle information. EMU3S works with ADCK, RDC3AL, and TSG3; motor current values are input from ADCK and angle information from RDC3AL. The PWM compare value generated by EMU3S is sent to TSG3, which outputs a PWM waveform. In this application note, EMU3S 's angle generation IP, input IP, PI control IP, and PWM IP are used for motor control.

Figure 2-1 shows the flow of motor control operation in which the EMU3S and each hardware function are linked.

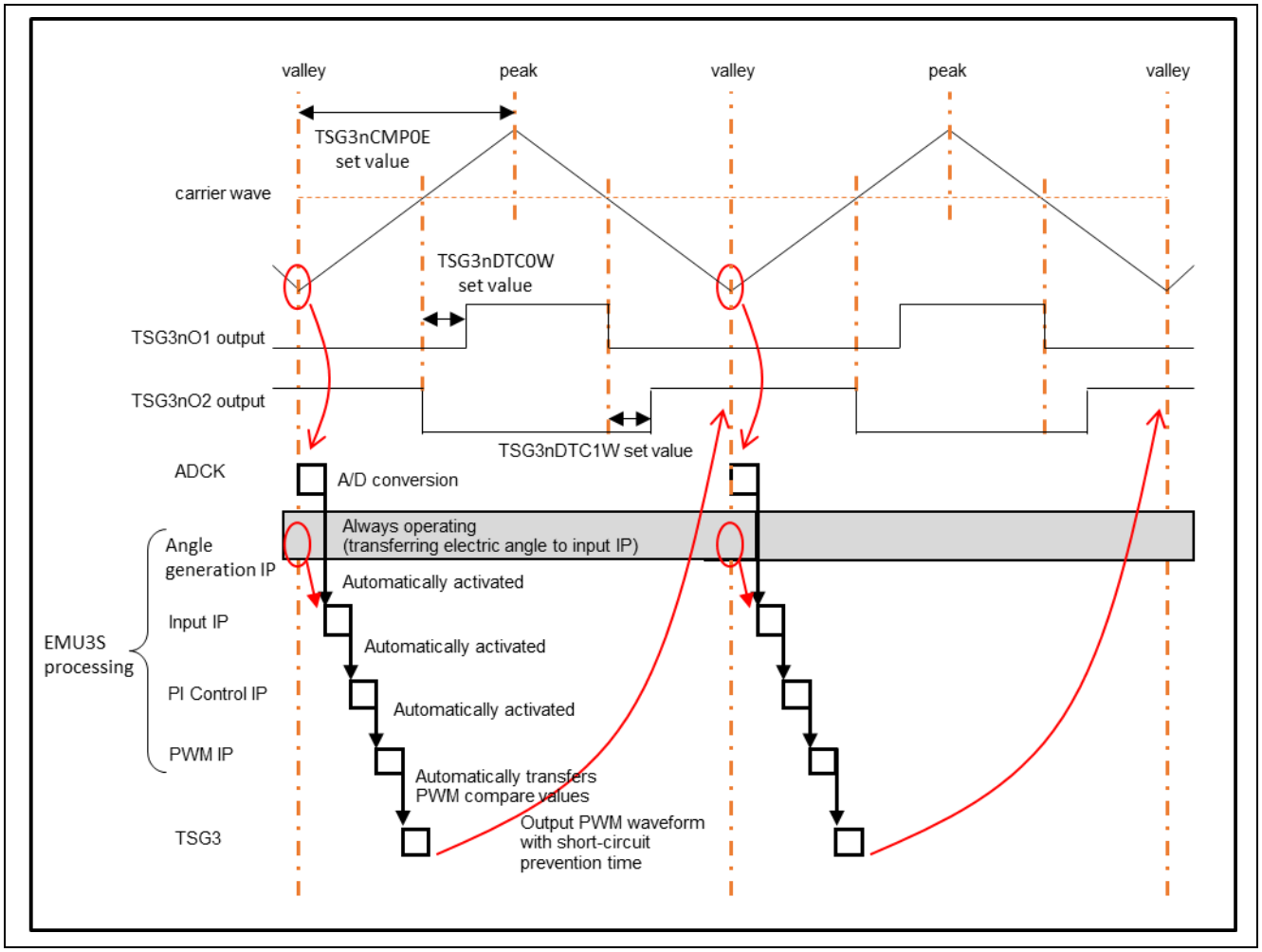

Figure 2-1 Motor control flow diagram by EMU3S

The following describes the operation of EMU3S 's angle generation IP, input IP, PI control IP, and PWM IP.

- The angle generation IP is activated each time the value of the angle data from RDC3AL (the upper 16 bits of RDC3ALnENC1 register) changes. It then adds the offset value (EMU3nANGOFS register) to the

value in RDC3ALnENC1 register before generating the electric angle. The generated electric angle is stored in EMU3nTHTEFIX register. Figure 2-2 shows a block diagram of the angle generation IP.

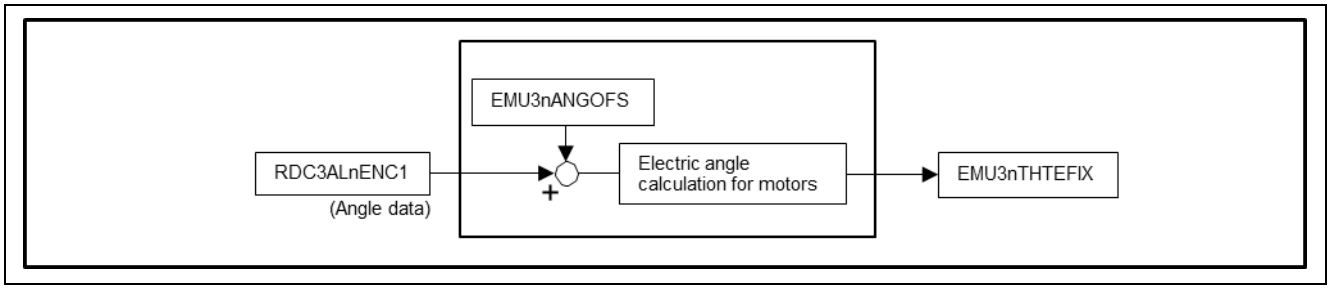

Figure 2-2 Block diagram of angle generation IP

- The input IP finds the current value of the remaining phase from the motor current values of the two phases, and then performs a dq conversion based on the obtained current value and the electric angle. When Bits INIPTRG [1:0] of EMU3nIPTRG register are set to "B'10", the input IP is automatically activated when A/D conversion is completed. The value stored in EMU3nTHTEFIX register is transferred to the input IP when the A/D trigger occurs and stored in EMU3nTHTE register. Figure 2-3 shows a block diagram of the input IP.

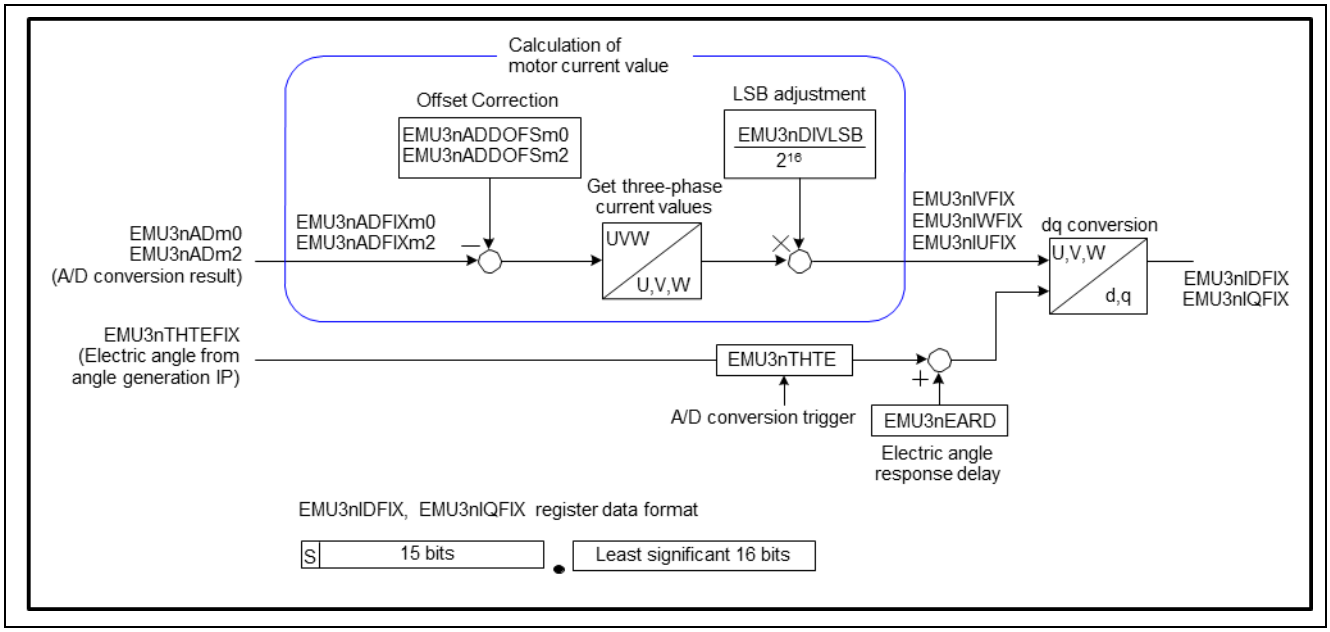

Figure 2-3 Block diagram of input IP

- The PI control IP calculates d and q-axis voltages using the d and q-axis currents (feedback values) calculated by dq conversion and the d and q-axis current values (command values) set by software. When PIIPTRG bit of EMU3nIPTRG register is set to "1", the PI control IP is automatically activated when the input IP processing is completed. Figure 2-4 shows a block diagram of the PI control IP. From the feedback values stored in EMU3nIDFIX and EMU3nIQFIX registers and the command values set in EMU3nIDIN and EMU3nIQIN registers, the d and q-axis voltages, which are the operating quantities, are calculated. As a result, the d-axis voltage is stored in EMU3nVD register and the q-axis voltage in EMU3nVQ register.

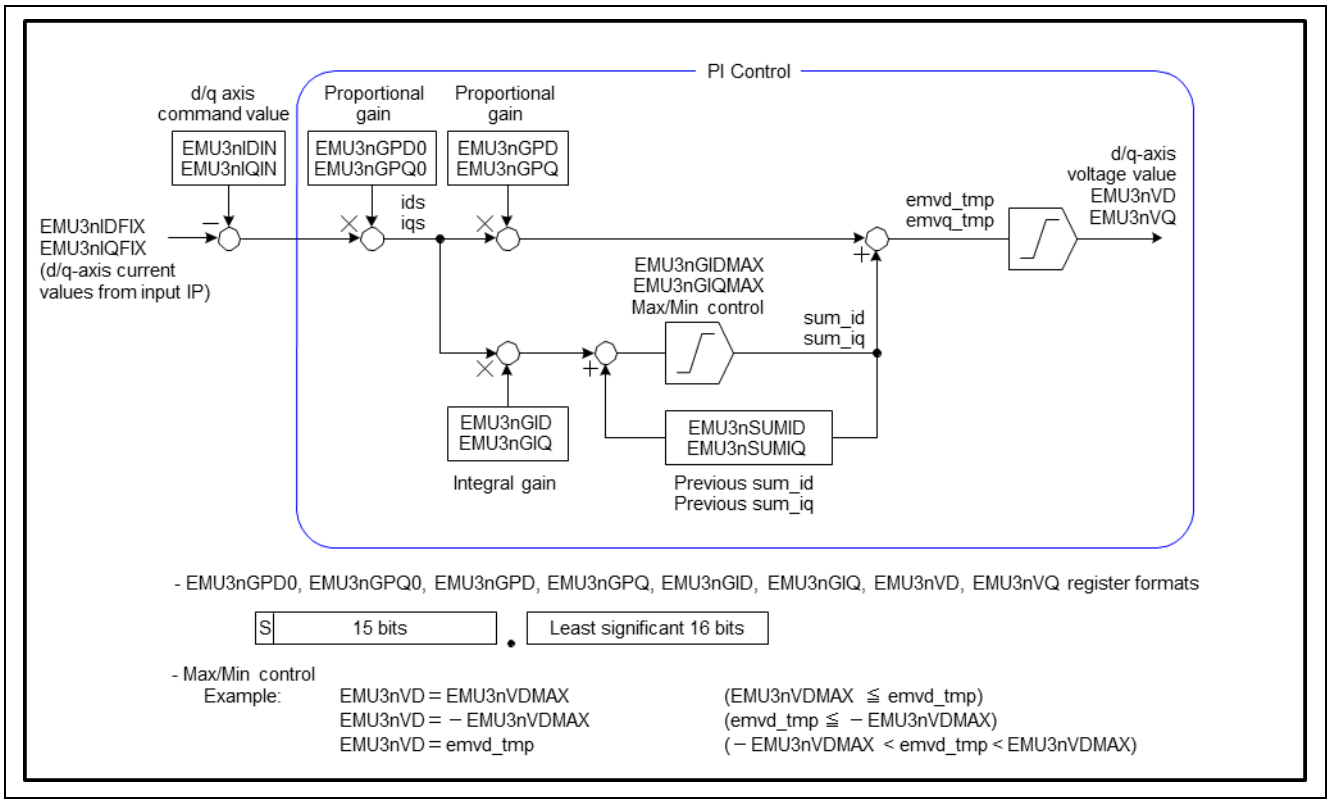

Figure 2-4 Block diagram of PI control IP

- The PWM IP uses the d and q-axis voltages calculated by the PI control IP to obtain the output voltages of the U/V/W phases, and calculates the duty ratio and compare register values for each phase in the PWM waveform output from these voltage values. When PWMIPTRG bit of EMU3nIPTRG register is set to "1", the PWM IP is automatically activated when the PI IP process is completed. Figure 2-5 shows a block diagram of the PWM IP.

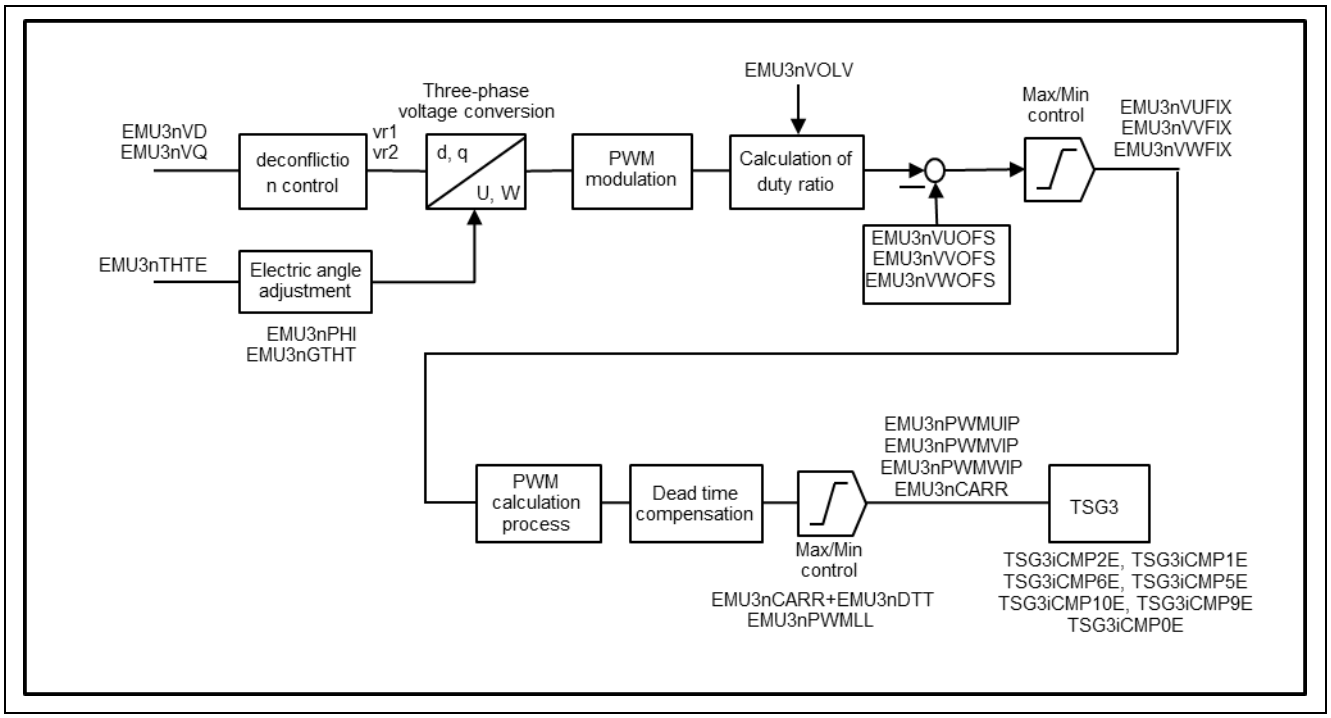

Figure 2-5 Block diagram of PWM IP

Other hardware features that work with EMU3S are listed below.

- R/D converter 3AL (RDC3AL)
  Analog signals output from the resolver are digitally converted to calculate angle values (resolver angle) and angular velocity.
- Peripheral interconnection (PIC)
  ADCK hardware trigger signal is generated based on the signal output from EMU3S synchronized with the carrier wave.
- A/D converter (ADCK)
  The motor current value is converted to A/D and the converted value is input to EMU3S. In this application note, A/D conversion is started by the trigger generated by the PIC in response to the output signal from EMU3S.When the trigger is input, ADCK0I00 converts the current value of phase V, ADCK0I01 converts the current value of phase W, and ADCK0I02 converts the current value of phase U. The current value of phase W is not used in the process.
- Motor control timer 3 (TSG3)
  TSG3 outputs three-phase PWM waveforms based on the compare values transferred from EMU3S. TSG3 generates duty from a compare match between an 18-bit counter and an 18-bit sub-counter (16 bits are used in combination with EMU3S) and outputs a 3-phase PWM waveform with added short-circuit prevention time.

2.1 Common setting

The following describes common register settings used in this application note.

Table 2-1 ADCK register setting

Register name	Set value	Function
ADCK0.VCR00	0x00002000H	T&H assignment of ADCK0I00 to virtual channel 0
ADCK0.VCR01	0x00002001H	T&H assignment of ADCK0I01 to virtual channel 1
ADCK0.VCR00	0x00002002H	T&H assignment of ADCK0I02 to virtual channel 2
ADCK0.VCR03	0x00000004H	Assign ADCK0I10 to virtual channel 3
ADCK0.SGVCPR4	0x0300H	VCSP = 0x00: Output from virtual channel 0 VCEP = 0x03: Ends with virtual channel 3
ADCK0.SGCR4	0x01H	Scan group 4 multi-cycle mode setting Enable H/W trigger input to scan group 4
ADCK0.ADCR2	0x10H	Signed integer
ADCK0.ADCR1	0x02H	Asynchronous Suspend
ADCK0.THCR	0x00H	T&H Sampling Mode
ADCK0.THER	0x07H	TH A 0-2 Permitted
ADCK0.THGSR	0x0000H	T&H Group A assignment
ADCK0.THACR	0x33H	T&H Group A set, T&H Group A operation permitted
ADCK0.THSMPSTCR	0x01H	T&H sampling start

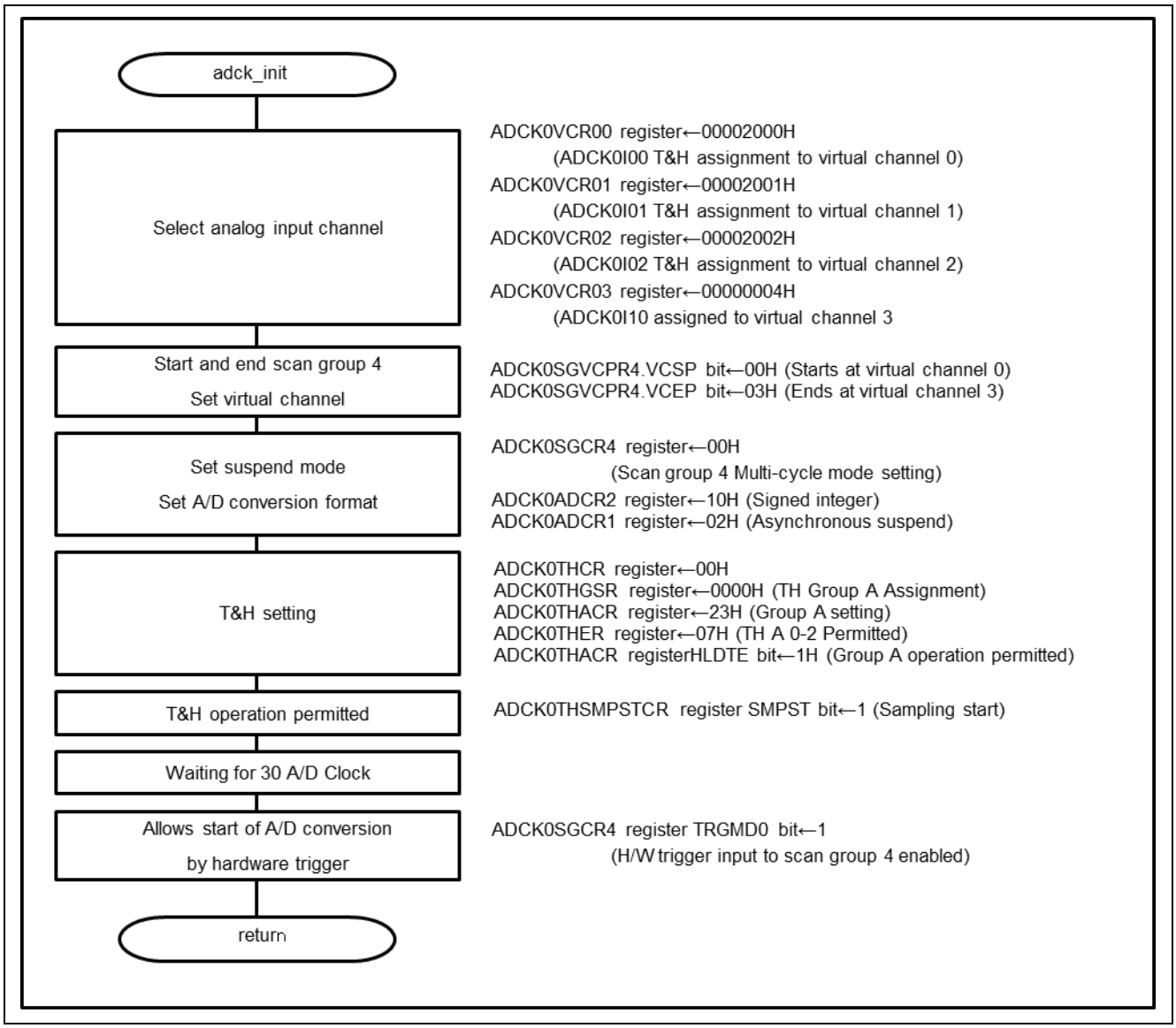

Figure 2-6 ADCK Initial Setup

Table 2-2 RDC3AL register setting

Register name	Set value	Function
RDC3AL0.REF	0x0B0F0400H	Excitation signal output 10kHz
RDC3AL0.PI0	0x00020017H	Automatic adjustment
RDC3AL0.PI1	0x00010001H	Speed 12bit
RDC3AL0.ATMNT0	0x00240200H	Amplitude automatic adjustment setting
RDC3AL0.DIAG0	0x001A2933H	2 path error 256LSB
RDC3AL0.DIAG1	0xB0010001H	Initialization
RDC3AL0.RDSTP	0x00000100H	Operation start
RDC3AL0.ADSTD1	0x00010000H	ADC calibration start
RDC3AL0.ROMCOR1	0x00001001H	ROM table modification setting
RDC3AL0.DCUR0	0x00000000H	Digital operation setting

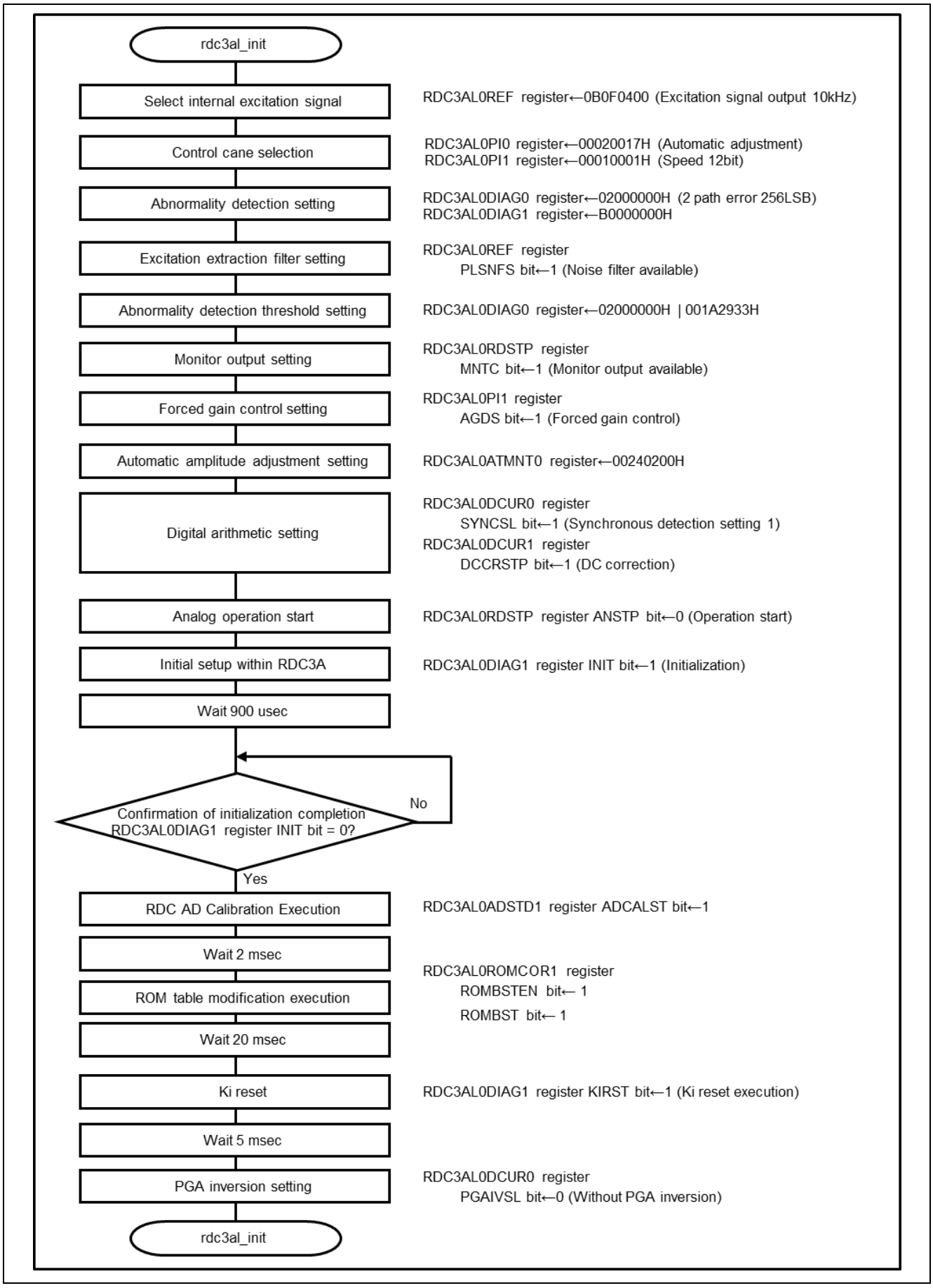

Figure 2-7 RDC3AL Initial Setup

Table 2-3 PIC register setting

Register name	Set value	Function
PIC21.ADCK0TSEL4	0x00300000H	EMU30 selected as trigger source for ADCK0 scan group 4

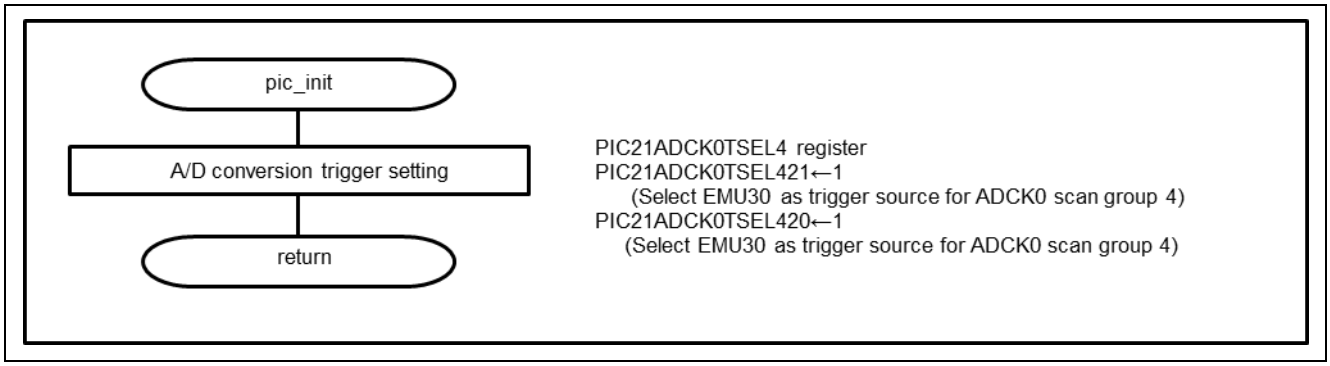

Figure 2-8 PIC Initial Setup

Table 2-4 TSG3 register setting

Register name	Set value	Function
TSG30.CTL0	0x01H	HT-PWM mode
TSG30.DTPR	0x0000H	Rewriting allowed
TSG30.DTC0W	0x00000140H	Reverse phase to positive phase dead time value 4us
TSG30.DTC1W	0x00000140H	Positive phase to reverse phase dead time value 4us
TSG30.CMP0E	0x00001F40H	PWM cycle set to 100us
TSG30.CMPUE	0x00000FA0H	Phase-U compare value (50%)
TSG30.CMPVE	0x00000FA0H	Phase-V compare value (50%)
TSG30.CMPWE	0x00000FA0H	Phase-W compare value (50%)
TSG30.CTL4	0x00000080H	Set PWM valley reload

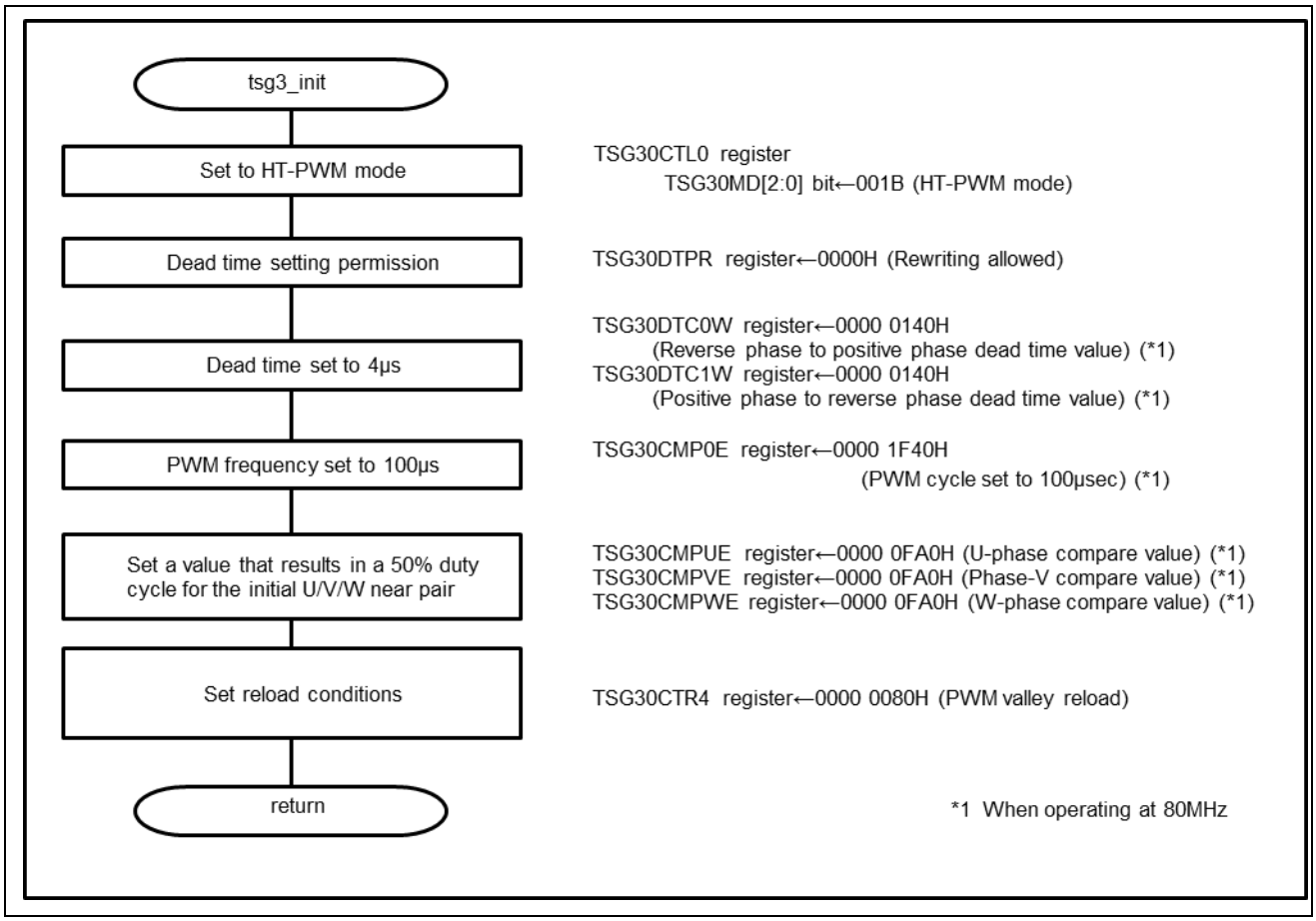

Figure 2-9 TSG3 Initial Setup

Table 2-5 EMU3S register setting (1/2)

Register name	Set value	Function
EMU30.CTR	0x01H	EMU3S launch
EMU30.ANGCTR	0x00H	Angle generation IP setting
EMU30.RESRLD	0x01H	Resolver axis double angle setting
EMU30.PXR	0x0100H	Electric angle generation factor setting
EMU30.ANGOFS	0x0000H	Angle offset
EMU30.CTRINMD	0x0025H	Input IP setting
EMU30.AD0OFS	0x0800H	AD0 data offset
EMU30.AD1OFS	0x0800H	AD1 data offset
EMU30.AD2OFS	0x0800H	AD2 data offset
EMU30.DIVLSB	0x00010000H	LSB adjustment
EMU30.SR2	0x0000D106H	dq conversion factor setting
EMU30.PICTR	0x03H	PI control IP setting
EMU30.IDIN	0x00000000H	ID input
EMU30.IQIN	0x00000000H	IQ input
EMU30.GPD0	0x00010000H	PI control coefficient
EMU30.GPQ0	0x00010000H	PI control coefficient
EMU30.GID	0x00000100H	PI control coefficient
EMU30.GIQ	0x00000100H	PI control coefficient

Table 2-6 EMU3S register setting (2/2)

Register name	Set value	Function
EMU30.GPD	0x00010000H	PI control coefficient
EMU30.GPQ	0x00010000H	PI control coefficient
EMU30.SUMID	0x00000000H	d-axis software settings
EMU30.SUMIQ	0x00000000H	q-axis software setting
EMU30.VDMAX	0x7FFFFFFFH	d-axis voltage maximum setting
EMU30.VQMAX	0x7FFFFFFFH	q-axis voltage maximum value setting
EMU30.GIDMAX	0x00000800H	GID maximum value setting
EMU30.GIQMAX	0x00000800H	GIQ maximum value setting
EMU30.REFCTR	0x01H	PWM IP register value reflection control
EMU30.PWMCTR	0x000102A1H	PWM IP setting
EMU30.DECVELG	0x00000000H	Incoherent control factor angular velocity value gain
EMU30.DECFLUX	0x00000000H	Incoherent control factor flux value
EMU30.DECLD	0x00000000H	Incoherent control coefficient Ld value
EMU30.DECLQ	0x00000000H	Incoherent control coefficient Lq value
EMU30.VDCRCT	0x00000000H	d-axis voltage correction value
EMU30.VQCRCT	0x00000000H	q-axis voltage correction value
EMU30.VD2MAX	0x7FFFFFFFH	Incoherent control d-axis maximum value
EMU30.VQ2MAX	0x7FFFFFFFH	Incoherent control q-axis max.
EMU30.PHI	0x0000H	Electric angle offset for PWM IP
EMU30.GTHT	0x00000100H	Electric angle adjustment factor for PWM IP
EMU30.SR23	0x0000D106H	Three-phase voltage conversion factor
EMU30.PWMK1	0x00800000H	Digit matching 1
EMU30.VOLV	0x1000H	Input voltage
EMU30.VUOFS	0x0000H	U-phase voltage correction value
EMU30.VVOFS	0x0000H	V-phase voltage correction value
EMU30.VWOFS	0x0000H	W-phase voltage correction value
EMU30.DTUL	0x7FFFFFFFH	Duty ratio upper limit
EMU30.DTLL	0x80000000H	Duty ratio lower limit
EMU30.PWMK2	0x00000100H	Adjusting the number of digits 2
EMU30.DTOTH	0x7FFFFFFFH	Dead time compensation threshold
EMU30.DTOPV	0x00000000H	Dead time compensation positive current addition value
EMU30.DTONV	0x00000000H	Dead time compensation negative current addition value
EMU30.PWMUL	0x0003FFFFH	PWM upper limit value
EMU30.PWMLL	0x00000000H	PWM lower limit value
EMU30.DTT	0x00000140H	Dead time setting
EMU30.CARR	0x00001F40H	Carrier cycle setting
EMU30.IPTRG	0x0EH	IP start trigger factor selection
EMU30.ADDCNT	0x00000000H	A/D value acquisition delay count setting
EMU30.RDDCNT	0x00000000H	Angle information acquisition delay count setting
EMU30.INT0	0x00000000H	EMU30 interrupt setting 0
EMU30.INT1	0x00000000H	EMU30 interrupt setting 1
EMU30.INT2	0x00000000H	EMU30 interrupt setting 2
EMU30.INT3	0x00000000H	EMU30 interrupt setting 3
EMU30.INT4	0x00000000H	EMU30 interrupt setting 4

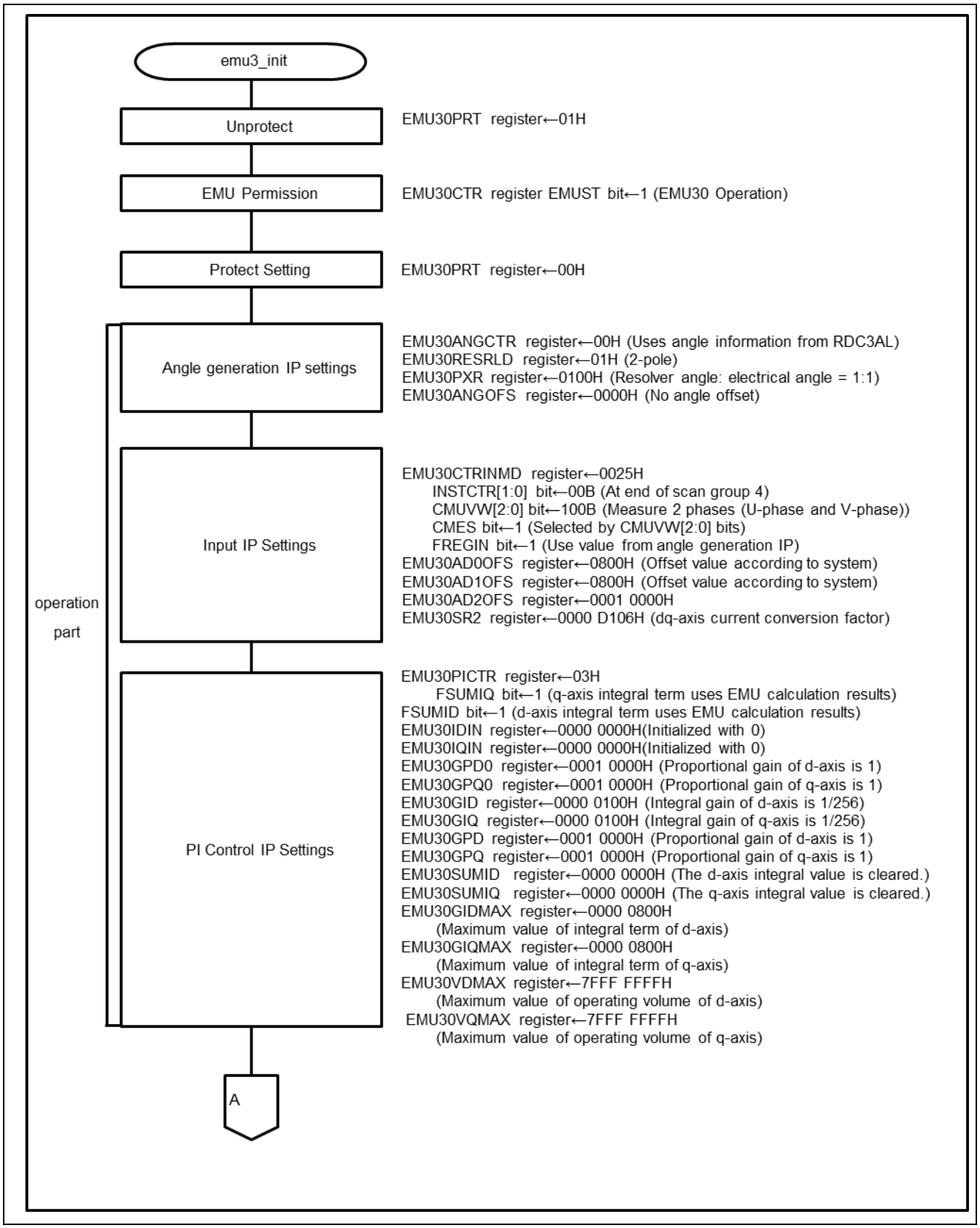

Figure 2-10 EMU3S Initial Setup (1)

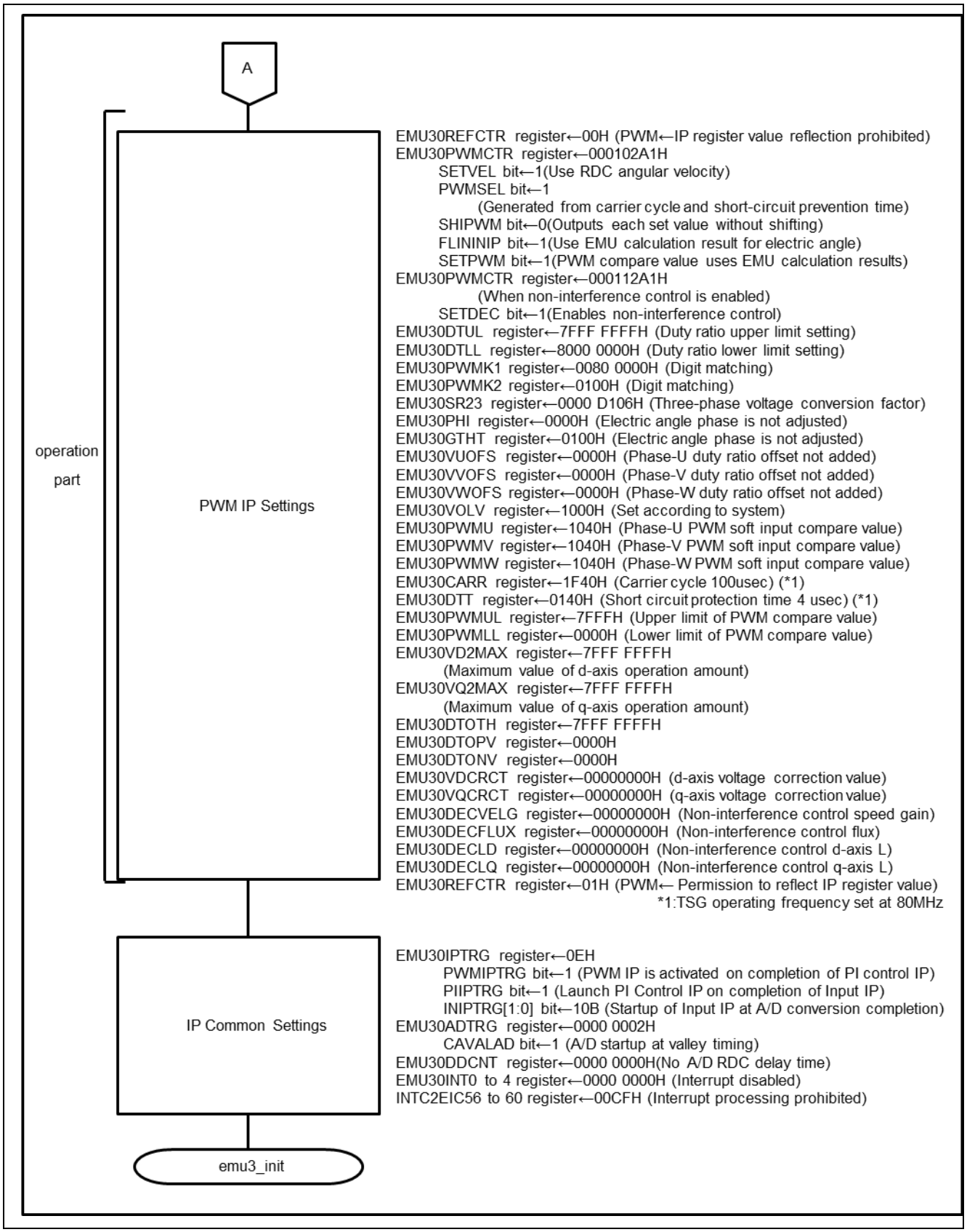

Figure 2-11 EMU3S Initial Setup (2)

2.2 A/D trigger generation using TSG3 sub-counters

2.2.1 Specifications overview

EMU3S can work with TSG3's HT-PWM mode to generate PWM waveforms for 3-phase synchronous motors. EMU3S can also work with ADCK to perform A/D conversion at a timing synchronized with the PWM carrier from TSG3. For the timing of A/D conversion requests, the EMU3S can output conversion requests at the peak and valley of the sub-counters of the PWM carrier, as shown in Figure 2-12.

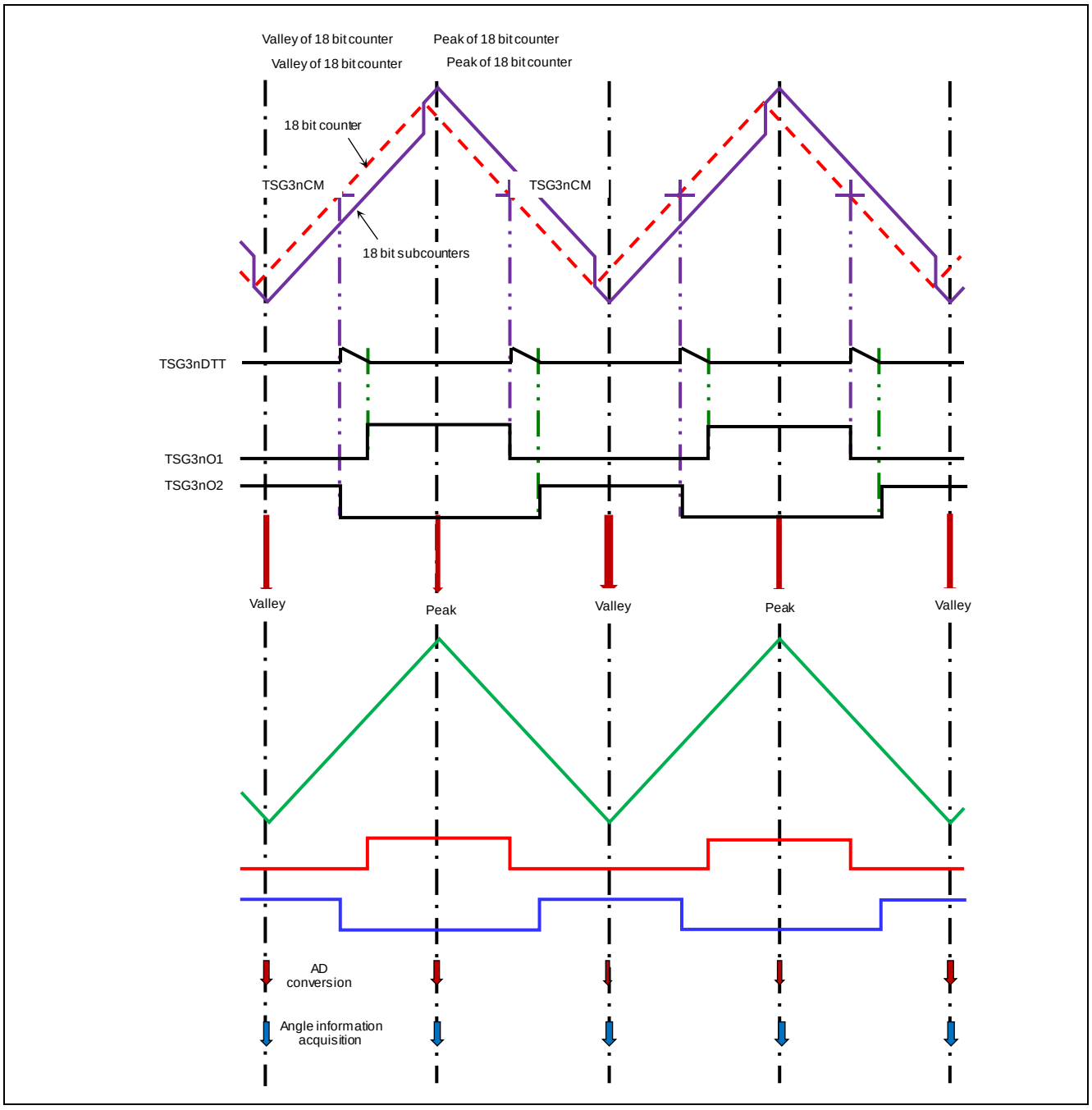

Figure 2-12 Operation overview

2.2.2 Operating conditions for specification functions

Below are the operating conditions for the A/D trigger function at the peak and valley timings of the sub-counters. For common settings, see 2.1.

Table 2-7 Function used

Item	Contents
Function used	● Function to perform A/D conversion at the timing of the peak and valley of the sub-counters of the carrier wave ● No trigger output delay for A/D conversion and R/D conversion

2.2.3 Operation description

In TSG3's HT-PWM mode, a PWM waveform is generated using a counter and a sub-counter. In EMU3S, A/D conversion request can be generated at the peak and valley of the sub-counters to operate ADCK. To realize the A/D conversion request function at the peak and valley of the sub-counter timing, EMU3S, TSG3, and PIC must be set respectively.

The output timing of the A/D conversion request in EMU3s is set by the EMU3nADTRG register.

The A/D conversion trigger output timing in TSG3 is set by the TSG3nCTL5 register for the carrier peak and the TSG3nCTL6 register for the carrier valley.

PIC can set the A/D conversion request to be output to ADCK, which is set in the PIC21ADCKnTSEL4 register.

2.2.4 Operation flow

Figure 2-13, Figure 2-14, and Figure 2-15 show the operational flow of EMU3S, TSG3, and PIC.

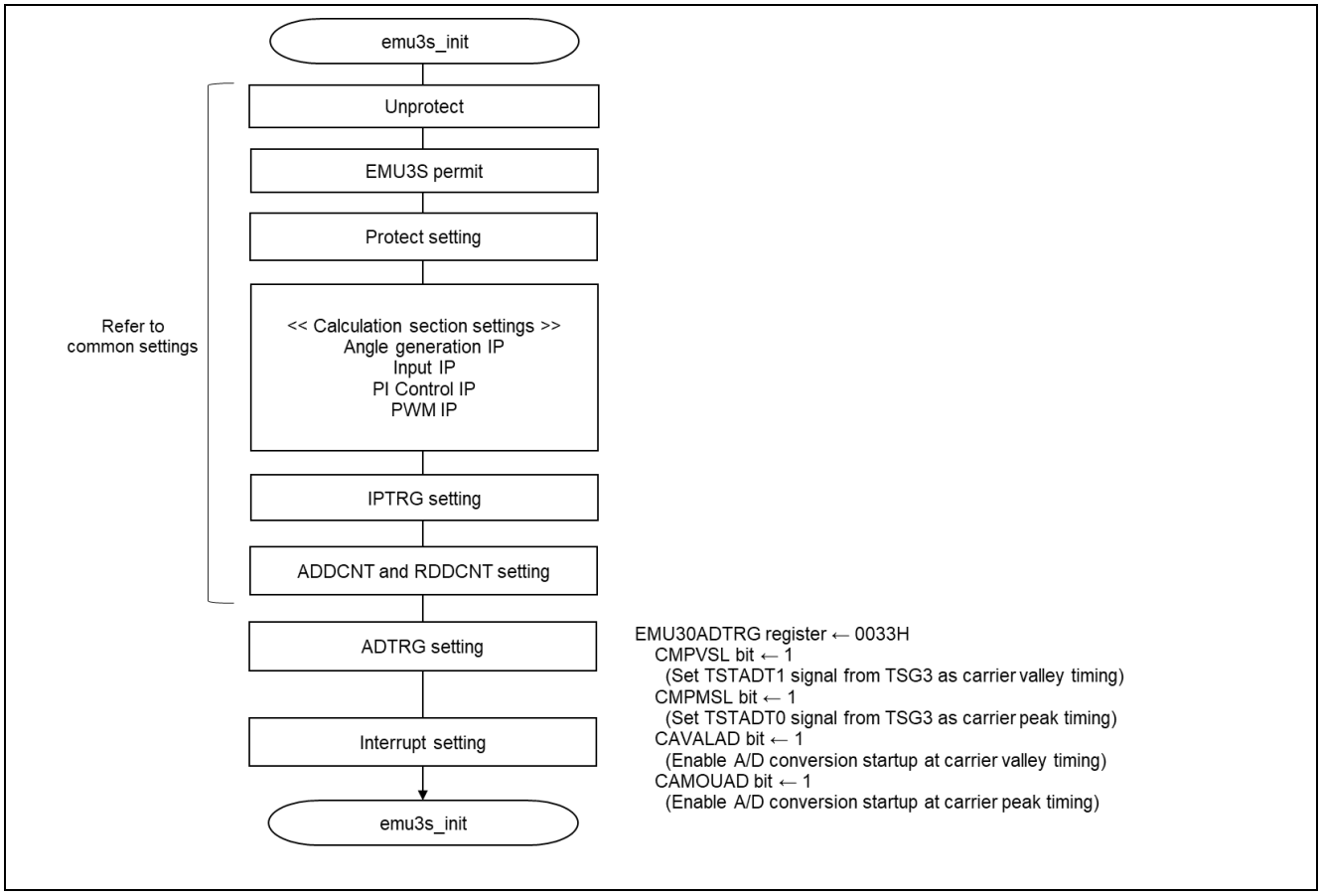

Figure 2-13 EMU3S operation flow

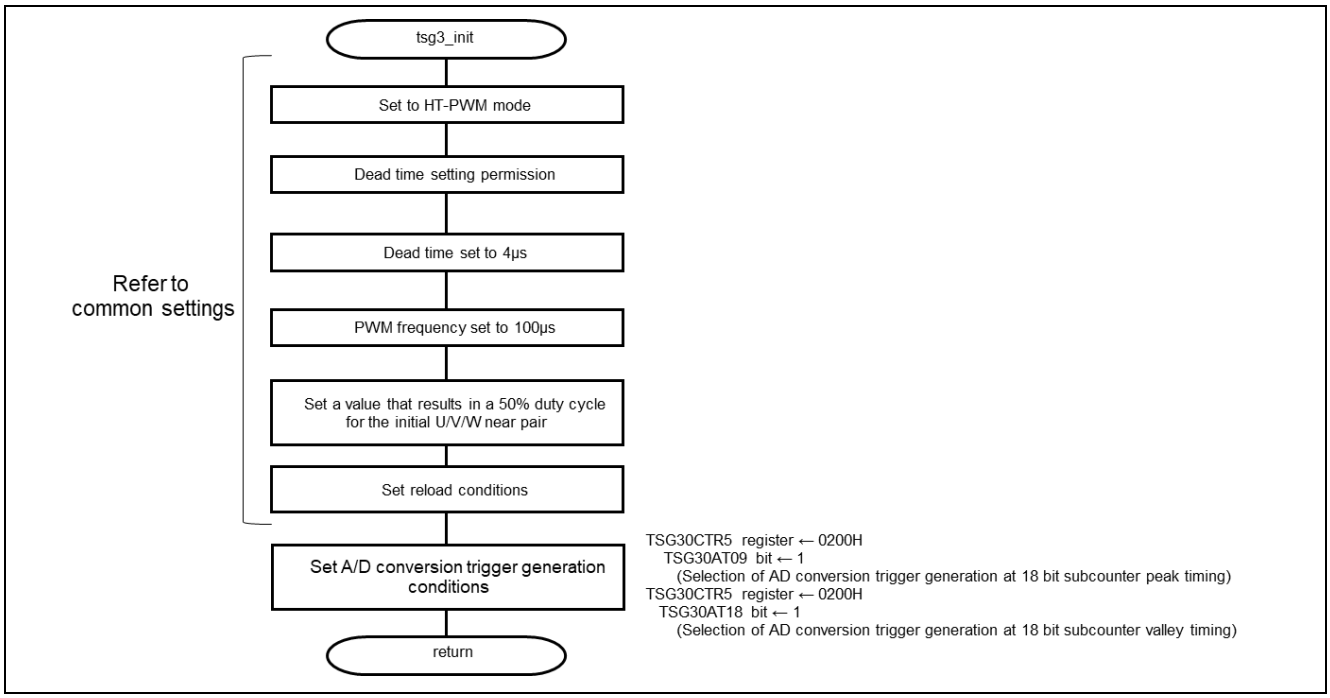

Figure 2-14 TSG3S operation flow

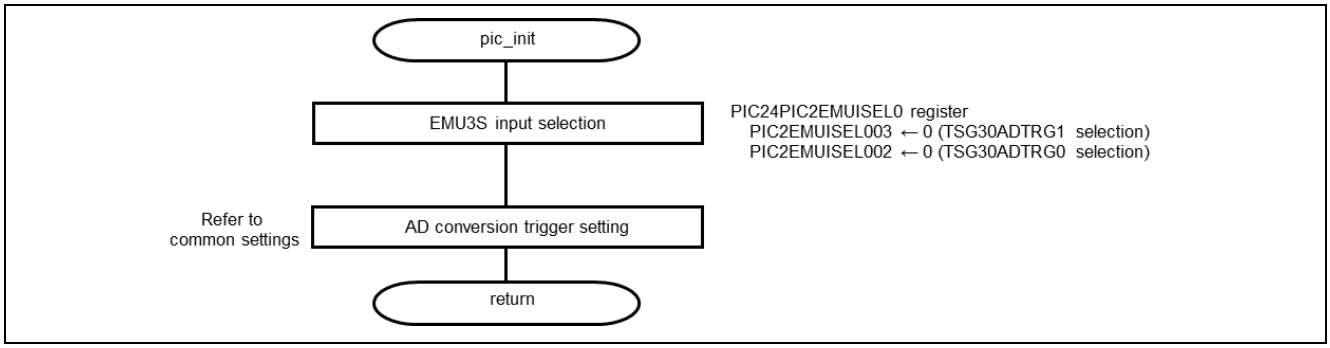

Figure 2-15 PIC operation flow

2.2.5 Software description

Table 2-8, Table 2-9, and Table 2-10 show examples of EMU3S, TSG3, and PIC register settings. Note that only the relevant portions are described here. For common settings, refer to 2.1.

Table 2-8 Example of EMU3S register setting (relevant part only)

Register name	Set value	Function
EMU30.ADTRG	0x0033H	CMPVSL = 1: Select TSTAD1 signal from TSG3 as carrier valley timing CMPMSL = 1: Select TSTAD0 signal from TSG3 as carrier peak timing CAVALAD = 1: A/D conversion start-up at carrier valley timing enabled CAMOUAD = 1: A/D conversion start-up at carrier peak timing enabled

Table 2-9 Example of TSG3 register setting (relevant part only)

Register name	Set value	Function
TSG30.CTL5	0x0200H	TSG3nAT09 = 1: Selection of A/D conversion trigger generation at sub-counter peak timing
TSG30.CTL6	0x0100H	TSG3nAT18 = 1: Selection of A/D conversion trigger generation at sub-counter valley timing

Table 2-10 Example of PIC register setting (relevant part only)

Register name	Set value	Function
PIC24.PIC2EMUISEL0	0x00000000H	PIC2EMUISEL003 = 0: Select TSG30ADTRG1 PIC2EMUISEL002 = 0: Select TSG30ADTRG0

2.3 Delay time setting to angle latch and current value latch of EMU3S

2.3.1 Specifications overview

Based on the A/D trigger generation method and operation example using TSG3 sub-counter described in 2.2 of EMU3S, this section further explains how to add delay time to A/D conversion trigger output and angle information acquisition.

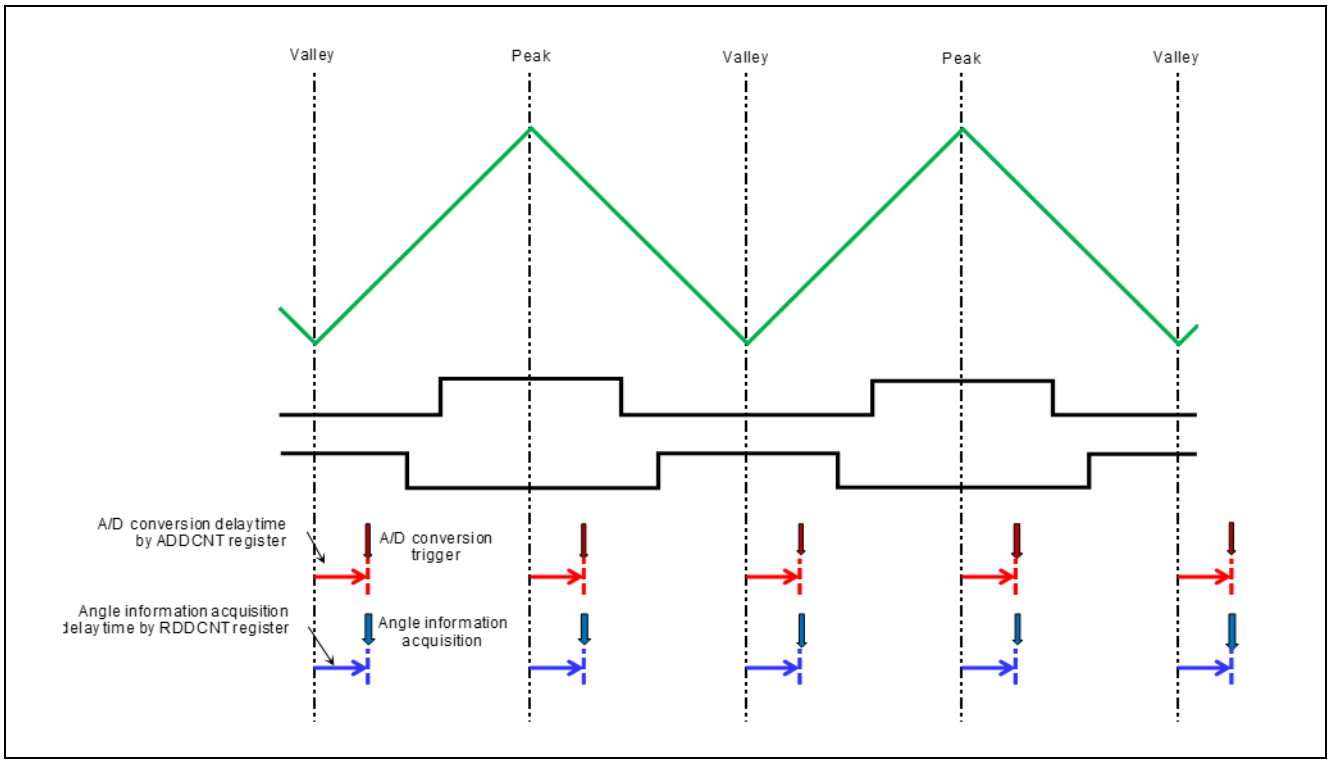

Figure 2-16 Operation overview

2.3.2 Operating conditions for specification functions

The following shows the operating conditions for the function to set the delay time for A/D conversion trigger output and angle information acquisition. Refer to 2.1 for common settings.

Table 2-11 Function used

Item	Contents
Function used	● A/D conversion function with timing of sub-counter peak and valley of carrier wave ● Trigger output delay of 10us for A/D conversion and R/D conversion

2.3.3 Operation description

EMU3S allows the user to set the delay time for the A/D conversion trigger synchronized with TSG3 PWM carrier and the latch of the angle value of the R/D conversion result. The A/D conversion trigger delay time is set in EMU3nADDCNT register. The delay time for acquiring angle information is also set in EMU3nRDDCNT register. Each delay time can be set individually. EMU3nADDCNT and EMU3nRDDCNT operate with 80-MHz CCLK. The count value is down-counted by 1 in synchronization with the clock, and a signal is output when the count value reaches 0x0000.

2.3.4 Operation flow

Figure 2-17 shows the EMU3S operational flow. For TSG3 and PIC flows, refer to 2.2.4, as the settings are the same as in 2.2.

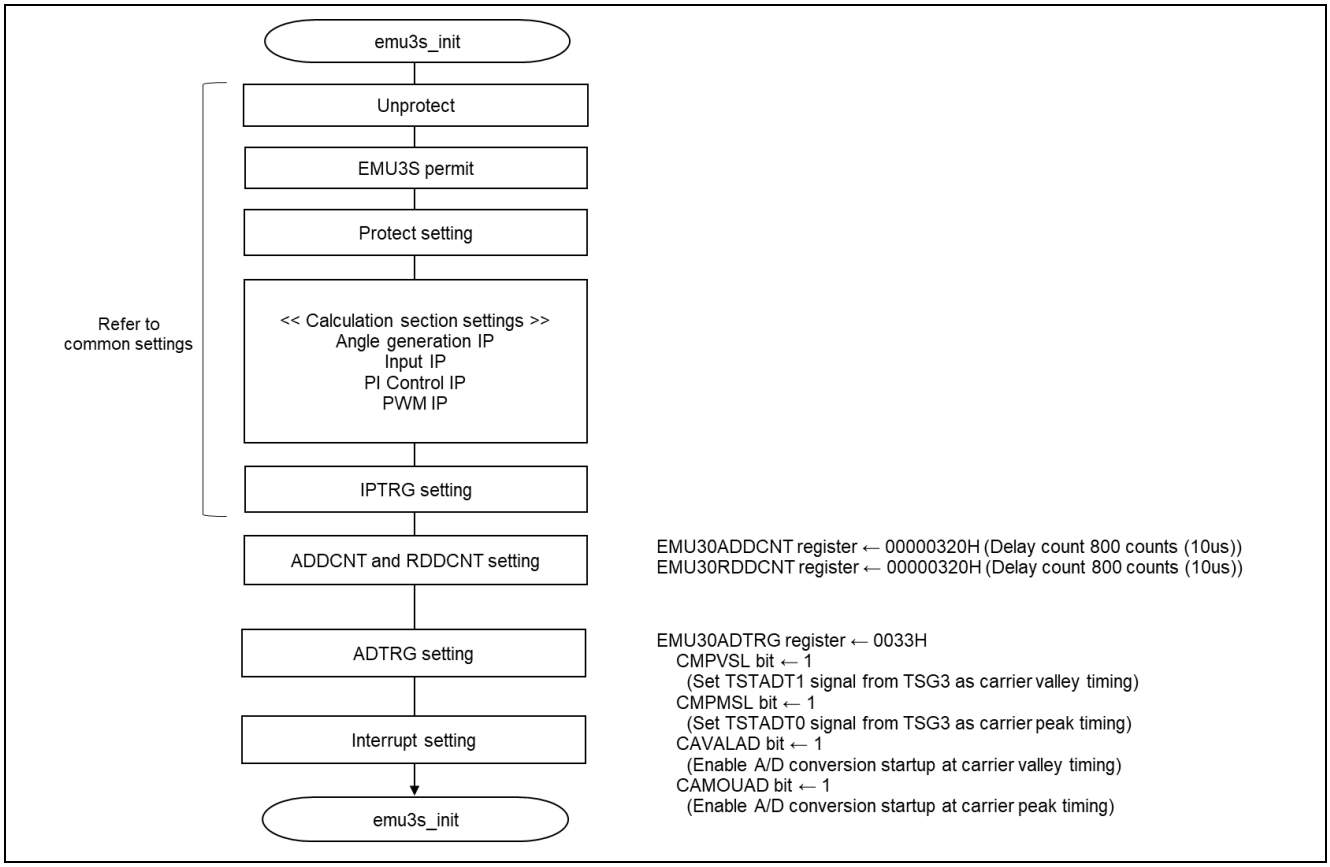

Figure 2-17 EMU3S operation flow

2.3.5 Software description

Table 2-12 shows an example of each register setting. Note that only the relevant parts are explained here. For common settings, refer to 2.1. Also, for TSG3 and PIC flows, refer to 2.2.5, as the settings are the same as in 2.2.

Table 2-12 Example of EMU3S register setting (relevant part only)

Register name	Set value	Function
EMU30.ADTRG	0x0033H	CMPVSL = 1: Select TSTAD1 signal from TSG3 as carrier valley timing CMPMSL = 1: Select TSTAD0 signal from TSG3 as carrier peak timing CAVALAD = 1: A/D conversion start-up at carrier valley timing enabled CAMOUAD = 1: A/D conversion start-up at carrier peak timing enabled
EMU30.ADDCNT	0x00000320H	A/D data acquisition delay count
EMU30.RDDCNT	0x00000320H	R/D angle information acquisition delay count

2.4 Multiple A/D conversion trigger generation and batch value acquisition in a carrier half cycle

2.4.1 Specifications overview

EMU3S can output multiple A/D conversion requests within one carrier in synchronization with the carrier managed by TSG3. In addition, EMU3S 's memory transfer function can be used to automatically transfer the conversion results output by ADCK to a user-specified area in response to an A/D conversion request that is generated. This application note describes multiple A/D conversion request outputs from EMU3S within one carrier and transfer of conversion results to memory. In this application note, the destination memory is assumed to be Cluster RAM (Cluster0).

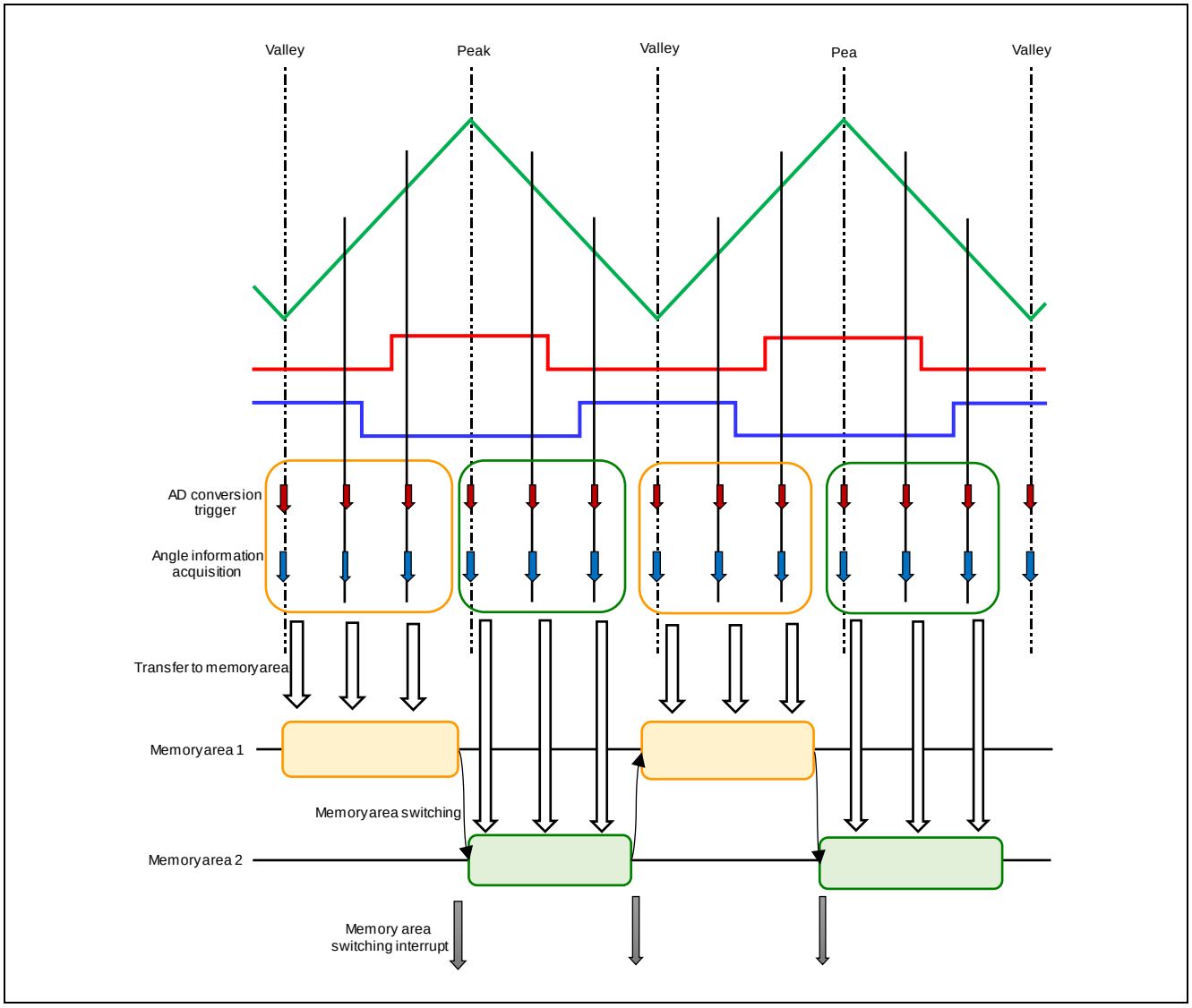

Figure 2-18 Operation overview

2.4.2 Operating conditions for specification functions

The operating conditions for the function of generating multiple A/D conversion triggers & batch acquisition of values in a carrier half cycle are shown below. For common settings, refer to 2.1.

Table 2-13 Function used

Item	Contents
Function used	● A/D conversion function with peak and valley timing of carrier wave sub-counters ● No trigger output delay for A/D conversion and R/D conversion ● Three A/D conversions at peak and valley timing ● No offset time for A/D conversion trigger ● Three memory transfer times ● Forwarded to ClusterRAM0 (0xFE001000) ● Transfer Completion Interrupt Setting

2.4.3 Operation description

In EMU3S, the EMU3nADSMTRG register can be used to set the number of A/D conversion trigger outputs and sampling interval starting from the A/D conversion trigger from TSG3. The EMU3nADSMOFS register can also be used to set the delay time for the starting A/D conversion trigger. The sampling interval and delay time operate at 80-MHz CLKC_HSB.

EMU3S also has a memory transfer function that can transfer the A/D conversion result and angle information to memory when triggered by the A/D conversion completion signal. The angle information to be transferred can be selected between resolver angle information and electric angle information by THTSEL bit of EMU3nADMWCTR register. The memory transfer function is enabled with EMU3nADMWCTR register. The number of memory transfers is set by EMU3nADMNCNT register, and the memory transfer destination is set by EMU3nTBLADR register and EMU3nADMOFS2 register. The memory is divided into Area 1 and Area 2, which are automatically switched at the timing of the carrier peak and valley. Figure 2-19 shows an example of memory area settings.

For the memory transfer function, an interrupt signal can be generated at the timing when a transfer occurs for the count set in the EMU3nADMNCNT register. The interrupt factor is assigned to the SMBIF bit of the EMU3nINTSD register.

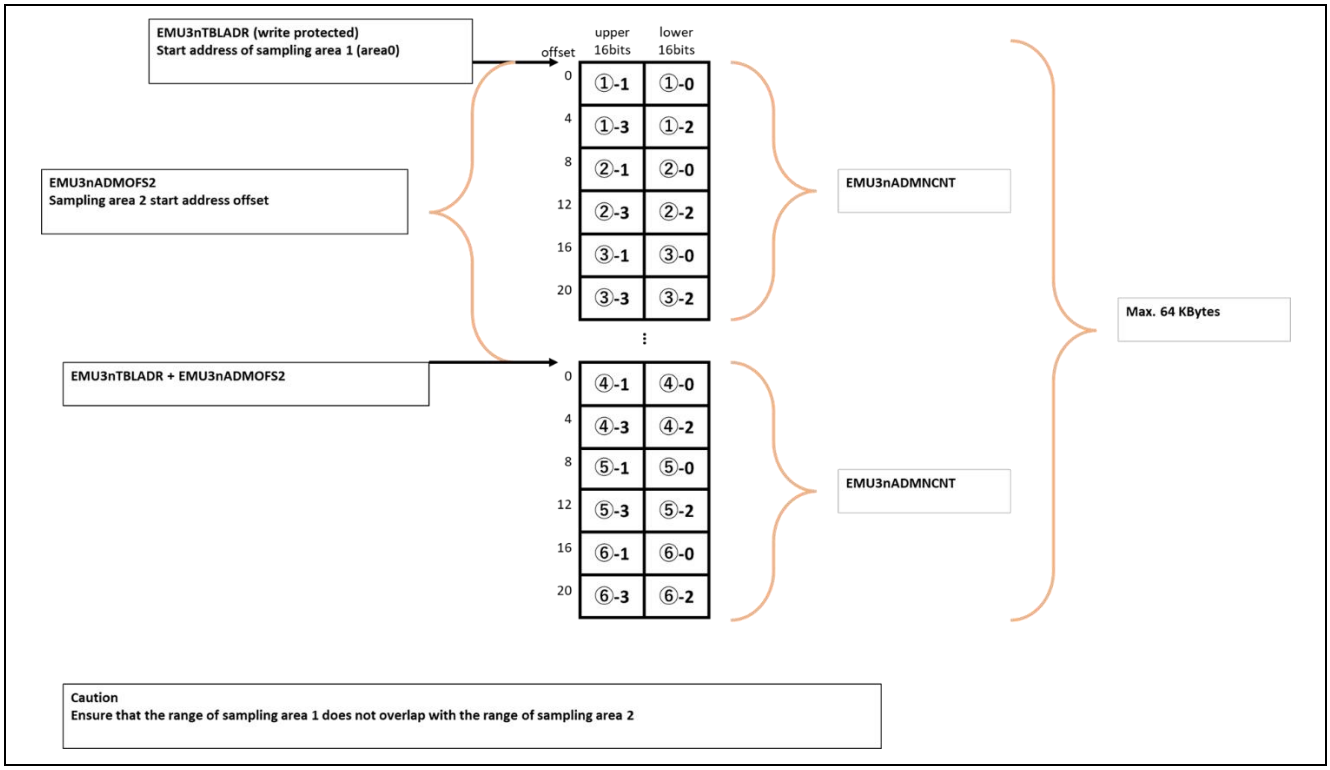

Figure 2-19 Example of memory area setting

2.4.4 Operation flow

Figure 2-20 shows the operation flow. Figure 2-21 shows the interrupt control flow.

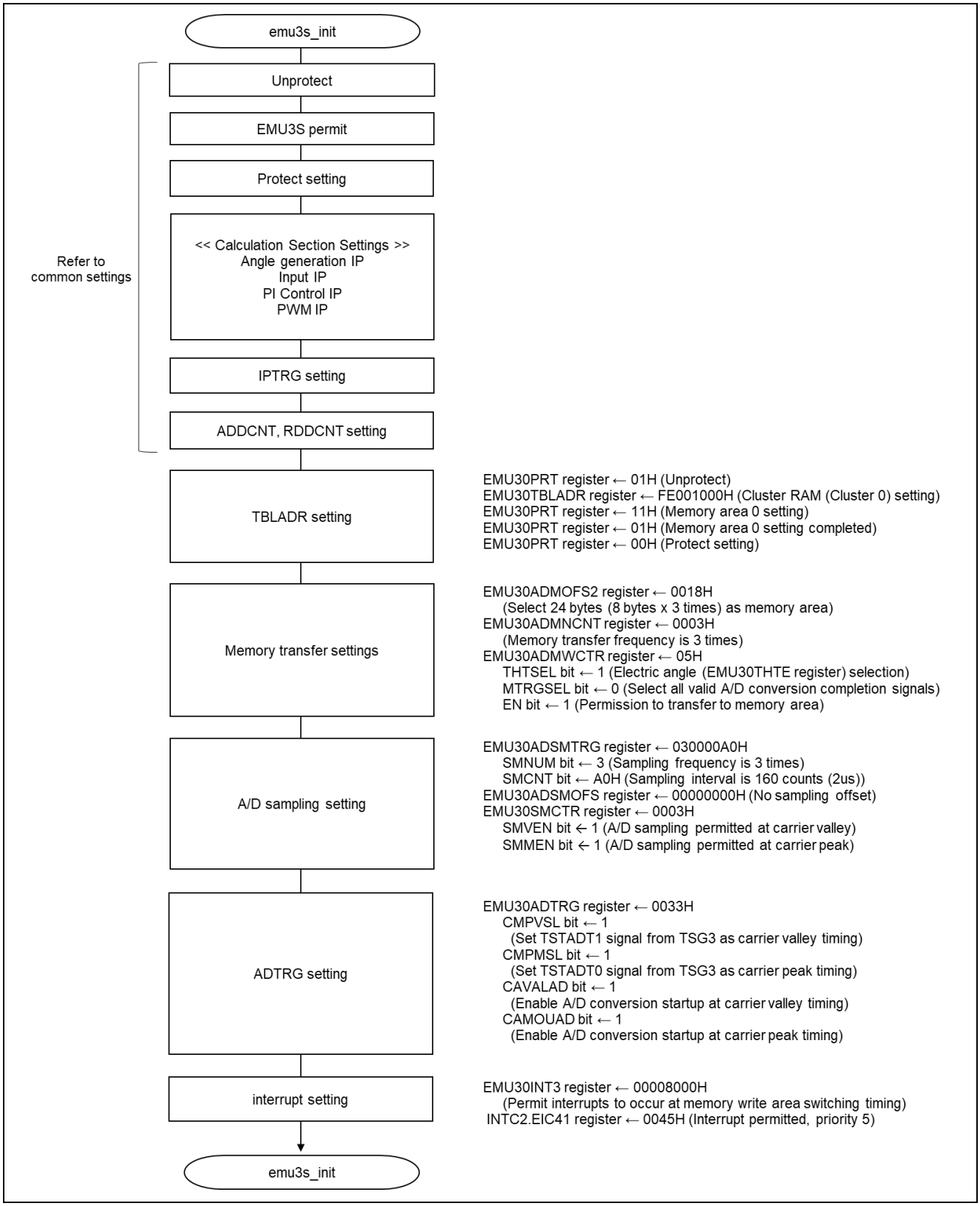

Figure 2-20 Operation flow

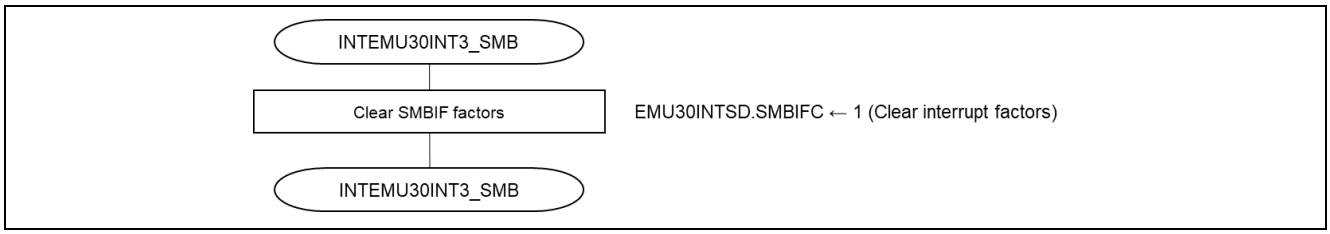

Figure 2-21 Interrupt control flow

2.4.5 Software description

Table 2-14 shows an example of each register setting.

Table 2-14 Example of EMU3S register setting (relevant part only)

Register name	Set value	Function
EMU30.SMCTR	0x0003H	SMVEN = 1: A/D conversion sampling permission at carrier valley SMMEN = 1: A/D conversion sampling permission at carrier peak
EMU30.ADSMTRG	0x030000A0H	SMNUM = 3: A/D conversion sampling frequency 3 times SMCNT = 160: A/D conversion request output sampling interval setting
EMU30.ADSMOFS	0x00000000H	SMOFS = 0: No offset time
EMU30.ADMWCTR	0x05	THTSEL = 1: Latch to memory area selects electric angle (EMU3nTHTE) MTRGSEL = 0: Set all valid A/D conversion completion signals EN = 1: Permission to transfer to memory area
EMU30.TBLADR	0xFE001000H	DATA = 0xFE001000: Set Cluster RAM (Cluster0)
EMU30.ADMOFS2	0x0018H	24 bytes set as memory area territory
EMU30.ADMNCNT	0x0003H	Memory write count 3
EMU30.INT3	0x00008000H	Allow interrupts to occur at memory write area switching timing
INTC2.EIC41	0x0045H	Interrupt permitted, priority 5

2.5 Interrupt thinning function for peak and valley and setting the number of thinnings

2.5.1 Specifications overview

EMU3S allows interrupt thinning for interrupt requests at the carrier peak and valley in conjunction with the TSG3. This section describes interrupt thinning at the carrier peak and valley timing using the interrupt thinning function.

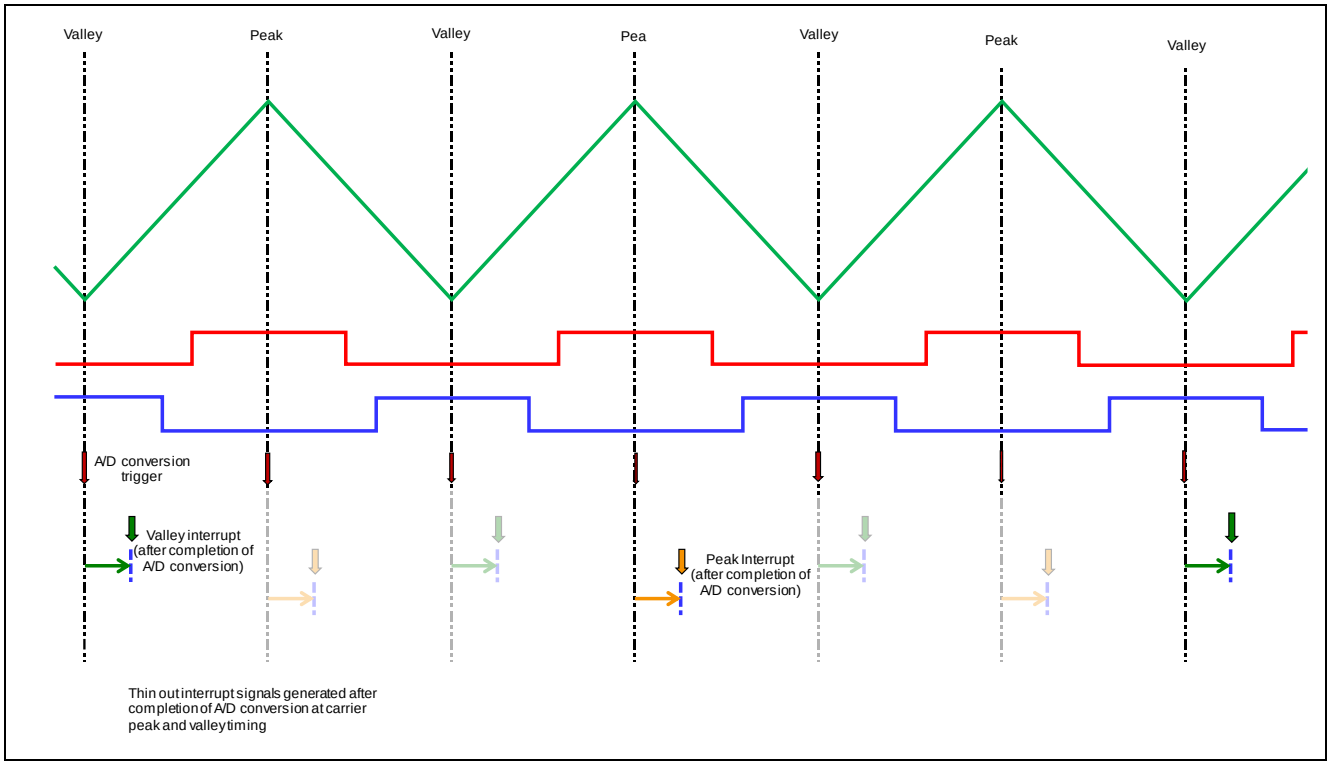

Figure 2-22 Operation overview

2.5.2 Operating conditions for specification functions

Below are the operating conditions for the carrier peak and valley timing interrupt thinning function. See 2.1 for common settings.

Table 2-15 Function used

Item	Contents
Function used	● A/D conversion trigger output at the timing of sub-counter peak and valley of carrier wave ● Interrupt occurs upon completion of A/D conversion ● Interrupt count setting (2 times)

2.5.3 Operation description

Interrupt thinning synchronized to the carrier peak and valley can be set in conjunction with the A/D conversion request trigger setting. EMU3nTRGGCM register specifies the A/D conversion completion signal thinning setting and the number of thinning times. The A/D conversion completion signal after thinning out is then utilized as an interrupt signal.

2.5.4 Operation flow

Figure 2-23 shows the operation flow. Figure 2-24 shows the interrupt control flow.

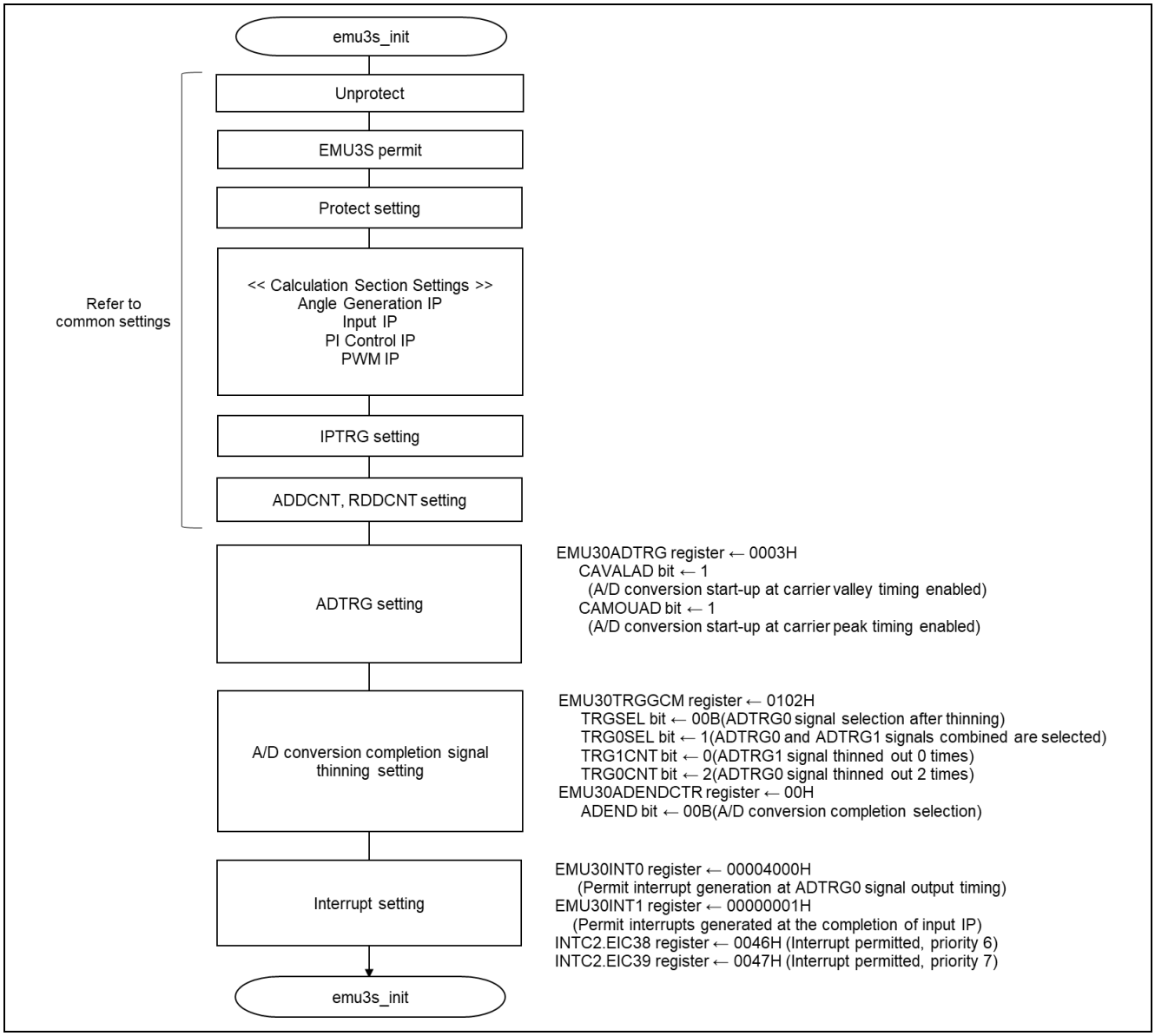

Figure 2-23 Operation flow

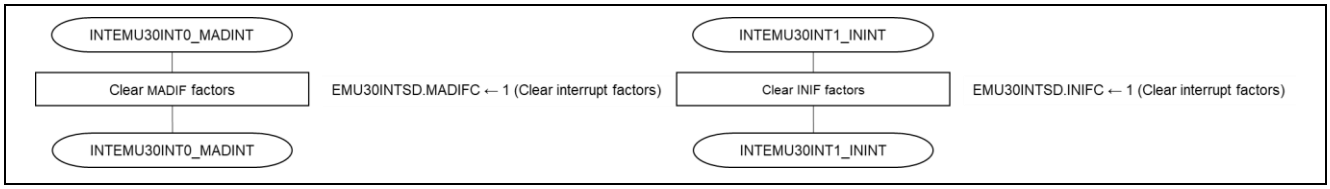

Figure 2-24 Interrupt control flow

2.5.5 Software description

Table 2-16 shows an example of each register setting. Note that only the relevant parts are explained here. For common settings, refer to 2.1.

Table 2-16 Example of EMU3S register setting (relevant part only)

Register name	Set value	Function
EMU30.TRGGCM	0x0102H	TRGSEL = 0: Select ADTRG0 signal after thinning out as the input IP start-up trigger TRG0SEL = 1: ADTRG0 and ADTRG1 signals are combined as ADTRG0 signal TRG1CNT = 0: ADTRG1 signal thinned out 0 times TRG0CNT = 2: ADTRG0 signal thinned out 2 times
EMU30.ADENDCTR	0x00H	ADEND = 0: Set A/D conversion completion timing to A/D conversion completion
EMU30.INT0	0x00004000H	Allow interrupts to be generated at ADTRG0 signal output timing
EMU30.INT1	0x00000001H	Allow interrupts to be generated at the input IP completion timing
INTC2.EIC38	0x0046H	Interrupt permitted, priority 6
INTC2.EIC39	0x0047H	Interrupt permitted, priority 7

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2022.01.01		First Edition
1.01	2023.05.18	8	ADC virtual CH setting value correction

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

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1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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