RH850/U2B6

DTS usage example

Introduction

This application note describes a setting example of the DTS function of the RH850 / U2B6.

Although the task examples and application examples described in this application note have been confirmed to work, please be sure to check the operating environment before using them.

Target Device

This application note applies to RH850/U2B6

Contents

1. Introduction 2

2. DMA transfer (DTS, Software reqest mode) 3

2.1 Overview 3

2.2 Operating conditions of the function used 3

2.3 Operation 4

2.4 Description of Software 5

2.5 Operation Flow 9

3. DMA transfer (DTS, Software reqest mode) 10

3.1 Overview 10

3.2 Operating conditions of the function used 10

3.3 Operation 11

3.4 Discription of Software 12

3.5 Operation Flow 16

Revision History 17

1. Introduction

This application note describes how to use the DMA function of the RH850 and an example of creating firmware.

The following usage is explained.

-DMA transfer using DTS (software factor)

-DMA transfer using DTS (hardware factor)

2. DMA transfer (DTS, Software reqest mode)

2.1 Overview

This chapter describes the method of performing DMA transfer by software transfer request among the DTS functions.
This operation example shows a method of periodically setting a DMA software transfer request and performing DMA transfer by DTS a specified number of times using the single transfer mode.

2.2 Operating conditions of the function used

The operating conditions of the functions used in this operation example are shown below.

Table 2-1 DMA setting

Item	Description
Channel	DTS CH0
Transfer mode	Single transfer
Trandfer trigger	Software DMA transfer reqests
Transfer cycle	50 cycles

Table 2-2 TAUD setting

Item	Description
Channel	TAUD0 CH0
Feature to be used	Interval timer
Clock supplied to TAUD	PLL output clock (80MHz)
Timer operation clock	Prescaler output CK0 = 80MHz / 1
Timer counter	0xFFFF

2.3 Operation

This operation example shows how to perform DTS transfer due to software factors.

In this operation example, the timer count value of TAUD0CNT0 is read in the main processing loop, and the timer count value read by DMA transfer by DTS is transferred to another RAM. DMA transfer is performed by setting a DTS FSL transfer request.

The transfer request is made every cycle, but when the number of transfers n (50 in this operation example) is reached, the software transfer request does not occur after that.

Figure 2-1 shows an operation example.

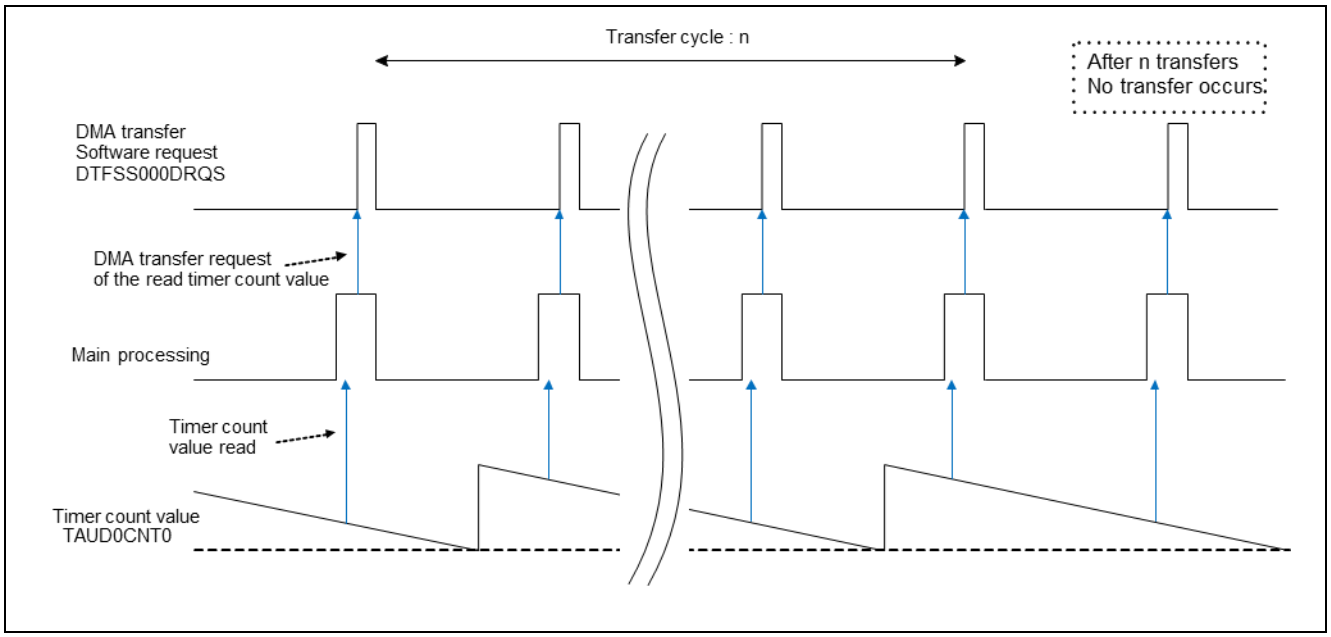

Figure 2-1 Example of Operation

2.4 Description of Software

Table 2-3 to Table 2-4 show setting examples of each register used in this operation example.

Table 2-3 Example of DTS Register Settings

Register Name	Address	Set Value	Description
DTS channel priority setting register (DTSPR0~DTSPR7)	0xFFF88060-0xFFF8807C	0x00000000	DTS channel priority setting register. DTSnPR[1:0] 0x0: Initial value (0: highest, 3: lowest) *n=0-127
DTS channel master setting register (DTS000CM)	0xFFF88200	0x00000000	Defide the channel master configuration foreach DTS (Not used chain function). SPID[1:0] 0x0: SPID=0 UM 0x0: superviser mode CMC[15:0] 0x0: Transfer count compare 0 (Not used)
DTSFSL operation setting register (DTFSL000)	0xFFF89020	REQEN: 0x0 REQEN: 0x1	Control the DTS transfer request of each channel. REQEN 0x0: The DTS transfer request is not used as a candidate for DTS channel arbitration. 0x1: The DTS transfer request is used as a candidate for DTS channel arbitration.
DTS source address register (DTSA000)	0xFFF89000	SA: &source_data	Specifies the DTS transfer source address of each channel.
DTS destination address register (DTDA000)	0xFFF89004	DA: &dest_data[0]	Specifies the DTS transfer destination address of each channel.
DTS transfer count register (DTTC000)	0xFFF89008	0x00000032	Specifies the DTS transfer count of each channel. ARC[15:0] 0x0: initial value (Disabale address reload function) TRC[15:0] 0x0032: 50 cycles

Register Name	Address	Set Value	Description
DTS transfer control register (DTTCT000)	0xFFF8900C	0x08000044	Define DTS transfer control configuration of the channel. ESE 0x1: DTS transfer is aborted when a DTS transfer error occurs. CHNSEL[6:0] 0x0: initial value (Disable chain function). CHNE[1:0] 0x0: Disable chain function. CCE 0x0: Disable transfer count match interrupt. TCE 0x0: Disable transfer end interrupt. RLD2M[1:0] 0x0: Reload function 2 is disable. RLD1M[1:0] 0x0: Reload function 1 is disable. DACM[1:0] 0x0: Destination address count is increment. SACM[1:0] 0x2: Sorce address count is fixed. DS[2:0] 0x1: Transfer data size is 16-bit. TRM[1:0] 0x0: Single transfer.
DTS reload source address register (DTRSA000)	0xFFF89010	RSA: 0x00000000	Specifies the DTS reload source address of each channel. RSA[31:0] 0x00000000: initial value (Disable address reload function).
DTS reload destination address register (DTRDA000)	0xFFF89014	RDA: 0x00000000	Specifies the DTS reload destination address of each channel. RDA[31:0] 0x00000000: Initial value (Disable address reload function).
DTS reload transfer count register (DTRTC000)	0xFFF89018	0x00000000	Specifies the DTS reload transfer count of eath channel. RARC[15:0] 0x0000: Initial value (Disable address reload function). RTRC[15:0] 0x0000: Initial value (Disable address reload function).
DTS transfer count compare regiater (DTTCC000)	0xFFF8901C	CMC: 0x00000000	Configure the transfer count to be compared to transfer count register. CMC[15:0] 0x0000: initial value (Disable transfer count match interrupt)
DTS transfer status clear register (DTFSC000)	0xFFF8902C	0x000000B3	Clear the status flag bits in the DTFSTnnn register. DRQC 0x1: Transfer request clear. TCC 0x1: Transfer end flag clear. CCC 0x1: Transfer count match flag clear ERC 0x1: Transfer error flag clear.
DTSFSL Transfer request set register (DTFSS000)	0xFFF89028	DRQS: 0x00000001	DTS transfer request set. DRQS 0x1: Generate a DTS transfer request.

Table 2-4 Example of TAUD register settings

Register Name	Address	Set Value	Descriiption
TAUD0 channel stop trigger register (TAUD0TT)	0xFFBF01C8	0x0001	This register stops counter operation of each channel. TAUD0TT15-02 0x0: No operation TAUD0TT01-00 0x1: Counter operation is stopped.
TAUD0 prescaler clock select register (TAUD0TPS)	0xFFBF0240	0x0000	This register specifies CK0, CK1, CK2, and CK3_PRE clocks of all channels of the PCLK prescaler. TAUD0PRS3-0[3:0] 0x0: PCLK/2^0
TAUD0 prescaler baud rate settting register (TAUD0BRS)	0xFFBF0244	0x4F	Specifies the division factor of prescaler clock CK3. TAUD0BRS[7:0] 0x50: CK3_PRE/80
TAUD0 channel mode OS register (TAUD0CMOR0)	0xFFBF0200	0xC000	This register controls operation of Channel 0. TAUD0CKS[1:0] 0x2: Operation clock CK3 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm. TAUD0MAS 0x1: Master channel TAUD0STS[2:0] 0x0: Software trigger. TAUD0MD[4:0] 0x0: Interval timer mode INTTAUDnIm is not output when count operation starts.
TAUD0 Chanel data register (TAUD0CDR0)	0xFFBF0000	2710	Initial down-count value of TAUD0CNT0
TAUD0 Channel start trigger register (TAUD0TS)	0xFFBF01C4	0x0001	Enable counter operation of each channels. TAUD0TS15-01 0x0: No operation. TAUD0TS00 0x1: Counter operation is enabled.

Table 2-5 to Table 2-6 show a list of functions, variables, and constants used in this operation example.

Table 2-5 List of Functions

Function Name	Description
pe0_main	Calls each function.
dts_init	Makes initial setting for DTS.
taud_init	Makes initial setting for TAUD0.
wait_mainloop	Wait for DMA transfer process.
dma_transfer	DMA transfer process.

Table 2-6 List of Variables

Variable Name	Description
source_data	Source data for DMA transfer.
dest_data[50]	RAM area of DMA transfer destination.

2.5 Operation Flow

Figure 2-2 shows the operation flow of this operation example.

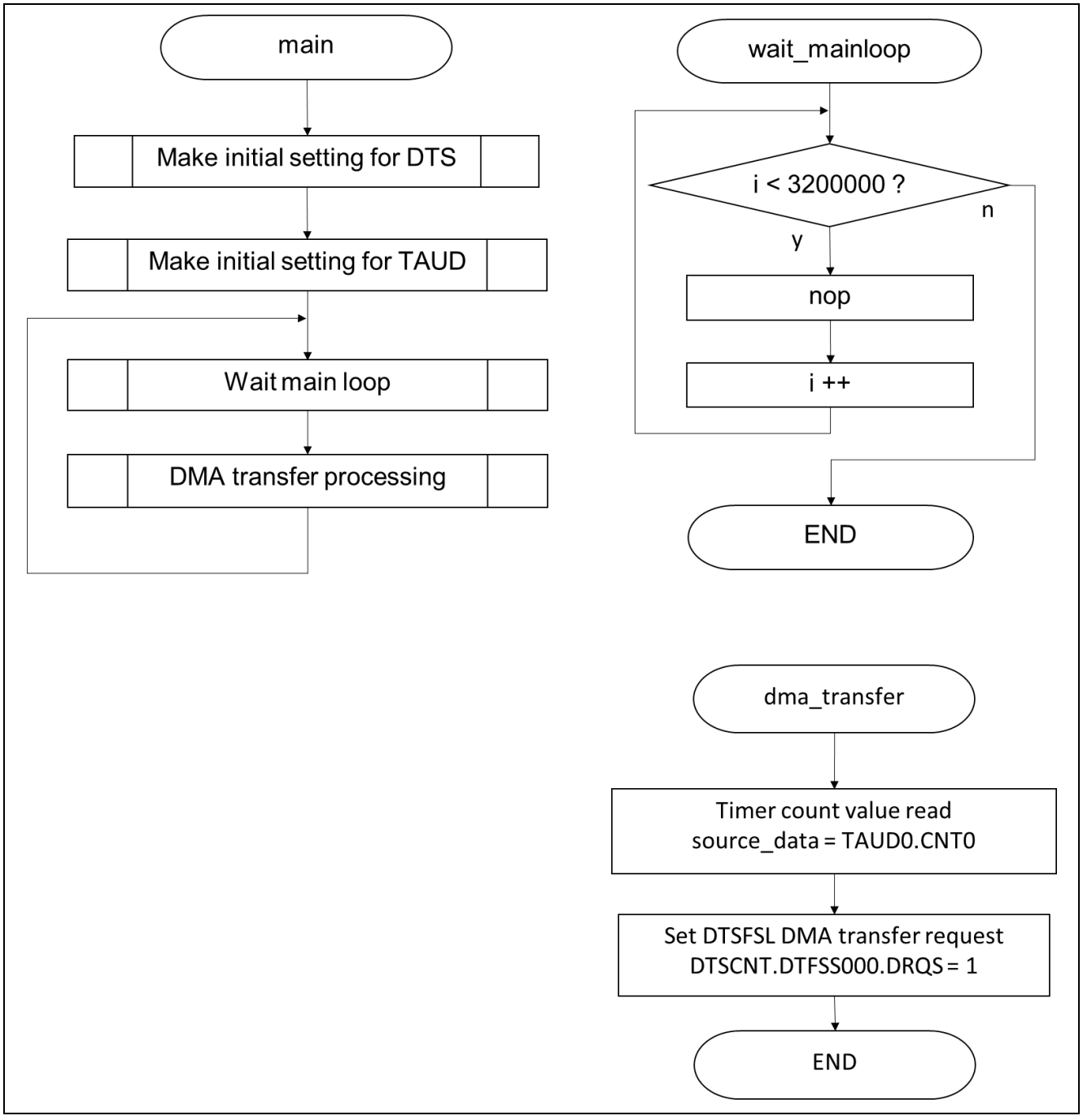

Figure 2-2 Operation Flow

3. DMA transfer (DTS, Software reqest mode)

3.1 Overview

This chapter describes how to use DTS hardware DMA transfer requests to perform DMA transfers.

In this operation example, INTTAUD0I0 interrupt is used to generate a hardware DMA transfer factor.

3.2 Operating conditions of the function used

The operating conditions of the functions used in this operation example are shown below.

Table 3-1 DMA settings

Item	Description
Channel	DTS CH065
Transfer mode	Block transfer 1
Transfer trigger	Hardware

Table 3-2 TAUD settings

Item	Description
Feature to be used	Interval timer
Clock supplied to TAUD	PLL output clock (80MHz)
Timer operation clock	Prescaler output CK3 = 80MHz / 8

3.3 Operation

In this operation example, 256 bytes of ROM data is transferred to the RAM area every time the 10 ms interval timer expires.

Figure 3-1 illustrates an operation example of a hardware DMA transfer request.

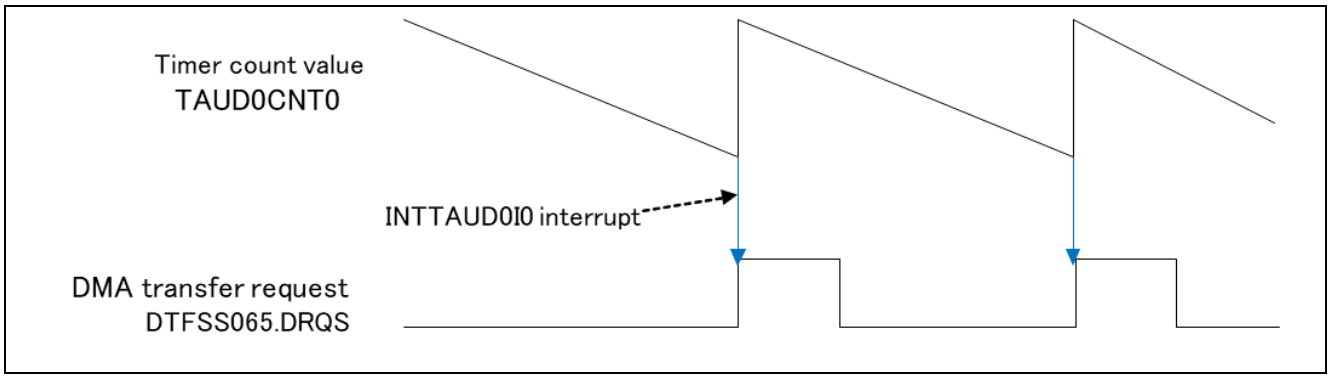

Figure 3-1 Example of Operation

Table 3-3 shows the ROM data used in this operation example.

Table 3-3 ROM data of DTS transfer

ROM data
0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08, 0x09, 0x0A, 0x0B, 0x0C, 0x0D, 0x0E, 0x0F, 0x10, 0x11, 0x12, 0x13, 0x14, 0x15, 0x16, 0x17, 0x18, 0x19, 0x1A, 0x1B, 0x1C, 0x1D, 0x1E, 0x1F, 0x20, 0x21, 0x22, 0x23, 0x24, 0x25, 0x26, 0x27, 0x28, 0x29, 0x2A, 0x2B, 0x2C, 0x2D, 0x2E, 0x2F, 0x30, 0x31, 0x32, 0x33, 0x34, 0x35, 0x36, 0x37, 0x38, 0x39, 0x3A, 0x3B, 0x3C, 0x3D, 0x3E, 0x3F, 0x40, 0x41, 0x42, 0x43, 0x44, 0x45, 0x46, 0x47, 0x48, 0x49, 0x4A, 0x4B, 0x4C, 0x4D, 0x4E, 0x4F, 0x50, 0x51, 0x52, 0x53, 0x54, 0x55, 0x56, 0x57, 0x58, 0x59, 0x5A, 0x5B, 0x5C, 0x5D, 0x5E, 0x5F, 0x60, 0x61, 0x62, 0x63, 0x64, 0x65, 0x66, 0x67, 0x68, 0x69, 0x6A, 0x6B, 0x6C, 0x6D, 0x6E, 0x6F, 0x70, 0x71, 0x72, 0x73, 0x74, 0x75, 0x76, 0x77, 0x78, 0x79, 0x7A, 0x7B, 0x7C, 0x7D, 0x7E, 0x7F, 0x80, 0x81, 0x82, 0x83, 0x84, 0x85, 0x86, 0x87, 0x88, 0x89, 0x8A, 0x8B, 0x8C, 0x8D, 0x8E, 0x8F, 0x90, 0x91, 0x92, 0x93, 0x94, 0x95, 0x96, 0x97, 0x98, 0x99, 0x9A, 0x9B, 0x9C, 0x9D, 0x9E, 0x9F, 0xA0, 0xA1, 0xA2, 0xA3, 0xA4, 0xA5, 0xA6, 0xA7, 0xA8, 0xA9, 0xAA, 0xAB, 0xAC, 0xAD, 0xAE, 0xAF, 0xB0, 0xB1, 0xB2, 0xB3, 0xB4, 0xB5, 0xB6, 0xB7, 0xB8, 0xB9, 0xBA, 0xBB, 0xBC, 0xBD, 0xBE, 0xBF, 0xC0, 0xC1, 0xC2, 0xC3, 0xC4, 0xC5, 0xC6, 0xC7, 0xC8, 0xC9, 0xCA, 0xCB, 0xCC, 0xCD, 0xCE, 0xCF, 0xD0, 0xD1, 0xD2, 0xD3, 0xD4, 0xD5, 0xD6, 0xD7, 0xD8, 0xD9, 0xDA, 0xDB, 0xDC, 0xDD, 0xDE, 0xDF, 0xE0, 0xE1, 0xE2, 0xE3, 0xE4, 0xE5, 0xE6, 0xE7, 0xE8, 0xE9, 0xEA, 0xEB, 0xEC, 0xED, 0xEE, 0xEF, 0xF0, 0xF1, 0xF2, 0xF3, 0xF4, 0xF5, 0xF6, 0xF7, 0xF8, 0xF9, 0xFA, 0xFB, 0xFC, 0xFD, 0xFE, 0xFF

3.4 Discription of Software

Table 3-4 to Table 3-5 show setting examples of each register used in this operation example.

Table 3-4 Example of DTS register settings

Register Name	Address	Set Value	Description
DTS transfer request group select register (DTSSEL8)	0xFF096620	0x00000030	Specifies the DTS transfer request group for each channel. ch65 = group3
DTS channel priority setting register (DTSPR0~DTSPR7)	0xFFF88060- 0xFFF8807C	0x00000000	DTS channel priority setting register. DTSnPR[1:0] 0x0: Initial value (0: highest, 3: lowest) ∗n=0-127
DTS channel master setting register (DTS065CM)	0xFFF88304	0x00000000	Defide the channel master configuration foreach DTS (Not used chain function). SPID[1:0] 0x0: SPID=0 UM 0x0: superviser mode CMC[15:0] 0x0: Transfer count compare 0 (Not used)
DTSFSL operation setting register (DTFSL065)	0xFFF89124	REQEN: 0x0 REQEN: 0x1	Control the DTS transfer request of each channel. REQEN 0x0: The DTS transfer request is not used as a candidate for DTS channel arbitration. 0x1: The DTS transfer request is used as a candidate for DTS channel arbitration.
DTS source address register (DTSA000)	0xFFF895C4	SA: &source_data_table[0]	Specifies the DTS transfer source address of each channel.
DTS destination address register (DTDA065)	0xFFF895C8	DA: &dest_data[0]	Specifies the DTS transfer destination address of each channel.
DTS transfer count register (DTTC065)	0xFFF895CC	0x00000100	Specifies the DTS transfer count of each channel. ARC[15:0] 0x0: initial value (Disabale address reload function) TRC[15:0] 0x00100: 256 cycles

Register Name	Address	Set Value	Description
DTS transfer control register (DTTCT065)	0xFFF895D0	0x08000001	Define DTS transfer control configuration of the channel. ESE 0x1: DTS transfer is aborted when a DTS transfer error occurs. CHNSEL[6:0] 0x0: initial value (Disable chain function). CHNE[1:0] 0x0: Disable chain function. CCE 0x0: Disable transfer count match interrupt. TCE 0x0: Disable transfer end interrupt. RLD2M[1:0] 0x0: Reload function 2 is disable. RLD1M[1:0] 0x0: Reload function 1 is disable. DACM[1:0] 0x0: Destination address count is increment. SACM[1:0] 0x2: Sorce address count is increment. DS[2:0] 0x0: Transfer data size is 8-bit. TRM[1:0] 0x1: Block transfer 1.
DTS reload source address register (DTRSA065)	0xFFF895D4	RSA : 0x00000000	Specifies the DTS reload source address of each channel. RSA[31:0] 0x00000000: initial value (Disable address reload function).
DTS reload destination address register (DTRDA065)	0xFFF895D8	RDA : 0x00000000	Specifies the DTS reload destination address of each channel. RDA[31:0] 0x00000000: Initial value (Disable address reload function).
DTS reload transfer count register (DTRTC065)	0xFFF895DC	0x00000000	Specifies the DTS reload transfer count of eath channel. RARC[15:0] 0x0000: Initial value (Disable address reload function). RTRC[15:0] 0x0000: Initial value (Disable address reload function).
DTS transfer count compare regiater (DTTCC065)	0xFFF895E0	CMC : 0x00000000	Configure the transfer count to be compared to transfer count register. CMC[15:0] 0x0000: initial value(Disable transfer count match interrupt)
DTS transfer status clear register (DTFSC065)	0xFFF89130	0x000000B3	Clear the status flag bits in the DTFSTnnn register. DRQC 0x1: Transfer request clear. TCC 0x1: Transfer end flag clear. CCC 0x1: Transfer count match flag clear ERC 0x1: Transfer error flag clear.

Table 3-5 Example of TAUD register settings

Register Name	Address	Set Value	Description
TAUD0 channel stop trigger register (TAUD0TT)	0xFFBF01C8	0x0001	This register stops counter operation of each channel. TAUD0TT15-02 0x0: No operation TAUD0TT01-00 0x1: Counter operation is stopped.
TAUD0 prescaler clock select register (TAUD0TPS)	0xFFBF0240	0x0000	This register specifies CK0, CK1, CK2, and CK3_PRE clocks of all channels of the PCLK prescaler. TAUD0PRS3-0[3:0] 0x0: PCLK/2^0
TAUD0 prescaler baud rate settting register (TAUD0BRS)	0xFFBF0244	0x4F	Specifies the division factor of prescaler clock CK3. TAUD0BRS[7:0] 0x50: CK3_PRE/80
TAUD0 channel mode OS register (TAUD0CMOR0)	0xFFBF0200	0xC000	This register controls operation of Channel 0. TAUD0CKS[1:0] 0x2: Operation clock CK3 TAUD0CCS[1:0] 0x0: Operation clock specified by TAUDnCKS[1:0] in TAUDnCMORm. TAUD0MAS 0x1: Master channel TAUD0STS[2:0] 0x0: Software trigger. TAUD0MD[4:0] 0x0: Interval timer mode INTTAUDnIm is not output when count operation starts.
TAUD0 Chanel data register (TAUD0CDR0)	0xFFBF0000	0x2710	Initial down-count value of TAUD0CNT0
TAUD0 Channel start trigger register (TAUD0TS)	0xFFBF01C4	0x0001	Enable counter operation of each channels. TAUD0TS15-01 0x0: No operation. TAUD0TS00 0x1: Counter operation is enabled.

Table 3-6 to Table 3-8 show a list of functions, variables, and constants used in this operation example.

Table 3-6 List of Functions

Function Name	Description
pe0_main	Calls each function.
dts_init	Makes initial settings for DTS.
taud_init	Makes initial settings for TAUD.

Table 3-7 List of Variables

Variable Name	Description
dest_data[256]	RAM area of transfer destination.

Table 3-8 List of Constants

Constants Name	Description
source_data_table[256]	ROM data of transfer source.

3.5 Operation Flow

Figure 3-2 shows the operation flow of this operation example.

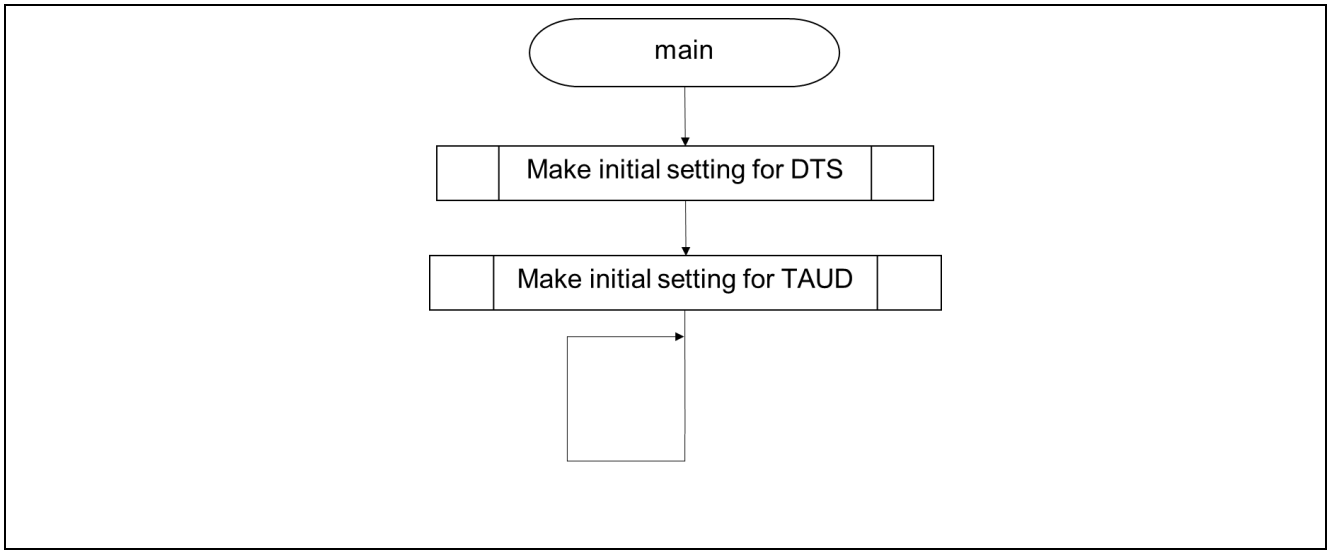

Figure 3-2 Operation Flow

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2023.09.22	-	First edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
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