RH850/U2B24

TAUJ operation example

Summary

This application note describes an example of PWM waveform output (Standard PWM) and an example of input pulse width measurement using RH850/U2B24 Timer Array Unit J (TAUJ).

The operation examples shown in this application note have been confirmed to work, but please be sure to check the operating environment before using the product.

Operation confirmation device

This article applies to RH850/U2B24.

Table of contents

1. Standard PWM

1.1 Overview

This chapter describes how to perform Standard PWM output using the PWM output function, which is one of the channel interlocking operation functions of TAUJ. The PWM output function can generate multiple PWM outputs by using the master channel and multiple slave channels. The PWM period is set on the master channel. The duty is set to the slave channel.

In this operation example, TAUJ is used for 2 channels (master and slave 1 channel), and the PWM waveform is output from one port. It also shows how interrupts can be used to continuously change the period and duty of the PWM waveform.

Figure 1-1 shows an overview diagram of the Standard PWM output.

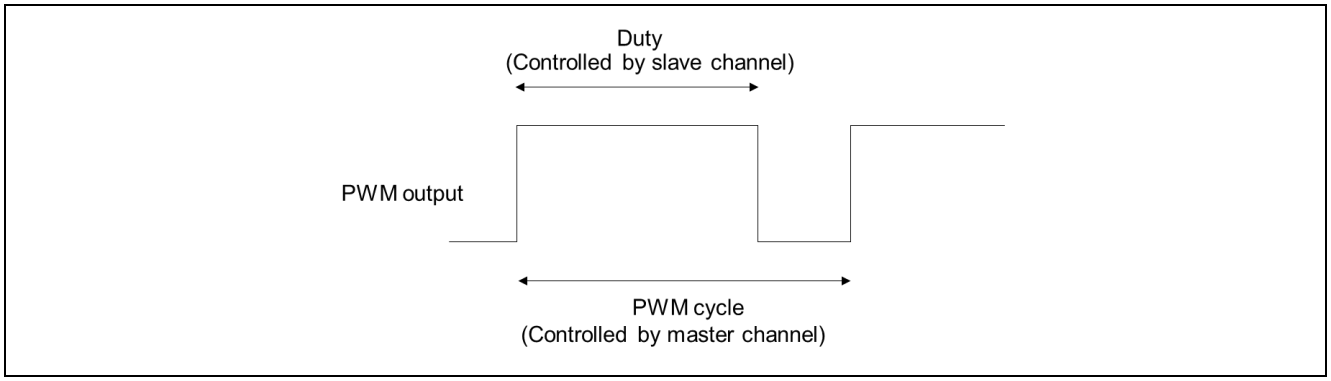

Figure 1-1 Overview diagram

1.2 Operating conditions of the function to be used

The operating conditions of the functions used in this operation example are shown below.

Table 1-1 Port settings

Item	Content
Used port	P31_11 : TAUJ2O2

Table 1-2 Timer TAUJ settings

Item	Content
Functions used	PWM output function of channel interlocking operation function
Supply clock to TAUJ	Peripheral high speed clock (80MHz)
Master channel	Timer channel 0 : Control PWM cycle
Slave channel	Timer channel 2 : Control duty
Timer operating clock	Prescaler output CK0 = (80MHz) / 1

Table 1-3 Interrupt settings

Item	Content
Interrupt method	Table reference method
INTTAUJ2I0 Interrupt	Valid (Priority 7)

1.3 Operation explanation

This example of operation shows how to continuously change the cycle and duty of the PWM waveform.

Table 1-4 shows the output waveform patterns used in this operation example. Figure 1-2 shows the output waveform.

Table 1-4 PWM output waveform pattern

Pattern No.	Period	Duty
1	50us	12.5us
2	50us	18.75us
3	50us	25us
4	75us	12.5us
5	75us	25us

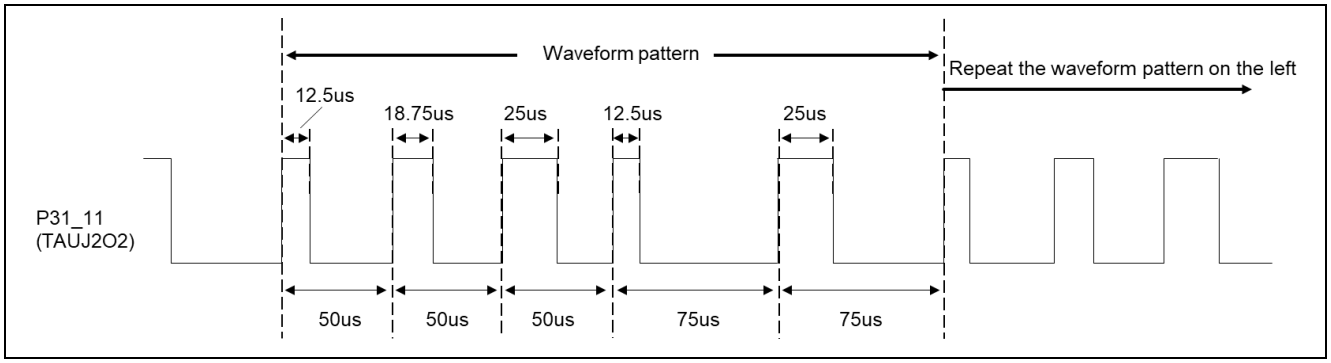

Figure 1-2 Output waveform

The operation shown in Figure 1-2 is an interrupt generated at the beginning of a PWM period and is achieved by the software changing the period / duty of the PWM waveform for the next period. Figure 1-3 shows an example of changing the PWM waveform output in the order of (Period T_a : Duty D_a) -> (Period T_b : Duty D_b) -> … by dividing it into hardware processing and software processing.

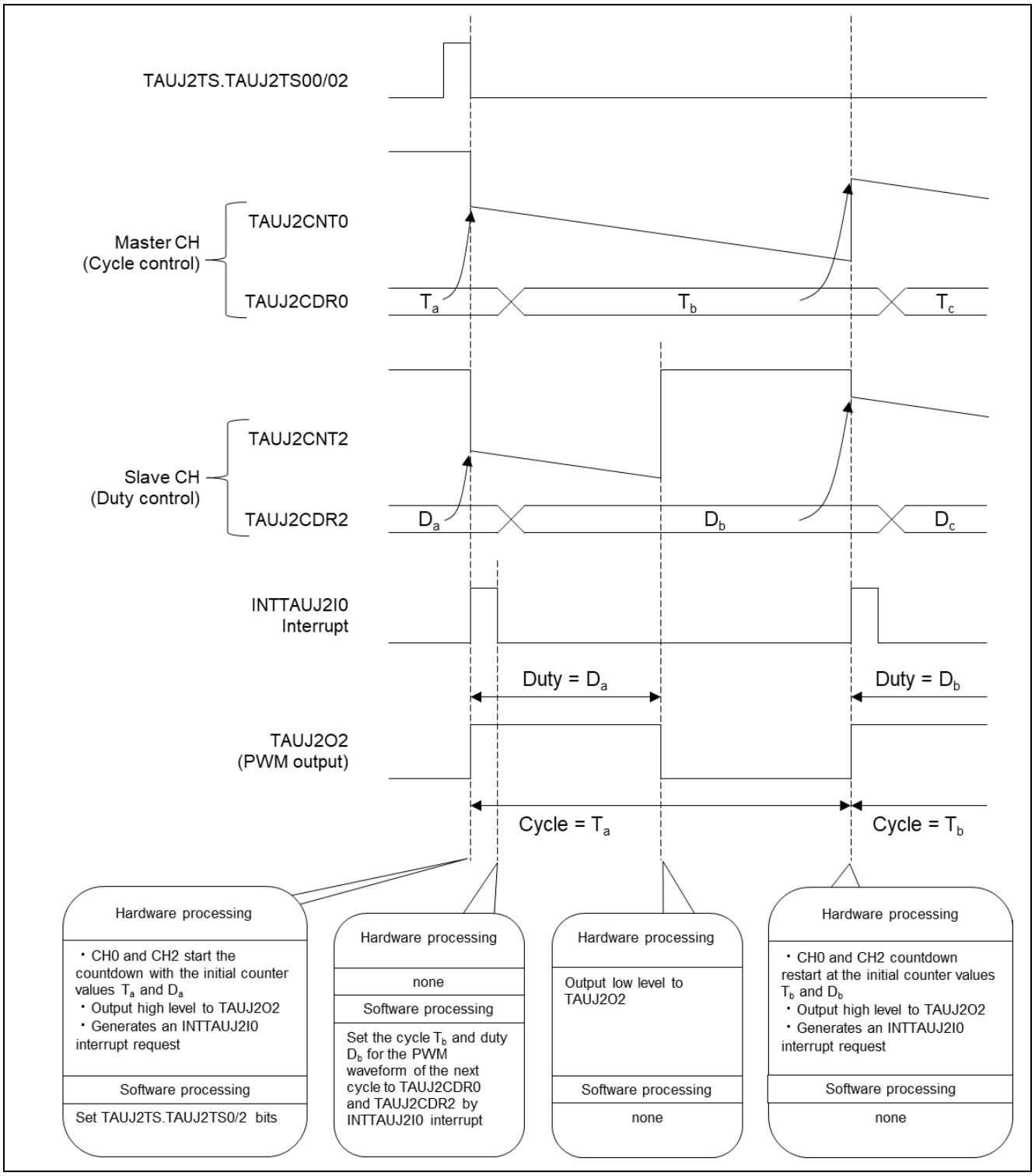

Figure 1-3 Operating principle diagram

1.4 Software description

Tables 1-5 to 1-7 show a setting example of each register used in this operation example.

Table 1-5 TAUJ register setting example

Register name	Address	Set value	Function
TAUJ2 Channel Stop Trigger Register (TAUJ2TT)	0xFFE80058	0x05	The counter operation of each channel is stopped TAUJ2TT3, 1 0x0 : No function TAUJ2TT2, 0 0x1 : Stops counter operation
TAUJ2 Prescaler Clock Select Register (TAUJ2TPS)	0xFFE80090	0x0000	A register that specifies the CK0, CK1, CK2, and CK3_PRE clocks for all channels of the PCLK prescaler TAUJ2PRS3-0[3:0] 0x0 : PCLK/2^0
TAUJ2 Prescaler Baud Rate Setting Register (TAUJ2BRS)	0xFFE80094	0x00	A register that specifies the division factor of the prescaler clock CK3 TAUJ2BRS[7:0] 0x0 : CK3_PRE/1
TAUJ2 Channel Mode OS Register 0 (TAUJ2CMOR0)	0xFFE80080	0x0801	Controls the behavior of channel 0 TAUJ2CKS[1:0] 0x0 : Operating clock CK0 TAUJ2CCS[1:0] 0x0 : Operating clock specified by TAUJnCMORm. TAUJnCKS[1:0] TAUJ2MAS 0x1 : Master channel TAUJ2STS[2:0] 0x0 : Software trigger TAUJ2MD[4:0] 0x1 : Interval timer mode Outputs INTTAUJnIm at the start of counting operation
TAUJ2 Channel Mode User Register 0 (TAUJ2CMUR0)	0xFFE80020	0x00	Specifies the type of valid edge detection used in the TAUJnTTINm input TAUJ2TIS[1:0] 0x0 : Falling edge
TAUJ2 Channel Data Register 0 (TAUJ2CDR0)	0xFFE80000	0x0F9F 0x176F	Initial value of TAUJ2CNT0 down count
TAUJ2 Channel Mode OS Register 2 (TAUJ2CMOR2)	0xFFE80088	0x0409	Controls the behavior of channel 2 TAUJ2CKS[1:0] 0x0 : Operating clock CK0 TAUJ2CCS[1:0] 0x0 : Operating clock specified by TAUJnCMORm. TAUJnCKS[1:0] TAUJ2MAS 0x0 : Slave channel TAUJ2STS[2:0] 0x4 : Master channel INTTAUJnIm is the start trigger TAUJ2MD[4:0] 0x9 : One-count mode Allow start trigger detection during counting
TAUJ2 Channel Mode User Register 2 (TAUJ2CMUR2)	0xFFE80028	0x00	Specifies the type of valid edge detection used in the TAUJnTTINm input TAUJ2TIS[1:0] 0x0 : Falling edge

Register name	Address	Set value	Function
TAUJ2 Channel Data Register 2 (TAUJ2CDR2)	0xFFE80008	0x03E7 0x05DB 0x07CF	Initial value of TAUJ2CNT2 down count
TAUJ2 Channel Output Enable Register (TAUJ2TOE)	0xFFE80060	0x00	This register enables and disables independent channel output mode controlled by software *Disable channel output before setting channel output TAUJ2TOE3-0 0x0 : Disables independent timer output function
		0x04	This register enables and disables independent channel output mode controlled by software *After configuring the channel output, allow the required channel output TAUJ2TOE3, 1-0 0x0 : Disables independent timer output function TAUJ2TOE2 0x1 : Enables independent timer output function
TAUJ2 Channel Output Register (TAUJ2TO)	0xFFE8005C	0x00	This register specifies and reads the level of TAUJnTTOUTm TAUJ2TO3-0 0x0 : Low level
TAUJ2 Channel Output Mode Register (TAUJ2TOM)	0xFFE80098	0x04	This register specifies the output mode of each channel TAUJ2TOM2 0x1 : Synchronous channel output mode TAUJ2TOM3, 1-0 0x0 : Independent channel output mode
TAUJ2 Channel Output Configuration Register (TAUJ2TOC)	0xFFE8009C	0x00	This register specifies the output mode of each channel in combination with TAUJnTOMm TAUJ2TOC3-0 0x0 : Operation mode 1
TAUJ2 Channel Output Active Level Register (TAUJ2TOL)	0xFFE80064	0x00	This register specifies the output logic of the channel output bit (TAUJnTO.TAUJnTOm) TAUJ2TOL3-0 0x0 : Positive logic (active high)
TAUJ2 Channel Reload Data Enable Register (TAUJ2RDE)	0xFFE800A0	0x05	Enables / disables simultaneous rewriting of data register TAUJnCDRm/TAUJnTOLm TAUJ2RDE3, 1 0x0 : Disables simultaneous rewrite TAUJ2RDE2, 0 0x1 : Enabled simultaneous rewrite
TAUJ2 Channel Reload Data Mode Register (TAUJ2RDM)	0xFFE800A4	0x00	Select the timing to generate the simultaneous rewrite control signal TAUJ2RDM3-0 0x0 : When the master channel counter starts counting
TAUJ2 Channel Start Trigger Register (TAUJ2TS)	0xFFE80054	0x05	Allows counter operation for each channel TAUJ2TS3, 1 0x0 : No function TAUJ2TS2, 0 0x1 : Allow counter operations and set TAUJnTE.TAUJnTEm = 1

Register name	Address	Set value	Function
TAUJ2 Channel Reload Data Trigger Register (TAUJ2RDT)	0xFFE80068	0x05	This register triggers the simultaneous rewrite enabling state TAUJ2RDT3, 1 0x0 : No function TAUJ2RDT2, 0 0x1 : Set the simultaneous rewrite permission flag (TAUJnRSFm) to "1" and wait for the simultaneous rewrite trigger

Table 1-6 Port register setting example

Register name	Address	Set value	Function
Port Control Register (PCR31_11)	0xFFD927EC	0x0000004E	This register can set all the functions of one terminal PUCC,PDSC 0x0 : Drive strength = 5 (very low) PBDC 0x0 : Bi-direction mode disabled PIBC 0x0 : Input buffer is disabled PMC 0x1 : Alternative mode PIPC 0x0 : Software I/O control PM 0x0 : Output mode (output enabled) PFCEAE,PFCAE, PFCE,PFC 0xE : Alternative output mode 15 (ALT-OUT15)

Table 1-7 Interrupt control register setting example

Register name	Address	Set value	Function
EI Level Interrupt Control Register 960 (EIC960)	0xFFF80780	0x0047	This register is prepared for each factor of EI level INT and sets the interrupt control condition for each factor EIMKn 0x0 : Interrupt processing is enabled EITBn 0x4 : Table reference method EIPn 0x7 : Priority 7

Tables 1-8 to 1-10 show a list of functions, variables, and constants used in this operation example.

Table 1-8 Function list

Function name	Overview
main_pe0	Make a call to each function
system_control_init	Select the clock source of TAUJ2 and start the module
int_init	Set the interrupt function (INTTAUJ2I0)
port_init	Set the P31_11 terminal to the TAUJ2O2 function
tauj_init	Make initial settings for TAUJ2
pwm_start	Start timers TAUJ2 CH0 and CH2 for PWM output
pwm_update_duty	This is the interrupt processing that occurs every time the TAUJ2 CH0 count starts (starts the PWM period) Change the PWM cycle and duty

Table 1-9 Variable list

Variable name	Overview
mode	Index for reading the cnt_table array

Table 1-10 Constant list

Constant name	Overview
cnt_table [5][2]	PWM period and duty set value array

1.5 Operation flowchart

Figure 1-4 shows the operation flowchart of this operation example.

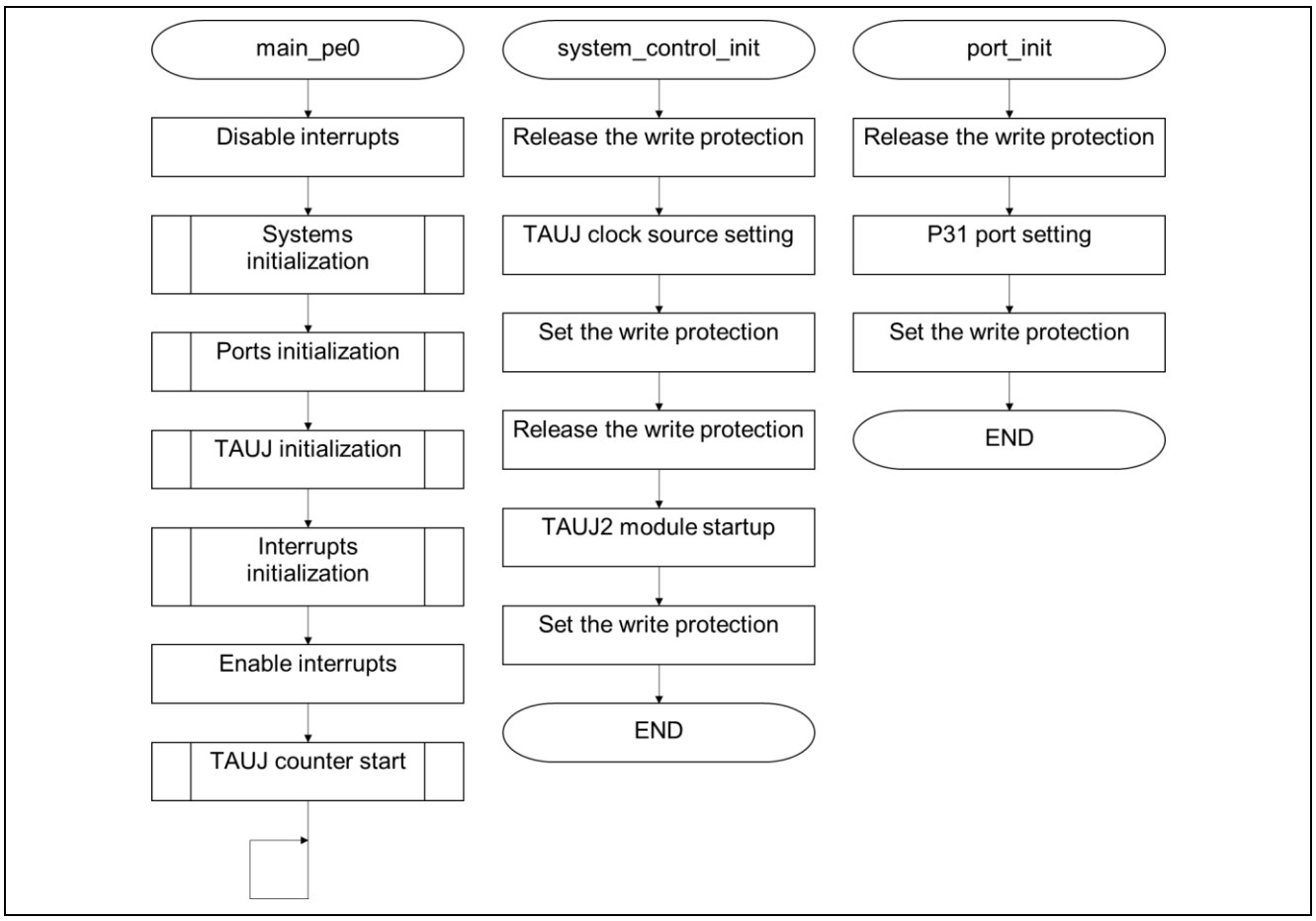

Figure 1-4 Operation flowchart (1/3)

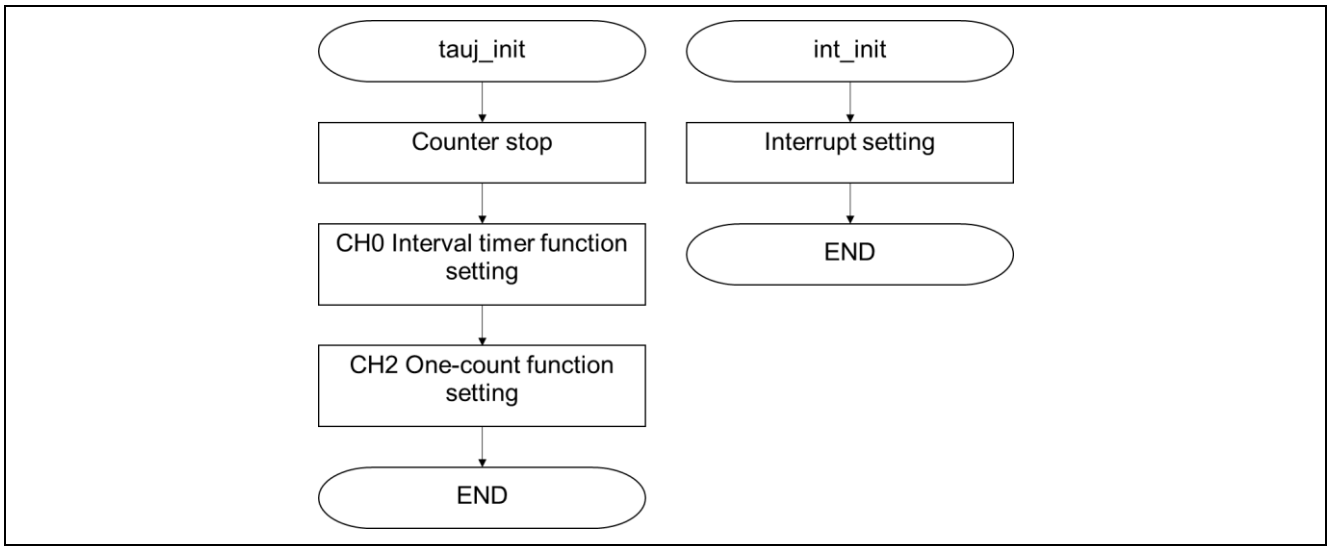

Figure 1-4 Operation flowchart (2/3)

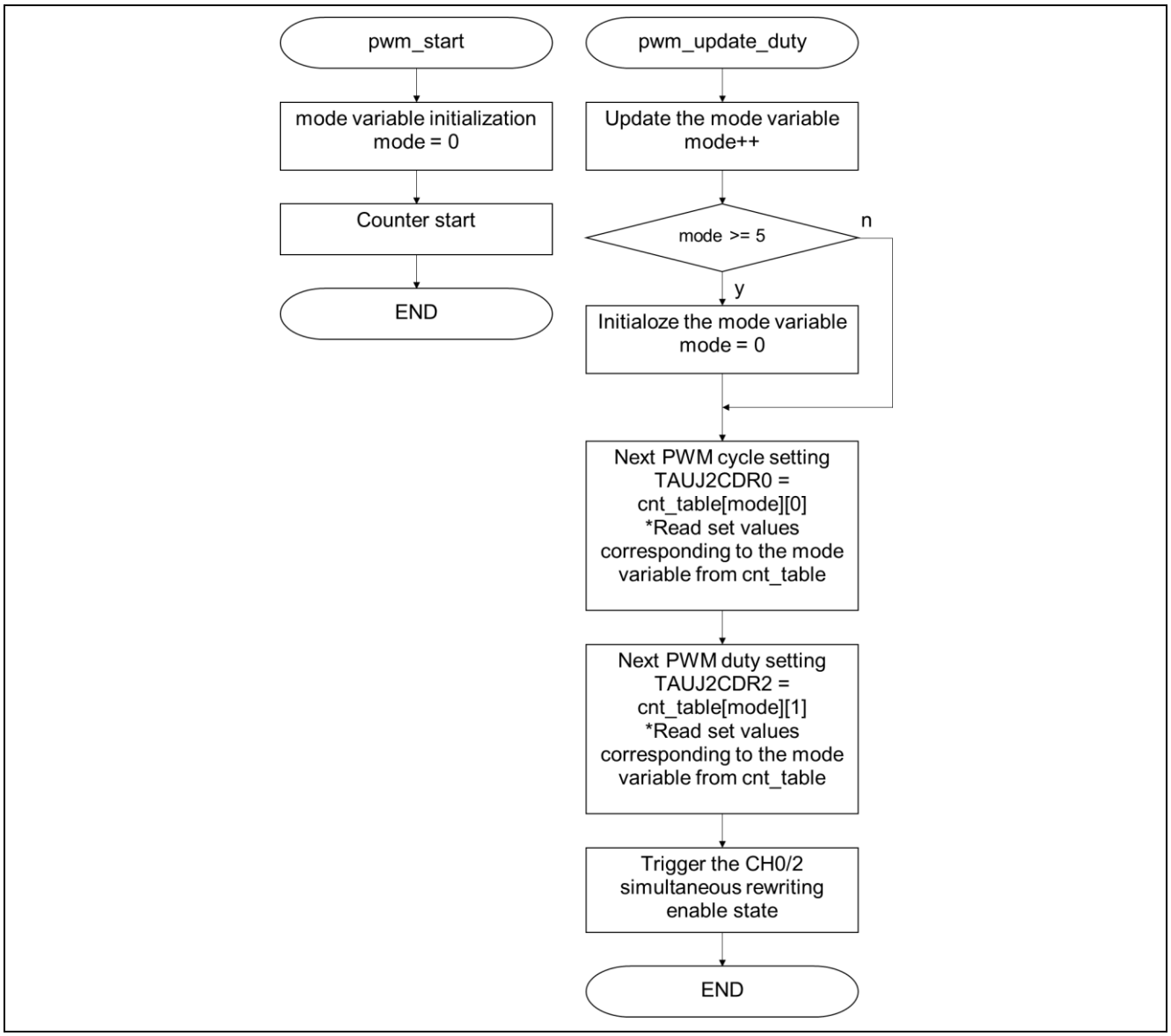

Figure 1-4 Operation flowchart (3/3)

2. Pulse signal generation and high level width measurement

2.1 Overview

This chapter describes the generation of the pulse signal by the interval timer function, which is the single channel operation function of TAUJ, and the high level width measurement of the pulse by the TAUJnTTINm input signal width measurement function.

Figure 2-1 shows an overview diagram of this operation example.

In this operation example, the pulse signal to be measured is generated by the interval timer function of TAUJ and output from the TAUJ2O2 terminal. This pulse signal is input to the TAUJ2I0 terminal and the TAUJnTTINm input signal width measurement function is used to measure the high level width.

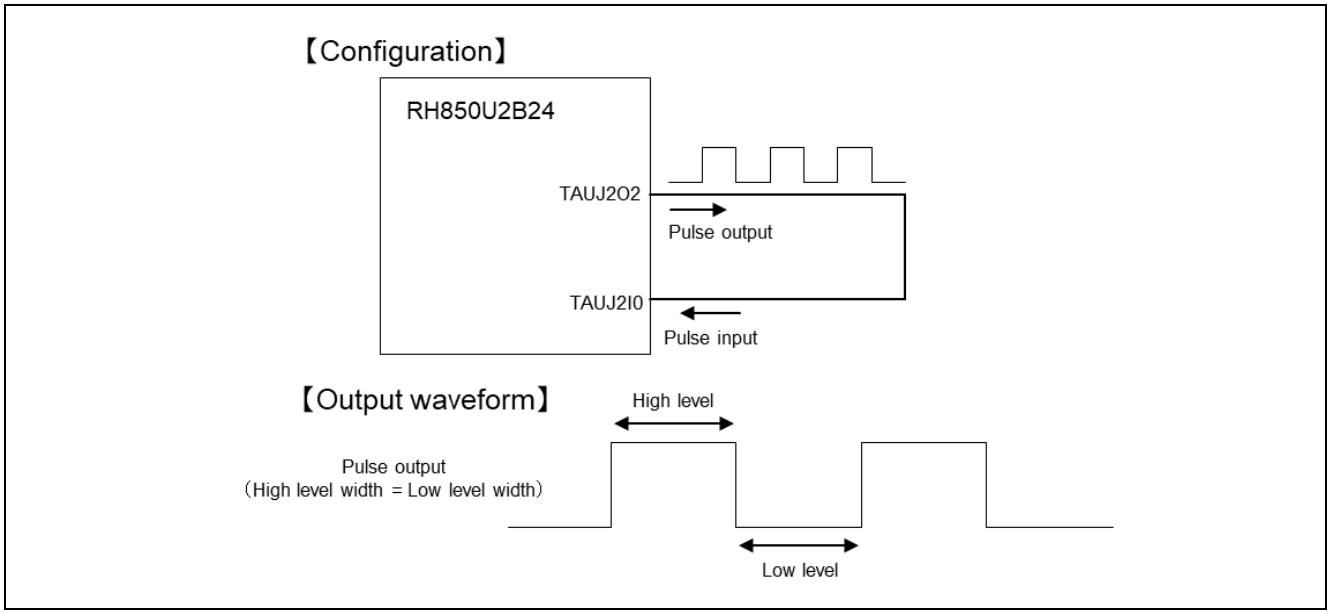

Figure 2-1 Overview diagram

2.2 Operating conditions of the function to be used

The operating conditions of the functions used in this operation example are shown below.

Table 2-1 Port settings

Item	Content
Used port	P34_1 : TAUJ2I0 P31_11 : TAUJ2O2

Table 2-2 Timer TAUJ settings

Item	Content
Functions used	Timer channel 0 : TAUJnTTINm Input signal width measurement function Timer channel 2 : Interval timer function (Pulse signal generation)
Supply clock to TAUJ	Peripheral high speed clock (80MHz)
Timer operating clock	Prescaler output CK0 = (80MHz) / 1

Table 2-3 Interrupt settings

Item	Content
Interrupt method	Table reference method
INTTAUJ2I0 Interrupt	Valid (Priority 15)

2.3 Operation explanation

The interval timer function switches the TAUJnTTOUTm signal at regular intervals to generate a pulse signal.

The TAUJnTTINm input signal width measurement function can measure the signal width of TAUJnTTINm by starting counting at the rising edge of the TAUJnTTINm and capturing the count value at the falling edge.

Figure 2-2 shows the working principle of pulse signal generation and high level width measurement separately for hardware and software processing. (In this example of operation, a 205us high level wide pulse signal is generated and time is measured.)

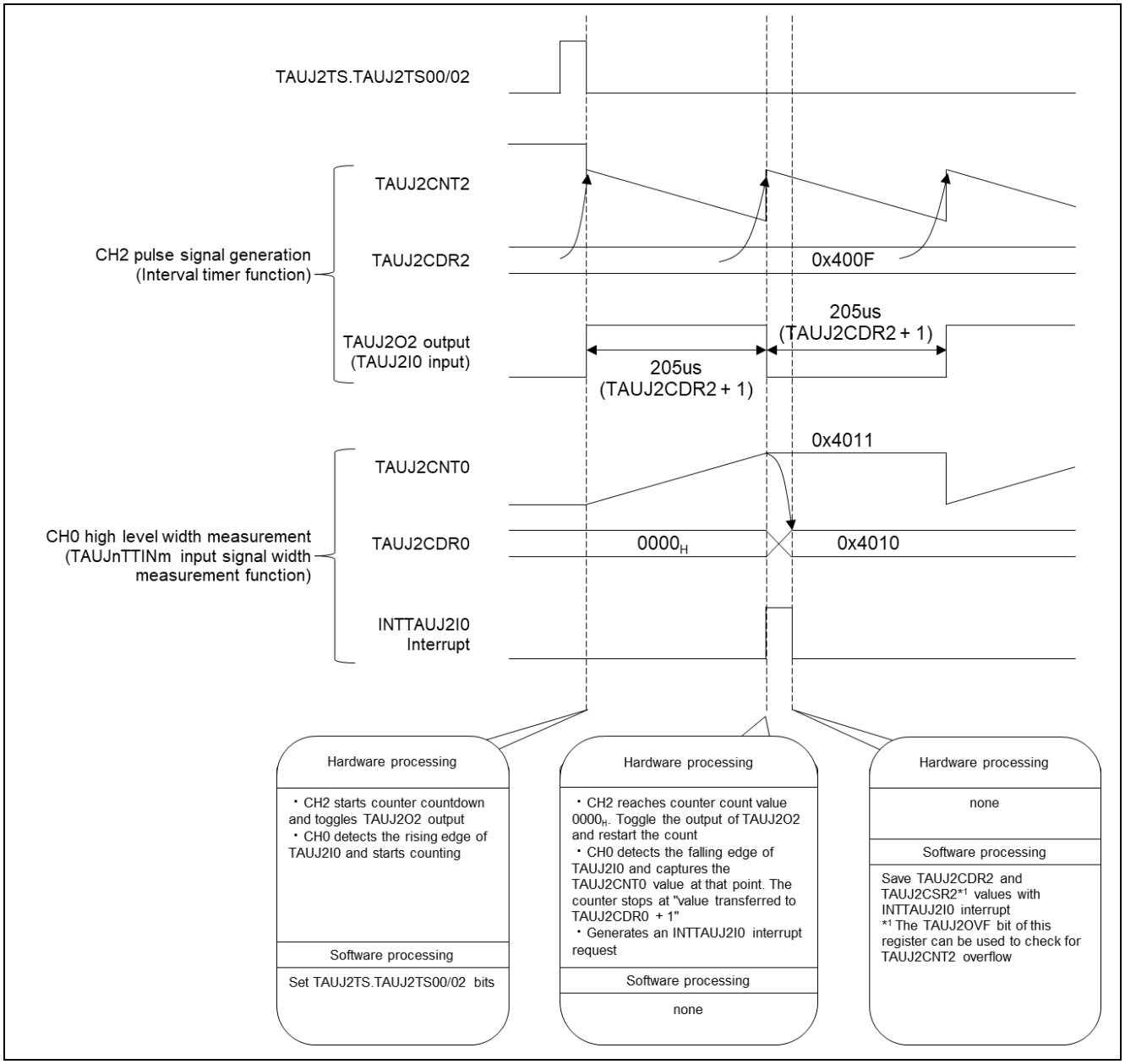

Figure 2-2 Operating diagram

2.4 Software description

Table 2-4 to 2-6 show a setting example of each register used in this operation example.

Table 2-4 TAUJ register setting example

Register name	Address	Set value	Function
TAUJ2 Channel Stop Trigger Register (TAUJ2TT)	0xFFE80058	0x05	The counter operation of each channel is stopped TAUJ2TT3, 1 0x0 : No function TAUJ2TT2, 0 0x1 : Stops counter operation
TAUJ2 Prescaler Clock Select Register (TAUJ2TPS)	0xFFE80090	0x0000	A register that specifies the CK0, CK1, CK2, and CK3_PRE clocks for all channels of the PCLK prescaler TAUJ2PRS3-0[3:0] 0x0 : PCLK/2^0
TAUJ2 Prescaler Baud Rate Setting Register (TAUJ2BRS)	0xFFE80094	0x00	A register that specifies the division factor of the prescaler clock CK3 TAUJ2BRS[7:0] 0x0 : CK3_PRE/1
TAUJ2 Channel Mode OS Register 2 (TAUJ2CMOR2)	0xFFE80088	0x0001	Controls the behavior of channel 2 TAUJ2CKS[1:0] 0x0 : Operating clock CK0 TAUJ2CCS[1:0] 0x0 : Operating clock specified by TAUJnCMORm. TAUJnCKS[1:0] TAUJ2STS[2:0] 0x0 : Software trigger TAUJ2MD[4:0] 0x1 : Interval timer mode Outputs INTTAUJnIm at the start of counting operation
TAUJ2 Channel Mode User Register 2 (TAUJ2CMUR2)	0xFFE80028	0x00	Specifies the type of valid edge detection used in the TAUJnTTINm input TAUJ2TIS[1:0] 0x0 : Falling edge (Set "0" because it is not used)
TAUJ2 Channel Data Register 2 (TAUJ2CDR2)	0xFFE80008	0x400F	Initial value of TAUJ2CNT2 down count

Register name	Address	Set value	Function
TAUJ2 Channel Mode OS Register 0 (TAUJ2CMOR0)	0xFFE80080	0x020C	Controls the behavior of channel 0 TAUJ2CKS[1:0] 0x0 : Operating clock CK0 TAUJ2CCS[1:0] 0x0 : Operating clock specified by TAUJnCMORm. TAUJnCKS[1:0] TAUJ2STS[2:0] 0x2 : Valid edge of TAUJnTTINm input signal is used as a start trigger and the reverse edge as a stop trigger TAUJ2COS[1:0] 0x0 : TAUJnCDRm updates when it detects a TAUJnTTINm input valid edge TAUJnCSRm. TAUJnOVF bit updates when TAUJnTTINm input valid edge is detected (Clear or set) TAUJ2MD[4:0] 0xC : Capture and one-count mode
TAUJ2 Channel Mode User Register 0 (TAUJ2CMUR0)	0xFFE80020	0x03	Specifies the type of valid edge detection used in the TAUJnTTINm input TAUJ2TIS[1:0] 0x3 : Both edge detection (high level width measurement selection)
TAUJ2 Channel Output Enable Register (TAUJ2TOE)	0xFFE80060	0x00	This register enables and disables independent channel output mode controlled by software *Disable channel output before setting channel output TAUJ2TOE3-0 0x0 : Disables independent timer output function
		0x04	This register enables and disables independent channel output mode controlled by software *After configuring the channel output, allow the required channel output TAUJ2TOE3, 1-0 0x0 : Disables independent timer output function TAUJ2TOE2 0x1 : Enables independent timer output function
TAUJ2 Channel Output Mode Register (TAUJ2TOM)	0xFFE80098	0x00	This register specifies the output mode of each channel TAUJ2TOM3-0 0x0 : Independent channel output mode
TAUJ2 Channel Output Configuration Register (TAUJ2TOC)	0xFFBE8009C	0x00	This register specifies the output mode of each channel in combination with TAUJnTOMm TAUJ2TOC3-0 0x0 : Operation mode 1

Register name	Address	Set value	Function
TAUJ2 Channel Output Active Level Register (TAUJ2TOL)	0xFFE80064	0x00	This register specifies the output logic of the channel output bit (TAUJnTO.TAUJnTOm) TAUJ2TOL3-0 0x0 : Positive logic (active high)
TAUJ2 Channel Reload Data Enable Register (TAUJ2RDE)	0xFFE800A0	0x00	Enables / disables simultaneous rewriting of data register TAUJnCDRm/TAUJnTOLm TAUJ2RDE3-0 0x0 : Disables simultaneous rewrite
TAUJ2 Channel Reload Data Mode Register (TAUJ2RDM)	0xFFE800A4	0x00	Select the timing to generate the simultaneous rewrite control signal TAUJ2RDM3-0 0x0 : When the master channel counter starts counting
TAUJ2 Channel Start Trigger Register (TAUJ2TS)	0xFFE80054	0x05	Allows counter operation for each channel TAUJ2TS3, 1 0x0 : No function TAUJ2TS2, 0 0x1 : Allow counter operations and set TAUJnTE.TAUJnTEm = 1

Table 2-5 Port register setting example

Register name	Address	Set value	Function
Digital Noise Elimination Control Register (DNFACTL_TAUJ2)	0xFFED1600	0x00	Specifies the characteristics of DNF NFSTS[2:0] 0x0 : Digital noise elimination sampling number 2 times PRS[2:0] 0x0 : Sampling clock supply/1
Digital Noise Elimination Enable Register (DNFAEN_TAUJ2)	0xFFED1604	0x0001	NFENH7-0 0x0 : Disable digital noise elimination NFENL7-1 0x0 : Disable digital noise elimination NFENL0 0x1 : Enable digital noise elimination
Port Control Register (PCR31_11)	0xFFD927EC	0x0000004E	This register can set all the functions of one terminal PUCC,PDSC 0x0 : Drive strength = 5 (very low) PBDC 0x0 : Bi-direction mode disabled PIBC 0x0 : Input buffer is disabled PMC 0x1 : Alternative mode PIPC 0x0 : Software I/O control PM 0x0 : Output mode (output enabled) PFCEAE,PFCAE, PFCE,PFC 0xE : Alternative output mode 15 (ALT-OUT15)
Port Control Register (PCR34_1)	0xFFD92884	0x0000005E	This register can set all the functions of one terminal PUCC,PDSC 0x0 : Drive strength = 5 (very low) PBDC 0x0 : Bi-direction mode disabled PIBC 0x0 : Input buffer is disabled PMC 0x1 : Alternative mode PIPC 0x0 : Software I/O control PM 0x1 : Input mode (output prohibited) PFCEAE,PFCAE, PFCE,PFC 0xE : Alternative Input mode 15 (ALT-IN15)

Table 2-6 Interrupt control register setting example

Register name	Address	Set value	Function
EI Level Interrupt Control Register 960 (EIC960)	0xFFF80780	0x004F	This register is prepared for each factor of EI level INT and sets the interrupt control condition for each factor EIMKn 0x0 : Interrupt processing is enabled EITBn 0x4 : Table reference method EIPn 0xF : Priority 15

Table 2-7 to 2-8 show a list of functions and variables used in this operation example.

Table 2-7 Function list

Function name	Overview
main_pe0	Make a call to each function
system_control_init	Select the clock source of TAUJ2 and start the module
int_init	Set the interrupt function (INTTAUJ2I0)
port_init	Set the P31_11 terminal to the TAUJ2O2 function and P34_1 to the TAUJ2I0 function
tauj_init	Make initial settings for TAUJ2
tauj_cnt_start	Start the timer TAUJ2 CH2 for pulse waveform output and CH0 for pulse width measurement
pulse_measure	This is the interrupt processing that occurs when CH0 of TAUJ2 captures the pulse width Saves the pulse width and the presence or absence of overflow

Table 2-8 Variable list

Variable name	Overview
pulsewidth	Saves the high level width of the measured pulse signal
overflow	Saves whether a counter overflow occurred during a high level width measurement

2.5 Operation flowchart

Figure 2-3 shows the operation flowchart of this operation example.

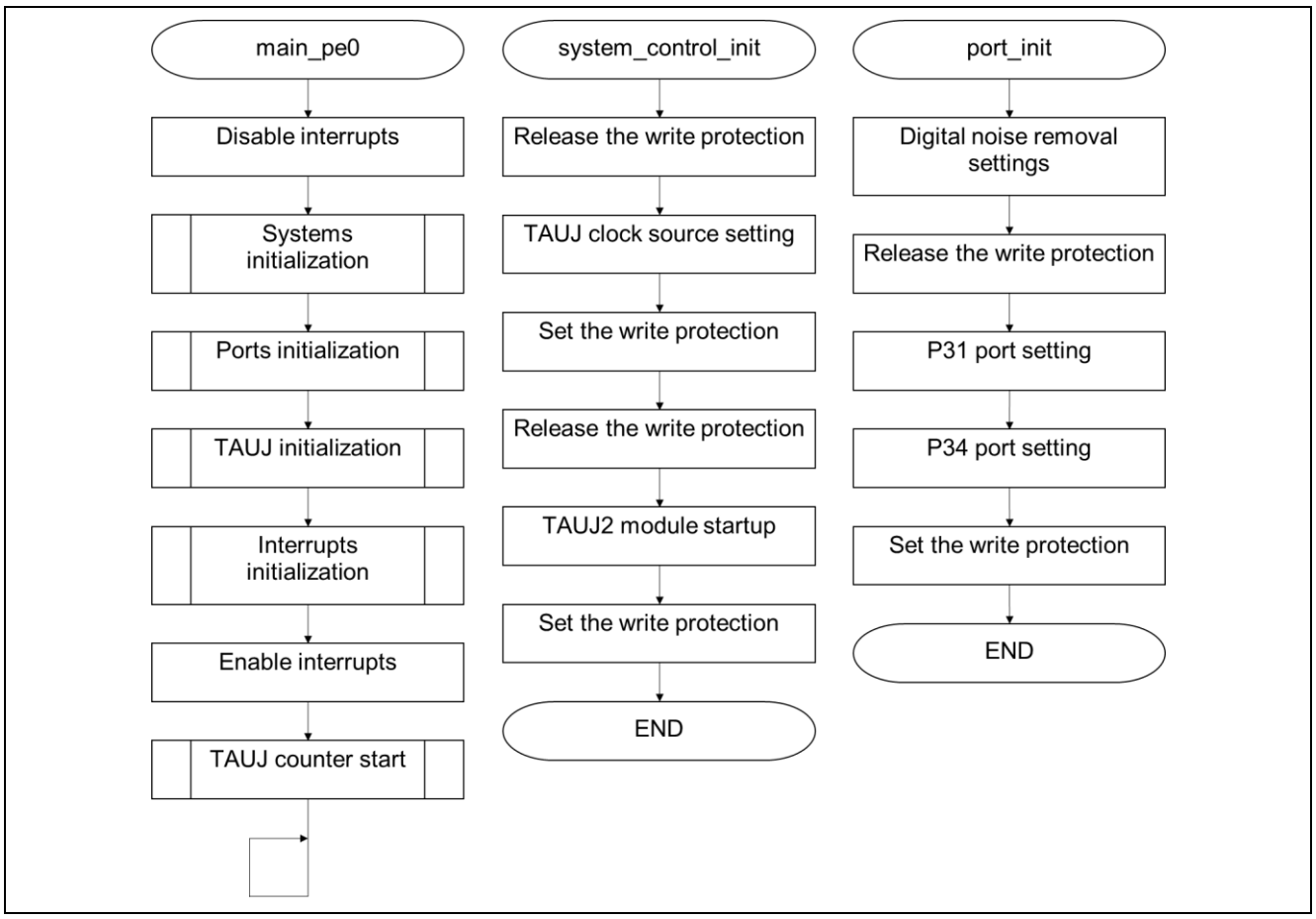

Figure 2-3 Operation flowchart (1/3)

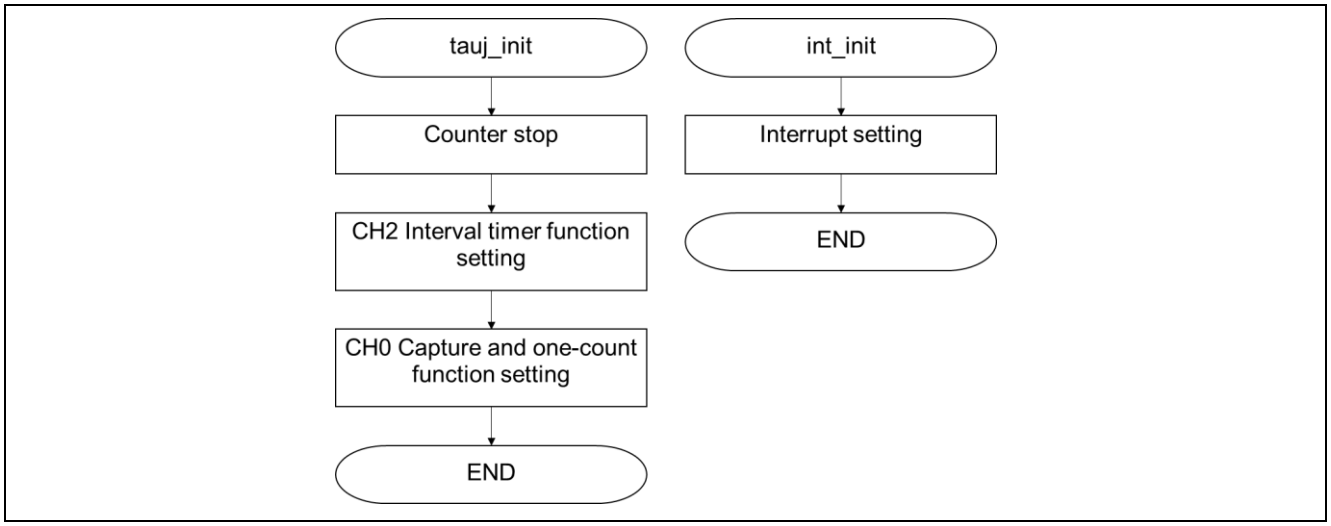

Figure 2-3 Operation flowchart (2/3)

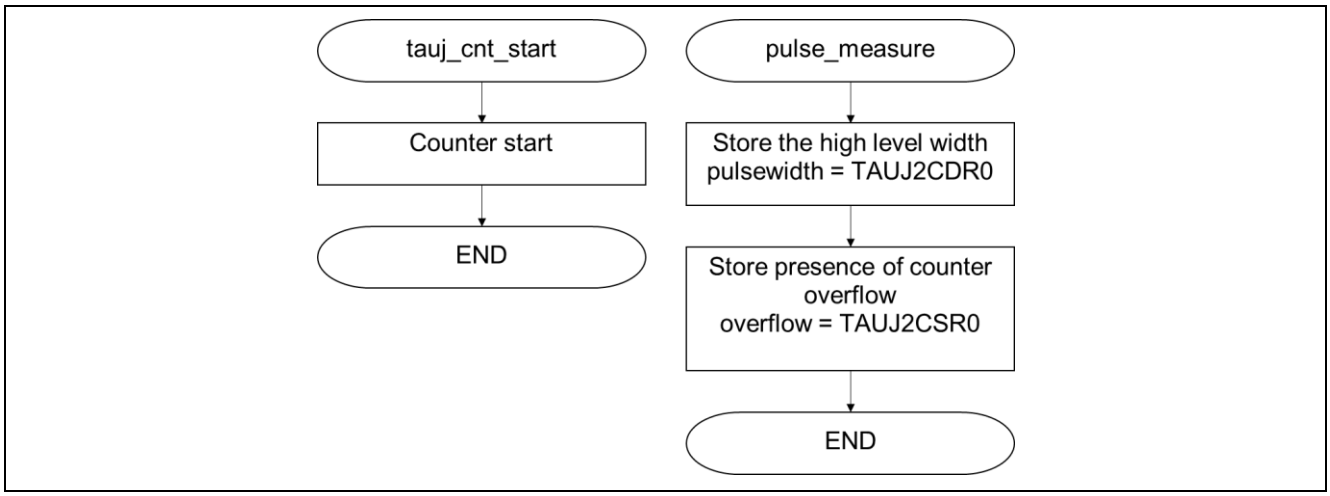

Figure 2-3 Operation flowchart (3/3)

Revised record

Rev.	Date of issue	Revised contents	
		page	point
1.00	2023.09.22	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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