RH850/U2B

Timer Option (TAPA)

Summary

This application note describes how to realize functions using TAPA on the RH850/U2B6.

The operation examples shown in this application note have been confirmed to work, but please be sure to check the operating environment before using the product.

Operation confirmation device

RH850/U2B6-FCC (R7F702Z22EDBB)

Table of Contents

1. Introduction

This application note describes how to use the following TAPA functions with the RH850/U2B6-FCC.

- Asynchronous Hi-Z control
- Interrupt signal output
- A/D Converter Conversion Trigger Selection Function

1.1 Functions

The hardware functions of RH850/U2B6 used in this application note are shown below.

- TAPA（Timer Option）
- PIC（Peripheral Interconnect）
- TAUD（Timer Array Unit D）
- TSG3（Motor Control Timer）

2. Asynchronous Hi-Z control

This chapter shows an example of Asynchronous Hi-Z control using TAPA.

2.1 Operation overview

If an error occurs in the motor control timer and a Hi-Z control signal is received from PIC, the motor control output can be set to the Hi-Z state without CPU control. Figure 2-1 shows an example of the operation overview.

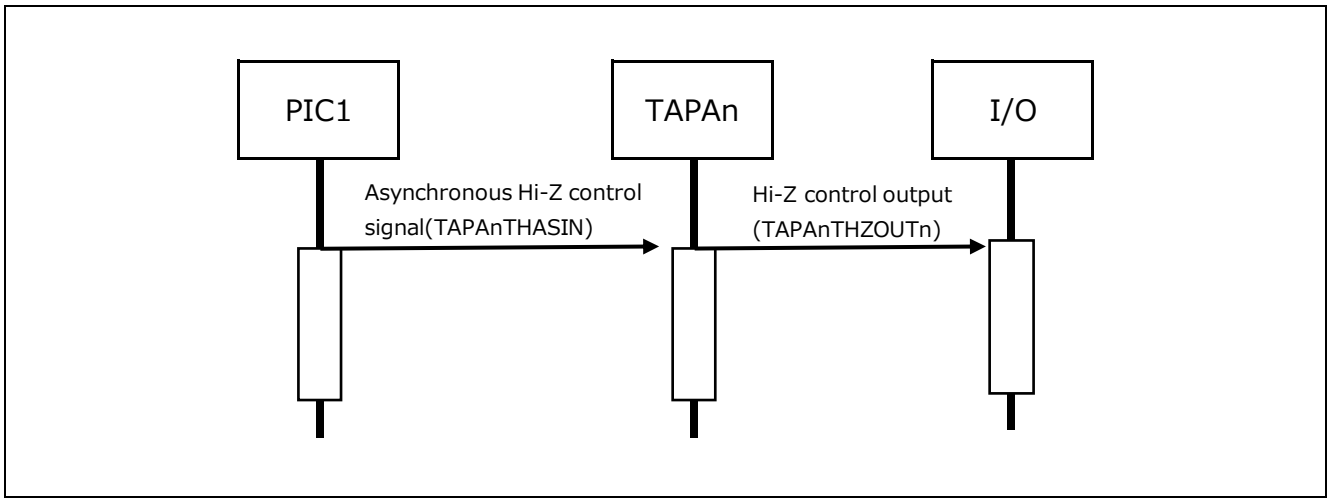

Figure 2-1 Asynchronous Hi-Z control operation

Timing Chart

The timing chart below shows the transition to the Hi-Z state upon detection of the Hi-Z control signal, and the timing chart from the transition to the release of the Hi-Z state. Figure **2-2** shows a timing chart for the case where the Hi-Z state can be released by setting the asynchronous Hi-Z control stop trigger bit (TAPAnOPHT0), regardless of the Hi-Z control signal input level.

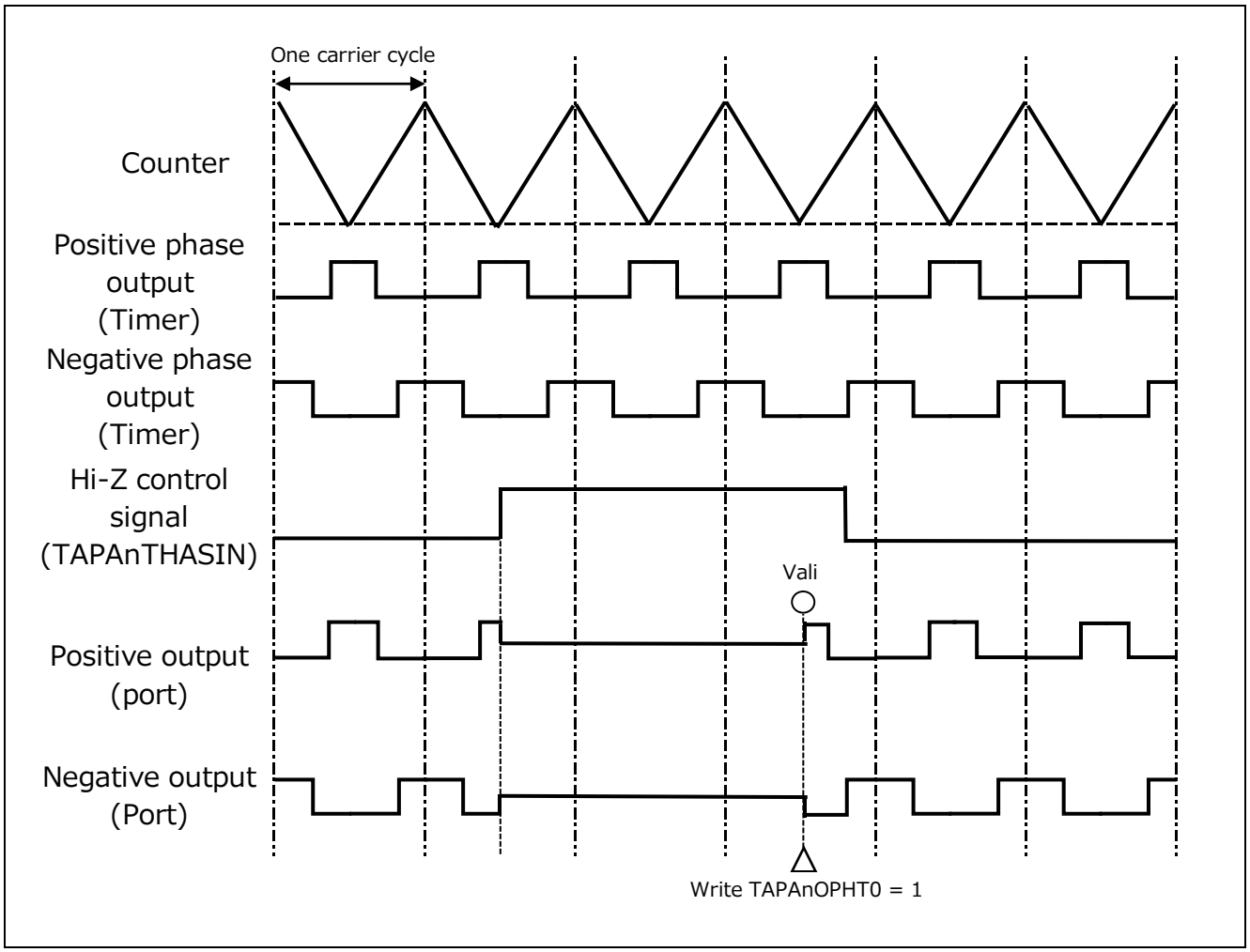

Figure 2-2 The Hi-Z state can be released regardless of the input level of the Hi-Z control signal

Figure **2-3** shows a timing chart for the case where the Hi-Z state can be released by setting the asynchronous Hi-Z control stop trigger bit (TAPAnOPHT0) only when the Hi-Z control signal input level is inactive.

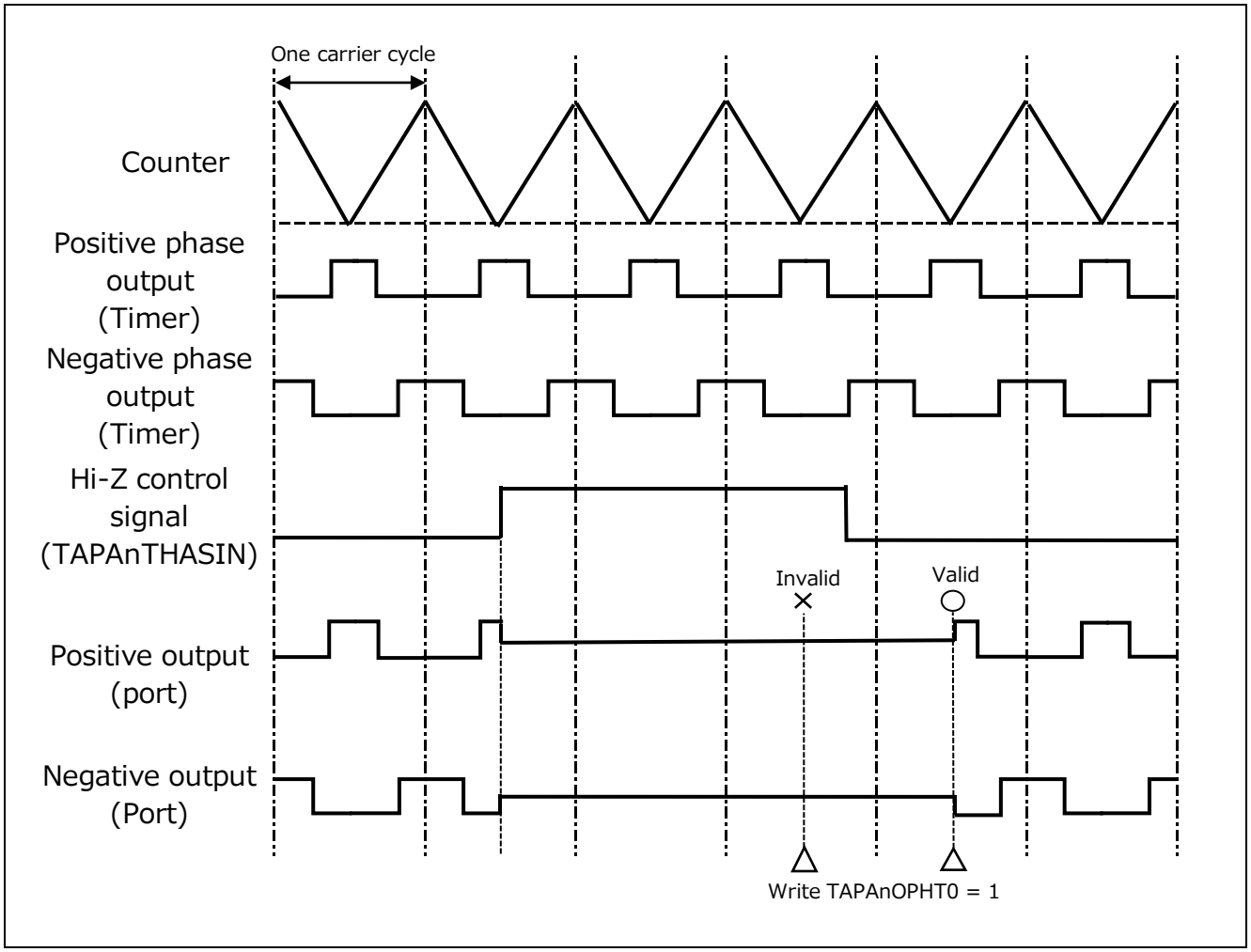

Figure 2-3 The Hi-Z state can be released only when the input level of the Hi-Z control signal is inactive

2.2 Operation flowchart

Figure **2-4** shows the operation flowchart when the Hi-Z state is released asynchronously.

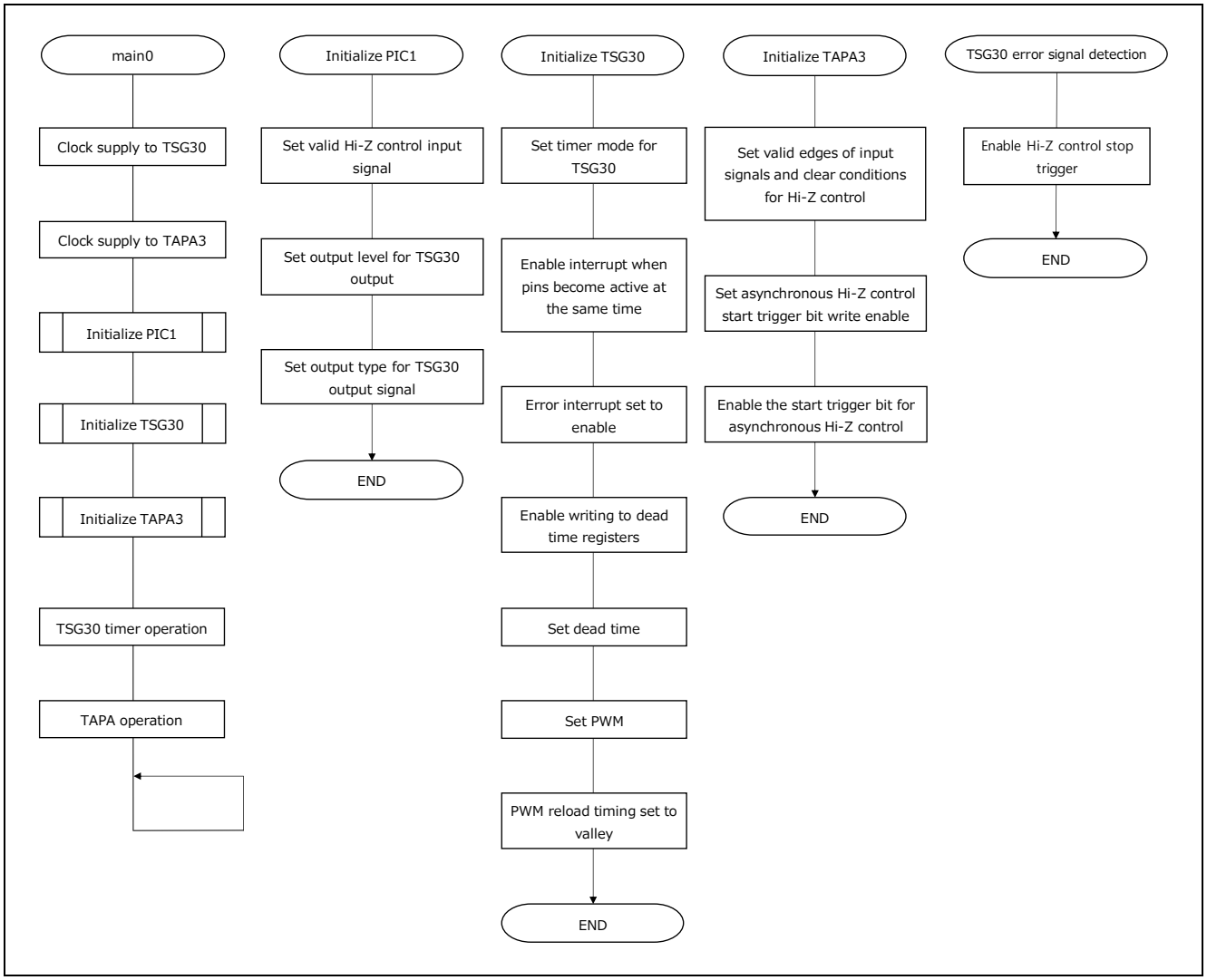

Figure 2-4 Operation flowchart when the Hi-Z state is released asynchronously

Figure **2-5** shows the operation flowchart when the Hi-Z state can be released only when the input level of the Hi-Z control signal is inactive.

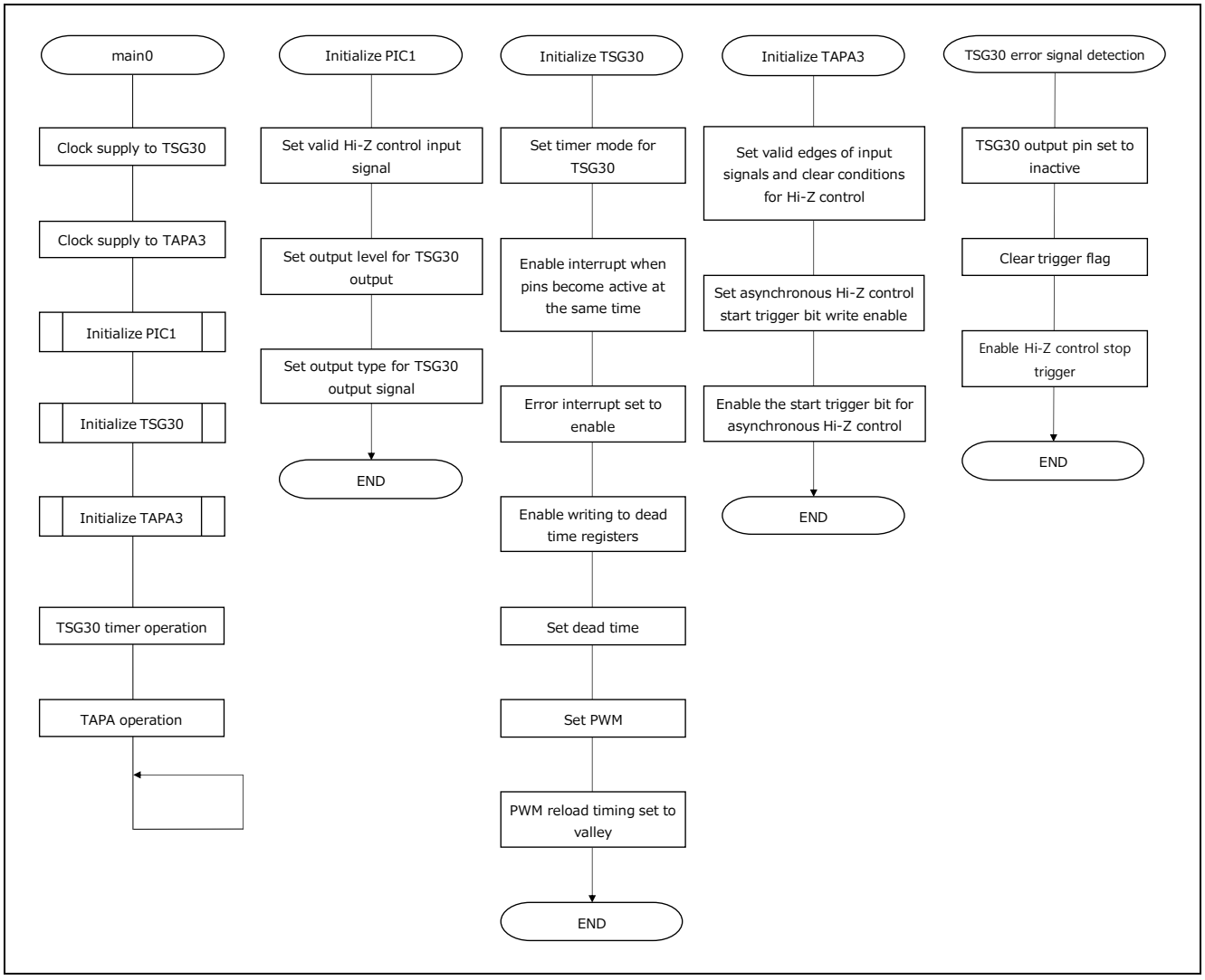

Figure 2-5 Operation flowchart when the Hi-Z state can be released only when the input level of the Hi-Z control signal is inactive

2.3 Software description

Table 2-1 to Table 2-3 shows an example of each register setting used in the Asynchronous Hi-Z control shown in Figure **2-4**.

Table 2-1 Register setting example (TAPA3)

Register name	Set value	Function
TAPA3CTL0	0x0004	Hi-Z control can be started at the rising edge of the Hi-Z control signal and stopped regardless of the Hi-Z control signal input level.
TAPA3ACWE	0x01	Sets Asynchronous Hi-Z control write enable.
TAPA3ACTS	0x01	Enable Asynchronous Hi-Z control start trigger.
TAPA3OPHT	0x01	Sets the Hi-Z control stop trigger.

Table 2-2 Register setting example (PIC1)

Register name	Set value	Function
PIC1HIZCEN02	0x08	Set the TSG30 error interrupt signal to enable.
PIC1LHSEL0	0x7E	Selects the High/Low level of TSG30 output.
PIC1TSGOUTCTR0	0x0000	Set the output signal to TSG30 output.

Table 2-3 Register setting example (TSG30)

Register name	Set value	Function
TSG30CTL0	0x01	Set the timer mode to HT-PWM mode.
TSG30CTL1	0x0200	Set the enable flag.
TSG30CTL4	0x00000080	Set PWM valley reload.
TSG30IOC0	0x1E	Set the timer output pins.
TSG30IOC1	0x08	Set the error interrupt for the timer output pins.
TSG30DTPR	0x0000	Allows rewriting.
TSG30DTC0W	0x00000140	Set the reverse phase to positive phase dead time value (4us).
TSG30DTC1W	0x00000140	Set the positive-phase to reverse-phase dead time value (4us).
TSG30CMP0E	0x00001F40	Set the PWM cycle to 100us.
TSG30CMPUE	0x00000FA0	Set the U-phase compare value (50%).
TSG30CMPVE	0x00000FA0	Set the phase-V compare value (50%).
TSG30CMPWE	0x00000FA0	Set the W-phase compare value (50%).
TSG30TRG0	0x01	Start TSG30 timer.

Table 2-4,

Table **2-5** lists the functions and variables used in the operation shown in Figure **2-4**.

Table 2-4 Function list

Function name	Overview
main0	Main Application
tapa3_init	Initialize TAPA3
pic1_init	Initialize PIC1
tsg3_init	Initialize TSG30
val_init	Variable initialization
tapa3_main	Hi-Z control output processing
hiz_ctl_sample	Sample timer error signal output
timer_err_sample	Stop Hi-Z control output process

hiz_ctl_stop	TSG30 error interrupt signal detection processing

Table 2-5 Variable list

Variable name	Overview
u4l_hiz_ctl_cnt	Counter for stopping Hi-Z control

Table 2-6 to Table 2-9 shows an example of each register setting used in the Asynchronous Hi-Z control shown in Figure **2-5**.

Table 2-6 Register setting example (TAPA3)

Register name	Set value	Function
TAPA3CTL0	0x0014	Hi-Z control is started on the rising edge of the Hi-Z control signal, and Hi-Z control can be stopped only when the Hi-Z control signal is inactive.
TAPA3ACWE	0x01	Set Asynchronous Hi-Z control write enable.
TAPA3ACTS	0x01	Enable Asynchronous Hi-Z control start trigger.
TAPA3OPHT	0x01	Set the Hi-Z control stop trigger.

Table 2-7 Register setting example (PIC1)

Register name	Set value	Function
PIC1HIZCEN02	0x08	Set the TSG30 error interrupt signal to enable.
PIC1LHSEL0	0x7E	Selects the High/Low level of TSG30 output.
PIC1TSGOUTCTR0	0x0000	Set the output signal to TSG30 output.

Table 2-8 Register setting example (TSG30)

Register name	Set value	Function
TSG30CTL0	0x01	Set the timer mode to HT-PWM mode.
TSG30CTL1	0x0200	Set the enable flag.
TSG30CTL4	0x00000080	Set PWM valley reload.
TSG30IOC0	0x1E	Set the timer output pins.
TSG30IOC1	0x08	Set the error interrupt for the timer output pins.
TSG30IOC2	0x0060, 0xFF9F	Set the level of the timer output pins.
TSG30STC	0x0200	Clear the trigger flag.
TSG30DTPR	0x0000	Allows rewriting.
TSG30DTC0W	0x00000140	Set the reverse phase to positive phase dead time value (4us).
TSG30DTC1W	0x00000140	Set the positive phase to reverse phase dead time value (4us).
TSG30CMP0E	0x00001F40	Set the PWM period to 100us.
TSG30CMPUE	0x00000FA0	Set the U-phase compare value (50%).
TSG30CMPVE	0x00000FA0	Set the phase-V compare value (50%).
TSG30CMPWE	0x00000FA0	Set the W-phase compare value (50%).
TSG30TRG0	0x01	Start TSG30 timer.

Table 2-9 Register setting example (EIC)

Register name	Set value	Function
INTC2.EIC37	0x0047	Interrupt allowed, priority 7

Table 2-10, Table 2-11 lists the functions and variables used in the operation shown in Figure **2-5**.

Table 2-10 Function list

Function name	Overview
main0	Main Application
tapa3_init	Initialize TAPA3
pic1_init	Initialize PIC1
tsg3_init	Initialize TSG30
val_init	Variable initialization
tapa3_main	Hi-Z control output processing
hiz_ctl_sample	Sample timer error signal output
timer_err_sample	Stop Hi-Z control output process
hiz_ctl_stop	TSG30 error interrupt signal detection processing
TSG30_ERR_INT	Hi-Z control output processing

Table 2-11 Variable list

Variable name	Overview
u4l_hiz_ctl_cnt	Counter for stopping Hi-Z control

3. Interrupt signal output

This chapter shows an example of using TAPA to output an interrupt request.

3.1 Operation overview

Interrupt requests (TAPAnTSIM0 and TAPAnTUDCM0) from the PIC are triggered to output interrupt requests to other modules. The peak period is the period during which an interrupt from the master channel occurs while the TAUD is counting up, and this interrupt is designated as the peak interrupt (INTTAPAnIPEKn). The period until the master channel interrupt occurs during the TAUD countdown is defined as the valley period, and this interrupt is referred to as the valley interrupt (INTTAPAnIVLYn). Figure **3**-**1** below shows an example of the operation outline.

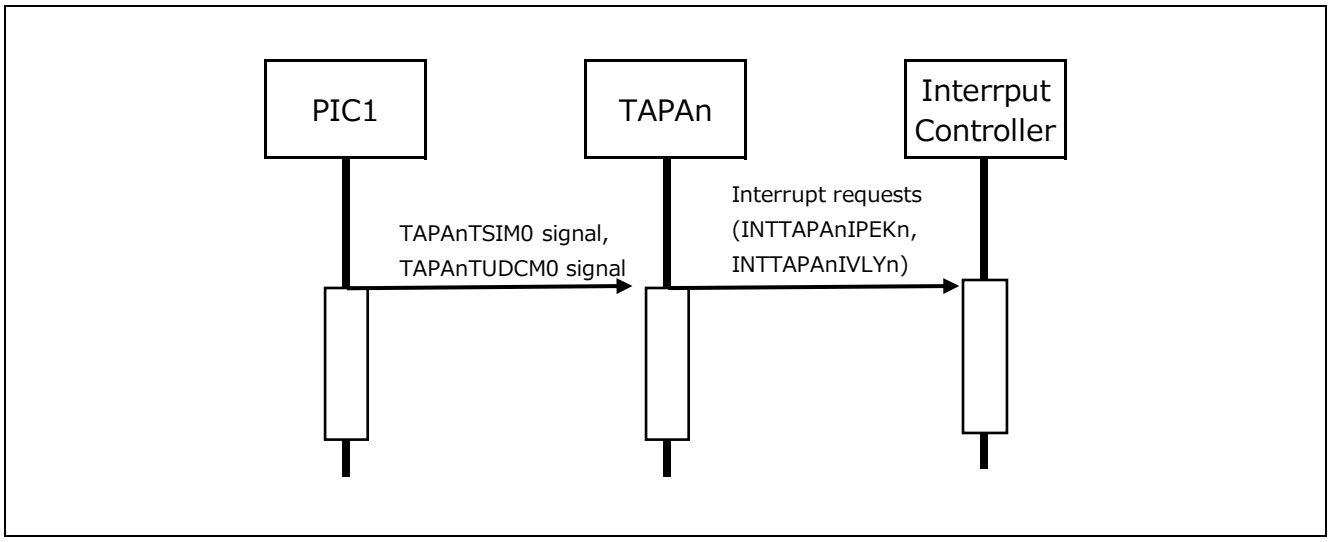

Figure 3-1 Interrupt request output

3.2 Operation flowchart

Figure **3-2** below shows the operational flowchart.

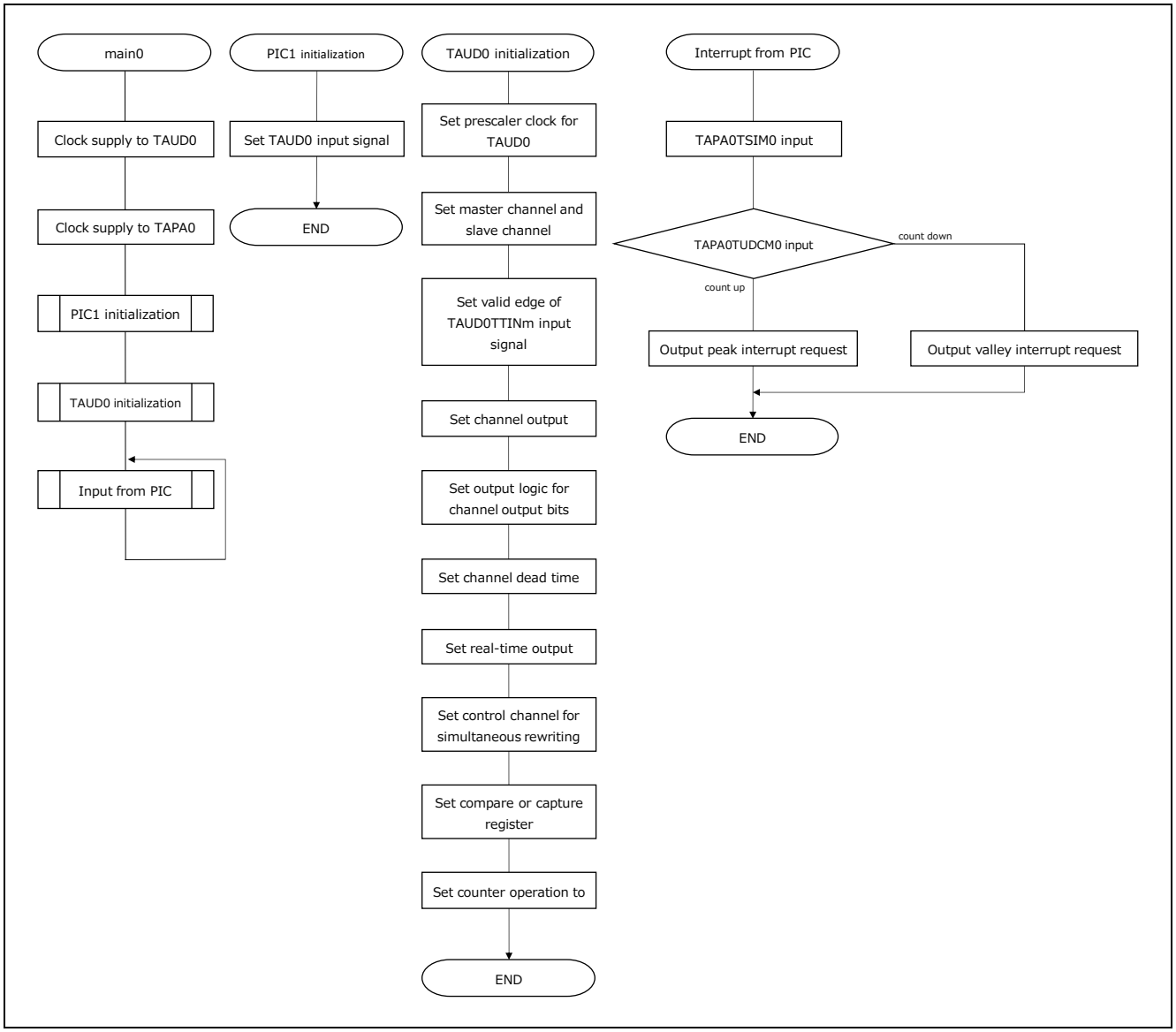

Figure 3-2 Interrupt Request Operation flowchart

3.3 Software description

Table 3-1 to Table 3-4 shows an example of each register setting used in the Interrupt signal output shown in Figure **3-2**.

Table 3-1 Register setting example (TAPA)

Register name	Set value	Function
-	-	-

Table 3-2 Register setting example (PIC1)

Register name	Set value	Function
PIC1REG200	0x01040A00	Set the input signal for TAUD0.

Table 3-3 Register setting example (TAUD0)

Register name	Set value	Function
TOUD0TPS	0x0001	Sets the prescaler clock for TAUD0.
TAUD0CMOR0	0x0800	TAUD0 Set channel 0 as the master channel.
TAUD0CMUR0	0x00	Sets the valid edge of the TAUD0TTINm input signal.
TAUD0CMOR1	0x0712	TAUD0 Set channel 0 as the slave channel.
TAUD0CMUR1	0x00	Sets the valid edge of the TAUD0TTINm input signal.
TAUD0TOE	0x0003	Sets the prescaler clock for TAUD0.
TAUD0TOM	0x0002	Sets the output mode for each channel of TAUD0.
TAUD0TOC	0x0002	Sets the output mode for each channel in combination with TAUD0TOM.
TAUD0TOL	0x0000	Sets the output logic of the channel output bits.
TAUD0TDE	0x0000	Sets the dead time operation of each channel.
TAUD0TDM	0x0000	Sets the timing for adding dead time when dead time is output.
TAUD0TRE	0x0000	Sets the real-time output.
TAUD0TRO	0x0000	Sets the output value to TAUD0TTOUTm.
TAUD0TRC	0x0000	Sets the real-time output for each channel.
TAUD0TME	0x0000	Sets the modulation output in timer output and real-time output.
TAUD0RDE	0x0300	Sets the simultaneous rewriting of the TAUD0CDRm/TAUD0TOLm data registers.
TAUD0RDS	0x0000	Sets the channel to control the simultaneous rewrite.
TAUD0RDM	0x0300	Sets the timing of simultaneous rewrite control signal generation.
TAUD0RDC	0x0000	Sets the channel that generates the INTTAUD0Im signal and triggers simultaneous rewriting.
TAUD0CDR0	0xF000	Sets as compare register or capture register depending on the operation mode specified by TAUD0CMOR0.TAUD0MD.
TAUD0CDR1	0x7800	Set as compare register or capture register depending on the operation mode specified by TAUD0CMOR1.TAUD0MD.
TAUD0TS	0x0003	Enables counter operation for TAUD channels 0 and 1.

Table 3-4 Register setting example (EIC)

Register name	Set value	Function
INTC2.EIC314	0x0047	Interrupt allowed, priority 7
INTC2.EIC315	0x0047	Interrupt allowed, priority 7

Table 3-5, Table 3-6
Table **2-5** lists the functions and variables used in the operation shown in Figure 3-2.

Table 3-5 Function list

Function name	Overview
main0	Main Application
tapa_init	Initialize TAPA
pic1_init	Initialize PIC1
taud0_init	Initialize TAUD0
val_init	Variable initialization
int_sin_main	Main processing of interrupt signal output
INT_SIN_DETECT_PEK	Peak interrupt signal detection process
INT_SIN_DETECT_VLY	Valley interrupt signal detection process

Table 3-6 Variable list

Variable name	Overview
u4l_int_sin_total_num	Holds the number of times an interrupt signal is detected
u4l_int_sin_peak_num	Holds the number of peak interrupts detected
u4l_int_sin_valley_num	Holds the number of valley interrupts detected

4. A/D Converter Conversion Trigger Selection Function

This chapter shows an example of using TAPA to select the A/D conversion start trigger.

4.1 Operation overview

Outputs the A/D conversion start trigger signal (TAPAnTADOUT0 or TAPAnTADOUT1) to PIC2 by selecting the trigger from the trigger signal (TAPAnTCDENS0 or TAPAnTCDENS1) from PIC2 or the valley interrupt generated by TAPA. Figure **4-1**, Figure **4-2** below shows an example of the operation outline.

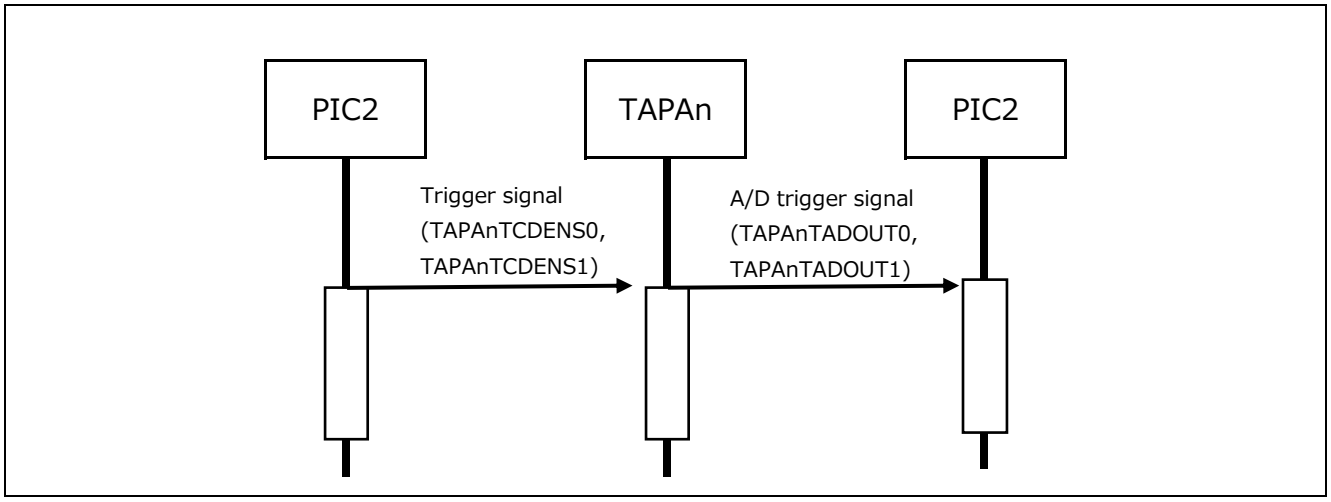

Figure 4-1 Operation when receiving signal from PIC2

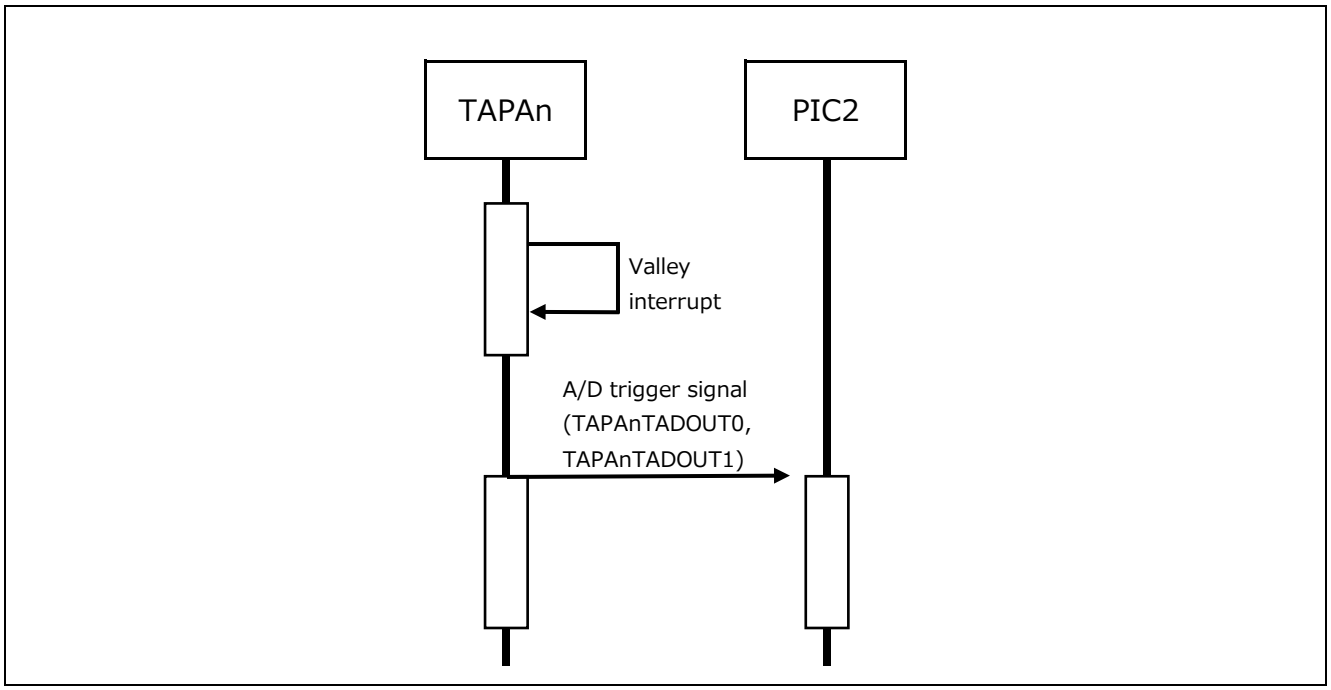

Figure 4-2 Operation when valley interrupt occurs

4.2 Operation flowchart

Figure **4-3** below shows the operational flowchart.

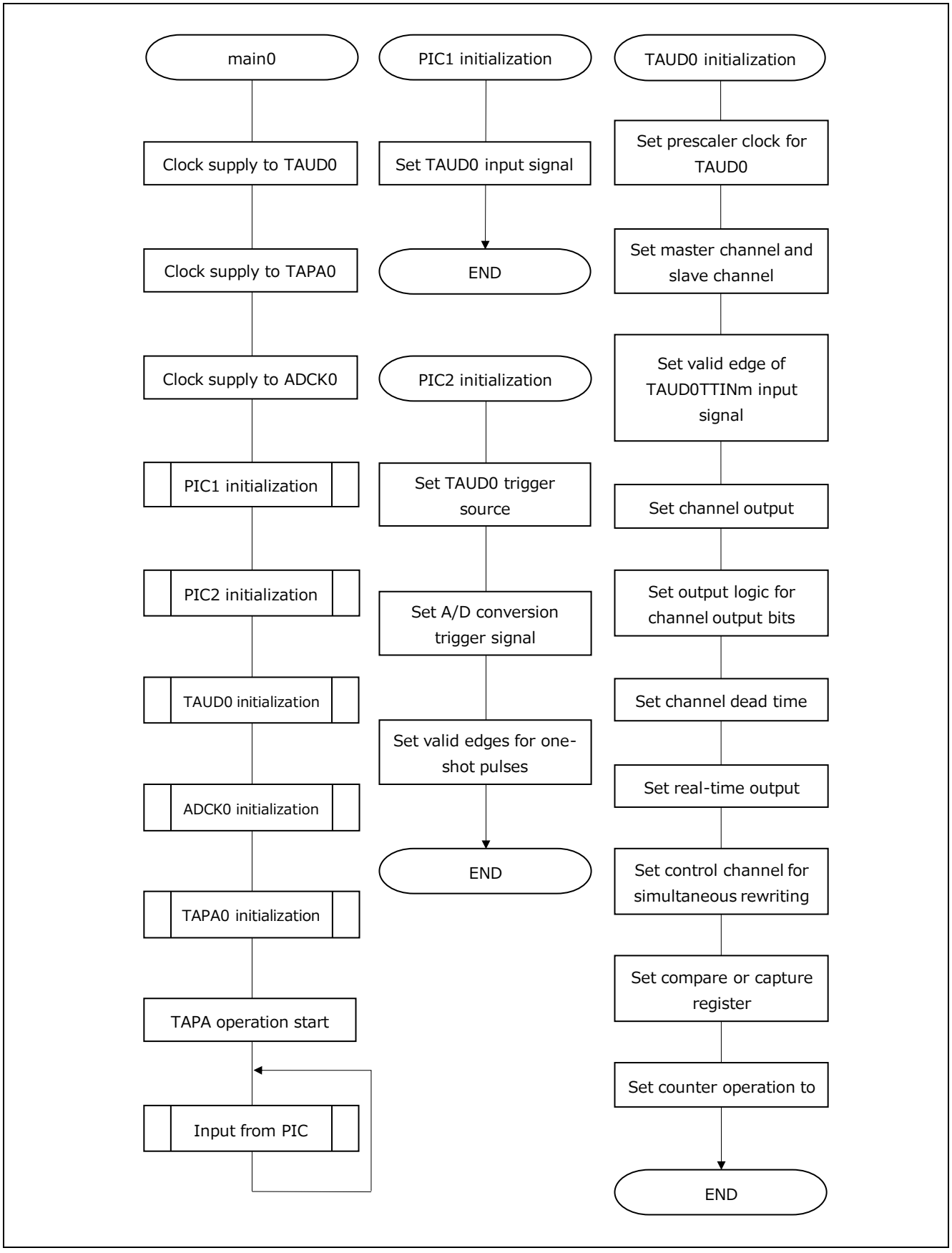

Figure 4-3 A/D conversion start trigger selection function Operation flowchart(1/2)

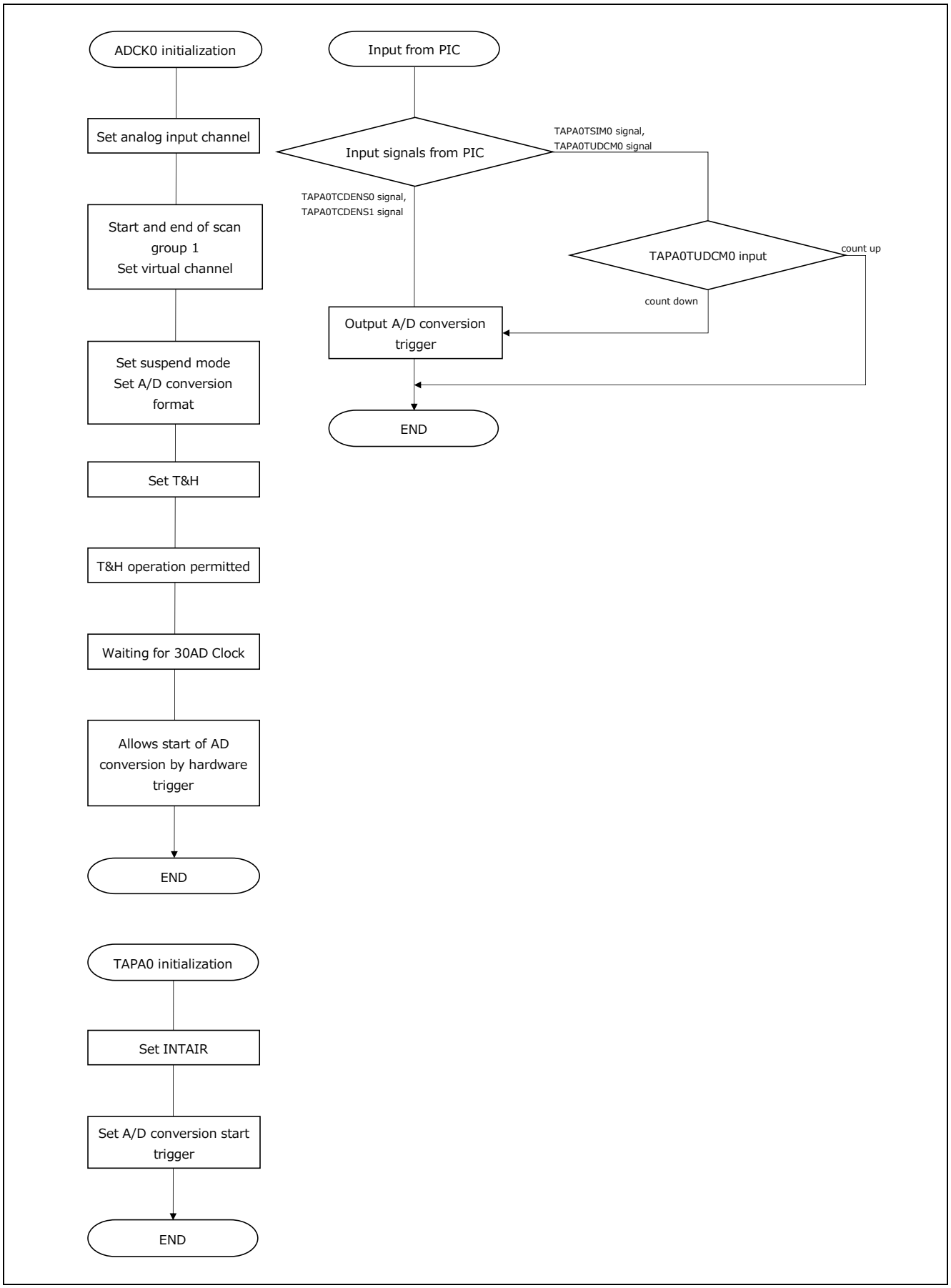

Figure4-3 A/D conversion start trigger selection function Operation flowchart(2/2)

4.3 Software description

Table **4-1** to Table 4-6Table **4-5** shows an example of each register setting used in the A/D Converter Conversion Trigger Selection Function shown in Figure **4-1**, Figure **4-3**.

Table 4-1 Register setting example (TAPA0)

Register name	Set value	Function
TAPA0CTL1	0x0002	Triggers an interrupt request at the rising edge of the triangle wave or during the rising edge, and outputs a signal to start A/D conversion.

Table 4-2 Register setting example (PIC1)

Register name	Set value	Function
PIC1REG200	0x01040A00	Set the TAUD0 input signal.

Table 4-3 Register setting example (PIC2)

Register name	Set value	Function
PIC20ADTEN400	0x0001	Select the trigger source from channel 0 of TAUD0 as ADCK trigger.
PIC20ADCK0TSEL0	0x00000000	Selects the signal that triggers the A/D conversion.
PIC21ADCK0TSEL1	0x00000080	Selects the signal that triggers the A/D conversion.
PIC20ADCK0EDGSEL	0x0000	Selects the edge that is valid for generating one-shot pulses from the signal selected by PIC20ADCK0TSEL0.
PIC21ADCK0EDGSEL	0x0000	Selects the edge that is valid for generating one-shot pulses from the signal selected by PIC21ADCK0TSEL0.

Table 4-4 Register setting example (TAUD0)

Register name	Set value	Function
TOUD0TPS	0x0001	Sets the prescaler clock for TAUD0.
TAUD0CMOR0	0x0912	TAUD0 Set channel 0 as the master channel.
TAUD0CMUR0	0x02	Sets the valid edge of the TAUD0TTINm input signal.
TAUD0CMOR1	0x0712	TAUD0 Set channel 0 as the slave channel.
TAUD0CMUR1	0x00	Sets the valid edge of the TAUD0TTINm input signal.
TAUD0TOE	0x0003	Sets the prescaler clock for TAUD0.
TAUD0TOM	0x0002	Sets the output mode for each channel of TAUD0.
TAUD0TOC	0x0002	Sets the output mode for each channel in combination with TAUD0TOM.
TAUD0TOL	0x0000	Sets the output logic of the channel output bits.
TAUD0TDE	0x0000	Sets the dead time operation of each channel.
TAUD0TDM	0x0000	Sets the timing for adding dead time when dead time is output.
TAUD0TRE	0x0000	Sets the real-time output.
TAUD0TRO	0x0000	Sets the output value to TAUD0TTOUTm.
TAUD0TRC	0x0000	Sets the real-time output for each channel.
TAUD0TME	0x0000	Sets the modulation output in timer output and real-time output.
TAUD0RDE	0x0003	Sets the simultaneous rewriting of the TAUD0CDRm/TAUD0TOLm data registers.
TAUD0RDS	0x0000	Sets the channel to control the simultaneous rewrite.
TAUD0RDM	0x0003	Sets the timing of simultaneous rewrite control signal generation.

Register name	Set value	Function
TAUD0RDC	0x0000	Sets the channel that generates the INTTAUD0Im signal and triggers simultaneous rewriting.
TAUD0CDR0	0xF000	Sets as compare register or capture register depending on the operation mode specified by TAUD0CMOR0.TAUD0MD.
TAUD0CDR1	0x7800	Set as compare register or capture register depending on the operation mode specified by TAUD0CMOR1.TAUD0MD.
TAUD0TS	0x0003	Enables counter operation for TAUD channels 0 and 1.

Table 4-5 Register setting example (ADCK0)

Register name	Set value	Function
ADCK0VCR00	0x00002000	T&H assignment of ADCK0I00 to virtual channel 0
ADCK0VCR01	0x00002001	T&H assignment of ADCK0I01 to virtual channel 1
ADCK0VCR02	0x00002002	T&H assignment of ADCK0I02 to virtual channel 2
ADCK0VCR03	0x00000004	Assign ADCK0I10 to virtual channel 3
ADCK0SGVCPR1	0x0300	VCSP = 0x00: Starts with virtual channel 0 VCEP = 0x03: Ends at virtual channel 3
ADCK0SGCR1	0x01	Scan group 1 multi-cycle mode setting Enable H/W trigger input to scan group 1
ADCK0ADCR2	0x10	Signed integer
ADCK0ADCR1	0x02	Asynchronous suspend
ADCK0THCR	0x00	T&H Sampling Mode
ADCK0THER	0x07	TH A 0-2 Permitted
ADCK0THGSR	0x0000	T&H Group A Assignment
ADCK0THACR	0x31	T&H Group A set, T&H Group A operation permitted
ADCK0THSMPSTCR	0x01	T&H sampling starts

Table 4-6 Register setting example (EIC)

Register name	Set value	Function
INTC2.EIC442	0x0047	Interrupt allowed, priority 7

Table **4-7**, Table 4-8Table **3-6**
Table **2-5** lists the functions and variables used in the operation shown in Figure **4-1**, Figure 4-3.

Table 4-7 Function list

Function name	Overview
main0	Main Application
tapa_init	Initialize TAPA
pic1_init	Initialize PIC1
pic2_init	Initialize PIC2
taud0_init	Initialize TAUD0
adck0_init	Initialize ADCK0
val_init	Variable initialization
ad_conv_main	Main processing of A/D conversion start trigger selection function
AD_CONV_COMP	A/D conversion completion interrupt signal detection processing

Table 4-8 Variable list

Variable name	Overview

u1l_ad_conv_sts	Holds the A/D conversion completion status
u4l_ad_conv_comp_cnt	Counts the number of A/D conversion completion interrupts

Table 4-9 to Table 4-14 shows an example of each register setting used in the A/D Converter Conversion Trigger Selection Function shown in Figure **4-2**, Figure **4-3**.

Table 4-9 Register setting example (TAPA0)

Register name	Set value	Function
TAPA0CTL1	0x0003	Triggered by an interrupt request at or during the rising edge of a triangular wave and a valley interrupt request, it outputs a signal to start A/D conversion.

Table 4-10 Register setting example (PIC1)

Register name	Set value	Function
PIC1REG200	0x01040A0F	Set the TAUD0 input signal.

Table 4-11 Example of register setting (PIC2)

Register name	Set value	Function
PIC20ADTEN400	0x0001	Select the trigger source from channel 0 of TAUD0 as ADCK trigger.
PIC20ADCK0TSEL0	0x00000000	Selects the signal that triggers the A/D conversion.
PIC21ADCK0TSEL1	0x00000080	Selects the signal that triggers the A/D conversion.
PIC20ADCK0EDGSEL	0x0000	Selects the edge that is valid for generating one-shot pulses from the signal selected by PIC20ADCK0TSEL0
PIC21ADCK0EDGSEL	0x0000	Selects the edge that is valid for generating one-shot pulses from the signal selected by PIC21ADCK0TSEL0

Table 4-12 Register setting example (TAUD0)

Register name	Set value	Function
TOUD0TPS	0x0001	Sets the prescaler clock for TAUD0.
TAUD0CMOR0	0x0800	TAUD0 Set channel 0 as the master channel.
TAUD0CMUR0	0x00	Sets the valid edge of the TAUD0TTINm input signal.
TAUD0CMOR1	0x0712	TAUD0 Set channel 0 as the slave channel.
TAUD0CMUR1	0x00	Sets the valid edge of the TAUD0TTINm input signal.
TAUD0TOE	0x0003	Sets the prescaler clock for TAUD0.
TAUD0TOM	0x0002	Sets the output mode for each channel of TAUD0.
TAUD0TOC	0x0002	Sets the output mode for each channel in combination with TAUD0TOM.
TAUD0TOL	0x0000	Sets the output logic of the channel output bits.
TAUD0TDE	0x0000	Sets the dead time operation of each channel.
TAUD0TDM	0x0000	Sets the timing for adding dead time when dead time is output.
TAUD0TRE	0x0000	Sets the real-time output.
TAUD0TRO	0x0000	Sets the output value to TAUD0TTOUTm.
TAUD0TRC	0x0000	Sets the real-time output for each channel.
TAUD0TME	0x0000	Sets the modulation output in timer output and real-time output.
TAUD0RDE	0x0003	Sets the simultaneous rewriting of the TAUD0CDRm/TAUD0TOLm data registers.
TAUD0RDS	0x0000	Sets the channel to control the simultaneous rewrite.
TAUD0RDM	0x0003	Sets the timing of simultaneous rewrite control signal generation.

Register name	Set value	Function
TAUD0RDC	0x0000	Sets the channel that generates the INTTAUD0Im signal and triggers simultaneous rewriting.
TAUD0CDR0	0xF000	Sets as compare register or capture register depending on the operation mode specified by TAUD0CMOR0.TAUD0MD.
TAUD0CDR1	0x7800	Set as compare register or capture register depending on the operation mode specified by TAUD0CMOR1.TAUD0MD.
TAUD0TS	0x0003	Enables counter operation for TAUD channels 0 and 1.

Table 4-13 Register setting example (ADCK0)

Register name	Set value	Function
ADCK0VCR00	0x00002000	T&H assignment of ADCK0I00 to virtual channel 0
ADCK0VCR01	0x00002001	T&H assignment of ADCK0I01 to virtual channel 1
ADCK0VCR02	0x00002002	T&H assignment of ADCK0I02 to virtual channel 2
ADCK0VCR03	0x00000004	Assign ADCK0I10 to virtual channel 3
ADCK0SGVCPR1	0x0300	VCSP = 0x00: Starts with virtual channel 0 VCEP = 0x03: Ends at virtual channel 3
ADCK0SGCR1	0x01	Scan group 1 multi-cycle mode setting Enable H/W trigger input to scan group 1
ADCK0ADCR2	0x10	Signed integer
ADCK0ADCR1	0x02	Asynchronous suspend
ADCK0THCR	0x00	T&H Sampling Mode
ADCK0THER	0x07	TH A 0-2 Permitted
ADCK0THGSR	0x0000	T&H Group A Assignment
ADCK0THACR	0x31	T&H Group A set, T&H Group A operation permitted
ADCK0THSMPSTCR	0x01	T&H sampling starts

Table 4-14 Register setting example (EIC)

Register name	Set value	Function
INTC2.EIC315	0x0047	Interrupt allowed, priority 7
INTC2.EIC442	0x0047	Interrupt allowed, priority 7

Table 4-15, Table 4-16Table **3-6**
Table **2-5** lists the functions and variables used in the operation shown in Figure **4-2**, Figure 4-3.

Table 4-15 Function list

Function name	Overview
main0	Main Application
tapa_init	Initialize TAPA
pic1_init	Initialize PIC1
pic2_init	Initialize PIC2
taud0_init	Initialize TAUD0
adck0_init	Initialize ADCK0
val_init	Variable initialization
ad_conv_main	Main processing of A/D conversion start trigger selection function
AD_CONV_VLY_INT	Valley interrupt signal detection processing
AD_CONV_COMP	A/D conversion completion interrupt signal detection processing

Table 4-16 Variable list

Variable name	Overview
u1l_ad_conv_sts	Holds the A/D conversion completion status
u4l_ad_conv_comp_cnt	Count the number of A/D conversion completion interrupts
u4l_ad_conv_valley_cnt	Count the number of valley interrupts

Revised record

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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