RH850/U2x Group

R01AN7505EJ0200
Rev.2.00

SFMA Application Note

Introduction

RH850/U2B series and RH850/U2C series provide Serial flash memory interface (SFMA) for external NOR or NAND serial flash memory.

This document provides a general introduction of serial flash memory type, SFMA configuration flow and sample software.

Target Device

This document describes the SFMA sample software on RH850/U2B Group and RH850/U2C Group (hereinafter referred to as U2x).

Used device for sample application are RH850/U2B R7F702Z21EDBA and RH850/U2C R7F702613. Concept described in this document applies to all member of U2x Group which have SFMA.

Presence of SFMA in RH850/U2B Group

Product name Package	RH850/U2B24 468pins	RH850/U2B24 373pins	RH850/U2B10 468pins	RH850/U2B10 373pins	RH850/U2B10 292pins	RH850/U2B6 292pins
Number of units	1	1	1	1	1	1
Name	SFMAn (n=0)					

Presence of SFMA in RH850/U2C Group

Product name Package	RH850/U2C8-EVA BGA404pins	RH850/U2C8 BGA292pins	RH850/U2C4 BGA292pins	RH850/U2C4 QFP100/144pins	RH850/U2C2 QFP100/144pins
Number of units	1	1	1	1	1
Name	SFMAn (n=0)				

Disclaimer

Table of Contents

1. Serial flash memory types

There two type of non-volatile serial flash memory – NOR and NAND. The names stand for different logic gate used in the memory. Commercial NOR flash memory was first introduced by Intel in 1988. NAND flash was introduced by Toshiba in 1989.

One of the main differences is capacity, NAND flash have higher density than NOR flash. The other difference is access speed - NAND flash is faster than NOR flash. In both types NOR and NAND, memory is organized in sectors, blocks and pages. Before write to those memories, you need to erase the cell, the smallest part to write is sector, the volume of it depends on producer how they make their product memory map. In both memory information is accessible by byte, but write access is always by smallest part – sector, hence you can't write only one byte of data, always need to write the complete sector at byte level. Serial flash memories support SPI protocol.

In this document used serial flash memory is NOR, with smallest sector to write/erase of 4KB, organized in 16383 sectors of 4KB or 2047 Blocks of 32KB or 1023 block of 64 KB in total 512Mb or 64MB.

2. RH850/U2x Serial Flash Memory Interface A

In RH850/U2x devices line are implemented serial flash memory interface A periphery. SFMA is part of H-Bus, outputs control signal to external serial flash memory are connected to the SPI multi I/O bus space, thus enable direct connection to external serial flash memory.

Module allows two types of access to external serial flash memory – SPI operating mode for read/write operation and External Address space read operating mode only for read operation.

SFMA set in External Address space read operating mode, translate read operation from internal address space

(3800 0000_H to 3BFF $FFFF_H$) to SPI bus sequence.

2.1 Overview

2.1.1 External Input/Output signals

SFMA module allow only one external serial flash memory to be connected to the device.

This module is available only in Port20 in U2B Group and Port17 in U2C Group.

Table 1 External Input/Output Signals (RH850/U2x)

Unit signal name	Description	Alternative port Pin Signal
SFMA0		
SPBCLK	Clock output	SFMA0CLK
SPBSSL	Slave select	SFMA0SSL
SPBMO/SPBIO0	Master transmit data/Data 0	SFMA0IO0
SPBMI/SPBIO1	Master input data/Data 1	SFMA0IO1
SPBIO2	Data 2	SFMA0IO2
SPBIO3	Data 3	SFMA0IO3

2.1.2 Clock supply

- Register access clock is CLKC_HSB_SFMA
- Bϕ source clock is CLKC_HSB_SFMA – for SFMA bit rate generator, generated by division of Bϕ. Maximum bit rate is 40MHz.

2.1.3 Reset sources

- All reset sources except for JTAG reset sources.

2.1.4 Interrupt sources

- SFMAn has no interrupts, DMA/DTS requests and no error notifications.

2.1.5 Registers

SFMA module have 18 registers separated in four types with base address 10040000_H.

1. Common control registers – for setting bit rate, SSL delay and communication transfer bus dimension
2. Data read control registers – for setting up an External Address space read operating mode
3. SPI mode registers – for setting up a SPI operating mode
4. Common status register

Table 2,3,4 and 5 show the function of Common Control register, Data Read register, SPI mode register and Common status register.

Table 2 Common Control Registers

Register Name	Function
SFMA0CMNCR	Select mode, data sampling timing, select SPBSSL's polarity
SFMA0SSLDR	Setting delay cycles
SFMA0SPBCR	Setting bit rate parameter: (n, N) Using follow formula Bit rate＝Bϕ/(2×n×2^N)

Table 3 Data read control registers

Register Name	Function
SFMA0DRCR	Setting normal or burst read, burst read length, SSL auto negation, cache flush
SFMA0DRCMR	Command, Optional command
SFMA0DREAR	Setting upper 6bits of serial flash address in External Address Space Read Mode
SFMA0DROPR	Store optional data
SFMA0DRENR	Setting data bus size, determine enable
SFMA0DRDMCR	Setting dummy cycles

Table 4 SPI mode registers

Register Name	Function
SFMA0SMCR	Setting Read/Write of SPI Operating Mode, enable of transmit and maintaining SPBSSL
SFMA0SMCMR	Setting command and optional command
SFMA0SMADR	Setting Address
SFMA0SMOPR	Setting optional data
SFMA0SMENR	Setting data bus size, determine enable
SFMA0SMRDR	Store read data
SFMA0SMWDR	Store write data
SFMA0SMDMCR	Setting dummy cycles

Table 5 Common status registers

Register Name	Function
SFMA0CMNSR	Showing SPBSSL Pin Monitor and Transfer End Flag

2.1.6 Block diagram

Figure 1 SFMA block diagram shows block diagram of SFMA module.

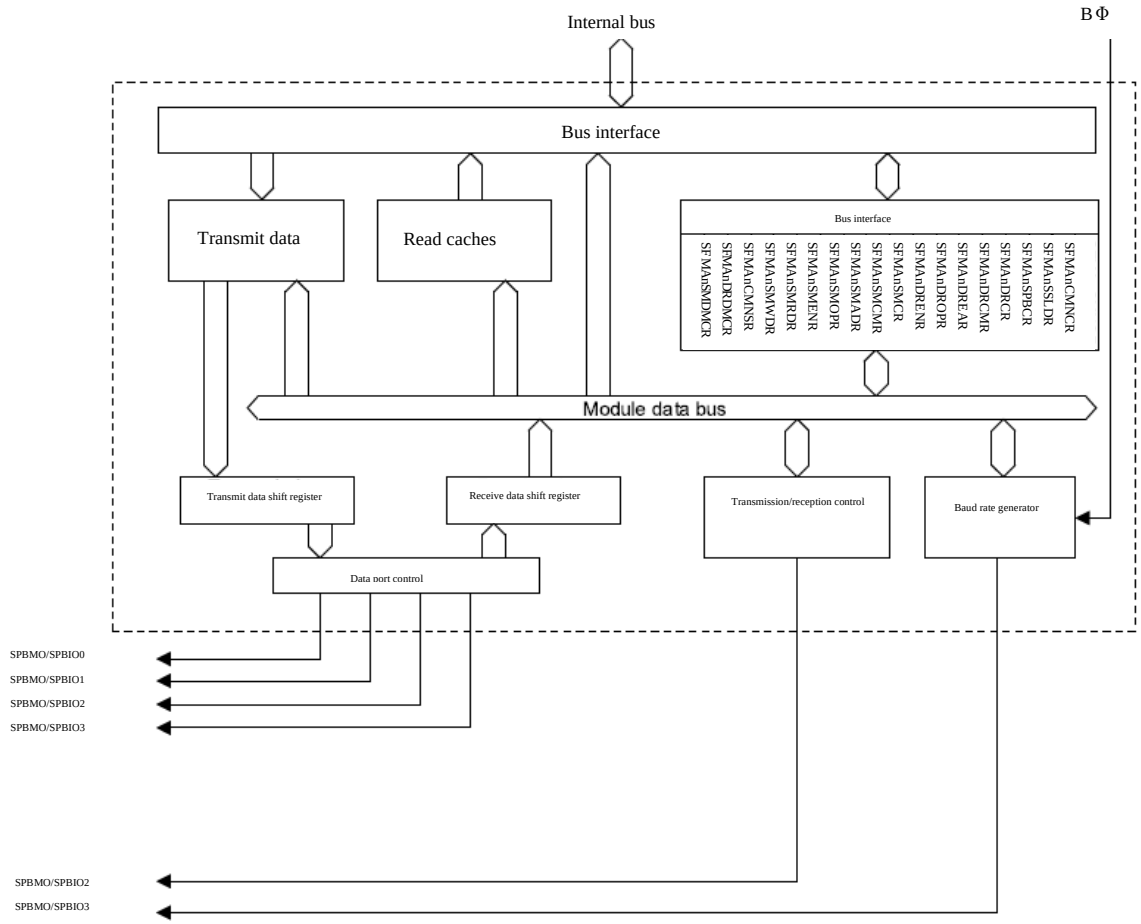


Figure 1 SFMA block diagram

2.1.7 Bit rate calculation

Bit rate for SFMA module is calculated of SPBR[7:0] and BRDV[1:0] set in register SFMAnSPBCR.

$$\text{Bit rate} = \frac{\text{B}\phi}{(2 * \text{SPBR}[7:0] * 2^{\text{BRDV}[1:0]})} \text{ [MHz]}$$

Bϕ=CLKC_HSB_SFMA (80MHz)

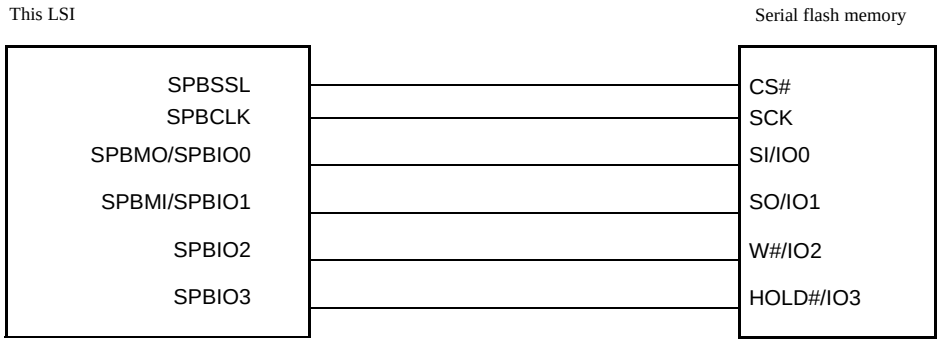
SPBR[7:0] is prohibited to be 0, before SFMA start SPI operation SPBR[7:0] need to be changed to non-zero value

2.2 Operation modes

2.2.1 System configuration

SFMA module support 3 type of SPI bus data size – 1bit, 2bit and 4bit

Figure 2 SFMA system configurationshows system configuration of SFMA module.



Note: Figure shows 4bit data size bus.
Recommendation is to attach external flash memory always like 4bit data size. SPBIO2, SPBIO3 can be configured durigng negation and idle period, when use 1bit or 2bit data size bus,to be on state which corespond with external memory demands for hold, word tansfer or hw write protection.

Notes: 1. Common used pin in independent of data bus size are SPBSSL, SPBCLK
2. 1bit size – used pin are SPBMO and SPBMI
3. 2bit size – used pin are SPBIO0 and SPBIO1
4. 4bit size – used pin are SPBIO0, SPBIO1, SPBIO2, SPBIO3

Figure 2 SFMA system configuration

2.2.2 SPI operating mode

SFMA SPI operating mode support 1bit, 2bit, and 4bit data size bus. Can transfer 8bit or 16bit command, 24bit or 32bit address as well as option bytes – 1byte, 2byte, 3byte or 4 bytes. SFMA SPI read operation can be perform only in 8bit, 16bit or 32bit – all other states are forbidden.

- If it is needed to transfer only command to external flash memory it is important to set SPIDE[3:0] in SFMAnSMENR to 0000, no matter if SPIRE=0 in SFMAnSMCR. Some serial flash memory accept command only when SSL pin goes high at the end of the command send ends. To be able SFMA to fulfil this demand, above suggestion should be kept.
- When use 2bit or 4bit data size bus – it is forbidden Read and Write operation to be set in SFMAnSMCR at the same time
- External serial flash support auto increment address during Read and Write operation for faster access, once first address is sent it is automatically increment when read or write access is issued – in this case SSL signal should be kept low during all operation and goes high after operation is completed – this is controlled by SSLKP bit in SFMAnSMCR

  Figure 3 SPI Operating Mode timing chartshows timing chart which is SPBSSL kept asserted.

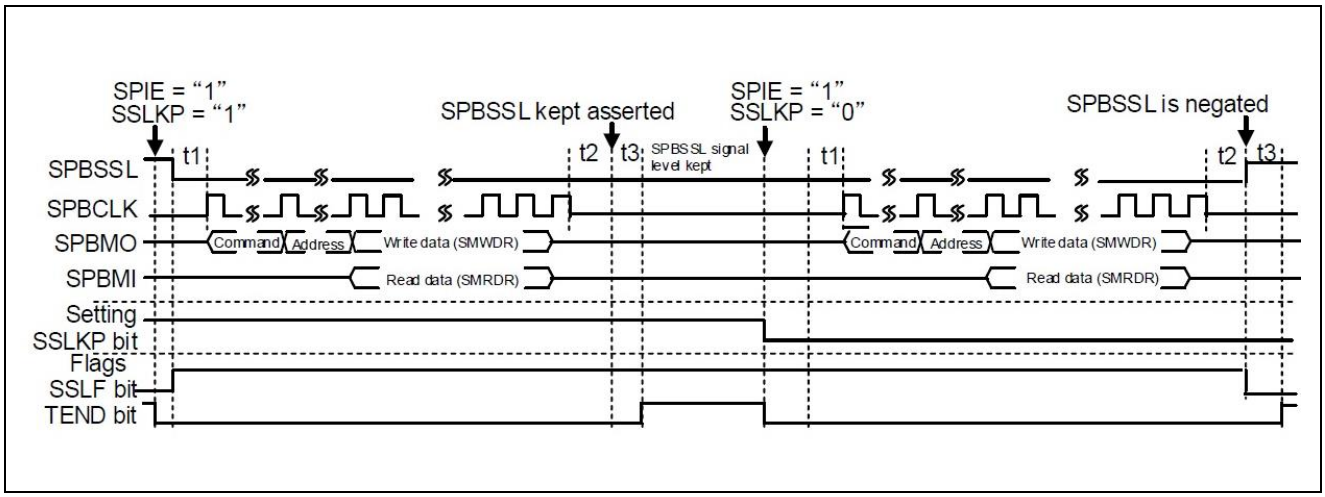


Figure 3 SPI Operating Mode timing chart

- In 2bit or 4bit data size some serial flash needs dummy cycle after address transfer to be send – bus size of dummy cycle is controlled by DMDB[1:0] in SFMAnSMDMCR register the number of dummy cycle are controlled by DMCYC[2:0] in SFMAnSMDMCR register. Enable or disable transfer of dummy cycles is controlled by DME bit in SFMAnSMENR register. SFMA support from 1 to 8 cycles.

2.2.3 SPI initial setting flow

Figure 4 SPI initial setting flow shows initial setting flow of SPI Operating mode.

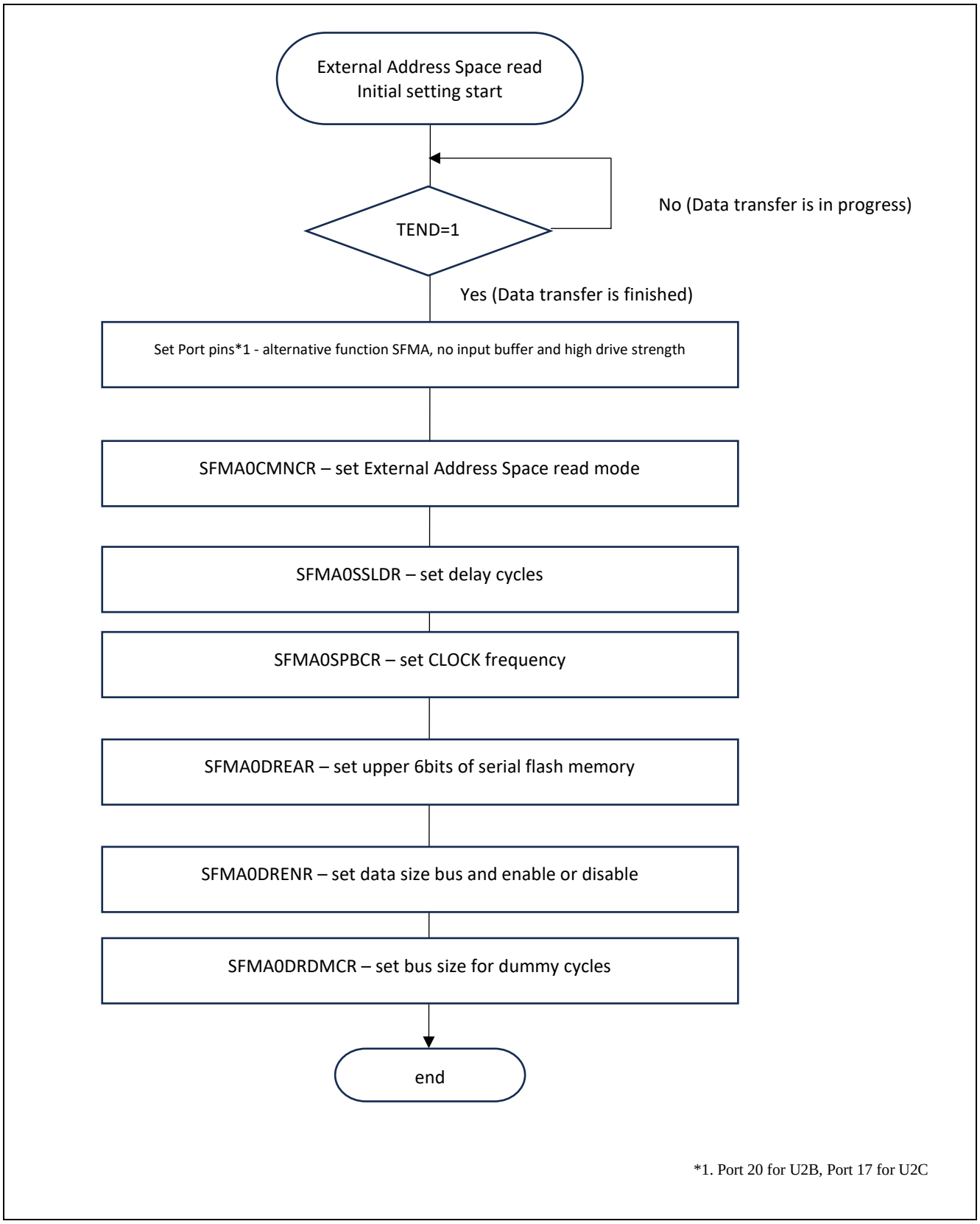


Figure 4 SPI initial setting flow

2.2.4 External Address Space Read Mode

SFMA External Address Space Read mode support 1bit, 2bit, and 4bit data size bus. Can transfer 8bit or 16bit command, 24bit or 32bit address as well as option bytes – 1byte, 2byte, 3byte or 4 bytes.

- In this mode, external serial flash memory is connected to the SPI multi I/O bus space. With other words read access issued to internal address (3800 0000_H to 3BFF $FFFF_H$) will be transform to SPI bus sequence. Since this space is only 64MB, only part of external serial flash can be accessed. To extend up to 4GB address space SFMA module have SFMAnDREAR — Data Read Extended Address Setting Register, where upper 6bits of 32-bit serial flash address can be stored.

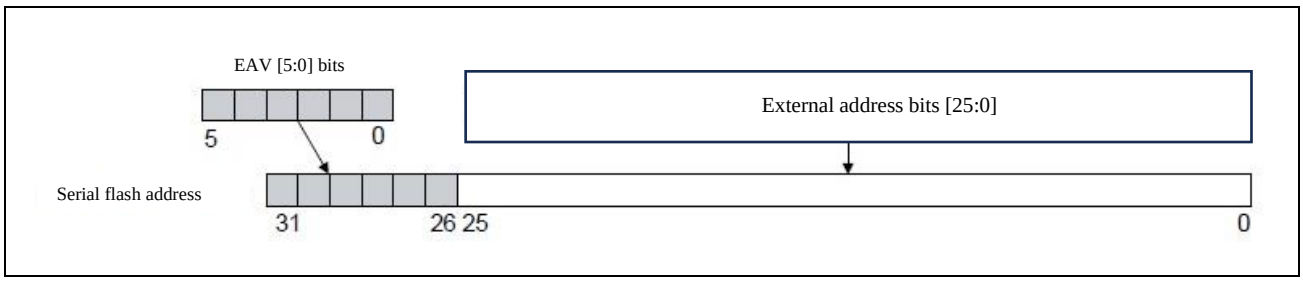


Figure 5 32-bit address setting

- In 2bit or 4bit data size some serial flash needs dummy cycle after address transfer to be send – bus size of dummy cycle is controlled by DMDB[1:0] in SFMAnDRDMCR register the number of dummy cycle are controlled by DMCYC[2:0] in SFMAnDRDMCR register. Enable or disable transfer is controlled by DME bit in SFMAnDRENR register. SFMA support from 1 to 8 cycles.
- In normal External Address Space Read operation – read can be issued by byte, halfword or word depends on the internal address space access issued. Figure 6 Normal read operation shows timing chart of Normal read operation.
- External Address Space Read mode support also burst read – in this mode read operation is always 64bits. This mode can use built-in read cache with size of 64bits and 16 entries. Figure 7 Burst read operationshows timing chart of Burst read operation.

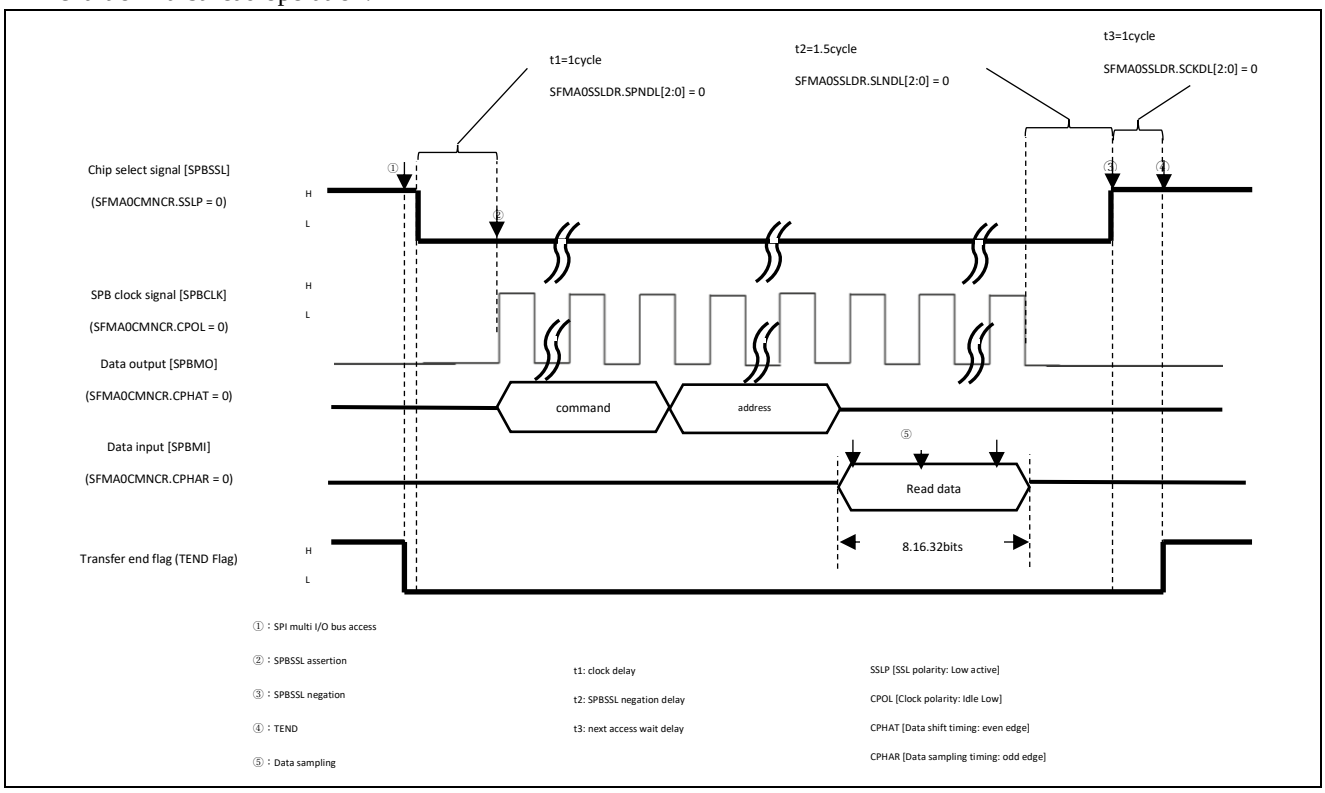


Figure 6 Normal read operation

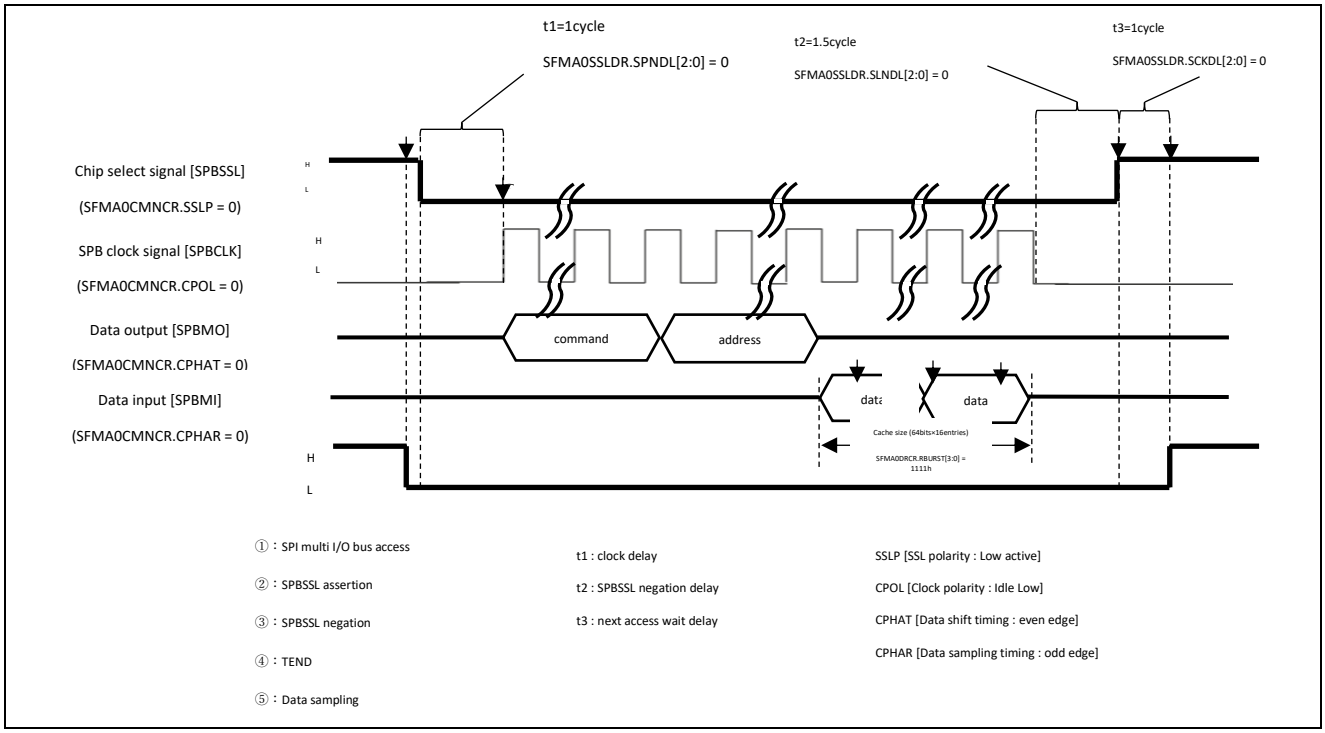


Figure 7 Burst read operation

2.2.5 External address space initial setting flow

Figure 8 External address space initial setting flowshows initial setting flow of External address space read mode.

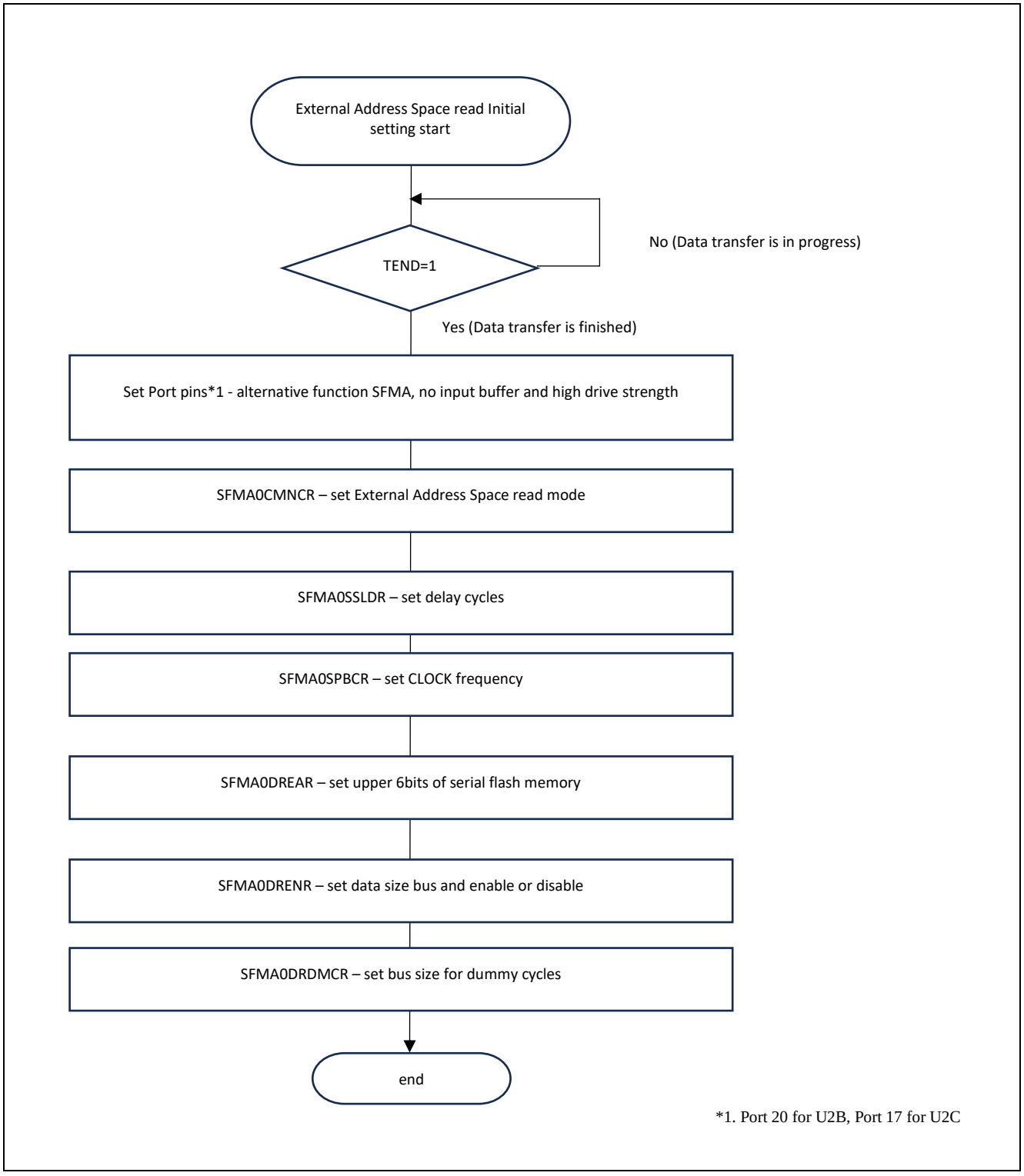


Figure 8 External address space initial setting flow

3. Software and hardware tools

This section contains information what tools and hardware development platform are used to implement SFMA samples software

3.1 Software development tools

- Compiler used for sample SFMA software is CS+
- Debug probe – Renesas E2 emulator

3.2 Hardware development tools

- Main board - Y-RH850-X2X-MB-T1-V1, the last version of this document can be obtained from the following web location: Y-RH850-X2X-MB-T1-V1 Documents
- Piggyback board for U2B Group - Y-RH850-U2B-292PIN-PB-T1-V1 with mounted device RH850/U2B10-FCC R7F702Z21EDBA, the latest document can be obtained from the following web location: Y-RH850-U2B-373PIN-PB-T1-V1 Documents
- Piggyback board for U2C Group – Y-RH850-U2C-292PIN-PB-T1-V1 with mounted device RH850/U2C4 R7F702613.
- Peripheral module eMMC/SFMA Y-RH850-EMMC-SFMA-EXT-BRD. The extension board includes one eMMC IC (swissbit SFEM4096B1EA1, 4GB NAND flash) and one serial flash NOR IC (Macronix MX25L51245GMISFMA, 512Mbit). Schematic and description of connection are described in Y-RH850-X2X-MB-T1-V1 user manual section 4.10 eMMC/SFMA module.

3.2.1 Setup hardware tools

This section describes how to connect main board, Piggyback board, and peripheral module

- Peripheral module eMMC/SFMA by default have main board connection to CN2. Jumper JP2 (Figure 9 Peripheral module eMMC/SFMA - RH850-EMMC-SFMA-EXT-BRDred ellipse) should be applied to power supply serial flash IC.
- Connection between U2x target device on Piggyback board and serial flash IC should be done by CN98 and CN2 (Figure 10 Connection Piggyback board to peripheral module eMMC/SFMA). Please refer to Table 6 Connection table for U2B Group between Piggyback board and peripheral module eMMC/SFMAand Table **7** Connection table for U2C Group between Piggyback board and peripheral module eMMC/SFMA.

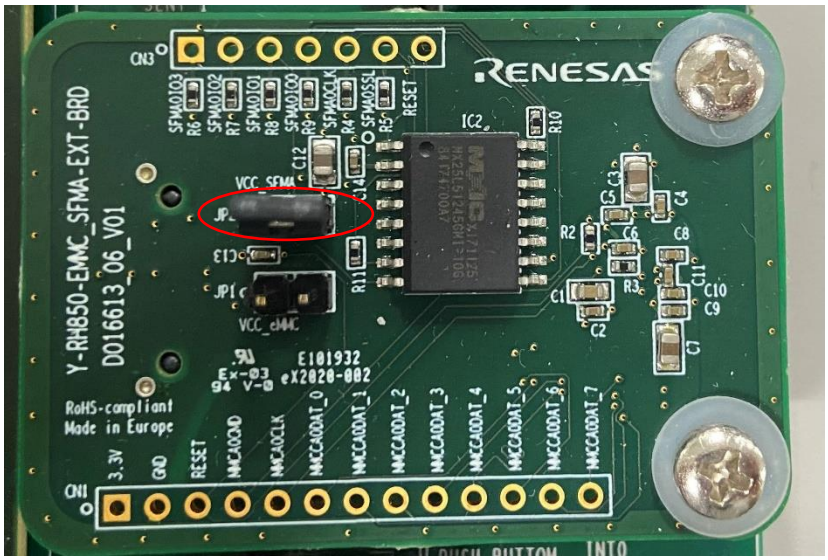


Figure 9 Peripheral module eMMC/SFMA - RH850-EMMC-SFMA-EXT-BRD

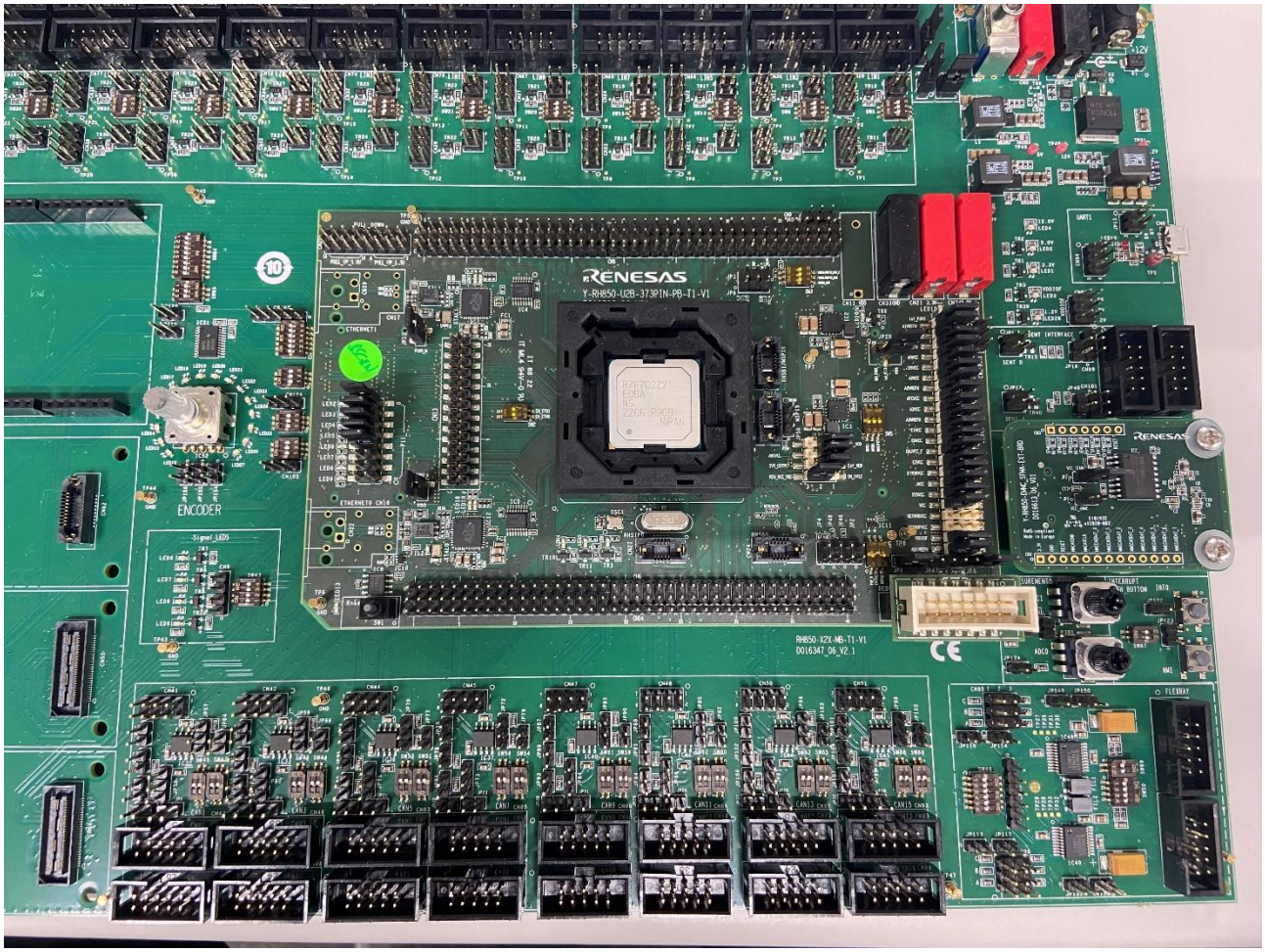


Figure 10 Connection Piggyback board to peripheral module eMMC/SFMA

Table 6 Connection table for U2B Group between Piggyback board and peripheral module eMMC/SFMA

SFMA signal name	Alternative port Pin Signal	Device port	Alternative mode	U2B10-373pin device	Piggyback board RH850/U2B-373pin	eMMC/SFMA extension module
		Port20		Pin	CN2	CN98
SPBCLK	SFMA0CLK	Port20_4	ALT_OUT6	AC6	CN2_79	CN98_4
SPBSSL	SFMA0SSL	Port20_5	ALT_OUT6	AD6	CN2_80	CN98_6
SPBMO/SPBIO0	SFMA0IO0	Port20_0	ALT_IN6, ALT_OUT6	AB6	CN2_81	CN98_7
SPBMI/SPBIO1	SFMA0IO1	Port20_1	ALT_IN6, ALT_OUT6	AC5	CN2_82	CN98_5
SPBIO2	SFMA0IO2	Port20_2	ALT_IN6, ALT_OUT6	AD5	CN2_83	CN98_3
SPBIO3	SFMA0IO3	Port20_3	ALT_IN6, ALT_OUT6	AE5	CN2_84	CN98_1

Table 7 Connection table for U2C Group between Piggyback board and peripheral module eMMC/SFMA

SFMA signal name	Alternative port Pin Signal	Device port	Alternative mode	U2C4 BGA292 device	Piggyback board RH850/U2C-292pin	eMMC/SFMA extension module
		Port17		Pin	CN2	CN98
SPBCLK	SFMA0CLK	Port17_5	ALT_OUT9	J1	CN2_79	CN98_4
SPBSSL	SFMA0SSL	Port17_4	ALT_OUT9	H2	CN2_80	CN98_6
SPBMO/SPBIO0	SFMA0IO0	Port17_3	ALT_IN9, ALT_OUT9	H1	CN2_81	CN98_7
SPBMI/SPBIO1	SFMA0IO1	Port17_2	ALT_IN9, ALT_OUT9	G2	CN2_82	CN98_5
SPBIO2	SFMA0IO2	Port17_1	ALT_IN9, ALT_OUT9	G1	CN2_83	CN98_3
SPBIO3	SFMA0IO3	Port17_0	ALT_IN9, ALT_OUT9	G4	CN2_84	CN98_1

4. Sample SFMA software

This section describes SFMA sample software

- Location of SFMA driver – {Project folder} \src
- Contain 5 file – main0.c, r_tasks.c, r_tasks.h, r_sfma.c and r_sfma.h

4.1 Functions description in sfma.c

The following shows the sample code which is used in operating example of SFMA and registers setting value.

Table 8 SFMA module Functions list shows the functions list of sample code.

Table 8 SFMA module Functions list

Function name	Function
void delay(uint32_t ms)	Make a delay
void R_SFMA_DeInit(void)	Put SFMA module register in reset state
r_Error_t R_SFMA_Init(uint32_t mode, uint32_t bus_size)	Set SFMA module to SPI or Address space mode and set SPI bus size to 1, 2, or 4bits
uint32_t R_SFMA_ExecCmd(uint8_t cmd, uint16_t response)	Send command via SFMA to external flash memory, return read value if desired
void R_SFMA_SECTORERASE4B(uint32_t address)	Execute sector erase sequence: WREN(write enable command) then Erase commands
void R_SFMA_ReadSPI4B(uint32_t readAddress,uint32_t byteNum,char_t * readBuff)	Read desire bytes from given address in external flash memory and store it in pointed buffer
void R_SFMA_WriteSPI4B(uint32_t writeAddress,uint32_t byteNum,char_t * writeBuff)	Execute write sequence, Sector Erase ->WREN -> write desire bytes to external flash to given address from pointed buffer

Table 9 shows the registers setting value in SPI Operating mode and External Address Space read mode.

Table 9 Register setting value in this sample code

Register name	Mode	Setting value	Function
SFMA0CMNCR	SPI mode	0x80FFF300	Select mode: SPI mode
			CPHA: Even shift, odd sampling
			SPBSSL's polarity: Active low
			Clock's polarity: Positive
			Idle fix value and 1-bit/2-bit size fix value: Hi-Z
	Quad SPI mode	0x80000000	Select mode: SPI mode
			CPHA: Even shift, odd sampling
			SPBSSL's polarity: Active low
			Clock's polarity: Positive
			Idle fix value and 1-bit/2-bit size fix value: 0
	External Address Space read mode	0x00FFF300	Select mode: External Address Space read mode
			CPHA: Even shift, odd sampling
			SPBSSL's polarity: Active low
			Clock's polarity: Positive
			Idle fix value and 1-bit/2-bit size fix value: Hi-Z
SFMA0SSLDR	common	0x00000000	Clock delay: 1cycle
			Negate delay: 1.5cycle
			Wait delay: 1cycle
SFMA0SPBCR	common	0x00000400	Bit rate: 10MHz
SFMA0SMCR	SPI/Quad SPI mode	0x00000107	SSLKP: 1
			Data read: Enable
			Data write: Enable
			Transfer: Enable
SFMA0SMCMR	SPI/Quad SPI mode	0	Store commands: When initialize SPI, setting initial value
SFMA0SMADR	SPI/Quad SPI mode	0	Store address (initial value)
SFMA0SMOPR	SPI/Quad SPI mode	0	Store optional data (initial value)
SFMA0SMENR	SPI mode	0x00004F0F	Bus size:1bit
			Address: 32bit
			Commands Enable
	Quad-SPI mode	0xA222CF0F	Data size bus: 4bits
			Address: 32bits
			Commands Enable
			Dummy cycles Enable

SFMA0SMRDR	SPI/Quad SPI mode	-	Read shift data（no initial value）
SFMA0SMWDR	SPI/Quad SPI mode	0	Store write data
SFMA0SMDMCR	SPI mode	0	Don't use (initial value)
	Quad-SPI mode	0x00000003	Setting number of dummy cycles: select 4cycles
		0x00000005	Setting number of dummy cycles: select 6cycles
		0x00000007	Setting number of dummy cycles: select 8cycles
SFMA0DRCR	External Address Space read mode	0x000F0300	Read mode: Burst Read
			Cache read length: 64bits×16
SFMA0DRCMR		0x00030000	Store commands: Initial Value
SFMA0DREAR		0x00000001	Store upper 6bits of Address
SFMA0DROPR		0	Store optional data: Don't use (Initial Value)
SFMA0DRENR		0x00004F00	Address: 32bits enable
			Commands: Enable
			Data size bus: 1bit
SFMA0DRDMCR		0	Dummy cycles setting: Don't use

4.2 Sample SFMA Software Block Schema

Figure 11 shows a flowchart of sample software in r_tasks.c.

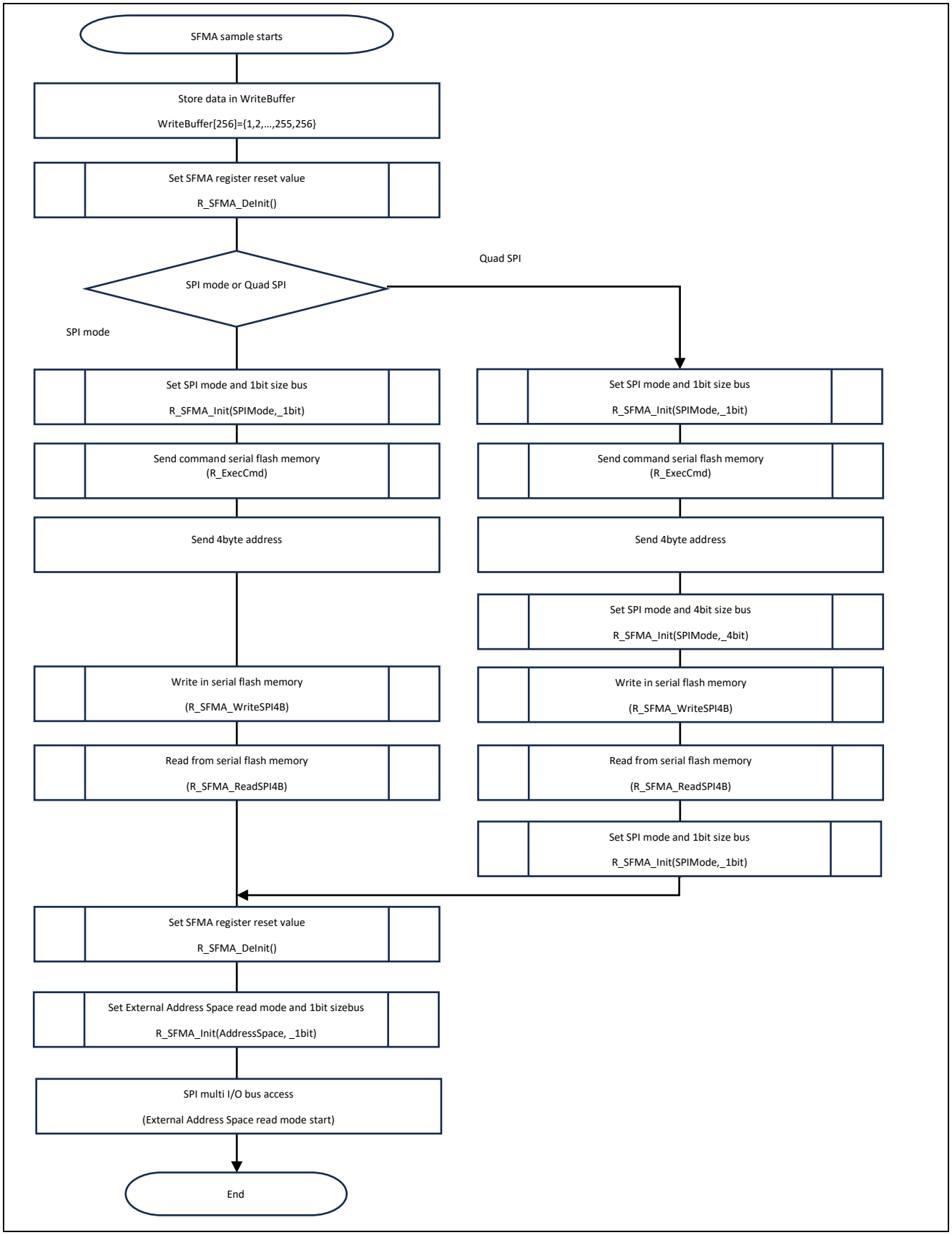


Figure 11 Flowchart of Sample S/W in r_tasks.c

Revision History

Rev.	Data	Description	
		Page	Summary
1.00	2024.9.25	—	Initial issue
2.00	2024.12.23	—	Added U2C as a support target.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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