RH850/U2B

Input control by GTM (TIM)

Summary

This application note describes how to realize input control by GTM (TIM) on the RH850/U2B6.

Although the examples of tasks and applications examples in this application note have been confirmed to work, please be sure to check the operating environment before using the product.

Operation confirmation device

RH850/U2B6-FCC (R7F702Z22EDBB).

Table of contents

1. Introduction

In this application note, describes how to implement input control using GTM (TIM) on the RH850/U2B6-FCC.

The functions described in this application note are listed below.

- Count start trigger function
- Timeout interrupt generation function
- Count capture trigger function

1.1 The function to be used

The RH850/U2B6 hardware functions used in this application note are shown below.

Also, in this application note, each hardware function is controlled from CPU0.

Hardware function name	Symbol
Enhanced Motor control Unit 3 S	EMU3S
Clock Management Unit	CMU
Timer Input Module	TIM
Peripheral Interconnect	PIC

2. Input control by GTM (TIM)

This chapter describes how to implement input control using GTM (TIM). Below is a schematic diagram of the GTM (TIM) used this time. The details of operation are explained in the section of each function.

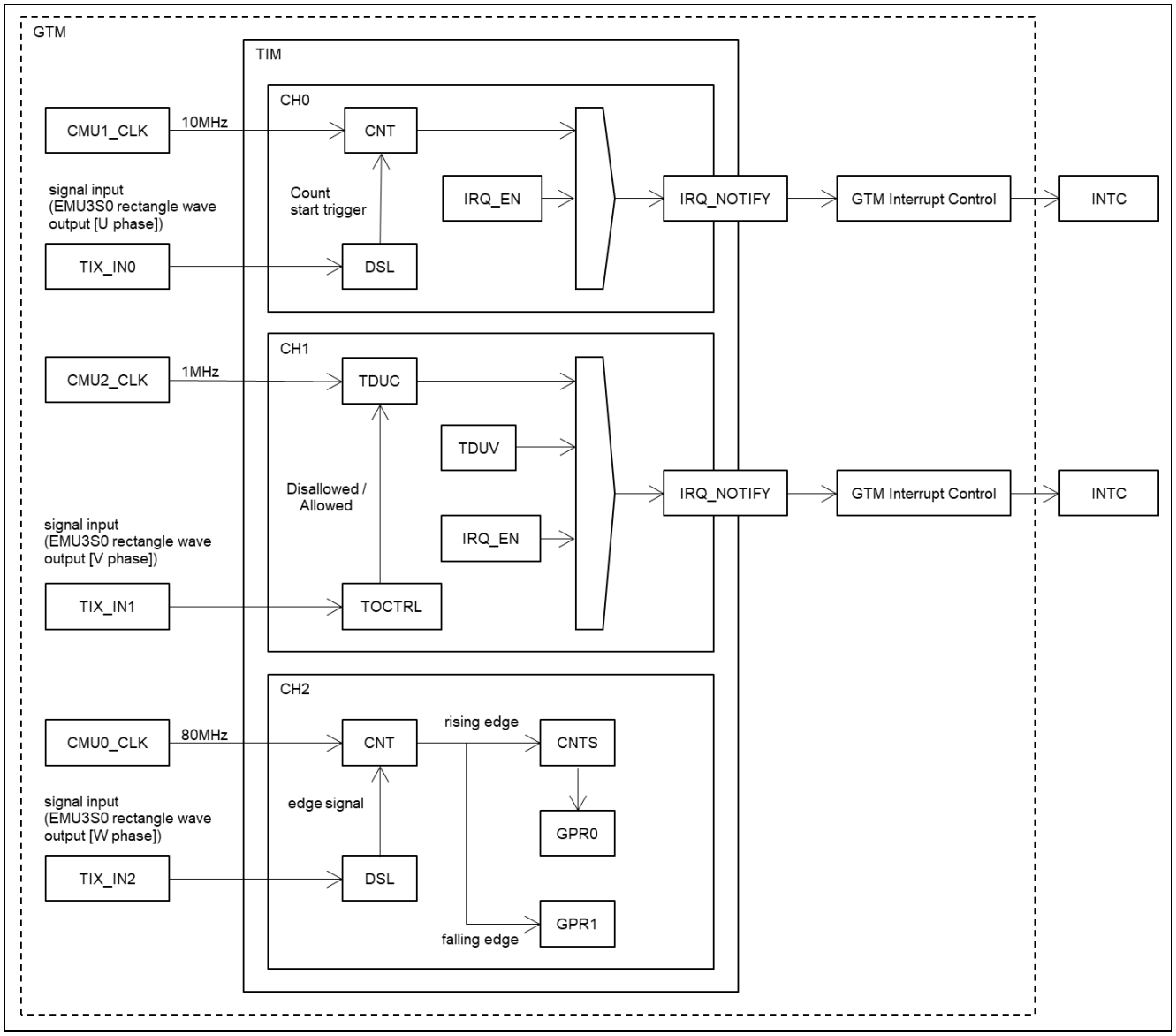

Figure 2-1 Schematic diagram of the GTM (TIM)

2.1 Common settings

The following describes common settings used in this application.

2.1.1 GTM clock supply

GTM is clocked from CLK_GTM to GTM main clock. The clock source for CLK_GTM is selected by an Option Byte (CKSEL_GTM). In this application, the Option Byte is set as the GTM main clock 160 MHz. Table 2-1 shows the Option Byte settings.

Table 2-1 OPBT setting

Register name	Set value	Description
Option Byte 8 (CKSEL_GTM)	CKSEL_GTM : 0x1	Clock source select for GTM 0x1 : CLKC_UHSB (160MHz)

2.1.2 GTM register common setting

To set the GTM registers, the reset function of the GTM Global control register must be enabled once. Also, the clock supply to each cluster of GTMs is deactivated and must be enabled. In this application, the clock supply is enabled by divider 2 so that the clock supply for Cluster0 is 80 MHz. Table 2-2 shows the above common settings.

Table 2-2 GTM (Top-Level) register setting

Register name	Set value	Description
GTM Global control register (GTM_CTRL)	0x00000000	Reset function enabled
GTM Cluster Clock Configuration register (GTM_CLS_CLK_CFG)	0x00000002	Cluster is enabled with clock divider 2 (80MHz)

This application uses the CMU and TIM installed in the GTM, and selects the input signal to the TIM with the PIC. Table 2-3 and Table 2-4 show the common settings of the CMU and PIC used in this application. Figure 2-2 shows the operation flowchart for initial setting of GTM and Figure 2-3 for initial setting of PIC. TIM setting and operation flowchart are explained in the section of each function.

CMU sets the clocks and clock sources used by GTM. The clock to be used is set by enabling the Ch to be used and setting the clock divider. In this application, clock sources 0 / 1 / 2 are set as 80MHz / 10MHz / 1MHz respectively.

PIC selects the input signal to be input to TIM. In this application, EMU3S0 rectangle wave output U phase / V phase / W phase is selected for GTM_TIM0_IN0 / 1 / 2 respectively.

Table 2-3 GTM(CMU) register settings

Register name	Set value	Description
CMU global clock control numerator register (CMU_GCLK_NUM)	0x00000001	Numerator for global clock divider
CMU global clock control denominator register (CMU_GCLK_DEN)	0x00000001	Denominator for global clock divider
CMU control for clock source 0 register (CMU_CLK_0_CTRL)	0x00000000	Defines count value for the clock divider Clock divider count value = 1x (12.5ns) (80MHz / 1 = 80MHz)
CMU control for clock source 1 register (CMU_CLK_1_CTRL)	0x00000007	Defines count value for the clock divider Clock divider count value = 8x (100ns) (80MHz / 8 = 10MHz)
CMU control for clock source 2 register (CMU_CLK_2_CTRL)	0x0000004F	Defines count value for the clock divider Clock divider count value = 80x (1us) (80MHz / 80 = 1MHz)
CMU control for clock source selection register (CMU_CLK_CTRL)	0x00000000	Clock Source Selection Use clock source CMU_GCLK_EN
CMU clock enable register (CMU_CLK_EN)	0x000000YY	CMU(Ch0, Ch1, Ch2) disable (YY : 15H) CMU(Ch0, Ch1, Ch2) enable (YY : 2AH)

Table 2-4 PIC register settings

Register name	Set value	Description
GTM Timer Input Module (TIM) Source Select Register 0 (PIC2GTMINEN0)	0x00760075	PIC2GTMINEN0[24:16] 0x76 : Select EMU3S0 rectangle wave output (V phase) for GTM_TIM0_IN1 PIC2GTMINEN0[8:0] 0x75 : Select EMU3S0 rectangle wave output (U phase) for GTM_TIM0_IN0
GTM Timer Input odule (TIM) Source Select Register 1 (PIC2GTMINEN1)	0x00000077	PIC2GTMINEN1[8:0] 0x77 : Select EMU3S0 rectangle wave output (W phase) for GTM_TIM0_IN2

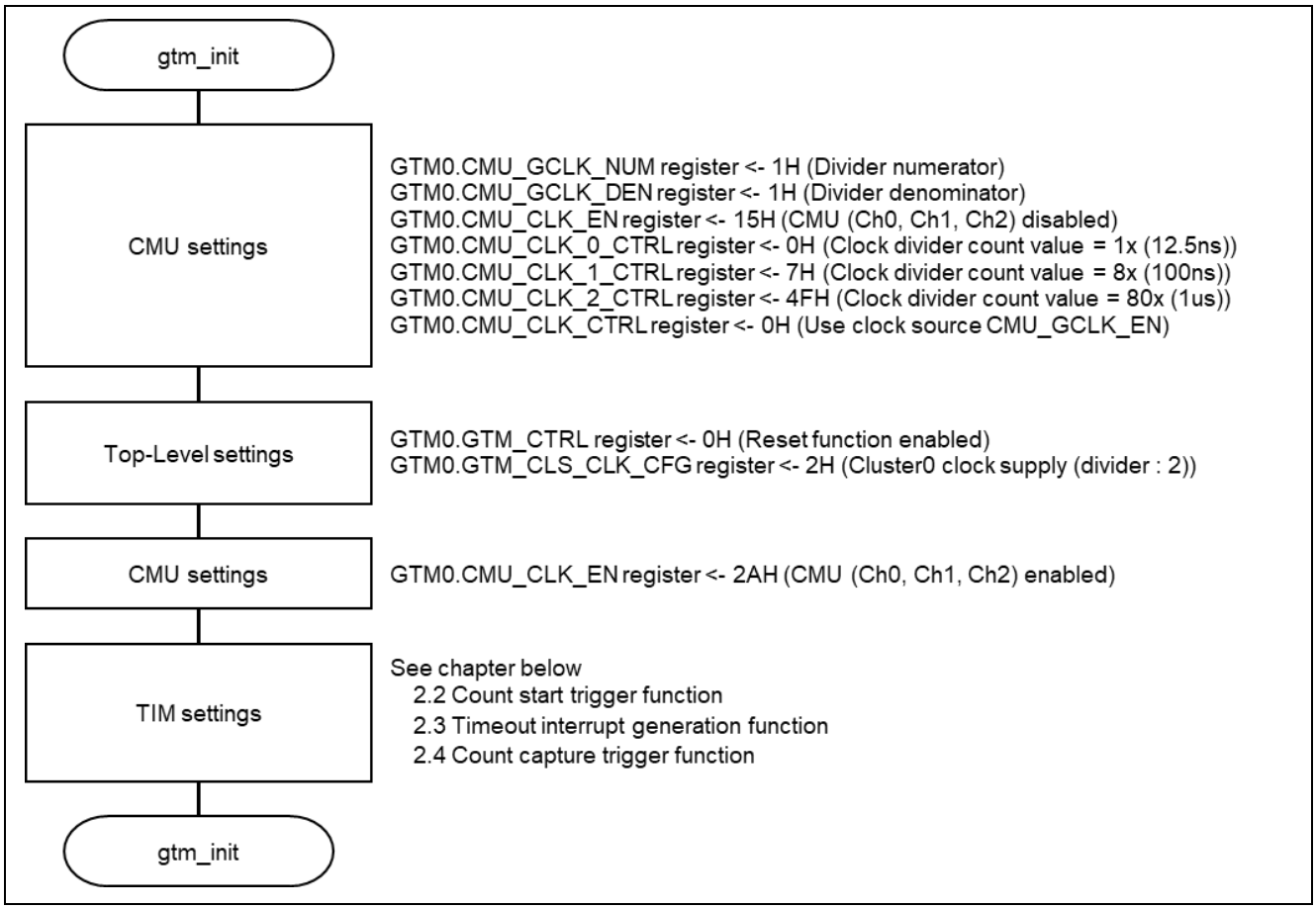

Figure 2-2 GTM initial settings

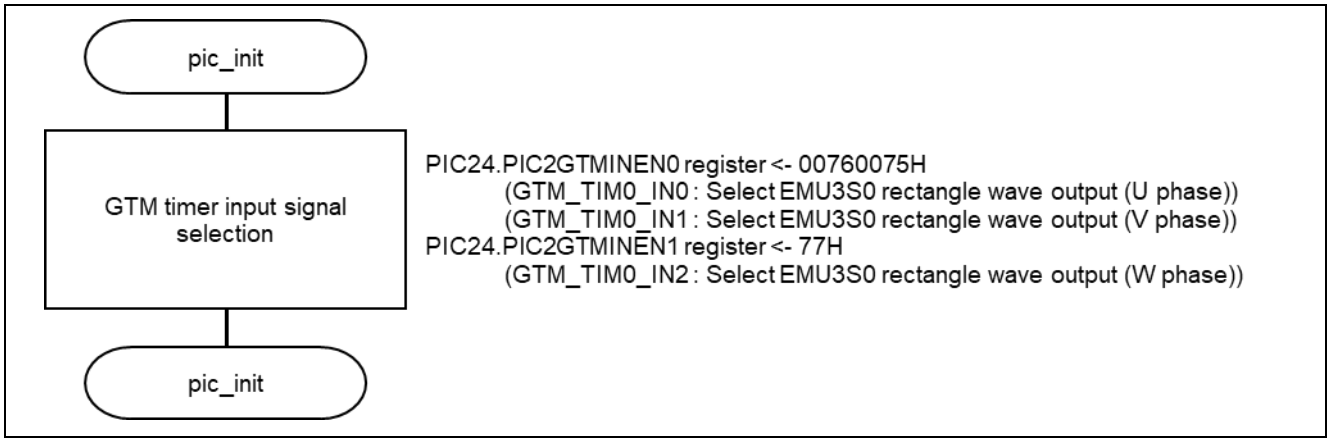

Figure 2-3 PIC initial settings

This application uses the waveform output from the EMU3S rectangle IP as the input to TIM.

An example of a waveform to be used is described below as a schematic diagram, register setting, operation flowchart, and rectangle IP operation flowchart. Figure 2-4 shows a schematic of the waveform output from the rectangle IP of EMU3S, Figure 2-5 shows the initial setup flowchart of EMU3, Figure 2-6 shows the operation flowchart of the rectangle IP, Table 2-5 shows the register settings used by EMU3S, and Table 2-6 shows the interrupt settings.

The rectangle IP in this application consists of 6 pattern switching 1 cycle, with each pattern setting a U-phase / V-phase / W-phase rectangle wave signal.

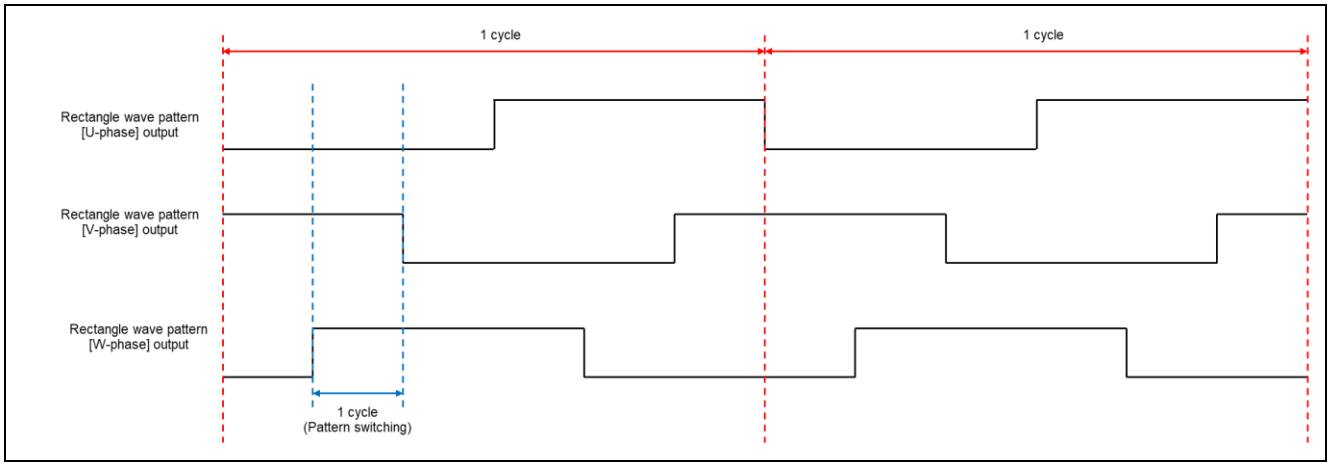

Figure 2-4 Rectangle wave schematic diagram (forward direction)

Table 2-5 EMU3S register settings (1/2)

Register name	Set value	Description
EMU30 Protect Register (PRT)	0xYY	Protection is released (YY : 0x01) Protection is set (YY : 0x00)
EMU30 Control Register (CTR)	0x01	EMU operation Runs the EMU
EMU30 Angle Generation IP Control Register (ANGCTR)	0x01	Angle information select Uses the value of the EMU3nRESTHSFT register
EMU30 Resolver Angle Pole Count Register (RESRLD)	0x01	Resolver axis double angle setting These bits must be set with the number of resolver angle poles minus 1
EMU30 Electrical Angle Generation Coefficient Register (PXR)	0x0100	Specifies the multiplier coefficient value to be used for electrical angle generation Use reset value of microcomputer
EMU30 Resolver Angle Offset Value Register (ANGOFS)	0x0000	Specifies the offset value for the resolver angle for use in the angle generation IP Angle generation IP is not used, so microcontroller Reset value is used
EMU30 Rectangle Wave Control Mode Register (RECMD)	0x00	Rectangle wave output mode switch Outputs the batch rectangle wave pattern to the TSG3
EMU30 Batch Rectangle IP Control Register (RECCTR)	0x04	Switching instruction select Uses the value of the EMU3nPSWSFT register
EMU30 Switching Instruction Software Input Register (PSWSFT)	0x00 0x01 0x02 0x03 0x04 0x05	Software input values for switching commands used in rectangle IP * Writing of values 6 or 7 is prohibited * Value must be one of 0 to 5
EMU30 q-axis Reference Voltage Phase Software Input Register (PHQSFT)	0x0000	The value for correction to be applied to the comparison value for use in detecting angle comparison 0 matches in the rectangle IP is specified in these bits Since the correction value is not used, use the reset value of the microcomputer
EMU30 Batch Rectangle Output Software Control Pattern Register (PTNN)	0x00 0x01 0x02 0x03 0x04 0x05 0x06	W / V / U-phase rectangle wave pattern set WPTN 0x1 : High level 0x0 : Low level VPTN 0x1 : High level 0x0 : Low level UPTN 0x1 : High level 0x0 : Low level
EMU30 Angle Comparison 0 Comparison Value Software Input Register (CMP0)	0x0000 0x0155 0x02AA 0x0555 0x0800 0x0AAA 0x0D55	The software input value for use in comparison of the angle comparison 0 (electrical angle) is specified in these bits

Table 2-5 EMU3S register settings (2/2)

Register name	Set value	Description
EMU30 IP Startup Trigger Source Select Register (IPTRG)	0x10	Rectangle IP startup trigger select Detection of a match in angle comparison 0
EMU30 Interrupt Source Select 3 Register (INT3)	0x00000080	Interrupt source setting k (an angle comparison 0 match detected) Enables interrupt of this source
EMU30 Resolver Angle Software Input Register (RESTHSFT)	-	Specifies the resolver angle to be input by software for use in the angle generation IP

Table 2-6 INTC2 register setting

Register name	Set value	Description
EI Level Interrupt Control Register 41 (EIC41)	0x0046	Table reference (priority 6)

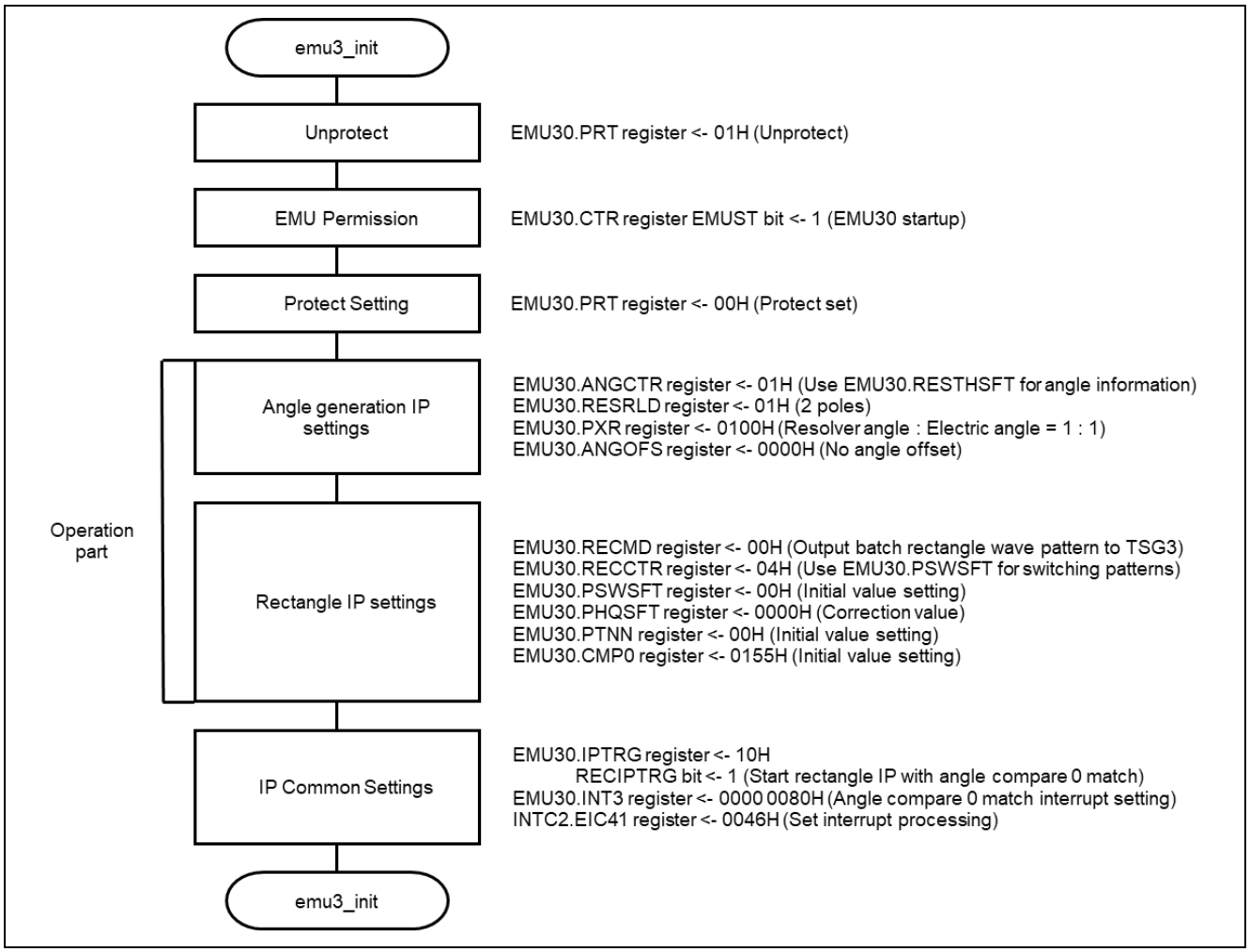

Figure 2-5 EMU3S initial settings

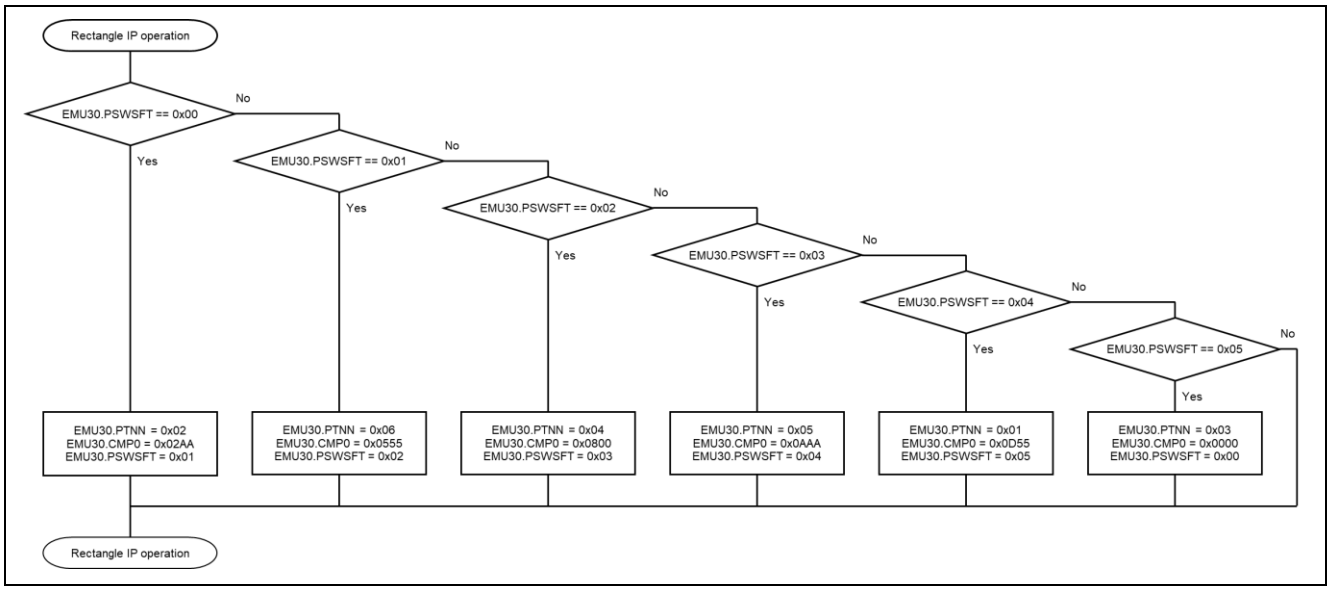

Figure 2-6 Operation flowchart of rectangle IP (handled by interrupt on angle compare 0 match)

2.2 Count start trigger function

2.2.1 Operation overview

The input signal is used as the start trigger to operate the counter (TIM0_CH0_CNT) of the TIM. This application uses the EMU3S0 rectangle wave output (U phase) as the input signal.

Triggered by the falling edge of the rectangle IP U-phase, TIM0_CH0_CNT starts counting.

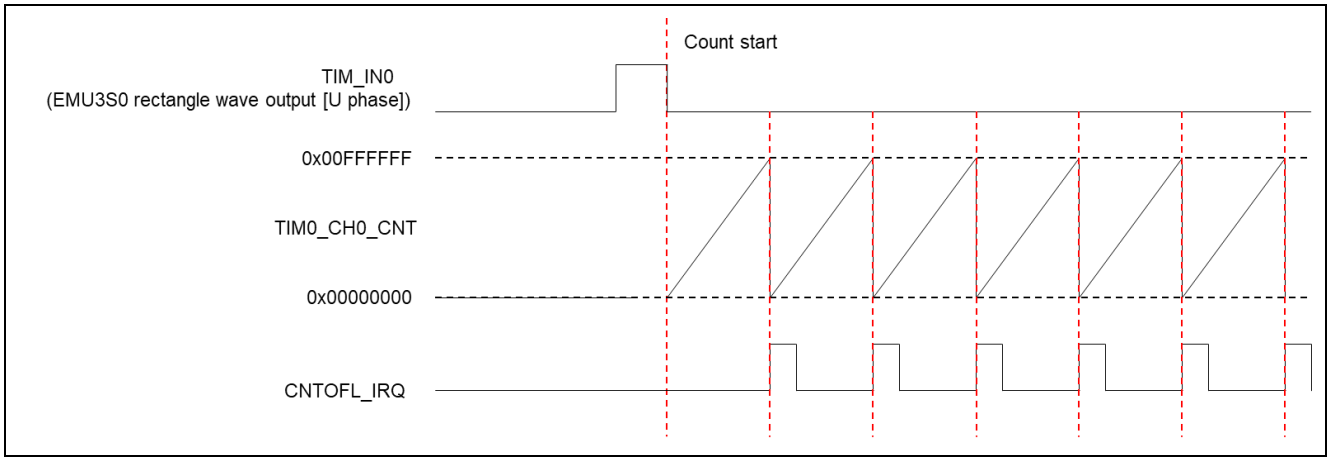

Figure 2-7 Operation overview

2.2.2 Operation flowchart

Figure 2-8 shows the operation flowchart of GTM (TIM).

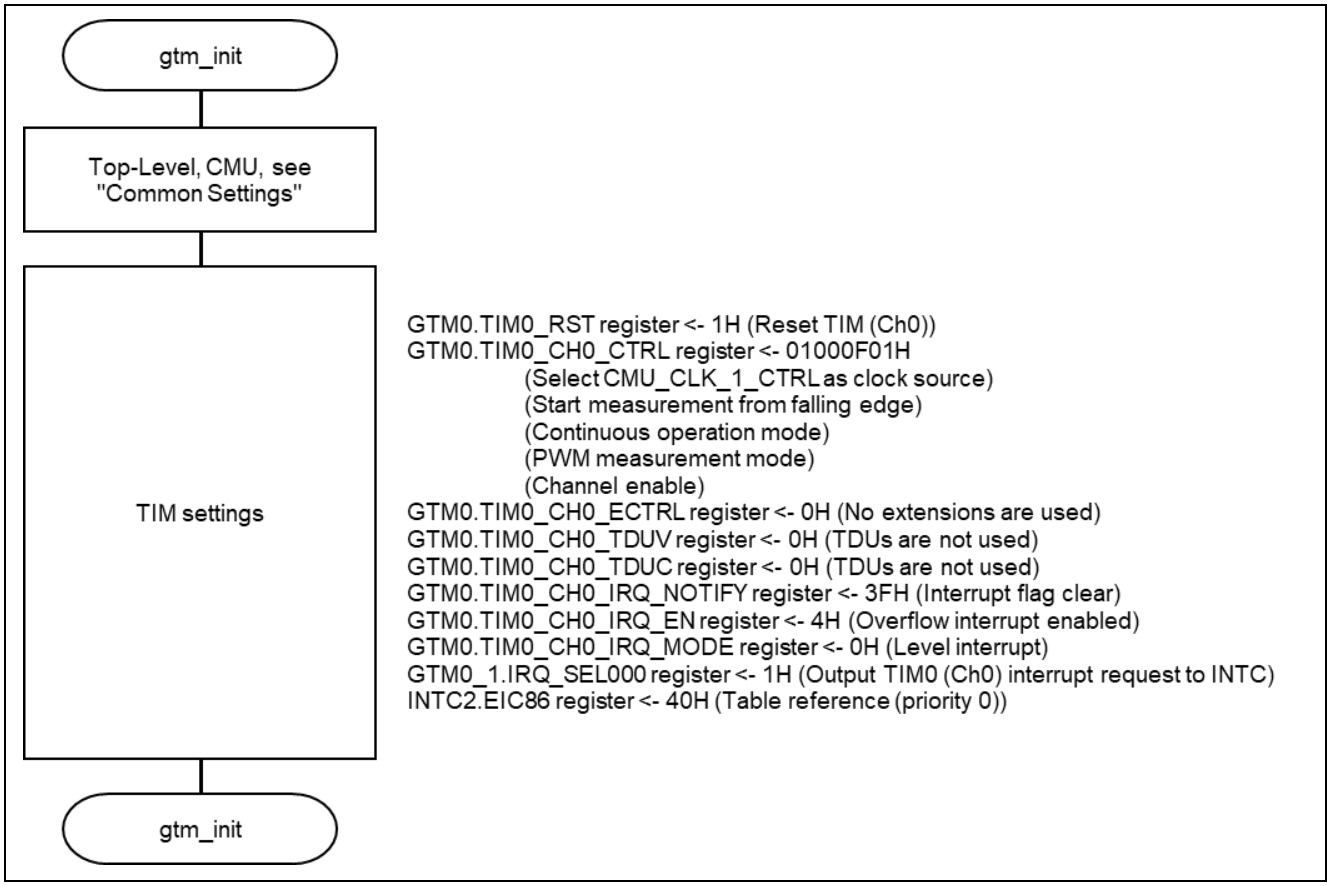

Figure 2-8 GTM (TIM) operation flowchart

2.2.3 Software description

Table 2-7 shows the register settings for GTM (TIM) and Table 2-8 shows the register settings used for GTM interrupts (CPU side).

For the count start trigger function, select CMU_CLK_1_CTRL (10 MHz) as the clock source and set the falling edge as the trigger to start counting. Also, set an overflow interrupt to occur when the counter overflows.

Table 2-7 GTM (TIM) register settings

Register name	Set value	Description
TIM0 global software reset register (TIM0_RST)	0x00000001	Reset channel 0
TIM0 channel 0 control register (TIM0_CH0_CTRL)	0x01000F01	Select CMU_CLK_1_CTRL as clock source Measurement starts with falling edge (low level measurement) Continuous operation mode PWM measurement mode (TPWM) Channel enabled
TIM0 channel 0 extended control register (TIM0_CH0_ECTRL)	0x00000000	Since the extended function is not used, use the reset value of the microcomputer
TIM0 channel 0 TDU control register (TIM0_CH0_TDUV)	0x00000000	Since TDU is not used, use the microcomputer Reset value
TIM0 channel 0 TDU counter register (TIM0_CH0_TDUC)	0x00000000	Since TDU is not used, use the microcomputer Reset value
TIM0 channel 0 interrupt notification register (TIM0_CH0_IRQ_NOTIFY)	0x0000003F	Interrupt flag clear
TIM0 channel 0 interrupt enable register (TIM0_CH0_IRQ_EN)	0x00000004	Overflow interrupt enabled
TIM0 channel 0 interrupt mode configuration register (TIM0_CH0_IRQ_MODE)	0x00000000	IRQ mode selection of channel 0 Level mode

Table 2-8 GTM (Interrupt select [to CPU]) register settings

Register name	Set value	Description
GTM Interrupt selection control register 000 (IRQ_SEL000)	0x00000001	Output TIM0 (Ch0) interrupt request to INTC
EI Level Interrupt Control Register 86 (EIC86)	0x0040	Table reference (priority 0)

2.3 Timeout interrupt generation function

2.3.1 Operation overview

The timeout detection function in the TIM function is used to generate an interrupt to the CPU side when the timeout counter (TDUC) reaches the threshold value (TDUV). This application uses the EMU3S0 rectangle wave output (V phase) as the input signal.

Triggered by the falling edge of the rectangle IP V-phase, TDUC starts counting. Triggered by the falling edge of the rectangle IP V phase, TDUC stops counting and maintains the count value. The rising edge of the rectangle IP V phase resets TDUC and starts counting. A timeout interrupt is generated when TDUC compares to the threshold set by TDUV without being stopped or reset.

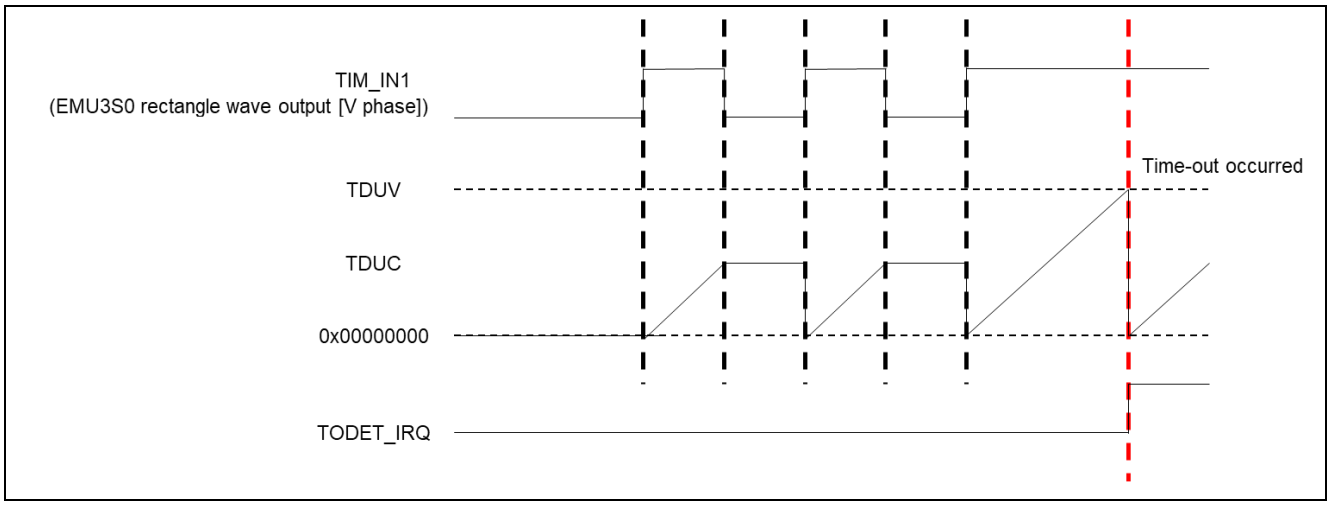

Figure 2-9 Operation overview

2.3.2 Operation flowchart

Figure 2-10 shows the operation flowchart of GTM (TIM).

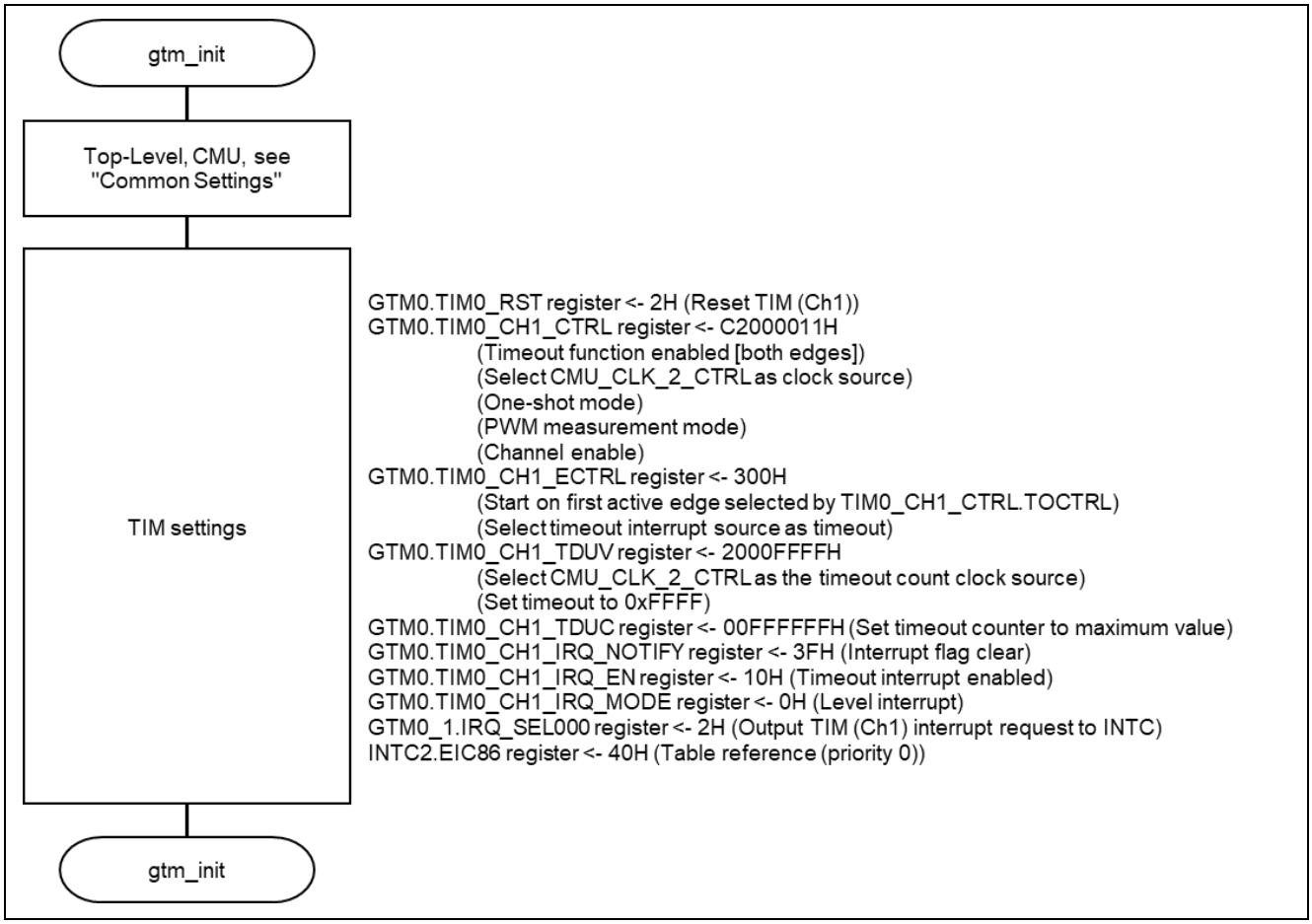

Figure 2-10 GTM (TIM) operation flowchart

2.3.3 Software description

Table 2-9 shows the register settings for GTM (TIM) and Table 2-10 shows the register settings used for GTM interrupts (CPU side).

For the timeout interrupt generation function, select CMU_CLK_2_CTRL (1 MHz) as the clock source and set both edges to trigger. Set the counter timeout value to 0xFFFF so that a timeout interrupt is generated when the counter times out.

Table 2-9 GTM(TIM) register settings

Register name	Set value	Description
TIM0 global software reset register (TIM0_RST)	0x00000002	Reset channel 1
TIM0 channel 1 control register (TIM0_CH1_CTRL)	0xC2000011	Timeout feature enabled for both edges Select CMU_CLK_2_CTRL as clock source One−shot mode PWM measurement mode (TPWM) Channel enabled
TIM0 channel 1 extended control register (TIM0_CH1_ECTRL)	0x00000300	Select timeout as the interrupt source for timeout Start counting at the occurrence of the first active edge selected by TIM0_CH1_CTRL.TOCTRL
TIM0 channel 1 TDU control register (TIM0_CH1_TDUV)	0x2000FFFF	Select CMU_CLK2 as the timeout count clock source Set timeout time to 0xFFFF
TIM0 channel 1 TDU counter register (TIM0_CH1_TDUC)	0x00FFFFFF	Set timeout counter to maximum value
TIM0 channel 1 interrupt notification register (TIM0_CH1_IRQ_NOTIFY)	0x0000003F	Interrupt flag clear
TIM0 channel 1 interrupt enable register (TIM0_CH1_IRQ_EN)	0x00000010	Timeout interrupt enabled
TIM0 channel 1 interrupt mode configuration register (TIM0_CH1_IRQ_MODE)	0x00000000	IRQ mode selection of channel 0 Level mode

Table 2-10 GTM (Interrupt select [to CPU]) register setting

Register name	Set value	Description
GTM Interrupt selection control register 000 (IRQ_SEL000)	0x00000002	Output TIM0 (Ch1) interrupt request to INTC
EI Level Interrupt Control Register 86 (EIC86)	0x0040	Table reference (priority 0)

2.4 Count capture trigger function

2.4.1 Operation overview

With the input signal as a trigger, the TIM counter (TIM0_CH2_CNT) value is transferred to the TIM registers (TIM0_CH2_CNTS, TIM0_CH2_GRP0, TIM0_CH2_GRP1) at each edge timing. This application uses the EMU3S0 rectangle wave output (W phase) as the input signal.

Starts counting TIM0_CH2_CNT triggered by the rising edge of the rectangle IP W phase. Transfer TIM0_CH2_CNT to TIM0_CH2_CNTS triggered by the falling edge of rectangle IP W phase. The rising edge of the rectangle IP W phase resets TIM0_CH2_CNT and starts counting. At the same time, TIM0_CH2_CNT is transferred to TIM0_CH2_GRP1 and TIM0_CH2_CNTS to TIM0_CH2_GRP0.

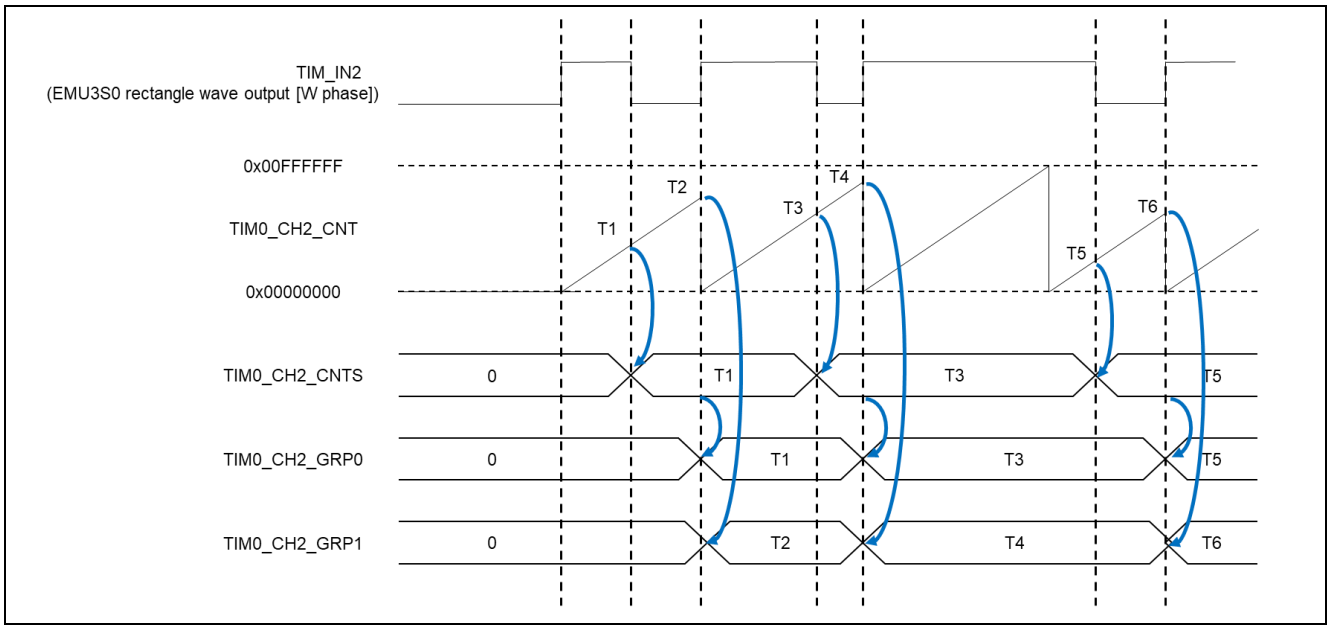

Figure 2-11 Operation overview

2.4.2 Operation flowchart

Figure 2-12 shows the operation flowchart of GTM (TIM).

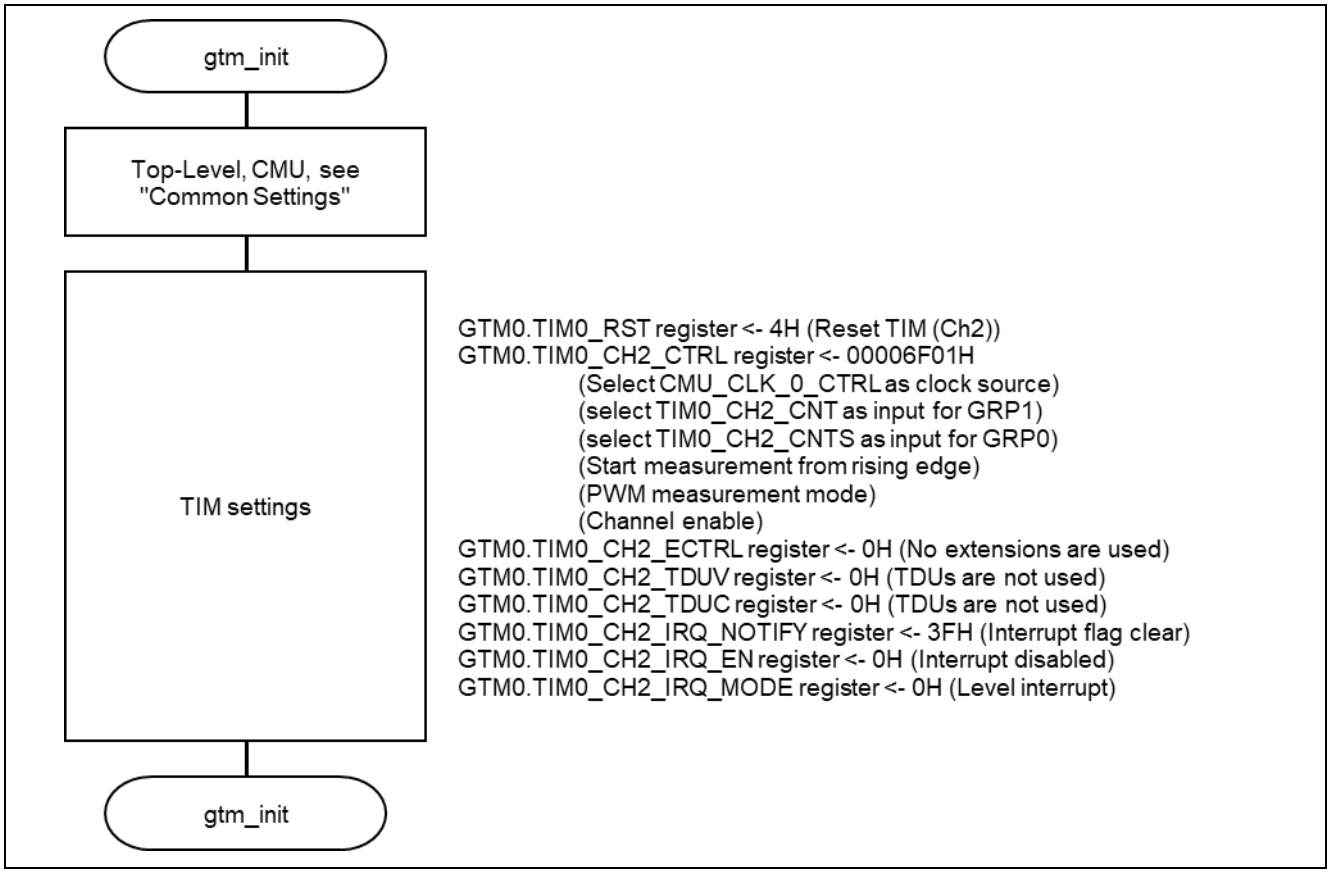

Figure 2-12 GTM (TIM) operation flowchart

2.4.3 Software description

Table 2-11 shows the register settings used in the GTM (TIM) register setting.

For the count capture trigger function, select CMU_CLK_0_CTRL (80 MHz) as the clock source and set the rising edge as the count start trigger. For counter capture, select TIM0_CH2_CNT for the input of TIM0_CH2_GRP1 and TIM0_CH2_CNTS for the input of TIM0_CH2_GRP0.

Table 2-11 GTM (TIM) register settings

Register name	Set value	Description
TIM0 global software reset register (TIM0_RST)	0x00000004	Reset channel 2
TIM0 channel 2 control register (TIM0_CH2_CTRL)	0x00006F01	Select CMU_CLK_0_CTRL as clock source Select TIM0_CH2_CNT as input for GRP1 Select TIM0_CH2_CNTS as input for GRP0 Measurement starts with rising edge (high level measurement) Continuous operation mode PWM measurement mode (TPWM) Channel enabled
TIM0 channel 2 extended control register (TIM0_CH2_ECTRL)	0x00000000	Since the extended function is not used, use the reset value of the microcomputer
TIM0 channel 2 TDU control register (TIM0_CH2_TDUV)	0x00000000	Since TDU is not used, use the microcomputer Reset value
TIM0 channel 2 TDU counter register (TIM0_CH2_TDUC)	0x00000000	Since TDU is not used, use the microcomputer Reset value
TIM0 channel 2 interrupt notification register (TIM0_CH2_IRQ_NOTIFY)	0x0000003F	Interrupt flag clear
TIM0 channel 2 interrupt enable register (TIM0_CH2_IRQ_EN)	0x00000000	Interrupt disabled
TIM0 channel 2 interrupt mode configuration register (TIM0_CH2_IRQ_MODE)	0x00000000	IRQ mode selection of channel 0 Level mode

3. Appendix

This chapter describes the selection of input signals for GTM (TIM). The input signal selection to GTM (TIM) can be set with the PIC register "PIC2GTMINENk (GTM Timer Input Module (TIM) Source Select Register k)". Table 3-1 lists the TIM trigger selection functions of the GTM.

In this application note, the EMU3S0 rectangle wave output U-phase / V-phase / W-phase is used as input for GTM(TIM). See 2.1.2 for details and setting values.

Table 3-1 TIM trigger selection function of GTM

No.	Signal name	Signal content
1	EMU3SnTSTWECMP (n=0-1)	EMU3Sn write enable for carrier period and comparison values
2	EMU3SnTSTIUP (n=0-1)	EMU3S0 rectangle wave output (U phase)
3	EMU3SnTSTIVP (n=0-1)	EMU3S0 rectangle wave output (V phase)
4	EMU3SnTSTIWP (n=0-1)	EMU3S0 rectangle wave output (W phase)
5	EMU3SnINTm (n=0-1,m=0-7)	EMU3Sn interrupt m
6	FCMPnCMPO (n=0-9)	Comparator output data for channel n
7	fcmpun_dacdata_change (n=0-9)	DAC data update for channel n
8	fcmpun_intc_intreq (n=0-9)	Comparator result interrupt for channel n
9	fcmpun_intc_erreq (n=0-9)	Error interrupt for channel n
10	OSTMnTINT (n=0-5)	OSTMn interrupt
11	INT_DSMIFnUPDATEm (n=0-1,m=0-1)	DSMIFn data update interrupt channel m
12	INTSDMACnCHm (n=0-1,m=0-15)	sDMACn channel m descriptor step end interrupt
13	INTDTSn (n=0-127)	DTS channel n transfer end
14	INTDTSCTn (n=0-127)	DTS channel n transfer count match
15	INTADCKnIj (n=0-3,j=0-4)	ADCKn Scan group j (SGj) end interrupt
16	INTADCK_SDn (n=0-3)	ADCKn SG-Diag end interrupt
17	DSADIn (n=00,10-15,20-22)	DSADCn A/D conversion end interrupt
18	DFEn_PHUPDm (n=0-1,m=0-3)	DFEn P/H updating trigger m
19	INTDFE0DOUTCNDm (m=0-15)	DFE0 CHm output data interrupt
20	INTDFE1DOUTCNDm (m=0-3)	DFE1 CHm output data interrupt
21	CADI00	CADC00 A/D conversion end interrupt
22	INTENCAnIm (n=0-1,m=0-1)	ENCAn capture/compare match interrupt m
23	INTENCAnIEC (n=0-1)	Clear interrupt signal by the ENCAn encoder input (Z phase)
24	ENCAnTCKEN (n=0-1)	ENCAn count clock output
25	ENCAnTUDC (n=0-1)	ENCAn down-count enable signal output
26	RDC3ALn_phicomp_m (n=0-1,m=0-2)	RDC3ALn phi comparison interrupt output m
27	RDC3ASn_phicomp_m (n=0-1,m=0-2)	RDC3ASn phi comparison interrupt output m
28	RDC3ALn_ENCA (n=0-1)	RDC3ALn Encoder pulse A output
29	RDC3ALn_ENCB (n=0-1)	RDC3ALn Encoder pulse B output
30	RDC3ALn_ENCZ (n=0-1)	RDC3ALn Encoder pulse Z output
31	RDC3ASn_ENCA (n=0-1)	RDC3ASn Encoder pulse A output
32	RDC3ASn_ENCB (n=0-1)	RDC3ASn Encoder pulse B output
33	RDC3ASn_ENCZ (n=0-1)	RDC3ASn Encoder pulse Z output
34	RLIN3nRX (n=0-3)	RLIN3n soft macro data input (RX)
35	ENCAnE0 (n=0-1)	ENCAn encoder input (count pulse 0)
36	ENCAnE1 (n=0-1)	ENCAn encoder input (count pulse 1)
37	ENCAnEC (n=0-1)	ENCAn encoder input (clear pulse)
38	CANnRX (m=0-9)	CANn receive data input
39	TIMn_CHm (n=0-6,m=0-7)	GTM timer input signal (TIMn)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2023.5.18		First edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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