RH850/U2B Group

R01AN7077EJ0100
Rev.1.00

RIIC Application Note

Summary

This application describes the operation example using I2C Bus Interface (RIIC) in RH850/U2Bx.

The operation example described in this application note have been confirmed to operate, be sure to confirm the operation before using it.

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1. Introduction

This application note describes the usage for I2C bus interface (RIIC) and the creating example for the farmwear in RH850/U2Bx.

1.1 Usage Function

The following shows the hardware used RH850/U2Bx function in this application note.

- I2C Bus Interface (RIIC)

2. Operation Example

2.1 EEPROM Write/Read

2.1.1 Specification Overview

In this operation example, perform the write read of 6 bytes data to EEPROM by the master mode in RIIC.

Use master for RIIC , and set 400kbps to the 7 bits address and the baud rate RIIC.

Use SCL synchronous circuit, digital noise filter, NACK reception transfer suspension, master arbitration lost detection, and timeout detection function.

Connect SCL pin and SDA pin of RIIC with the slave system side.

Write the 6 bites data from an address of 0 in EEPROM. After writing, read 6 bytes data by specifying the read address to an address of 0.

Read 6 bytes data.

2.1.2 System Configuration

Figure 2-1 shows the system configuration.

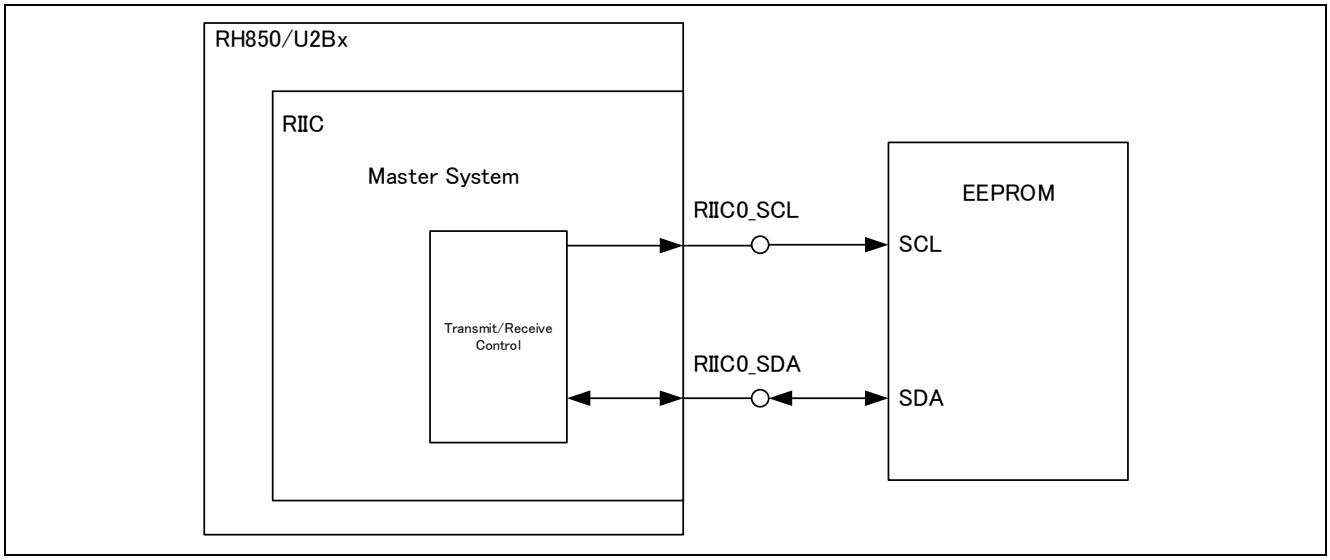

Figure 2-1 System Configuration

2.1.3 Software Explanation

- Module Explanation

The following shows the module list in this operation example.

Table 2-1 Module List

Module Name	Function Name	Function
Main Routine	main_pe0	Perform various settings and application starting.
Port Initialization Routine	port_init	Perform port initialization.
RIIC Initialization Routine	riic_init	Perform RIIC initialization.
RIIC Start Routine	riic _start	Start RIIC.
Interrupt Function Initial Setting Routine	intc_init	Perform RIIC interrupt setting.
Transmit Data Empty Interrupt Processing Routine	riic0_ti	Perform transmit data setting processing.
Transmit Complition Interrupt Processing Routine	riic0_tei	Perform transmit completion processing.
Receive Complition Interrupt Processing Routine	riic0_ri	Perform read processing of transmit data.

- Register Setting

The following shows the register settings for various functions in this operation example.

Table 2-2 RIIC ch0 Register

Register Name	Setting Value	Function
RIIC0CR1	0x00000001	Reset.
RIIC0CR2	0x0000000A	Issue start condition and stop condition.
RIIC0MR1	0x00000018	Enable bit counter write protection.
		400kbps
		9 bits : Bit counter
RIIC0MR2	0x00000000	SDA output delay clock source : IICφ
		SDA output delay counter : 0
		Timeout H count control : Disable
		Timeout L count control : Disable
		Timeout detection timer selection : Long mode
RIIC0MR3	0x0000007C	WAIT (No wait in last byte)
		RDRF set timing : 9th clock (8th clock in last byte)
		Release ACKBT write protection : Enable
		Transmit acknowledge : Enable
RIIC0BRL	0x000000F6	Bit rate low level cycle : 0x16
RIIC0BRH	0x000000E8	Bit rate high level cycle : 0x08
RIIC0FER	0x00000073	Enable SCL synchronization circuit.
		Enable digital noise filter circuit.
		Enable transmit suspension in NACK receiving.
		Enable master arbitration lost detection.
		Enable timeout detection function.
RIIC0IER	0x000000F3	Enable transmit data empty interrupt.
		Enable transmit completion interrupt.
		Enable receive completion interrupt.
		Enable transmit suspension interrupt in NACK receiving.
		Enable arbitration lost interrupt.
		Enable timeout interrupt.

Table 2-3 Interrupt Register Setting

Register Name	Setting Value	Function
EIBD882	0x00000000	Bind RIIC reception completion interrupt to PE0 (CPU0).
EIBD883	0x00000000	Bind RIIC transmit data empty interrupt to PE0 (CPU0).
EIBD887	0x00000000	Bind RIIC transmit completion interrupt to PE0 (CPU0).
EIC882	0x0040	Table reference/Priority level 0
EIC883	0x0040	Table reference/Priority level 0
EIC887	0x0040	Table reference/Priority level 0

Table 2-4 Port Register Setting

Register Name	Setting Value	Function
PORT0.PCR00_1	0x10020043	Set P00_1 to ALT_RIIC0SCL.
PORT0.PCR00_2	0x10020043	Set P00_2 to ALT_RIIC0SDA.

- Operation Flow

The following shows the flowchart in this operation example.

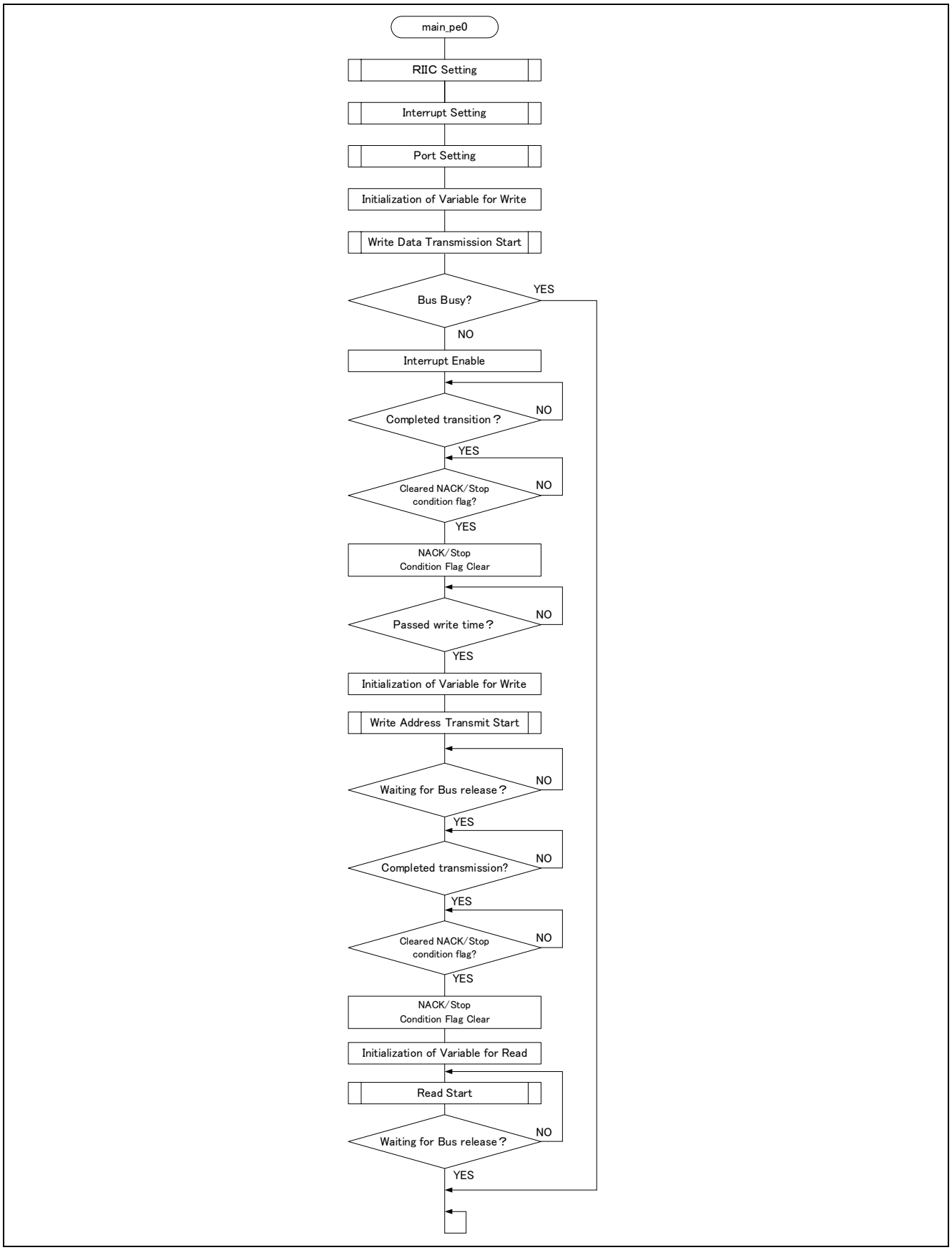

Figure 2-2 main Function Flowchart

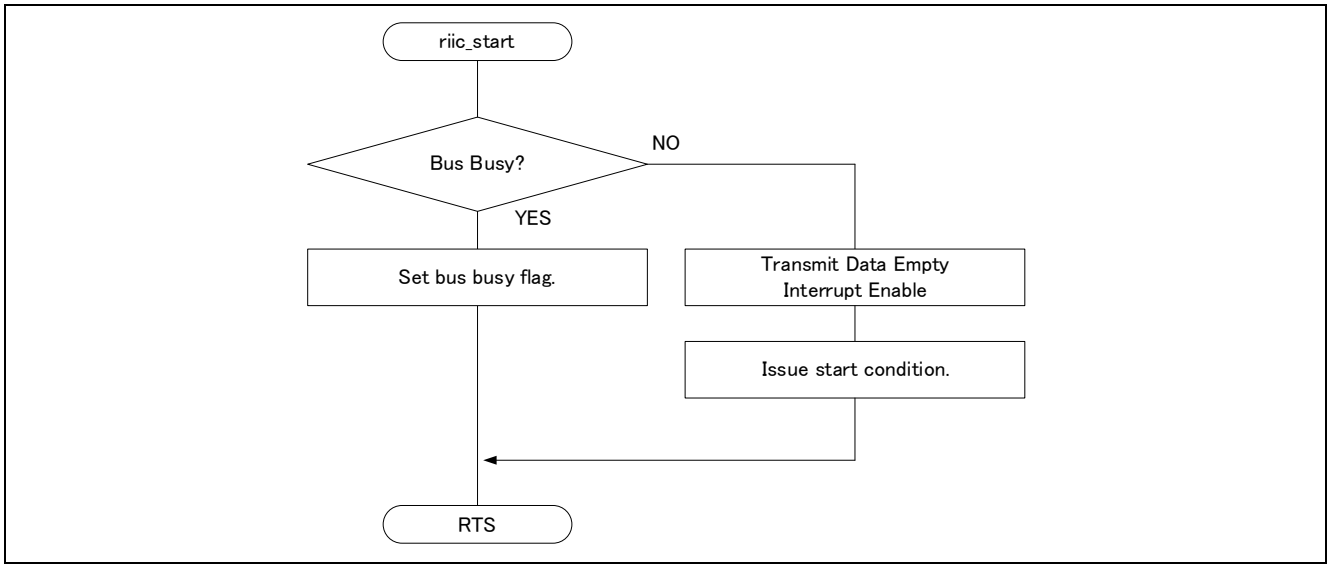

Figure 2-3 RIIC Start Function Flowchart

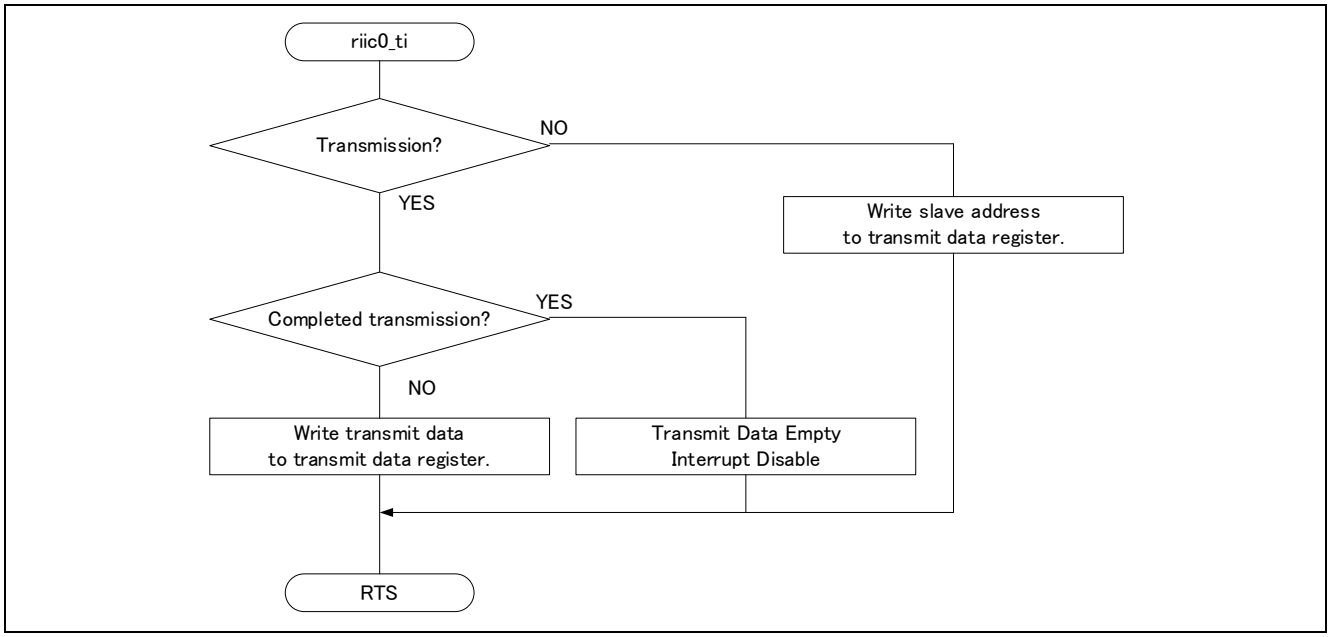

Figure 2-4 RIIC Transmit Data Empty Interrupt Function Flowchart

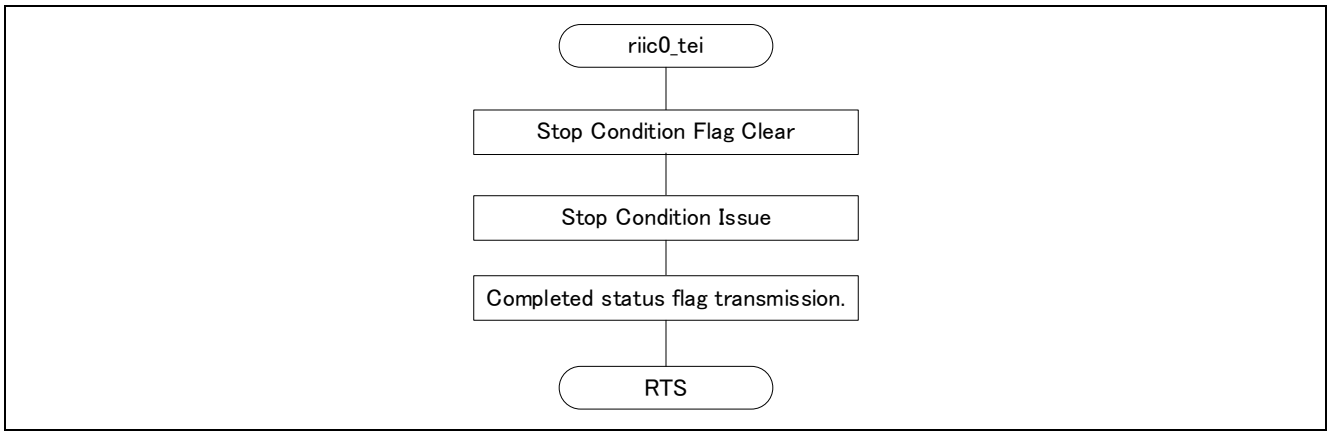

Figure 2-5 RIIC Transmit Completion Interrupt Function Flowchart

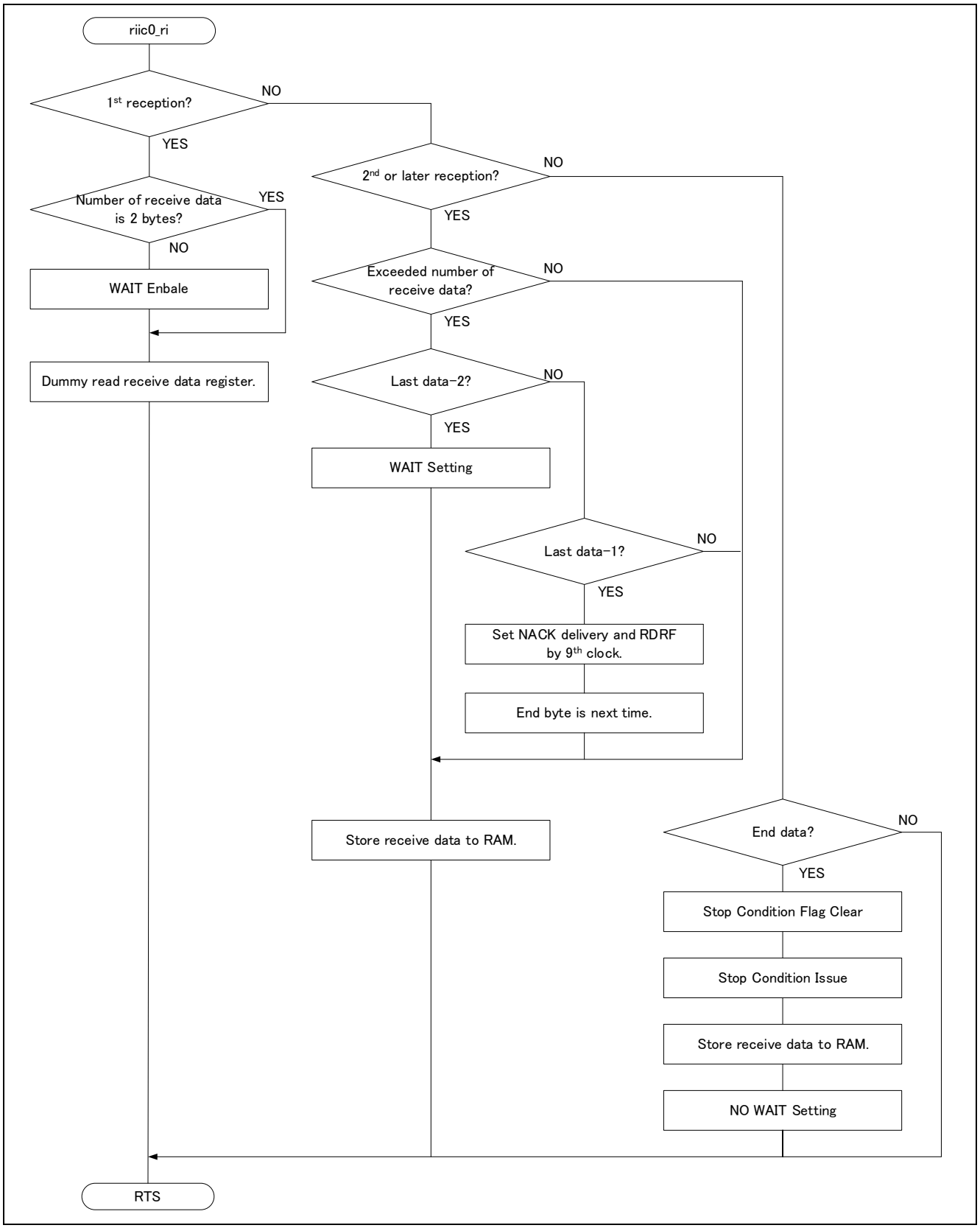

Figure 2-6 RIIC Receive Completion Interrupt Function Flowchart

2.2 EEPROM Write/Read (Interlocked sDMAC)

2.2.1 Specification Overview

In this operation example, perform the 6 bytes data write read to EEPROM by the master mode in RIIC. Use sDMAC for the data writing to RAM and register without the initial setting, and CPU is not interposed.

Use master for RIIC , and set 400kbps to the 7 bits address and the baud rate RIIC.

Use SCL synchronous circuit, digital noise filter, NACK reception transfer suspension, master arbitration lost detection, and timeout detection function.

Connect SCL pin and SDA pin of RIIC with the slave system side.

Write the 6 bites data from an address of 0 in EEPROM. After writing, read 6 bytes data by specifying the read address to an address of 0.

Read 6 bytes data.

2.2.2 System Configuration

Figure 2-7 shows the system configuration.

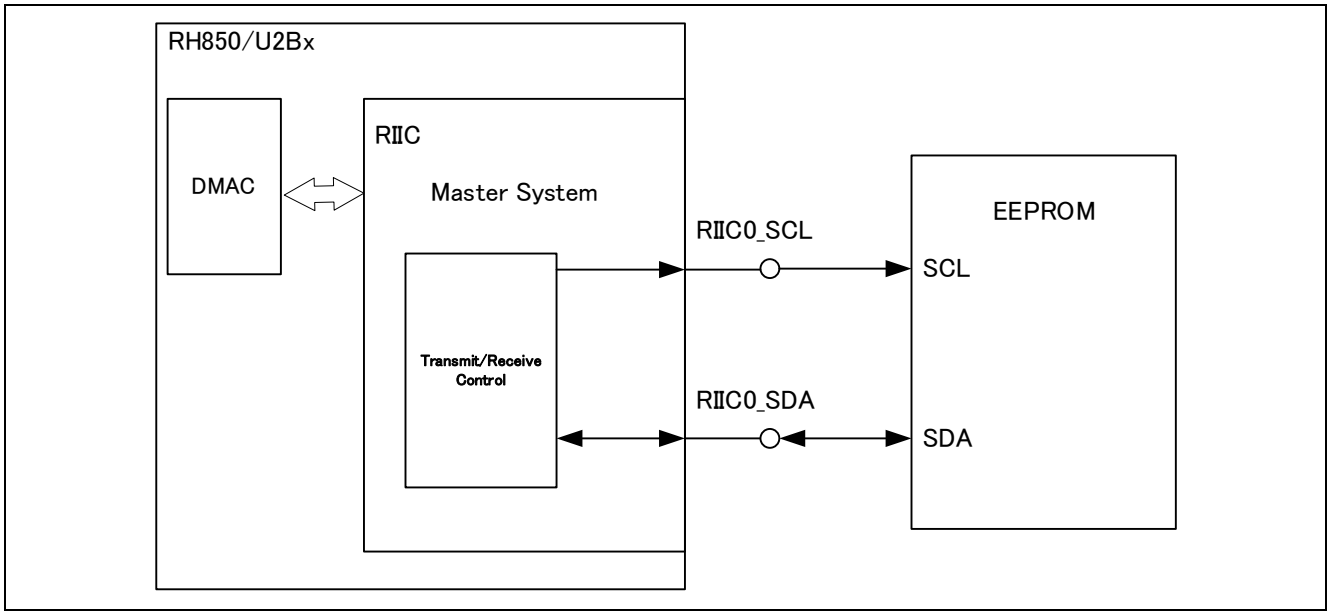

Figure 2-7 System Configuration

2.2.3 Descriptor Setting

In sDMAC use the descriptor (start address : 0xFFF94000) for the setting of the transfer information. The setting procedure to RAM and the register is same with “2.1 EEPROM Write/Read”. Table 2-5 and Table 2-6 show the list of the descriptor setting.

Table 2-5 Descriptor Setting List (Channel0)

No.	Transfer Source	Transfer Detection	Times	Transfer Contents
1	tr_data[0]	RIIC0.DRT	8	Slave Address, Write Address, Write Data Transmission
2	tr_data[0]	RIIC0.DRT	2	Slave Address, Read Address Transmission
3	dummy_tr_data[0]	RIIC0.DRT	1	Raed Start

Table 2-6 Descriptor Setting List (Channel1)

No.	Transfer Source	Transfer Detection	Times	Transfer Contents
4	RIIC0.DRR	rx_data	4	Read Data Transmission (1st to 4th data)
5	rx_mr3[0]	RIIC0.MR3	1	WAIT Setting
6	RIIC0.DRR	rx_data	1	Read Data Transmit (5th data)
7	rx_mr3[1]	RIIC0.MR3	1	ACKBT Write Enable Setting
8	rx_mr3[2]	RIIC0.MR3	1	NACK Delivery Setting
9	RIIC0.DRR	rx_data	1	Read Data Receive (6th data)
10	RIIC0.SR2	dummy32	1	Stop Condition Flag Read
11	rx_mr3[3]	RIIC0.SR2	1	Stop Condition Flag Clear
12	rx_mr3[4]	RIIC0.CR2	1	Stop Condition Issuing
13	RIIC0.DRR	rx_data	1	Read Data Reception (7th data)
14	rx_mr3[2]	RIIC0.MR3	1	No WAIT Setting

2.2.4 Software Explanation

- Module Explanation

The following shows the module list in this operation example.

Table 2-7 Module List

Module Name	Function Name	Function
Main Routine	main_pe0	Perform various settings and application starting.
Port Initialization Routine	port_init	Perform port initialization.
RIIC Initialization Routine	riic_init	Perform RIIC initialization.
RIIC Start Routine	riic _start	Start RIIC.
Interrupt Function Initial Setting Routine	intc_init	Perform RIIC interrupt setting.
Transmit Completion Interrupt Processing Routine	riic0_tei	Perform transmit completion processing.
sDMAC Channel 0 Initial Setting Routine	sdmac_snd_init	Perform initialization sDMAC for transmission.
sDMAC Channel 1 Initial Setting Routine	sdmac_rcv_init	Perform initialization sDMAC for reception.
Descriptor Initial Setting Routine	descriptor_init	Perform setting for descriptor.

-

- Register Setting

The following shows the register settings for various functions in this operation example.

Table 2-8 RIIC ch0 Register

Register Name	Setting Value	Function
RIIC0CR1	0x00000001	Reset.
RIIC0CR2	0x0000000A	Issue start condition and stop condition.
RIIC0MR1	0x00000018	Enable bit counter write protection.
		400kbps
		9 bits : Bit counter
RIIC0MR2	0x00000000	SDA output delay clock source : IICφ
		SDA output delay counter : 0
		Timeout H count control : Disable
		Timeout L count control : Disable
		Timeout detection timer selection : Long mode
RIIC0MR3	0x0000007C	WAIT (No wait in last byte)
		RDRF set timing : 9th clock (8th clock in last byte)
		Release ACKBT write protection : Enable
		Transmit acknowledge : Enable
RIIC0BRL	0x000000F6	Bit rate low level cycle : 0x16
RIIC0BRH	0x000000E8	Bit rate high level cycle : 0x08
RIIC0FER	0x00000073	Enable SCL synchronization circuit.
		Enable digital noise filter circuit.
		Enable transmit suspension in NACK receiving.
		Enable master arbitration lost detection.
		Enable timeout detection function.
RIIC0IER	0x000000F3	Enable transmit data empty interrupt.
		Enable transmit completion interrupt.
		Enable receive completion interrupt.
		Enable transmit suspension interrupt in NACK receiving.
		Enable arbitration lost interrupt.
		Enable timeout interrupt.

Table 2-9 PBG Register Setting

Register Name	Setting Value	Function
PBGERRSLV11L0 GKCPROT	0xA5A5A501	Enable register access of PBG11L0.
PBG11L0 PBGPROT1_2	0x10000001	SPID for RIIC0 : Set 1 to sDMAC and CPU0.

Table 2-10 sDMAC ch0 Register

Register Name	Setting Value	Function
DMA0CM_0	0x00001C00	Channel Master SPID Setting SPID=0x1C (Initial Value)
		Supervisor Mode
DMA0RS_0	0x00010058	Transfer times in every hardware request : 1 time
		Hardware DMA transfer source selection : group 0-88 (RIIC0 transmit data empty interrupt (INTRIIC0TI))
DMA0DPPTR_0	0x00000000	Descriptor pointer : Address 0x000
DMACSEL 0_5	0xFFFCFFFF	DMA transmit request group : INTRIIC0TI (group 0-88)
DMA0CHFCR_0	0x00000002	Transmit completion flag clear
DMA0OR	0x0001	DMA transfer enable
DMA0CHCR_0	0x00303	Descriptor execution enable
		Descriptor setting value copy
		Transfer completion interrupt enable
		Channel operation enable

Table 2-11 sDMAC ch1 Register

Register Name	Setting Value	Function
DMA0CM_1	0x00001C00	Channel Master SPID Setting SPID=0x1C (Initial Value)
		Supervisor Mode
DMA0RS_1	0x00010057	Transfer times in every hardware request : 1 time
		Hardware DMA transfer source selection : group 0-87 (RIIC0 transmit data empty interrupt (INTRIIC0RI))
DMA0DPPTR_1	0x00000100	Descriptor pointer : Address 0x040
DMACSEL 0_5	0xFFF3FFFF	DMA transmit request group : INTRIIC0RI (group 0-87)
DMA0CHFCR_1	0x00000002	Transmit completion flag clear
DMA0CHCR_1	0x00303	DMA transfer enable
		Descriptor execution enable
		Descriptor setting value copy
		Transfer completion interrupt enable

Table 2-12 Interrupt Register Setting

Register Name	Setting Value	Function
EIBD887	0x00000000	Bind RIIC transmit completion interrupt to PE0 (CPU0).
EIC887	0x0040	Table reference/Priority level 0

Table 2-13 Port Register Setting

Register Name	Setting Value	Function
PORT0.PCR00_1	0x10020043	Set P00_1 to ALT_RIIC0SCL.
PORT0.PCR00_2	0x10020043	Set P00_2 to ALT_RIIC0SD.

- Operation Flow

The following shows the flowchart in this operation flowchart.

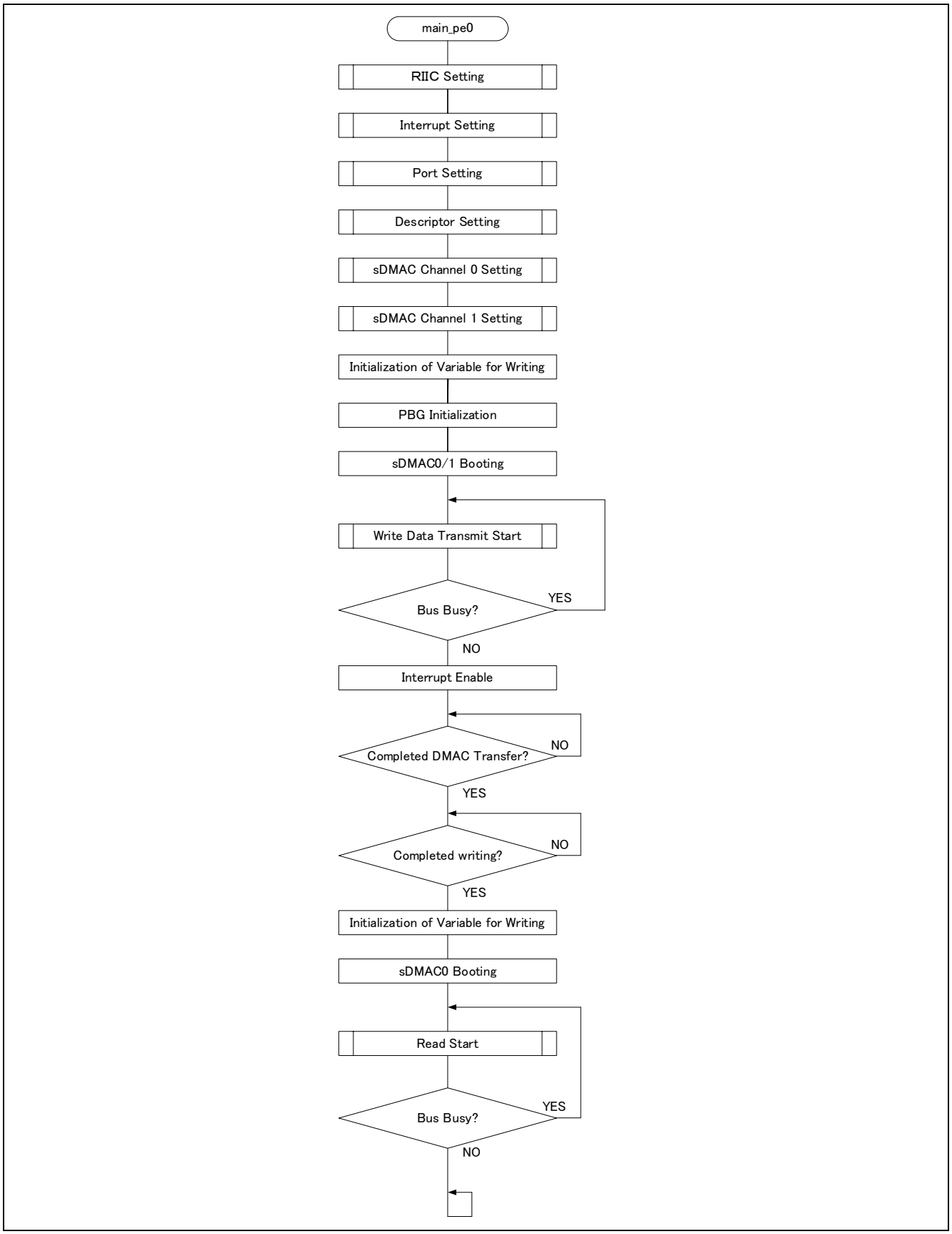

Figure 2-8 main Function Flowchart

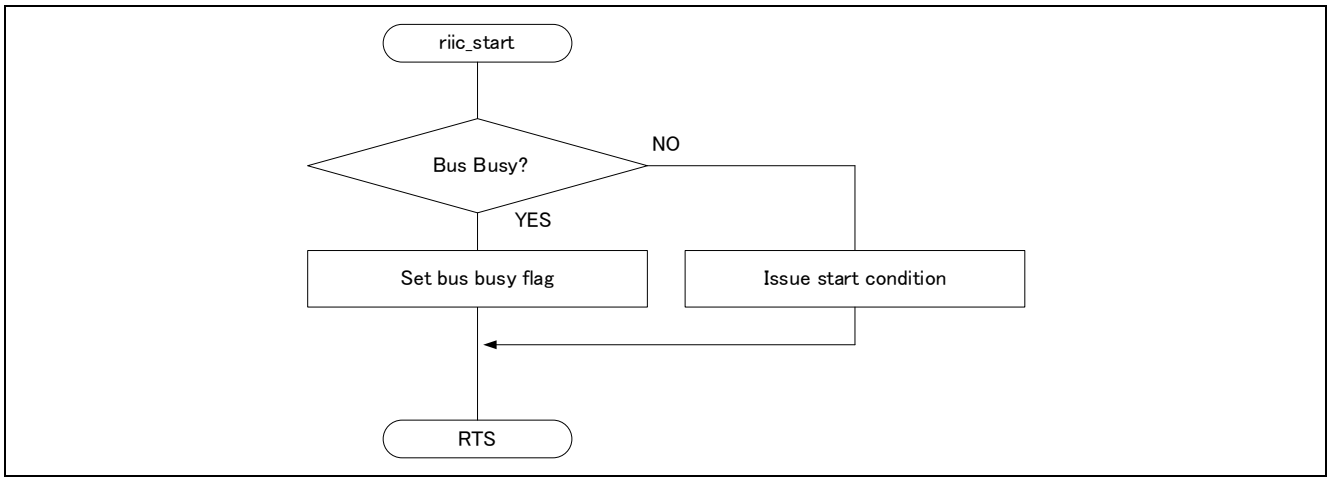

Figure 2-9 RIIC Start Function Flowchart

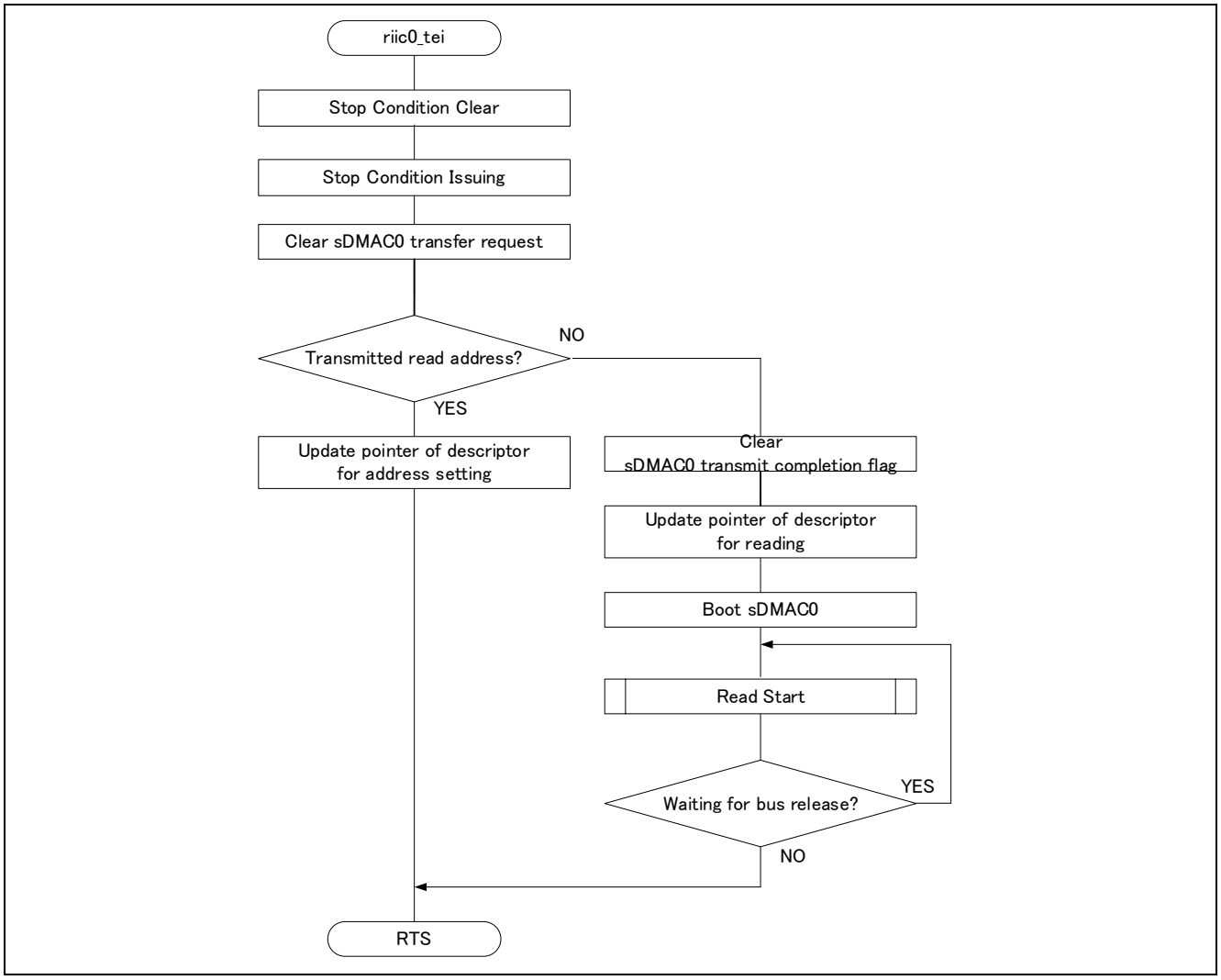

Figure 2-10 RIIC Transmit Complition Interrupt Function Flowchart

2.3 Master Transmit/Receive Operation

2.3.1 Specification Overview

In this operation example, perform 8 bytes data transition/reception by RIIC master.

Use master for RIIC , and set 400kbps to the 7 bits address and the baud rate RIIC.

Use SCL synchronous circuit, digital noise filter, NACK reception transfer suspension, master arbitration lost detection, and timeout detection function.

Connect SCL pin and SDA pin of RIIC with the slave system side.

2.3.2 System Configuration

Figure 2-11 shows the system configuration.

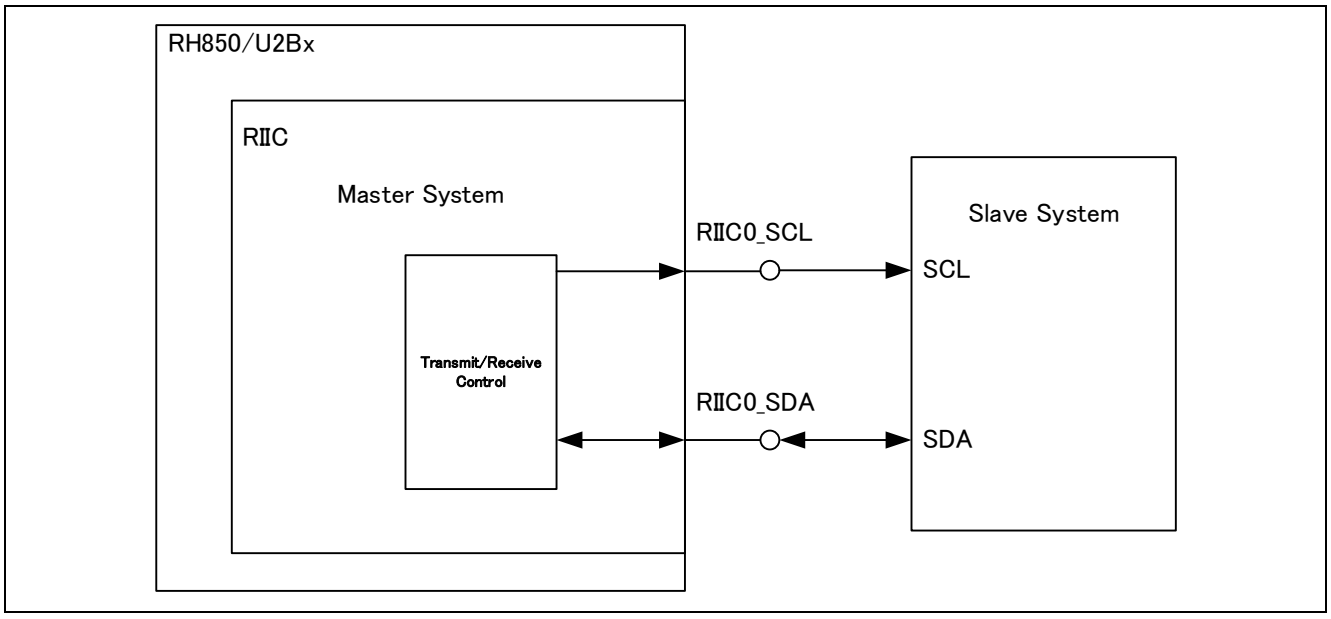

Figure 2-11 System Configuration

2.3.3 Software Explanation

- Module Explanation

The following shows the module list in this operation example.

Table 2-14 Module List

Module Name	Function Name	Function
Main Routine	main_pe0	Perform various settings and application starting.
Port Initialization Routine	port_init	Perform port initialization.
RIIC Initialization Routine	riic_init	Perform RIIC initialization.
RIIC Start Routine	riic _start	Start RIIC.
Interrupt Function Initial Setting Routine	intc_init	Perform RIIC interrupt setting.
Transmit Data Empty Interrupt Processing Routine	riic0_ti	Perform transmit data setting processing.
Transmit Complition Interrupt Processing Routine	riic0_tei	Perform transmit completion processing.
Receive Complition Interrupt Processing Routine	riic0_ri	Perform read processing of transmit data.

- Register Setting

The following shows the register settings for various functions in this operation example.

Table 2-15 RIIC Ch0 Register

Register Name	Setting Value	Function
RIIC0CR1	0x00000001	Reset.
RIIC0CR2	0x0000000A	Issue start condition and stop condition.
RIIC0MR1	0x00000018	Enable bit counter write protection.
		400kbps
		9 bits : Bit counter
RIIC0MR2	0x00000000	SDA output delay clock source : IICφ
		SDA output delay counter : 0
		Timeout H count control : Disable
		Timeout L count control : Disable
		Timeout detection timer selection : Long mode
RIIC0MR3	0x0000007C	WAIT (No wait in last byte)
		RDRF set timing : 9th clock (8th clock in last byte)
		Release ACKBT write protection : Enable
		Transmit acknowledge : Enable
RIIC0BRL	0x000000F6	Bit rate low level cycle : 0x16
RIIC0BRH	0x000000E8	Bit rate high level cycle : 0x08
RIIC0FER	0x00000073	Enable SCL synchronization circuit.
		Enable digital noise filter circuit.
		Enable transmit suspension in NACK receiving.
		Enable master arbitration lost detection.
		Enable timeout detection function.
RIIC0IER	0x000000F3	Enable transmit data empty interrupt.
		Enable transmit completion interrupt.
		Enable receive completion interrupt.
		Enable transmit suspension interrupt in NACK receiving.
		Enable arbitration lost interrupt.
		Enable timeout interrupt.

Table 2-16 Interrupt Register Setting

Register Name	Setting Value	Function
EIBD882	0x00000000	Bind RIIC reception completion interrupt to PE0 (CPU0).
EIBD883	0x00000000	Bind RIIC transmit data empty interrupt to PE0 (CPU0).
EIBD887	0x00000000	Bind RIIC transmit completion interrupt to PE0 (CPU0).
EIC882	0x0040	Table reference/Priority level 0
EIC883	0x0040	Table reference/Priority level 0
EIC887	0x0040	Table reference/Priority level 0

Table 2-17 Port Register Setting

Register Name	Setting Value	Function
PORT0.PCR00_1	0x10020043	Set P00_1 to ALT_RIIC0SCL.
PORT0.PCR00_2	0x10020043	Set P00_2 to ALT_RIIC0SDA.

- Operation Flow

The following shows the flowchart in this operation example.

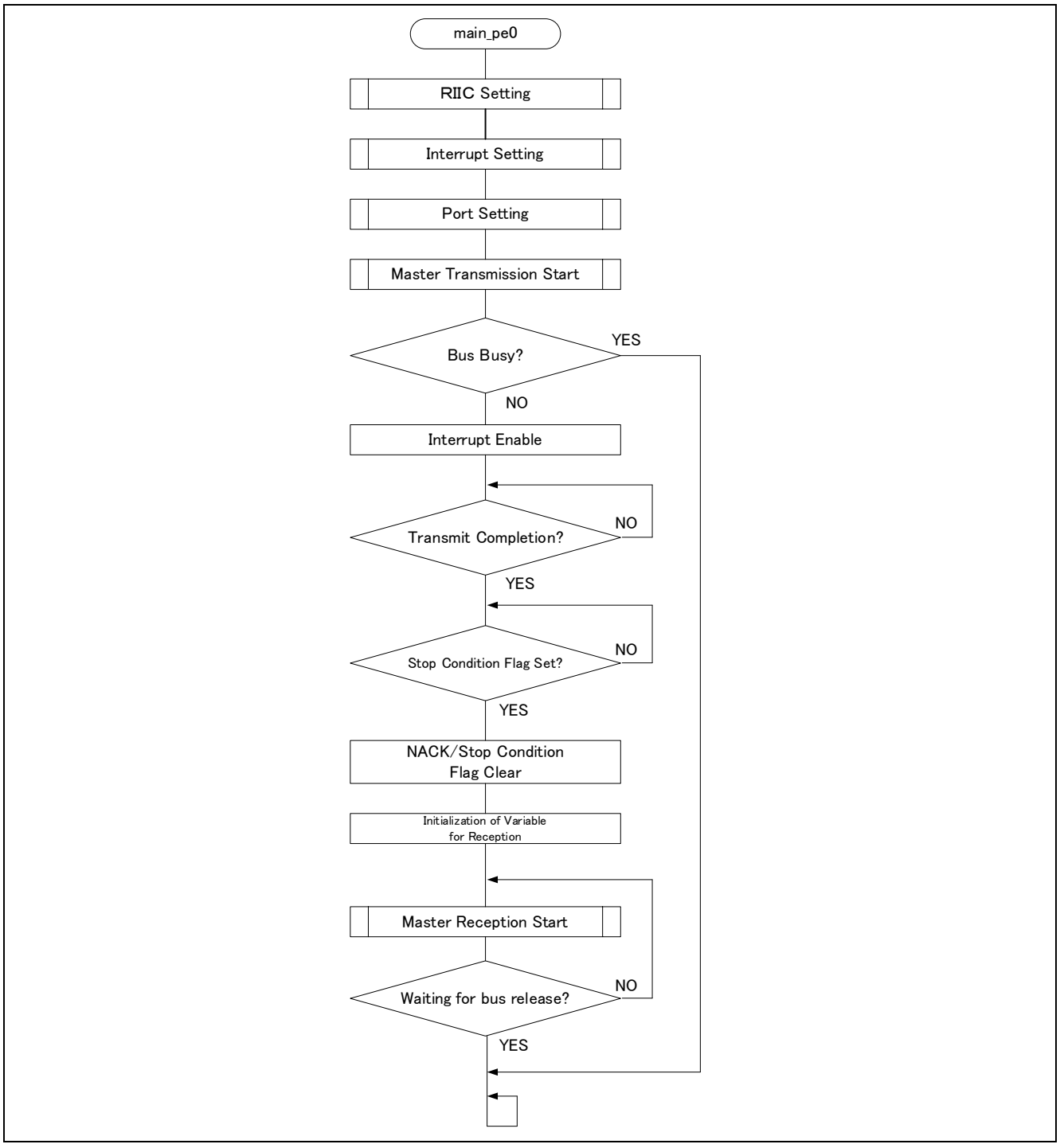

Figure 2-12 Main Function Flowchart

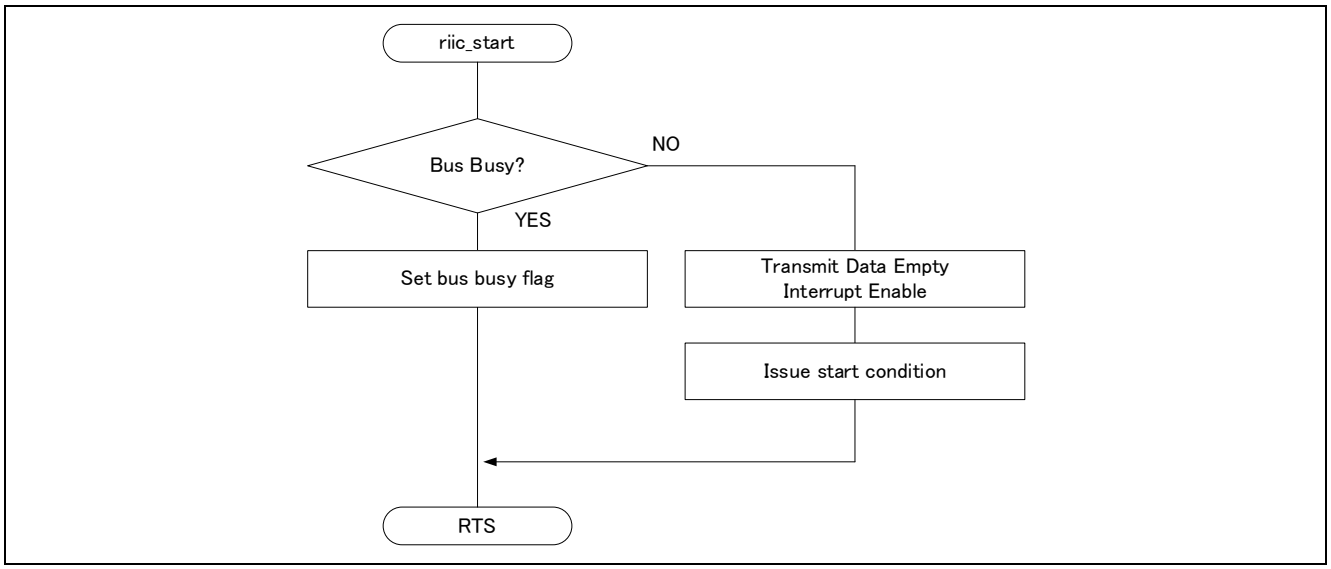

Figure 2-13 RIIC Start Function Flowchart

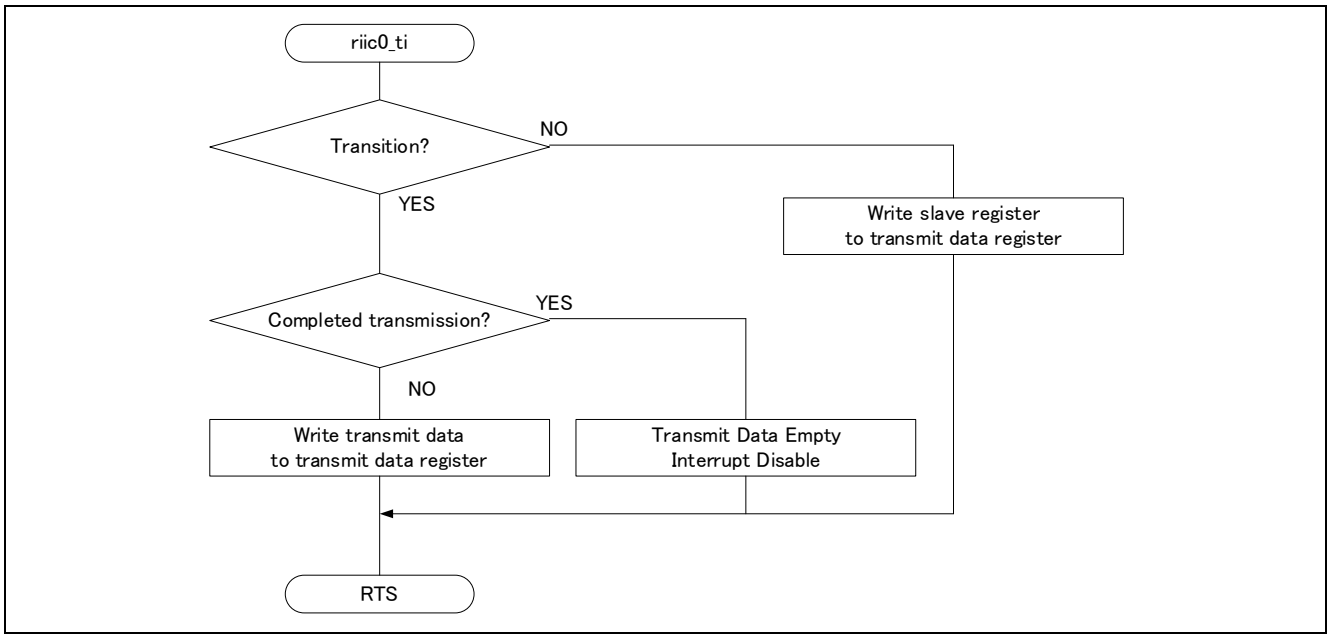

Figure 2-14 RIIC Transmit Data Empty Interrupt Function Flowchart

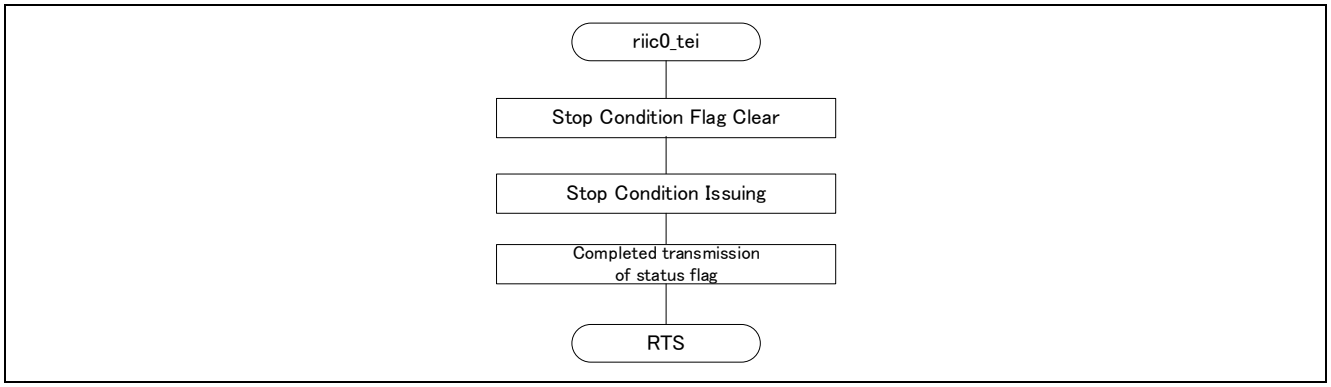

Figure 2-15 RIIC Transmit Complition Interrupt Function Flowchart

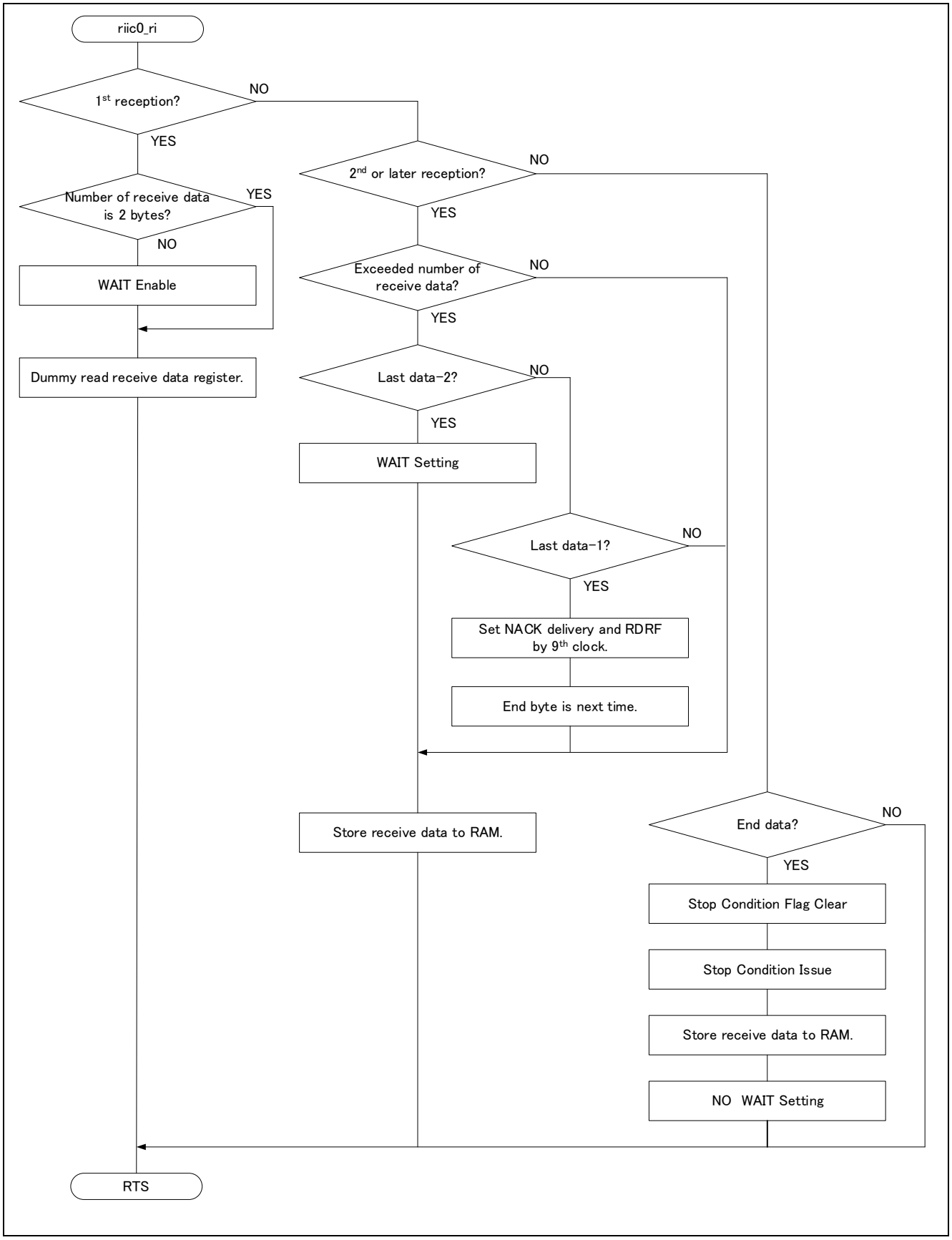

Figure 2-16 RIIC Receive Completion Interrupt Function Flowchart

2.4 Slave Transmit/Receive Operation

2.4.1 Specification Overview

In this operation example, perform 8 bytes data transition/reception by RIIC master.

Use master for RIIC , and set 400kbps to the 7 bits address and the baud rate RIIC.

Use SCL synchronous circuit, digital noise filter, NACK reception transfer suspension.

Connect SCL pin and SDA pin of RIIC with the slave system side.

2.4.2 System Configuration

Figure 2-17 shows the system configuration.

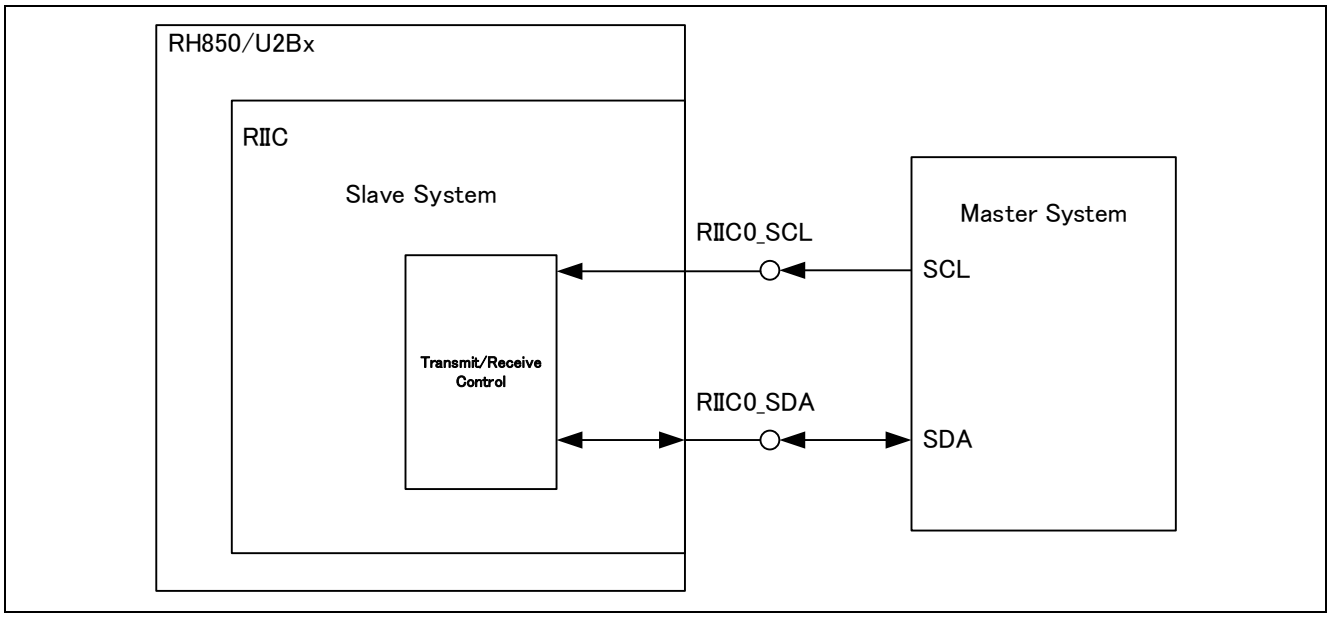

Figure 2-17 System Configuration

2.4.3 Software Explanation

- Module Explanation

The following shows the module list in this operation example.

Table 2-18 Module List

Module Name	Function Name	Function
Main routine	main_pe0	Perform various settings and application starting.
Port initialization routine	port_init	Perform port initialization.
RIIC initialization routine	riic_init	Perform RIIC initialization.
RIIC receive start routine	riic_receive	Set RIIC to receive start status.
RIIC transmit start routine	riic_send	Set RIIC to transmit start status.
Interrupt function initialize setting routine	intc_init	Perform RIIC interrupt setting.
Transmit data empty interrupt processing routine	riic0_ti	Perform transmit data setting processing.
Transmit completion interrupt processing routine	riic0_tei	Perform transmit completion processing.
RIIC error/event issue interrupt processing routine	riic0_ee	Perform start condition detection and stop condition detection processing.
Receive Complition Interrupt Processing Routine	riic0_ri	Perform read processing of transmit data.

- Register Setting

The following shows the register settings for various functions in this operation example.

Table 2-19 RIIC Ch0 Register

Register Name	Setting Value	Function
RIIC0CR1	0x00000001	Reset.
RIIC0CR2	0x0000000A	Issue start condition and stop condition.
RIIC0SAR0	0x00000040	Slave address : 0x20
RIIC0SER	0x00000009	Enable GCE enable slave address register 0.
		Enable slave address register 0.
RIIC0MR1	0x000000B8	Enable MST/TRS write protect.
		Enable bit counter write protection.
		PCLK/8
		9 bits : Bit counter
RIIC0MR2	0x00000000	SDA output delay clock source : IICφ
		SDA output delay counter : 0
		Timeout H count control : Disable
		Timeout L count control : Disable
		Timeout detection timer selection : Long mode
RIIC0MR3	0x0000007C	WAIT (No wait in last byte)
		RDRF set timing : 8th clock (9th clock in last byte)
		ACKBT write protection releasing : Enable
		Transmit acknowledge : Disable
RIIC0BRL	0x000000FF	Bit rate low level cycle : 0x1F
RIIC0BRH	0x000000FF	Bit rate high level cycle : 0x1F
RIIC0FER	0x00000070	Enable SCL synchronization circuit.
		Enable digital noise filter circuit.
		Enable transmit suspension in NACK receiving.
RIIC0IER	0x00000034	Enable transmit data empty interrupt.
		Enable transmit completion interrupt.
		Enable receive completion interrupt.
		Enable transmit suspension interrupt in NACK receiving.
		Enable start condition detection interrupt.

Table 2-20 Interrupt Register Setting

Register Name	Setting Value	Function
EIBD882	0x00000000	Bind RIIC reception completion interrupt to PE0 (CPU0).
EIBD883	0x00000000	Bind RIIC transmit data empty interrupt to PE0 (CPU0).
EIBD886	0x00000000	Bind RIIC error interrupt to PE0 (CPU0).
EIBD887	0x00000000	Bind RIIC transmit completion interrupt to PE0 (CPU0).
EIC882	0x0040	Table reference/Priority level 0
EIC883	0x0040	Table reference/Priority level 0
EIC886	0x0040	Table reference/Priority level 0
EIC887	0x0040	Table reference/Priority level 0

Table 2-21 Port Register Setting

Register Name	Setting Value	Function
PORT0.PCR00_1	0x10020043	Set P00_1 to ALT_RIIC0SCL.
PORT0.PCR00_2	0x10020043	Set P00_2 to ALT_RIIC0SDA.

- Operation Flow

The following shows the flowchart in this operation example.

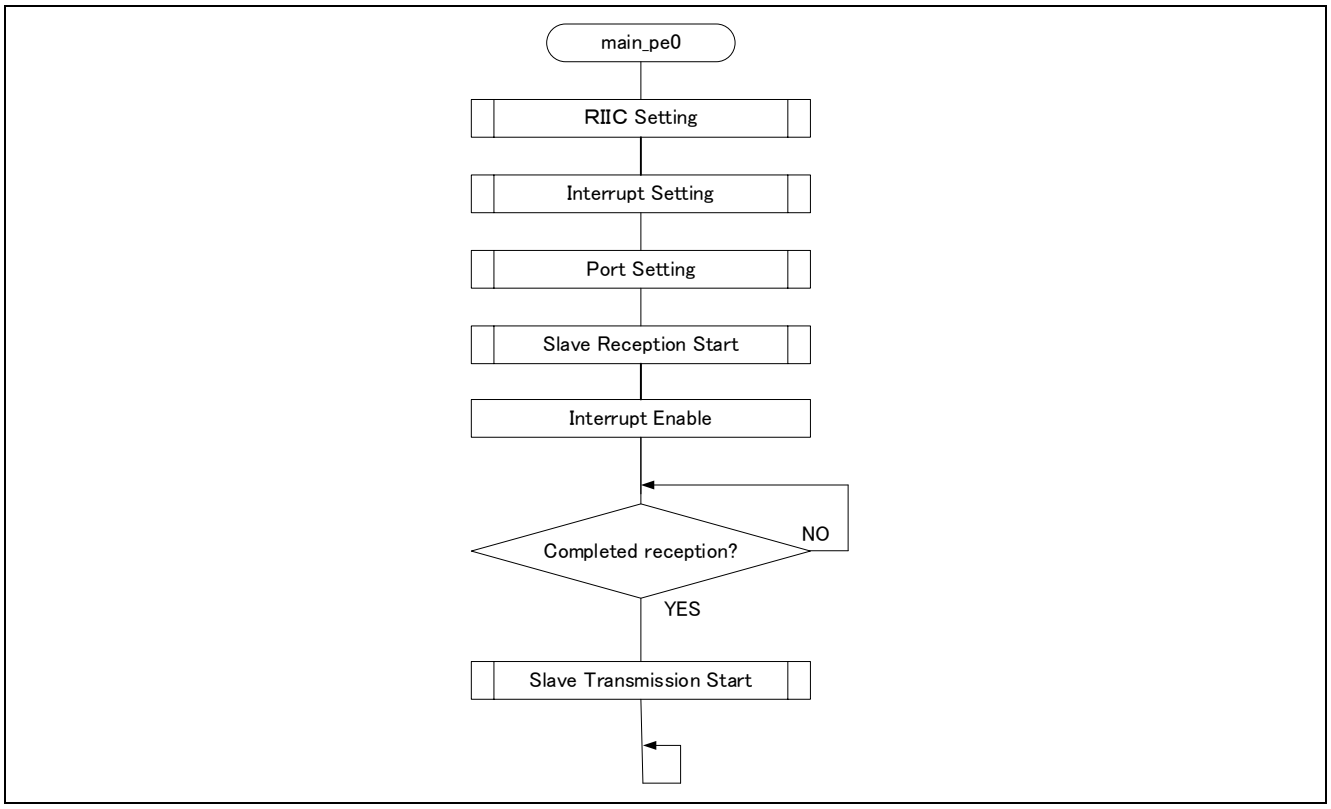

Figure 2-18 main Function Flowchart

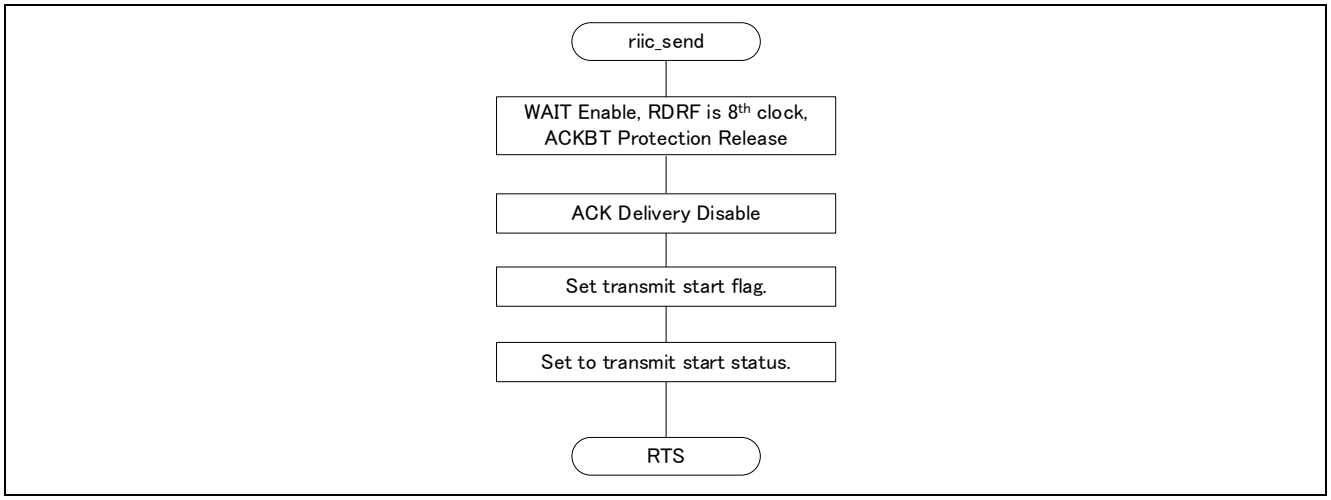

Figure 2-19 RIIC Transmit Function Flowchart

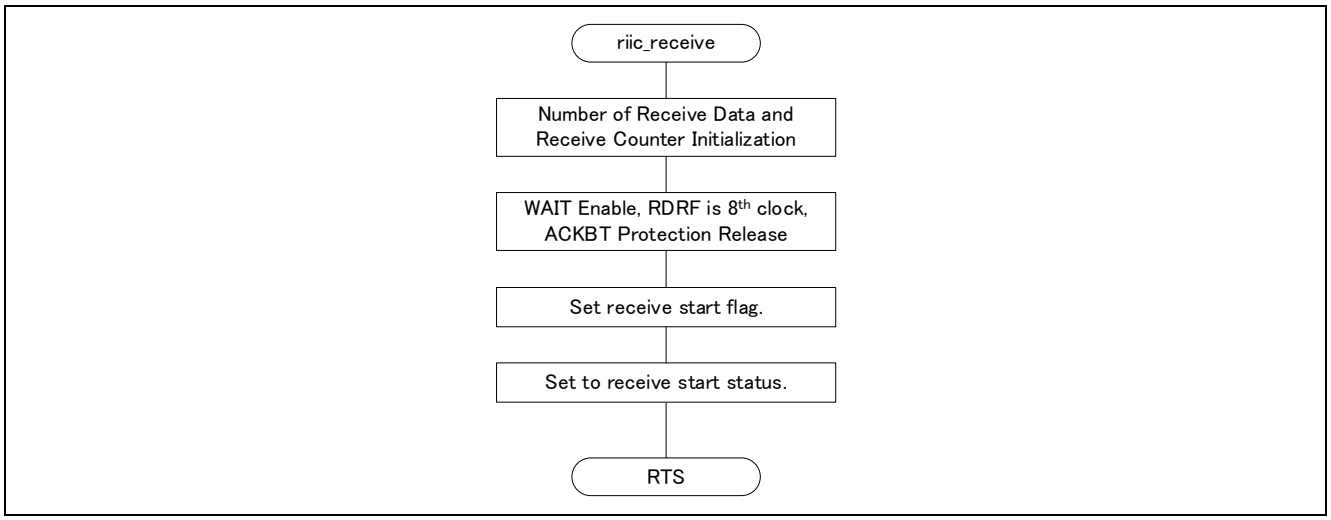

Figure 2-20 RIIC Receive Function Flowchart

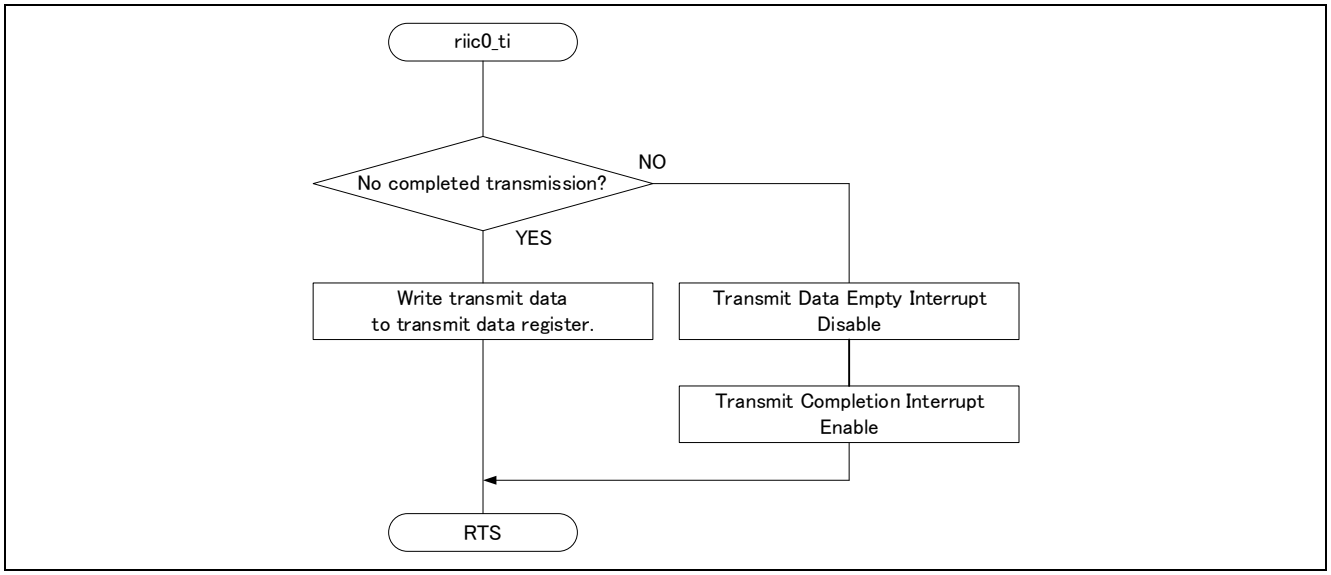

Figure 2-21 RIIC Transmit Data Empty Interrupt Function Flowchart

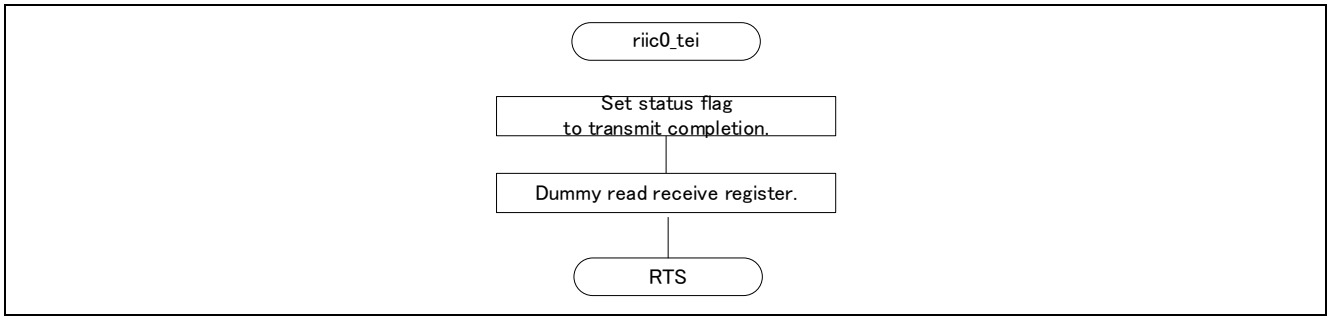

Figure 2-22 RIIC Transmit Completion Interrupt Function Flowchart

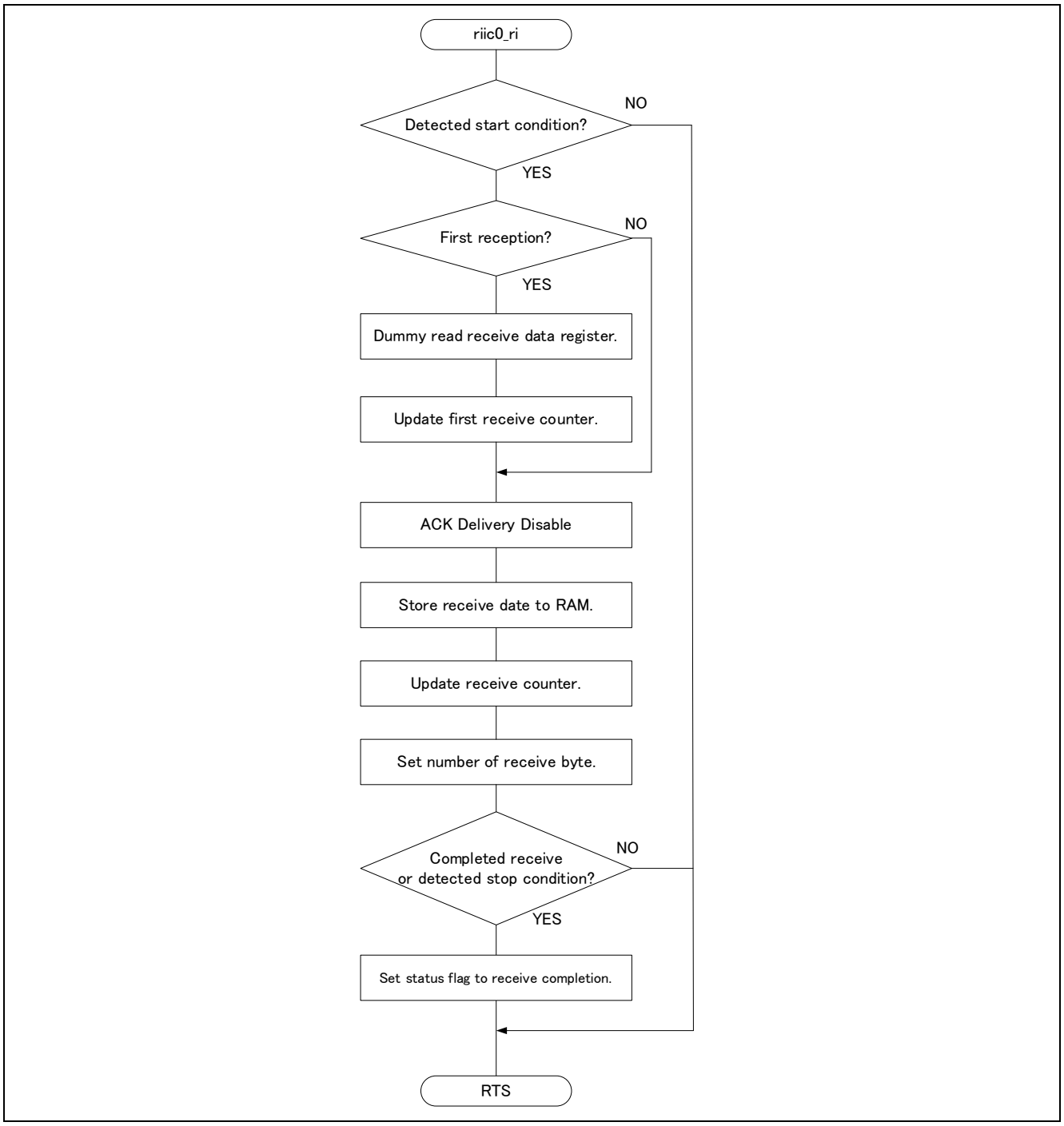

Figure 2-23 RIIC Receive Complition Interrupt Function Flowchart

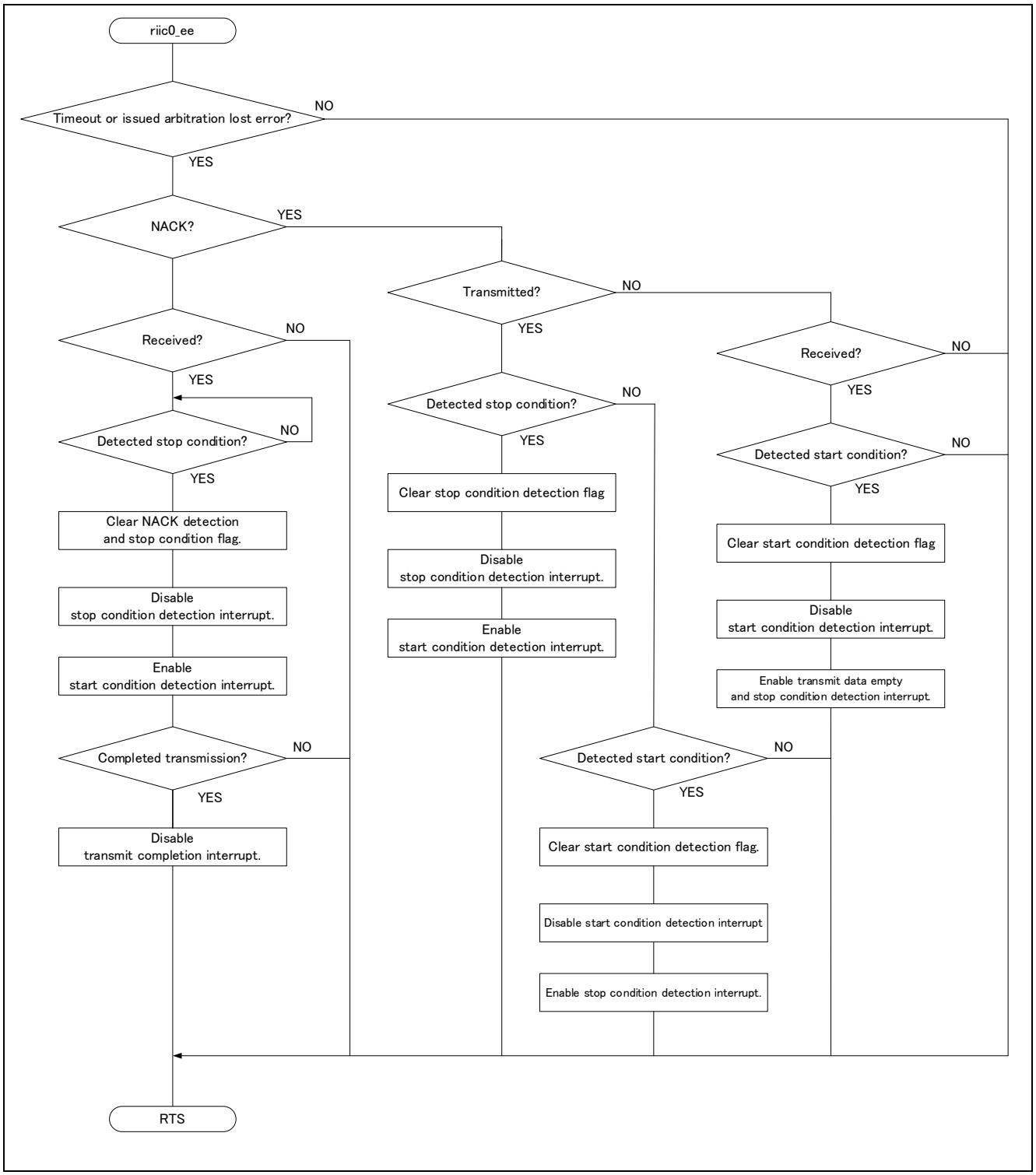

Figure 2-24 RIIC Error/Event Occurrence Interrupt Function Flowchart

Our Company’s Website and Inquiry

Website
http://japan.renesas.com/

Inquiry
http://japan.renesas.com/contact/

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2023.9.27	-	First Issue

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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