RH850/U2B Group

R01AN6570EJ0100
Rev.1.00

RHSB Application Note

Summary

This application note summarizes the operation example by using Renesas High-speed Bus.

The operation example described in this application note have been confirmed to operate, be sure to confirm the operation before using it.

Contents

1. Introduction

This application note describes the usage and creation example of Renesas High-speed Bus (RHSB) and Xross Bar (XBAR).

1.1 Use Function

The hardware functions for RH850/U2Bx using in this application note are shown below.

- Renesas High-speed Bus (RHSB)
- Xross Bar (XBAR)
- Virtual Port (P41_0～P41_15)
- ATU-Ⅴ (Timer A)

2. IC Control Corresponding to Microsecond Bus by RHSB Function

2.1 RHSB Overview

Figure 2-1 shows the block diagram of dawn stream part of RHSB Module. Figure 2-2 shows the block diagram of up stream part.

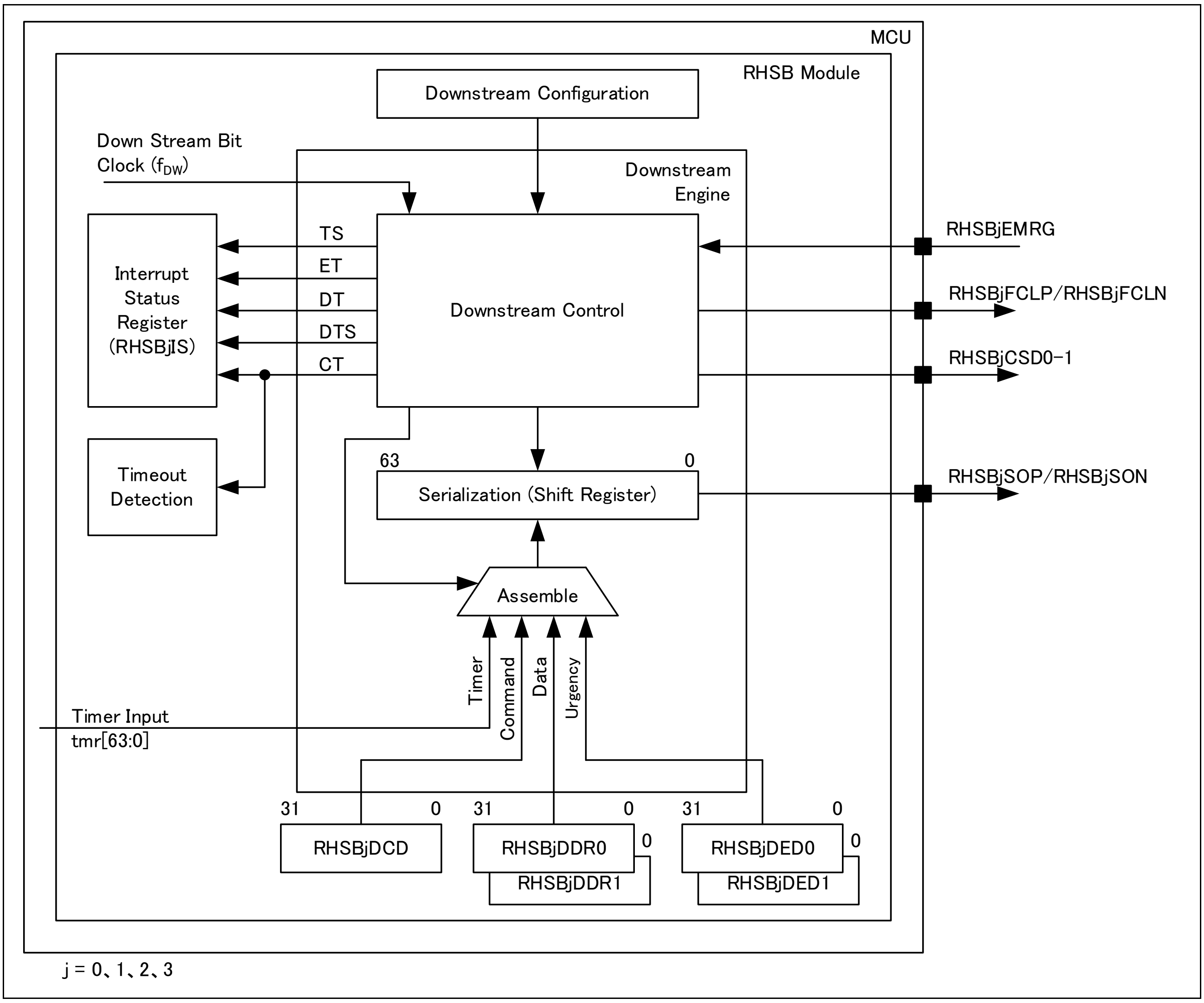

Figure 2-1 Block Diagram of Dawn Stream

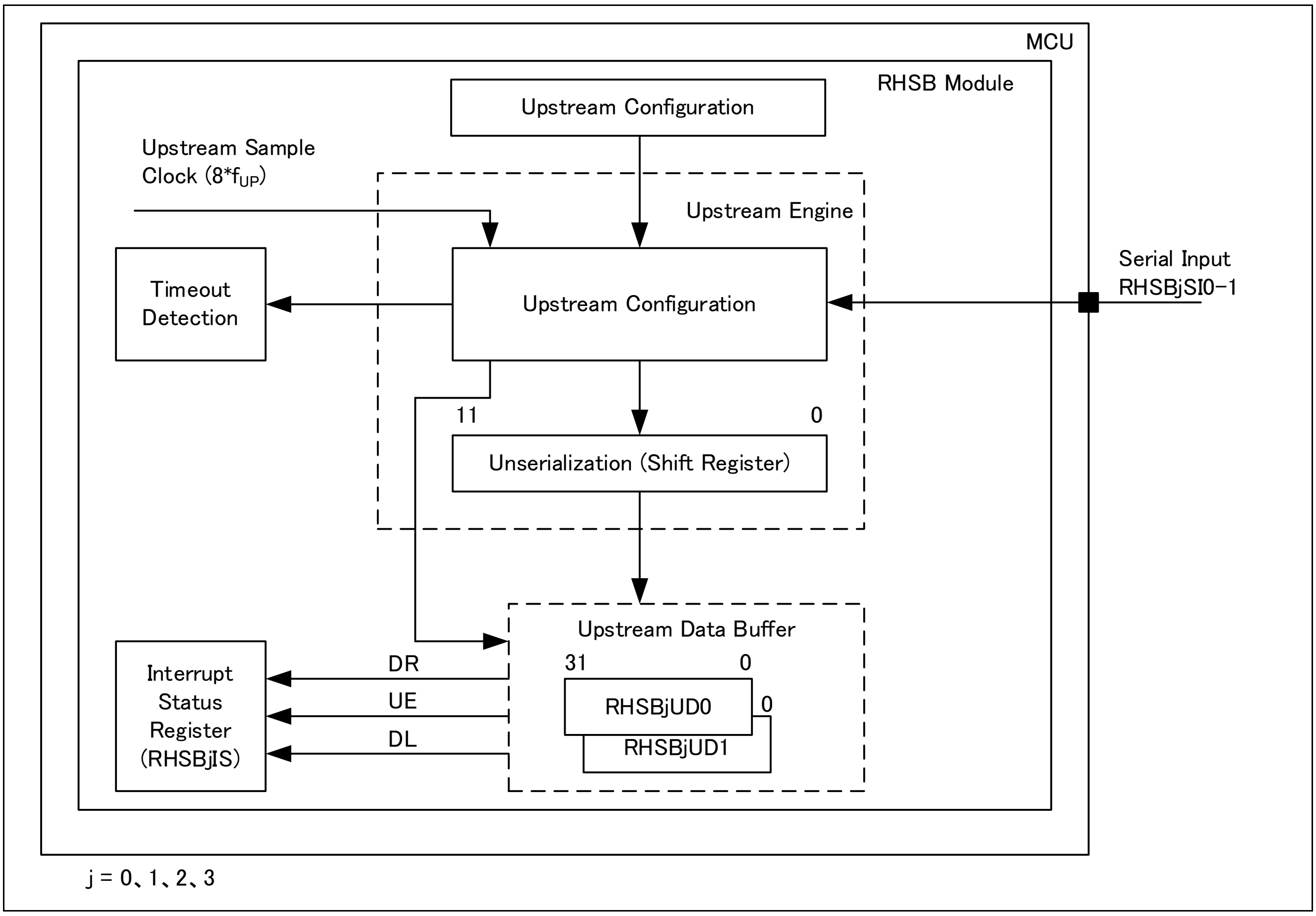

Figure 2-2 Upstream Block Diagram

2.2 IC Control Operation Corresponding to Microsecond Bus by RHSB Function

This section explains the reception of the command frame by RHSB downstream channel communication function and the data by the upstream channel communication function.

2.2.1 RHSB Input Format

Use Channel: RHSB0

Sequence Length: 1 DFTE(DFTE0)

Data Frame Passive Length: 16 bits

Downstream Bit Rate: fDW = fPE/8

Continues Time Length: 512 bits

Downstream Mode: Trigger Mode

Number of Downstream Data Receive Bit: 16 bits

Upstream Mode: DEDICATED Mode

Upstream Bit Rate: fUP=fDW/64

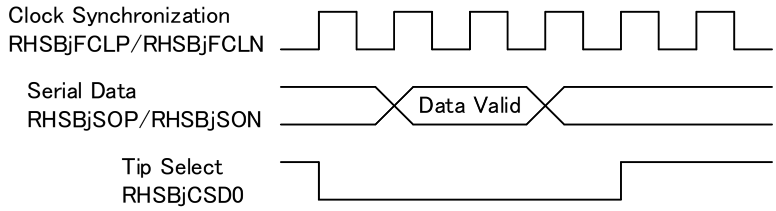

Figure 2-3 RHSB Downstream Communication (Synchronization)

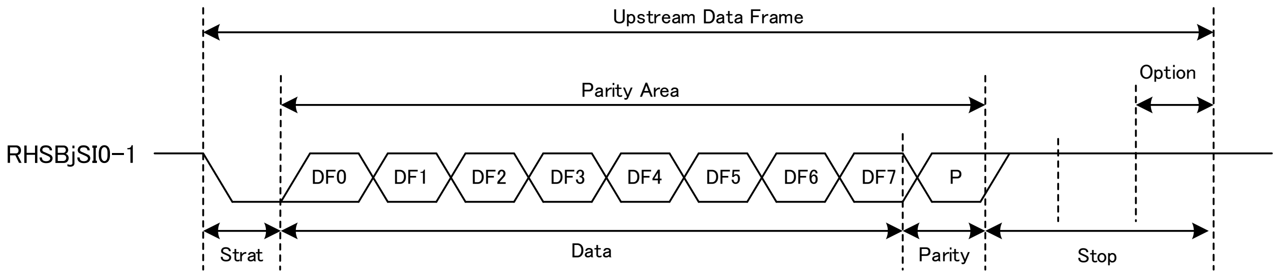

Figure 2-4 RHSB Upstream Communication (Unsynchronization)

2.2.2 System Configuration

Figure 2-5 shows the system configuration. For connecting with IC corresponding to the microsecond bus, ch0 of RHSB is used.

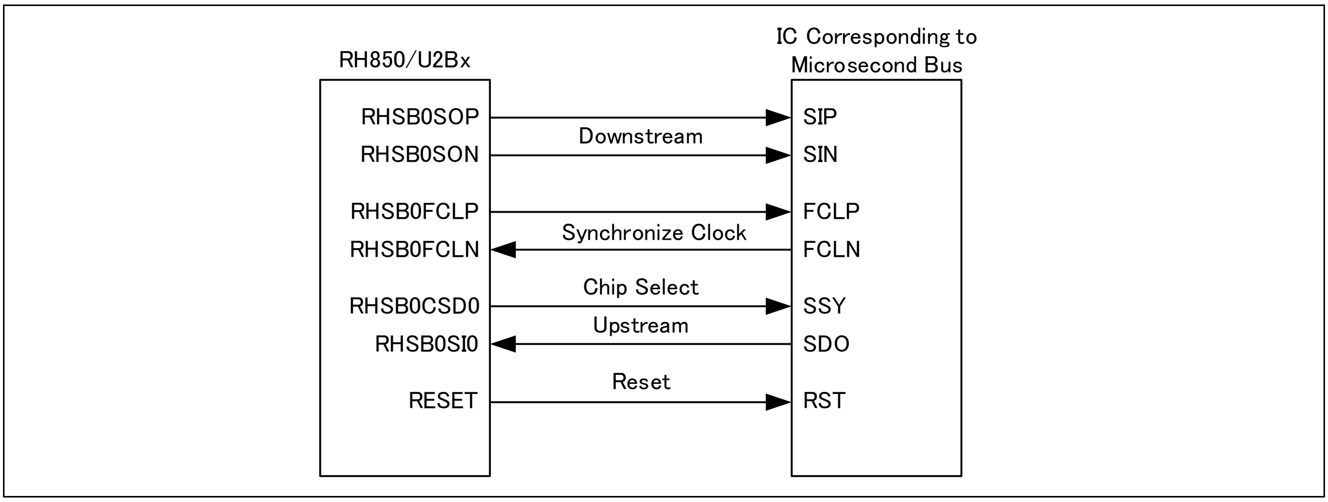

Figure 2-5 Block Diagram of RHSB Communication Block by RH850/U2Bx

2.2.3 Operation Status Explanation

In this operation example, perform the writing and reading for the internal register corresponding to the microsecond bus by the downstream communication.

At first, transmit H’AA write command (H’1541) to IC corresponding to the microsecond bus and write the external register to H’AA. Next, transmit the data frame (H’F0F0). At last, transmit the read command (H’1010), and receive the data of the internal register written first by the upstream communication.

2.2.4 Software Explanation

- Module Explanation

The following shows the module list in this operation example.

Table 2-1 Module List

Module Name	Label Name	Function
Maine routine	main_pe0	Perform each setting and the application booting.
RHSB initialization	rhsb0_init	Transfer to the port allocation of RHSB module and CONFIG mode, and perform the initial setting for the downstream and upstream.
RHSB data communication	rhsb0_comm	Transfer to ACTIVE mode and perform the transmission/reception of the data.

- Register Explanation

The following shows the use internal register of this task explanation.

Table 2-2 RHSB Register Setting

Register Name	Setting Value	Function
RHSB0GC	0x00000001	Operation status: CONFIG state
	↓	↓
	0x00000002	Operation status: ACTIVE state

RHSB0DCR	0x0F71FF41	Sequence length: 1 DFTE (DFTE0)
		Data frame passive length: 16 bits
		Downstream bit rate: fDW = fPE/8
		continuous time length: 512 bits
		Clock line phase: Change in rising edge.
		Clock active control: Clock is always active.
		Downstream mode: Trigger mode
RHSB0DEC	0x0F000000	Number of data bit 0: 16 bits
RHSB0SDC0	0x00280000	Tip select line polarity: Active “L”
		Content phase selection bit enable: With selection bit
RHSB0DEBA0	0xAAAAAAAA	Data source of DFTE0: Entire bit DDR0
RHSB0UCR	0x00001808	Receive timeout time: 25 bits
		Upstream: Enable
		Upstream mode: DEDICATED mode
RHSB0UCC	0x460F0F0F	Upstream frame: 8 bits
		Number of stop bit: 3bits Upstream bit rate: fUP=fDW/64
RHSB0UCS	0x00000000	Upstream reception: Channel 0
RHSB0DCD	0x1541	Downstream command data: 16 bits
RHSB0DTC	0x0F0X000X	Number of downstream command bit: 16 bits
		Downstream data transmission: Enable
RHSB0DDR0	0xF0F0	Downstream data frame: 16 bits
RHSB0UDR	0xXXXXXXXX	Indicate the data and status when receiving the upstream.
RHSB0IS	0xXXXXXXXX	Indicate the status when transmitting/receiving.

Table 2-3 Port Register Setting

Register Name	Setting Value	Function
PCR21_2	0x03000043	P21_2: RHSB0CSD0
PCR22_2	0x00000056	P22_2: RHSB0SI0
PCR25_3	0x00000052	P25_3: RHSB0FCLN
PCR25_4	0x00000052	P25_4: RHSB0FCLP
PCR25_5	0x00000052	P25_5: RHSB0SON
PCR25_6	0x00000052	P25_6: RHSB0SOP
LVDSCTRLD	0x0001000A	LVDS output enable of P25_6, P25_5, P25_4, and P25_3
		3V mode of P25_4 and P25_3

- Use Variable Explanation

The following shows the use variable in this task explanation.

Table 2-4 Use Variable Explanation

Variable Name	Setting Value	Function
wait	0x00000800	Variable for software wait. It is used as the wait generation of LVDS input for LVDS output wait time after setting RHSB pin function.
read_UDR	0xXXXXXXXX	Variable for RHSB0UDR reading.

2.3 Flowchart

The following shows the flowchart in the operation example.

2.3.1 Main

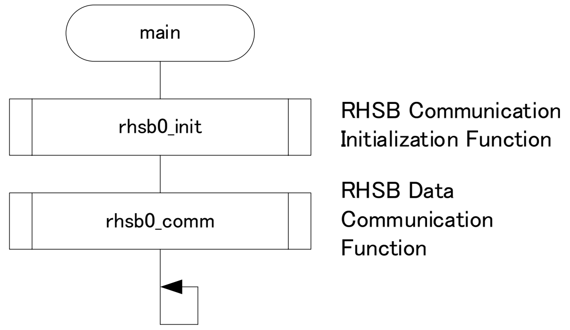

Figure 2-6 Main Module Flowchart

2.3.2 RHSB Initialization

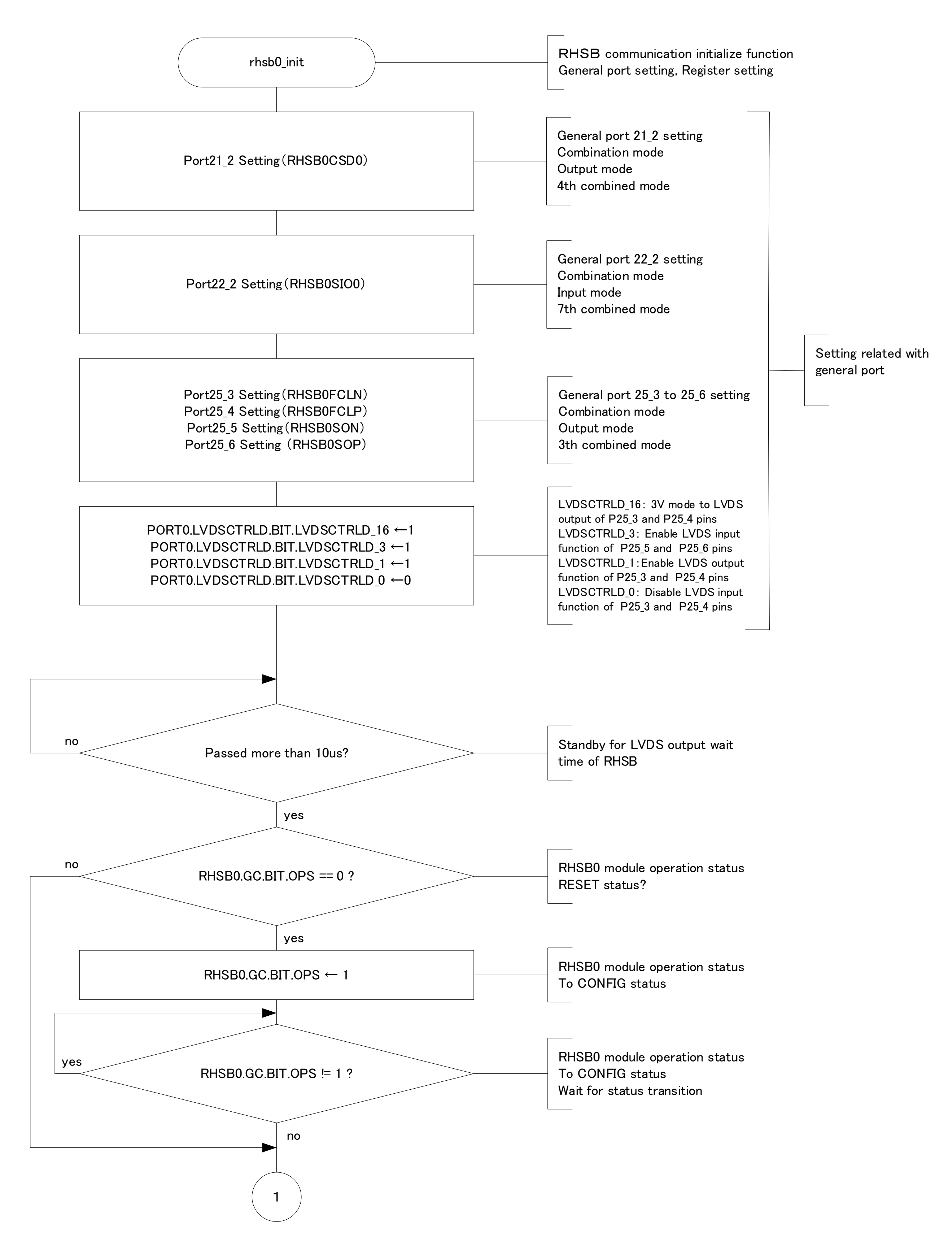

Figure 2-7 rhsb0_init Module Flowchart (Part 1)

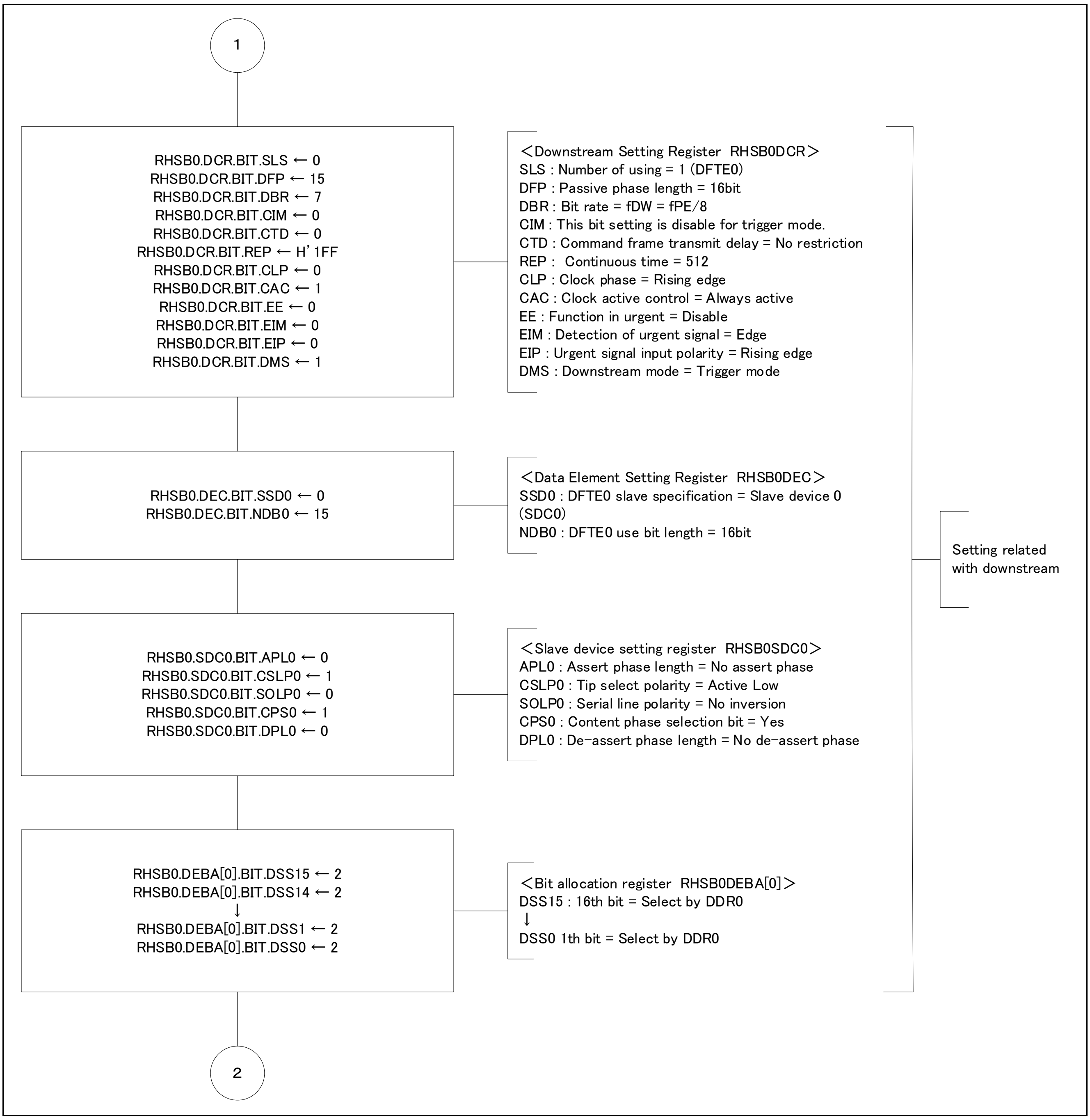

Figure 2-8 rhsb0_init Module Flowchart (Part 2)

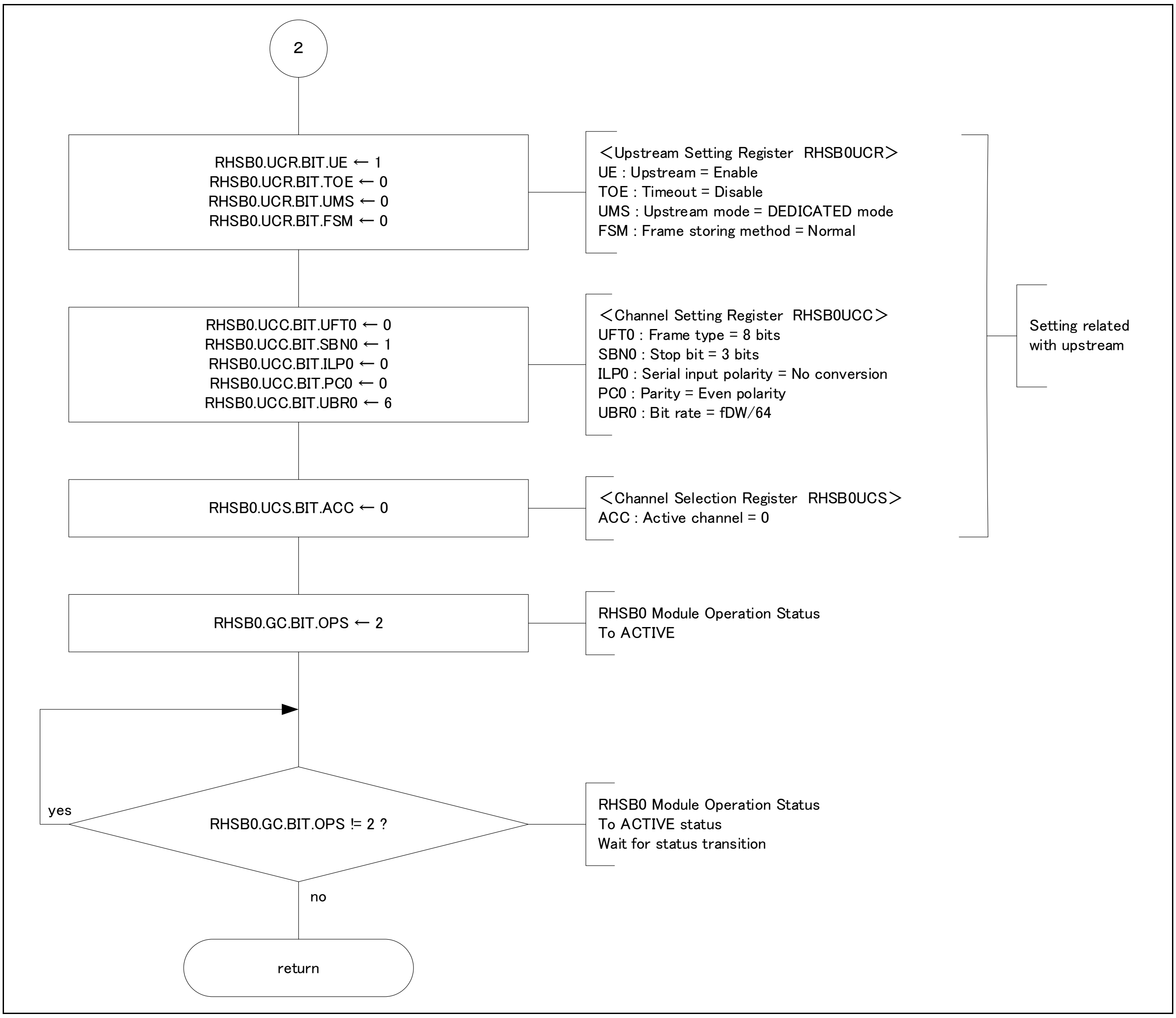

Figure 2-9 rhsb0_init Module Flowchart (Part 3)

2.3.3 RHSB Data Communication

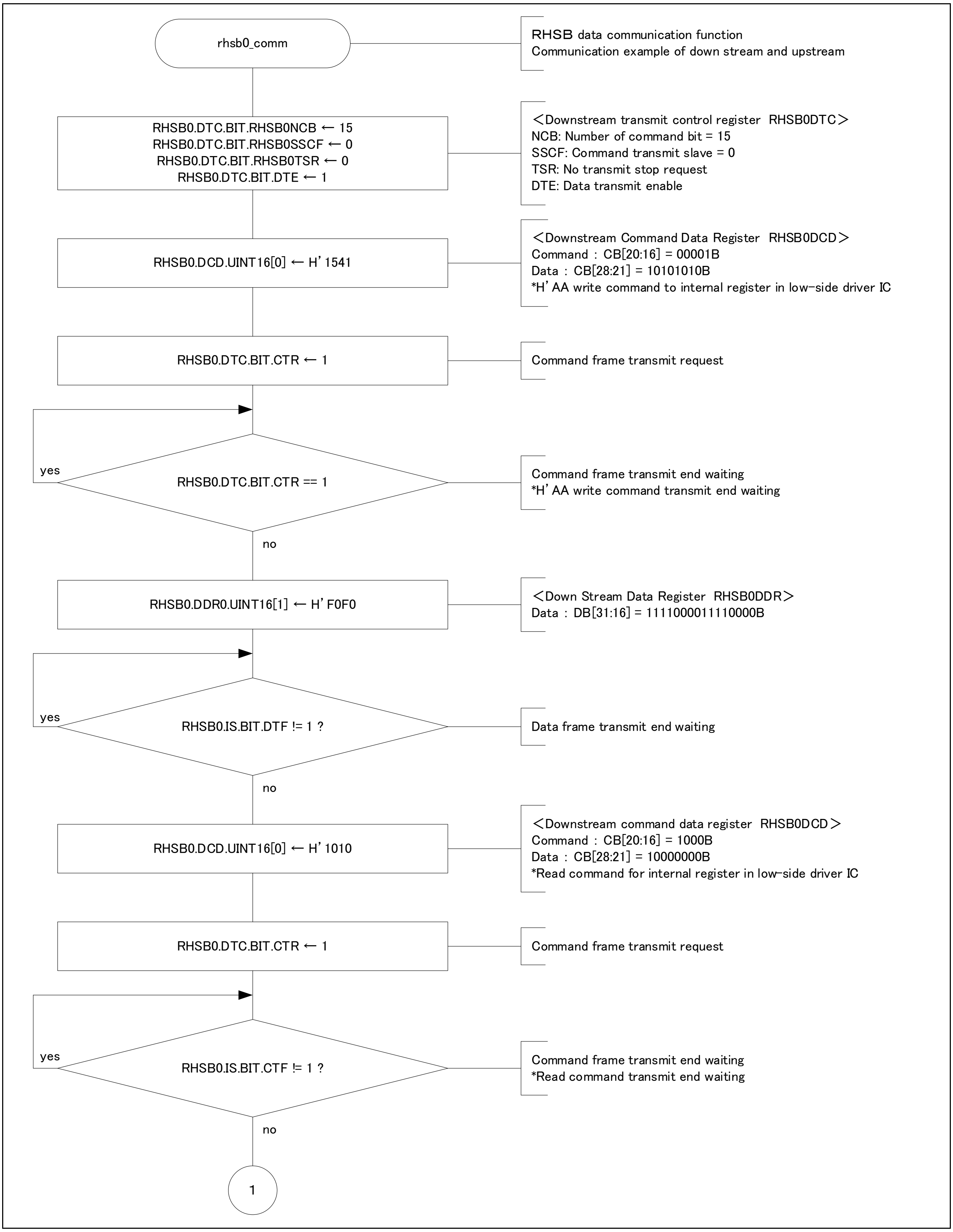

Figure 2-10 rhsb0_comm Module Flowchart (Part 1)

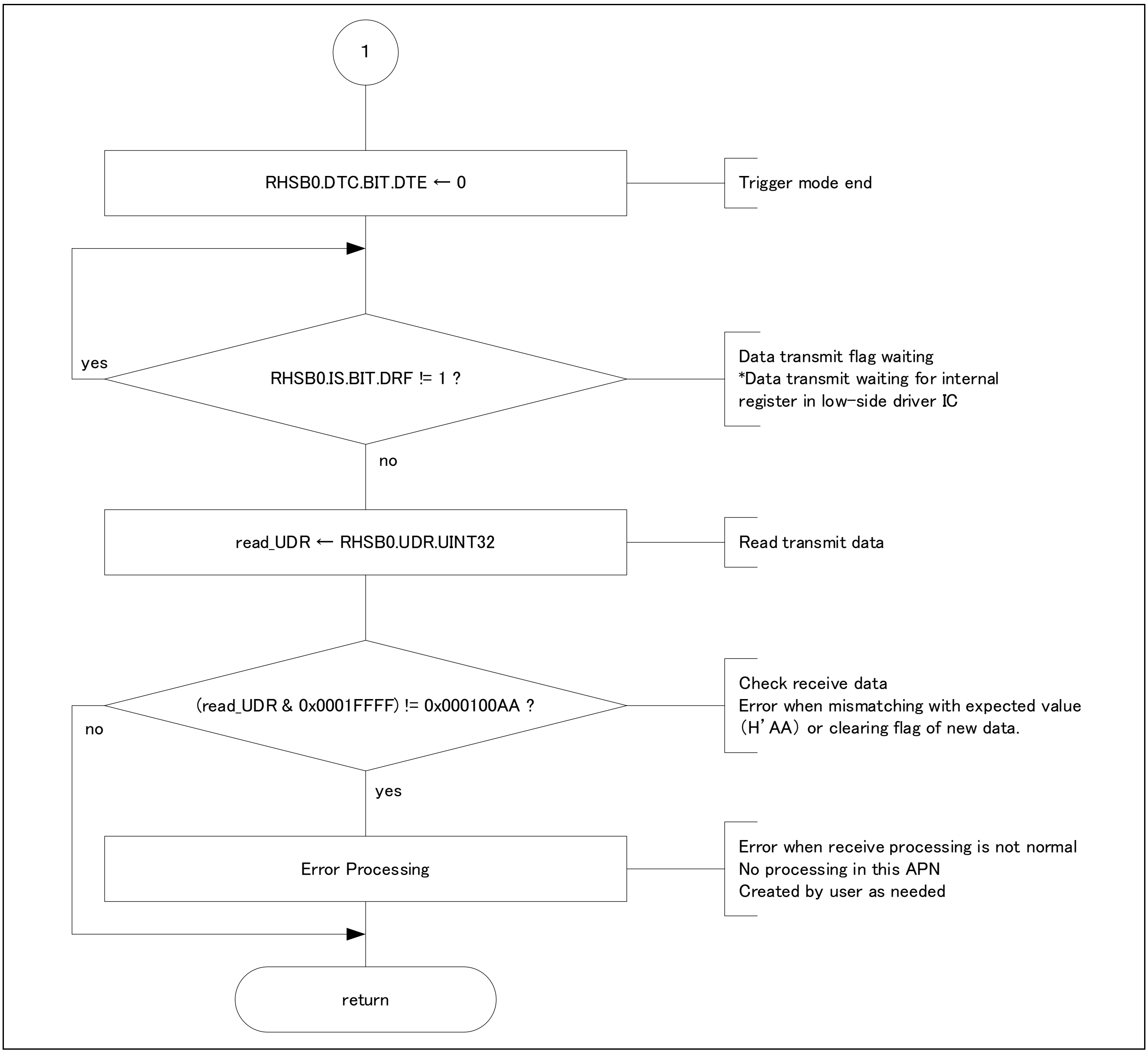

Figure 2-11 rhsb0_comm Module Flow Chart (Part 2)

3. Xross Bar (XBAR) Operation Example

3.1 Xross Bar (XBAR) Overview

Xross bar (XBAR) selects the signal form the virtual port by the multiplexer, and outputs the any signal to RHSB.

Figure 3-1 shows the xross bar configuration. The xross bar is selection logic that connects between ATU-Ⅳ/ GTM and the virtual port. It has four sub XBAR in 16 bits for RHSB1 channel.

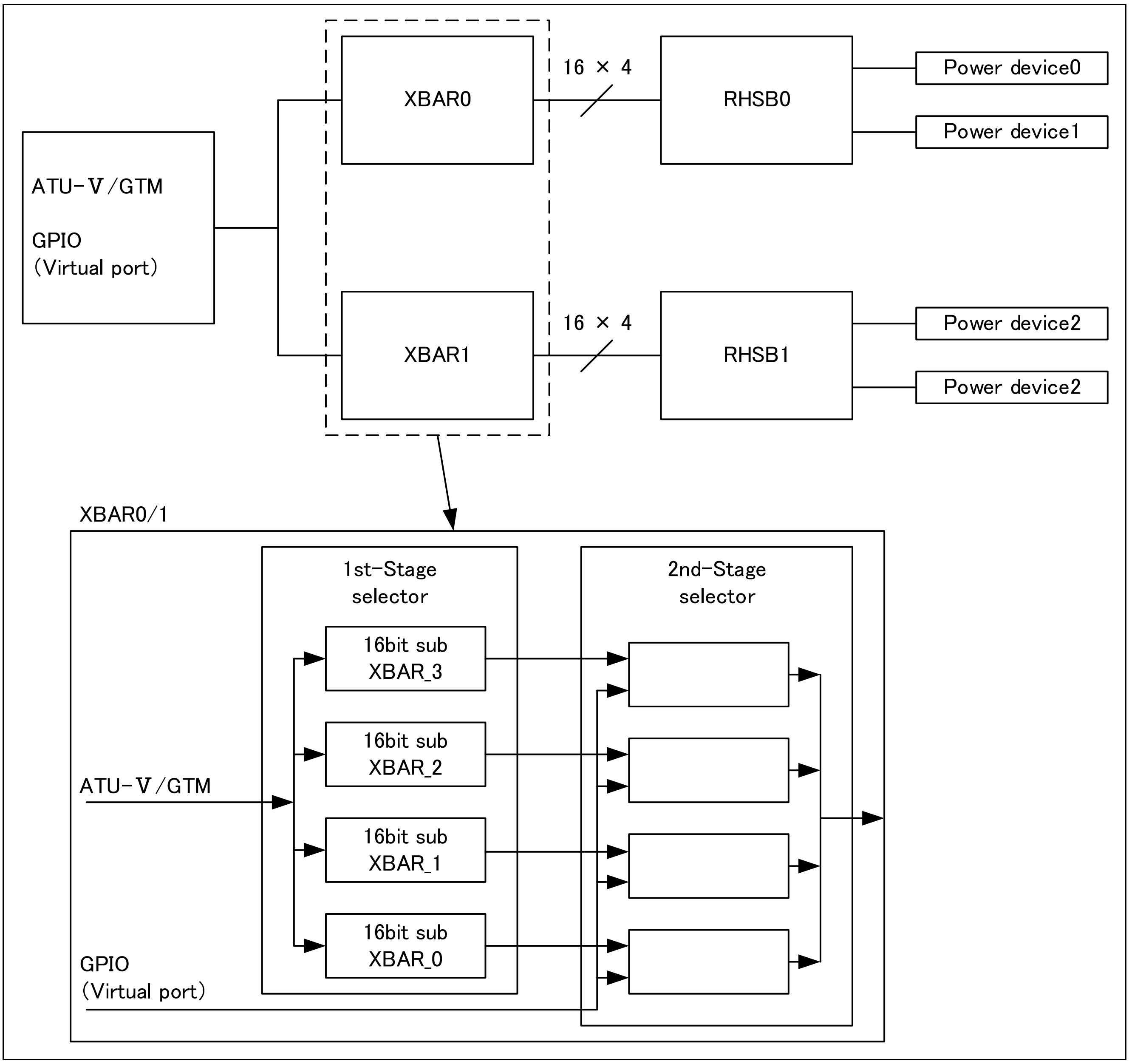

Figure 3-1 Xross Bar Configuration

3.2 Xross Bar (XBAR) Operation Used Virtual Port

This section explains the method outputting the value of the virtual port by RHSB.

3.2.1 RHSB Output Format

Use channel: RHSB1

Sequence length: 1 DFTE (DFTE0)

Data frame passive length: 16 bits

Downstream bit rate: fDW = fPE/16

Continuous time length: 512 bits

Downstream mode: Single cycle continuous mode

Data bit: 16 bits

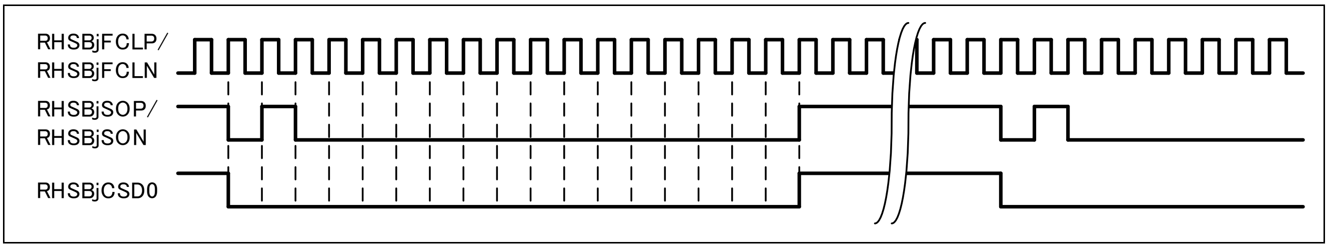

Figure 3-2 RHSB Output Waveform Example

3.2.2 System Configuration

Figure 3-3 shows the system configuration.

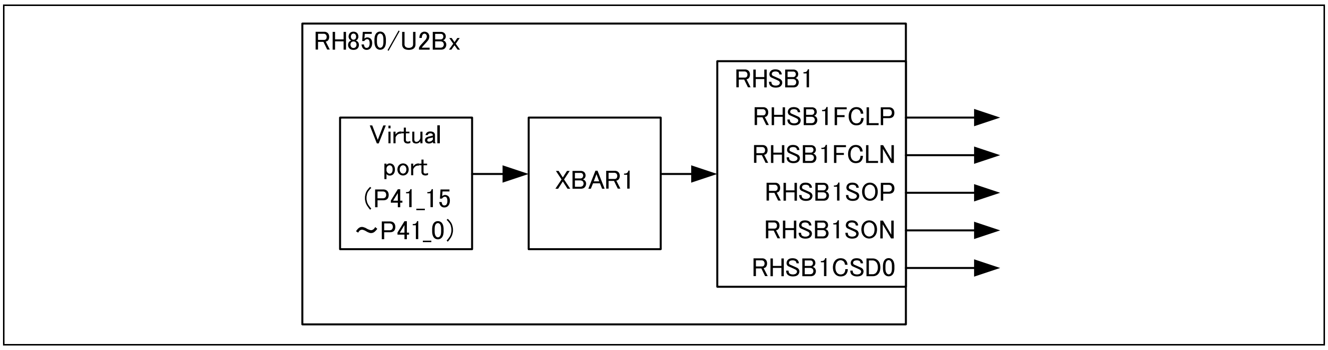

Figure 3-3 System Configuration

3.2.3 Operation Status Explanation

In this operation example, the port register value of the virtual port (P41_15~P41_0) is outputted in RHSB1.

Update the port register in the certain cycle. When the port register is updated, the output of RHSB1 is changed.

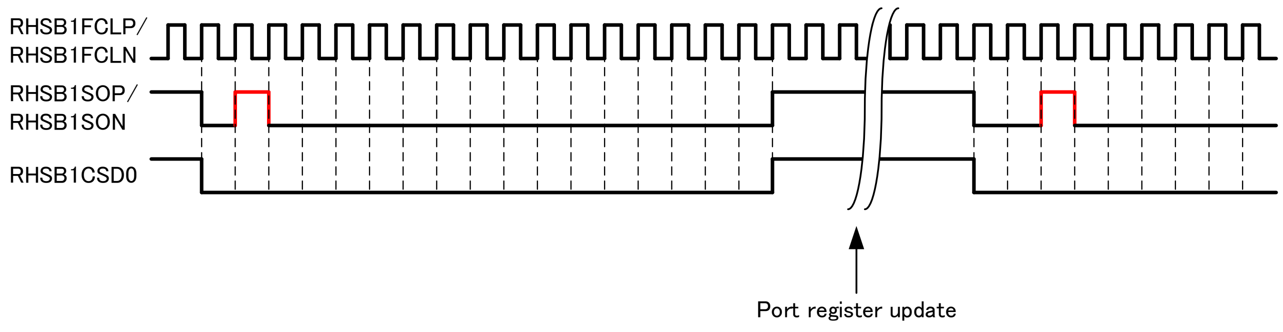

Figure 3-4 Operation Example

3.2.4 Software Explanation

- Module Explanation

The following shows the module list in this operation example.

Table 3-1 Module List

Module Name	Label Name	Function
Maine routine	main_pe0	Perform each setting and the application booting.
Port initialization routine	port_init	Perform the initial setting of the port.
RHSB1 initialization routine	rhsb1_init	Perform initialization setting of RHSB1.
Software timer	Wait_Timer	Count 200ms by timer A for processing waiting.

- Register Setting

The following shows the register setting of each function.

Table 3-2 RHSB Register Setting

Register Name	Setting Value	Function
RHSB1GC	0x00000001	Operation status: CONFIG state
	↓	↓
	0x00000002	Operation status: ACTIVE state
RHSB1DTC	0x00000001	Data transmission: Enable
RHSB1DCR	0x0F81FF40	Sequence length: 1 DFTE (DFTE0)
		Data frame passive length: 16 bits
		Downstream bit rate: fDW = fPE/16
		Continues time length: 512 bits
		Clock line phase: Change in rising edge.
		Clock active control: Clock is always active.
		Downstream mode: single cycle continuous mode
RHSB1DEC	0x0F000000	Number of data bit 0: 16 bits

Register Name	Setting Value	Function
RHSB1SDC0	0x00280000	Chip select line polarity: Active “L”
		Content phase selection bit enable: With selection bit
RHSBG1CRO0	0x00000000	XBAR1 output: P41_15～P41_0

Table 3-3 Port Register Setting

Register Name	Setting Value	Function
PCR10_0	0x00000042	P10_0: RHSB1FCLP
PCR10_1	0x00000042	P10_1: RHSB1FCLN
PCR10_2	0x00000042	P10_2: RHSB1SOP
PCR10_3	0x00000042	P10_3: RHSB1SON
PCR10_7	0x00000042	P10_7: RHSB1CSD0
PCR11_6	0x00000051	P11_6: RHSB1SI0
PCR11_3	0x00000051	P11_3: RHSB1EMRG
LVDSCTRLC	0x0000000A	Enable LVDS output function of P10_2, P10_3.
		Enable LVDS output function of P10_0, P10_1.

Table 3-4 ATU (Timer A) Register Setting

Register Name	Setting Value	Function
TCNTA	0xFF85EDFF	Free running counter A count start value
ATUENR	0x0003	Timer A count operation enable
		Enable clock generation of prescaler

3.3 Flowchart

The following shows the flowchart in this operation example.

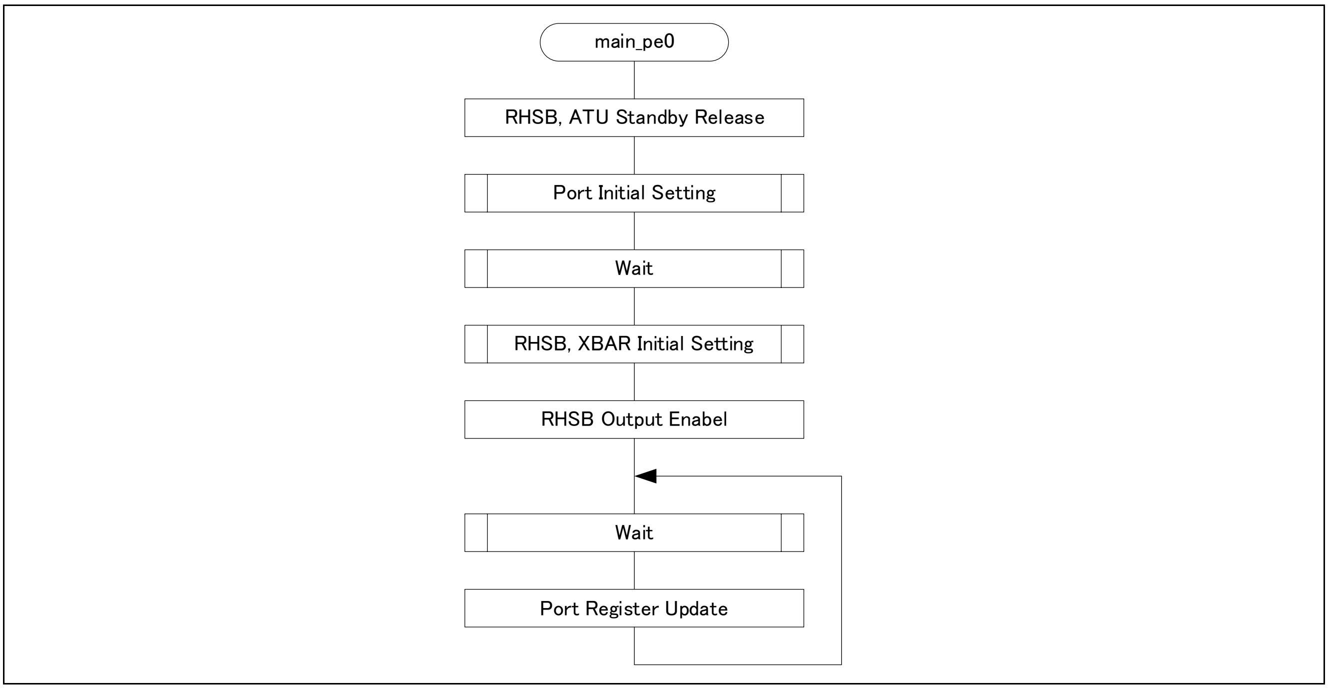

Figure 3-5 Flowchart

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Revision History

Rev.	Data	Description	
		Page	Summary
1.00	2023.10.5	-	First edition issued

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