RH850/U2B Group

QoS Application Note

R01AN6484EJ0010
Rev.0.10

Summary

This application describes QoS function in single chip microcomputer for automobile“RH850/U2Bx” series.

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Target Device

- RH850/U2B Group

Target Integrated Development Environment

CS+(from RENESAS Electronics)

Version : E8.07.00g6

Device file : DR7F702Z21EDBB.DVF

Reference Document

RH850/U2B User’s Manual: Hardware

For function details and electrical characteristics, please refer to “User’s Manual: Hardware”.

This application note is based on the following manual.

・ RH850/U2B User’s Manual (Rev.0.50): R01UH0923EJ0050

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1. Application

This application describes the QoS operation example for RH850/U2B.

2. Function Overview

There are the following functions for QoS of U2B.

Table 2-1 Function Overview

Function	Explanation
Bandwidth regulator	● Control the access from the bus master during specified period. ● Selectable from two modes for controlling the access. ➢ Interval Mode ➢ Threshold Mode ● Individually count the number of read/write accesses from the bus master. ● Support the next bus master. ➢ Code Flash Bus of Each CPU ➢ Peripheral Bus of Each CPU ➢ CRAM Bus of Each CPU ➢ System Bus of DMA (sDMAC or DTS) ➢ H-Bus of GTM, RHSIF, FLXA and R_SWITCH ➢ Code Flash Bus of DFP ➢ System Bus of DFP ➢ Code Flash Bus of ICUM ➢ System Bus of ICUM and AES
Latency monitor	● Monitor the request and response of the bus master, and count the access latency cycle. ● Individually monitor the read/write access. ● The specific access is possible to count by filtering the following. ➢ Address area ➢ SPID ● Supports 4 monitor channels per QoS unit. ● The interrupt function that detects the excessive access latency for a monitor channel. ● Mounted eight interrupt pins and possible to bind the interrupt from the monitor channel. ● Support the next bus master. ➢ Code Flash Bus of Each CPU ➢ Peripheral Bus of Each CPU ➢ CRAM Bus of Each CPU ➢ System Bus of DMA (sDMAC or DTS) ➢ H-Bus of GTM, RHSIF, FLXA and R_SWITCH ➢ Code Flash Bus of DFP ➢ System Bus of DFP ➢ Code Flash Bus of ICUM ➢ System Bus of ICUM and AES

2.1 Number of QoS Unit

The QoSID and unit name that corresponding to the bus master supported by QoS are listed below.

Table 2-2 Bus Master Supported by QoS

QoS ID	Unit Name	Bus Master	R/W	U2B24	U2B20	U2B10	U2B6
0	QOSCNT_FL_PE0CL0	CPU0 Code Flash Bus	R	Yes	Yes	Yes	No
1	QOSCNT_VC_PE0CL0	CPU0 Peripheral Bus	R/W	Yes	Yes	Yes	No
2	QOSCNT_MB_PE0CL0	CPU0 Cluster RAM Bus	R/W	Yes	Yes	Yes	No
3	QOSCNT_FL_PE1CL0	CPU1 Code Flash Bus	R	Yes	Yes	Yes	No
4	QOSCNT_VC_PE1CL0	CPU1 Peripheral Bus	R/W	Yes	Yes	Yes	No
5	QOSCNT_MB_PE1CL0	CPU1 Cluster RAM Bus	R/W	Yes	Yes	Yes	No
6	QOSCNT_FL_PE0CL1	CPU2 Code Flash Bus	R	Yes	Yes	Yes	No
7	QOSCNT_VC_PE0CL1	CPU2 Peripheral Bus	R/W	Yes	Yes	Yes	No
8	QOSCNT_MB_PE0CL1	CPU2 Cluster RAM Bus	R/W	Yes	Yes	Yes	No
9	QOSCNT_FL_PE1CL1	CPU3 Code Flash Bus	R	Yes	Yes	Yes	No
10	QOSCNT_VC_PE1CL1	CPU3 Peripheral Bus	R/W	Yes	Yes	Yes	No
11	QOSCNT_MB_PE1CL1	CPU3 Cluster RAM Bus	R/W	Yes	Yes	Yes	No
12	QOSCNT_FL_PE0CL2	CPU4 Code Flash Bus	R	Yes	Yes	No	No
13	QOSCNT_VC_PE0CL2	CPU4 Peripheral Bus	R/W	Yes	Yes	No	No
14	QOSCNT_MB_PE0CL2	CPU4 Cluster RAM Bus	R/W	Yes	Yes	No	No
15	QOSCNT_FL_PE1CL2	CPU5 Code Flash Bus	R	Yes	Yes	No	No
16	QOSCNT_VC_PE1CL2	CPU5 Peripheral Bus	R/W	Yes	Yes	No	No
17	QOSCNT_MB_PE1CL2	CPU5 Cluster RAM Bus	R/W	Yes	Yes	No	No
24	QOSCNT_DTS	DTS AXI Bus	R/W	Yes	Yes	Yes	No
25	QOSCNT_SDMAC0	SDMAC0 AXI Bus	R/W	Yes	Yes	Yes	No
26	QOSCNT_SDMAC1	SDMAC1 AXI Bus	R/W	Yes	Yes	Yes	No
27	QOSCNT_FL_ICUM	ICUM Code Flash Bus	R	Yes	Yes	Yes	No
28	QOSCNT_SYS_ICUM	ICUM System Bus	R/W	Yes	Yes	Yes	No
29	QOSCNT_ACEU0	ACEU0 AXIBus	R/W	Yes	Yes	No	No
30	QOSCNT_ACEU1	ACEU1 AXIBus	R/W	Yes	Yes	No	No
31	QOSCNT_FL_DFP	DFP Code Flash Bus	R	Yes	Yes	Yes	No
32	QOSCNT_SYS_DFP	DFP System Bus	R/W	Yes	Yes	Yes	No
33	QOSCNT_GTM	GTM AXIBus	R/W	Yes	Yes	Yes	No
34	QOSCNT_RHSIF0	RHSIF0 AXI Bus	R/W	Yes	Yes	Yes	No
35	QOSCNT_RHSIF1	RHSIF1 AXI Bus	R/W	Yes	No	No	No
36	QOSCNT_FLXA0	FLXA0 AXIBus	R/W	Yes	Yes	Yes	No
38	QOSCNT_ETHER0	Ether 0 AXI Bus	R/W	No	Yes	Yes	No
39	QOSCNT_ETHER1	Ether 1 AXI Bus	R/W	No	Yes	No	No
40	QOSCNT_R_SWITCH	R_SWITCH AXIBus	R/W	Yes	No	No	No

Yes: Support.

No: Not support.

2.2 QoS Clock Supply

The clock supply to each unit of QOS is listed below.

Table 2-3 Clock Supply

Unit Name	Unit/Clock Name	Supplied Clock Name
QOSCNT_FL_PEpCLk(p=0-1, k=0-2)	CLK	CLK_CPU
	PCLK	CLK_HBUS
QOSCNT_VC_PEpCLk(p = 0-1, k = 0-2)	CLK	CLK_CPU
	PCLK	CLK_HBUS
QOSCNT_MB_PEpCLk(p = 0-1, k = 0-2)	CLK	CLK_CPU
	PCLK	CLK_HBUS
QOSCNT_DTS	CLK	CLK_HBUS
	PCLK	CLK_HBUS
QOSCNT_SDMACj(j=0-1)	CLK	CLK_SBUS
	PCLK	CLK_HBUS
QOSCNT_FL_ICUM	CLK	CLK_SBUS
	PCLK	CLK_HBUS
QOSCNT_SYS_ICUM	CLK	CLK_SBUS
	PCLK	CLK_HBUS
QOSCNT_ACEUj (j=0-1)	CLK	CLK_HBUS
	PCLK	CLK_HBUS
QOSCNT_FL_DFP	CLK	CLK_CPU
	PCLK	CLK_HBUS
QOSCNT_SYS_DFP	CLK	CLK_SBUS
	PCLK	CLK_HBUS
QOSCNT_GTM	CLK	CLK_HBUS
	PCLK	CLK_HBUS
QOSCNT_RHSIFj (j=0-1)	CLK	CLK_HBUS
	PCLK	CLK_HBUS
QOSCNT_FLXAj (j=0)	CLK	CLK_HBUS
	PCLK	CLK_HBUS
QOSCNT_ETHERj (j=0-1)	CLK	CLKC_HBUS
	PCLK	CLKC_HBUS
QOSCNT_R_SWITCH	CLK	CLKC_HBUS
	PCLK	CLKC_HBUS

2.3 QoS Interrupt

The following shows the QoS interrupt.

Table 2-4 QoS Interrupt

Interrupt Symbol Name	Explanation	Interrupt Number
INTQOS0_x*1	QoS Latency Monitor Interrupt CH 0 for Master[x]*2	822
INTQOS1_x*1	QoS Latency Monitor Interrupt CH 1 for Master[x]*2	823
INTQOS2_x*1	QoS Latency Monitor Interrupt CH 2 for Master[x]*2	824
INTQOS3_x*1	QoS Latency Monitor Interrupt CH 3 for Master[x]*2	717
INTQOS4_x*1	QoS Latency Monitor Interrupt CH 4 for Master[x]*2	718
INTQOS5_x*1	QoS Latency Monitor Interrupt CH 5 for Master[x]*2	719
INTQOS6_x*1	QoS Latency Monitor Interrupt CH 6 for Master[x]*2	720
INTQOS7_x*1	QoS Latency Monitor Interrupt CH 7 for Master[x]*2	721

Note 1. Refer to QoSID of Table 2-2 QoS for "x" of INTQOSm_x.

Note 2. Each QoS interrupt is merged per channel. Refer to "*RH850/U2B User's Manual 6.3.36, INTQOS0MON0 — QoS(Ch0) Interrupt monitor Register0 to 6.3.51, INTQOS7MON1 — QoS(Ch7) Interrupt monitor Register1"* for the monitor of each QoS IP interrupt.

2.4 QoS Interrupt Route

The following shows the QoS interrupt route.

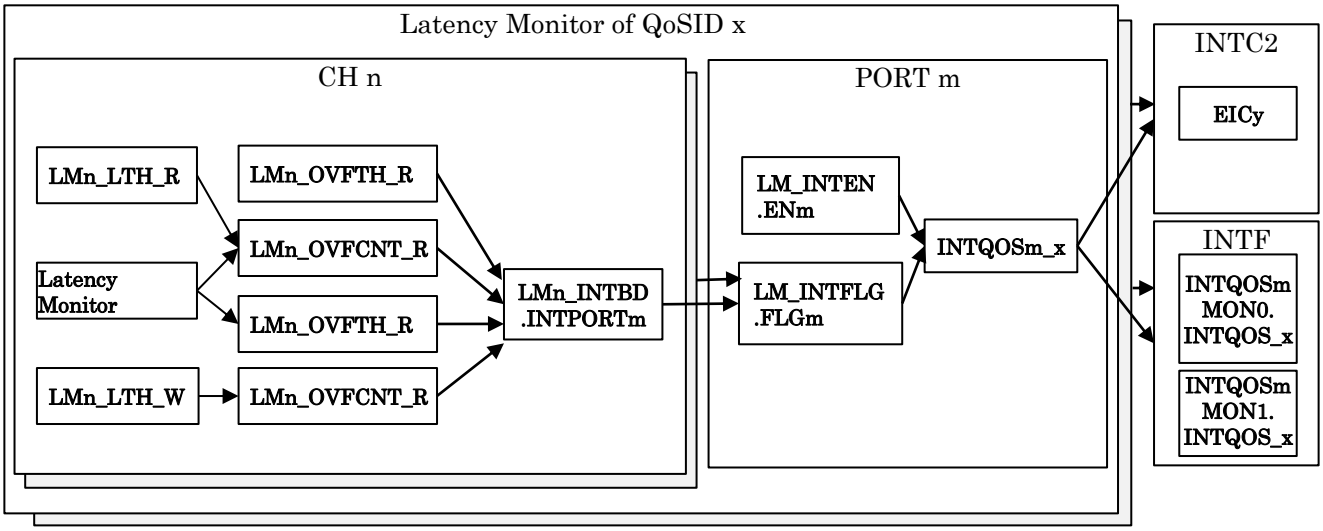

Figure 2-1 QoS Interrupt Route

2.5 SPID of Bus Master

The following shows the SPID initial value of U2B bus master.

Table 2-5 SPID Initial Value of U2B Bus Master

SPID Initial Value	Bus Master
0	CPU0
1	CPU1
2	CPU2
3	CPU3
4	CPU4
5	CPU5
6 to 9	Reserved
10	GTM (Cluster 0 to Cluster 9)
11	EMU3S0 (EMU3S core)
12	EMU3S1 (EMU3S core)
13	R-Switch
14	ACEU0
15	ACEU1
16 to 17	Reserved
18	RHSIF1
19	RHSIF0
20 to 22	Reserved
23	FlexRay0
24	ETND1
25	ETND0
26	ICUMHB (ICUM core, AES and ICUM DMA)
27	sDMAC1
28	sDMAC0
29	DTS
30	DFP
31	MAU
	DFP, ICUM (debug master)

Refer to "*RH850/U2B User's Manual Table 55.387 Initial Value and Register Location of SPID"* for the SPIID details.

3. Operation Example

This section describes the following QoS operation example. It is assumed that the QoS registers and bit settings that are not included in this operation example are set to the values after reset.

Table 3-1 Operation Example List

Operation Example	Band Width Regrater		Latency Monitor Target
	Bus Master of Access Control Target	Operation Mode of Band Width Regulator	
3.1 Band Width Regulator (Interval Mode)	CPU1 peripheral bus	Interval mode	—
3.2 Band Width Regulator (Threshold Mode)	CPU1 peripheral bus	Threshold mode	—
3.3 Latency Monitor	—	—	CPU1 peripheral bus

3.1 Band Width Regulator (Interval Mode)

3.1.1 Specification Overview

In this operation example, the writing for PORT register by CPU1 is controlled by the Interval Mode of the band width regulator in QoS. The band width regulator is set in CPU0.

- Band Width Regulator
  - The bus master of the access suppression target is the CPU1 peripheral bus.
  - Set Interval Mode for the operation mode.
  - Set 100us to the suppression period of bus access by interval mode, “PERIOD”.

Refer to ”*RH850/U2B User’s Manual 3.9.4.1 Bandwidth Regulator*” for the details of the band width regulator.

3.1.2 System Configuration

The following shows the system configuration in this operation example.

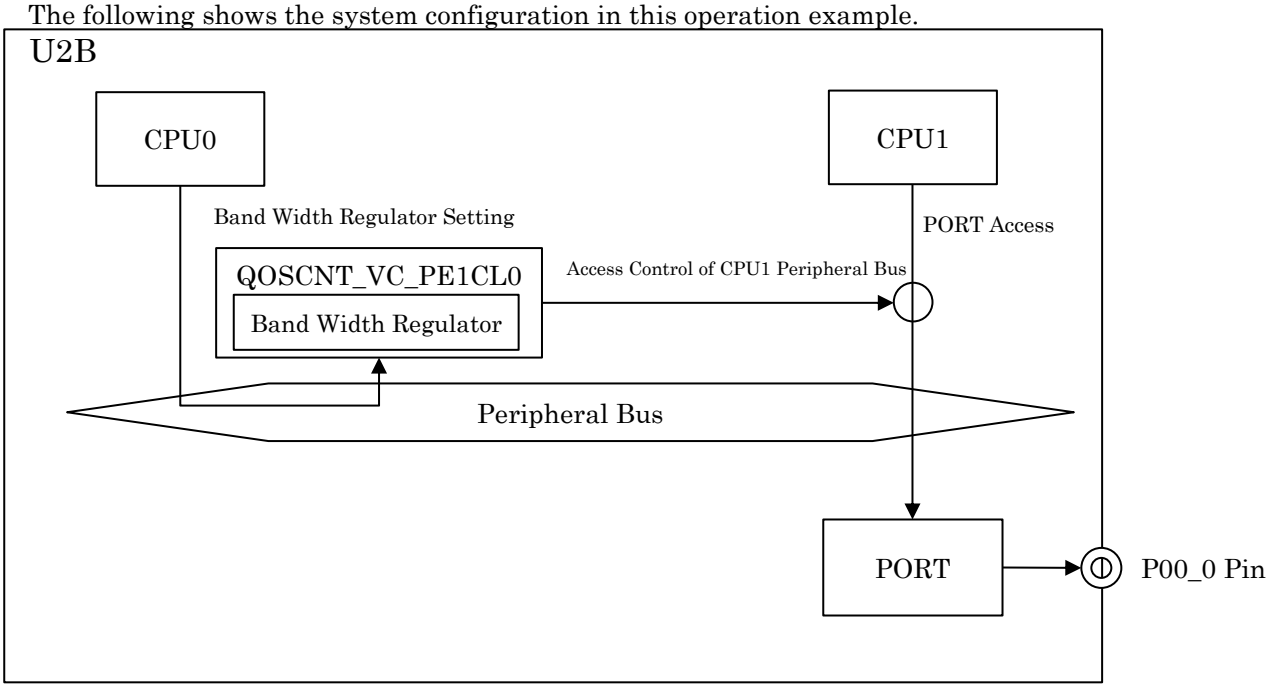

Figure 3-1 System Configuration

3.1.3 Timing Chart

The following shows the timing chart in this operation example.

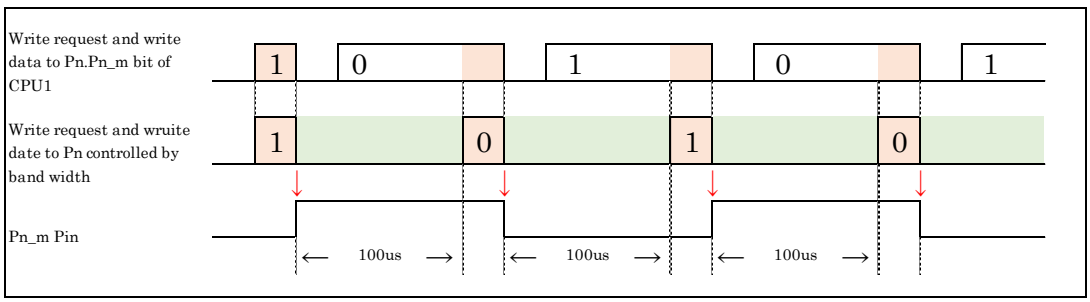

Figure 3-2 PORT Register Rewrite Control of CPU1 by Band Width Regulator (Interval Mode)

3.1.4 Software Explanation

3.1.4.1 Module Explanation

Module list in this operation example is shown below.

Table 3-2 Module

Module Name	Function Name	Function
QoS Initial Setting Function	qos_init	Initial set QoS.
PORT Initial Setting Function	port_init	Initial set PORT. Set access permission of CPU1 since CPU0 is only accessible to PORT register after resetting

3.1.4.1 Register Setting

The following shows the register initial setting of each function in this operation example.

(a) QoS Initial Setting

Table 3-3 QoS Initial Setting

Unit Name	Register Name	Bit Name	Setting Value	Function
QOSCNT_VC_PE1CL0	BR_MODE	MODE[1:0]	0x2	Band width regulator is operated in Interval Mode.
	BR_PERIOD	CFG[15:0]	0x9C3F	Cycles in control period of Interval Timer. When f_{CLK_CPU}=400MHz, the cycles required to 100us is calculated by the following. CFG = 100us * f_{CLK_CPU} - 1 = 100us * 400MHz - 1 = 40,000 – 1 = 0x9C3F

(b) PORT Initial Setting Function

Table 3-4 PORT Initial Setting

Unit Name (PBG Group)	Register Name	Bit Name	Setting Value	Function
PBG20	PBGPROT1_12	SPID[31:0]	0x0000 0003	When SPIDm bit=1, enable to access bus master of SPIDm to port setting register categorized A. In this operation example, enable to access CPU1 for PKCPROT and PWE register setting required for register setting of PORT group.
PBG20	PBGPROT1_14	SPID[31:0]	0x0000 0003	When SPIDm bit=1, enable to access bus master of SPIDm to port setting register categorized C. In this operation example, enable to access CPU1 for PCRn_m register setting.
PBG21	PBGPROT1_4	SPID[31:0]	0x0000 0003	When SPIDm bit=1, enable to access bus master of SPIDm to port group 00 setting register categorized F. In this operation example, enable to access CPU1 (SPID0) for P00 register setting.

Refer to "*RH850/U2B User's Manual*" for the details of PORT categorization and PBG group.

- Table 55.497 List of Peripheral Circuit Modules to be Protected
- Table 55.498 Relation between categories and target registers for PORT configuration registers

3.1.4.2 Operation Flow

The following shows the flowchart in this operation example.

(a) CPU0

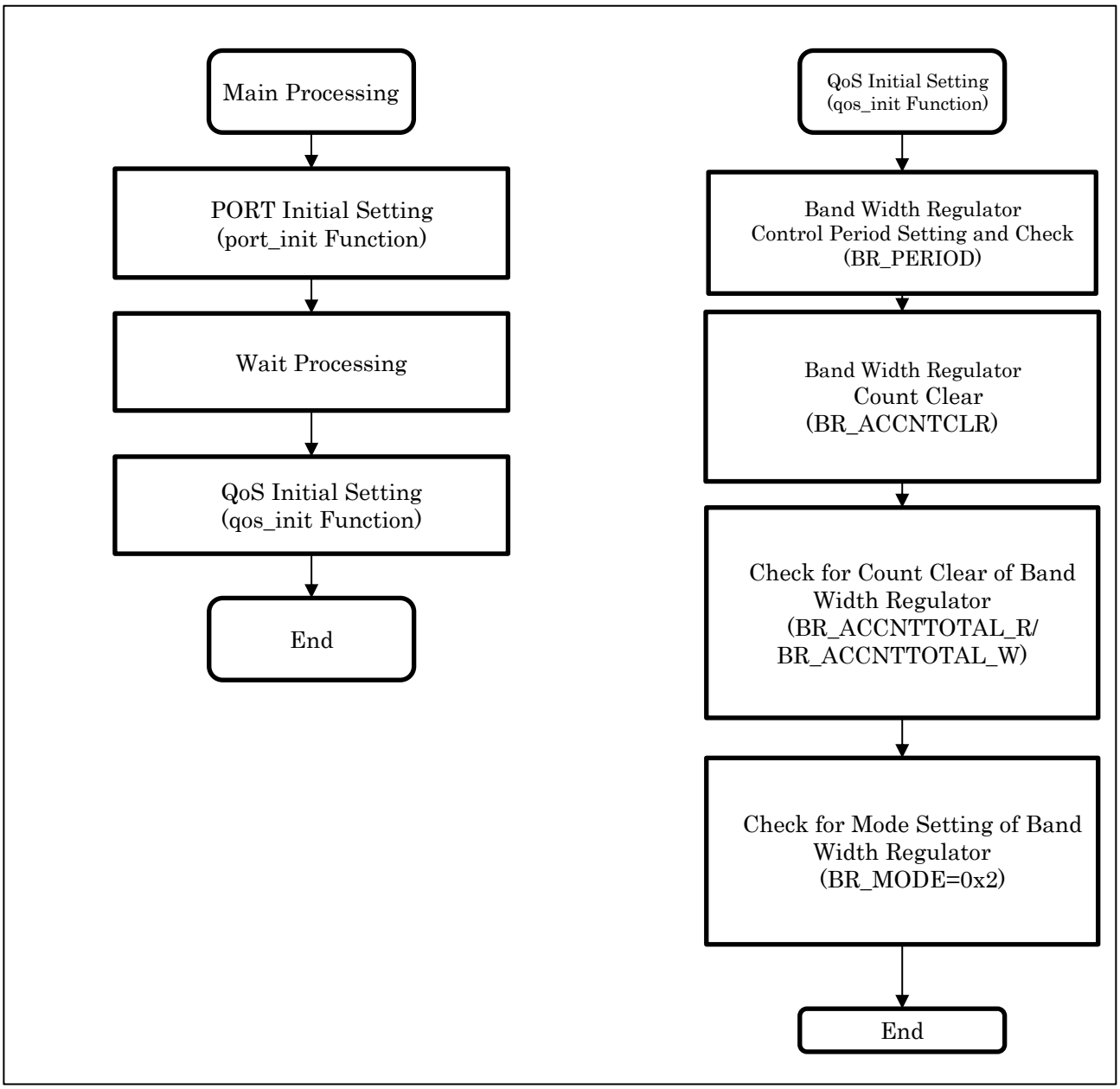

Figure 3-3 Setting Flow of PORT Register Rewrite Control by Band Width Regulator (Interval Mode)

Refer to "*RH850/U2B User's Manual Figure 3.68 Initial setting flow of Bandwidth regulator (Interval mode)*" for the setting flow details of Interval Mode in Band Width Regulator.

(b) CPU1

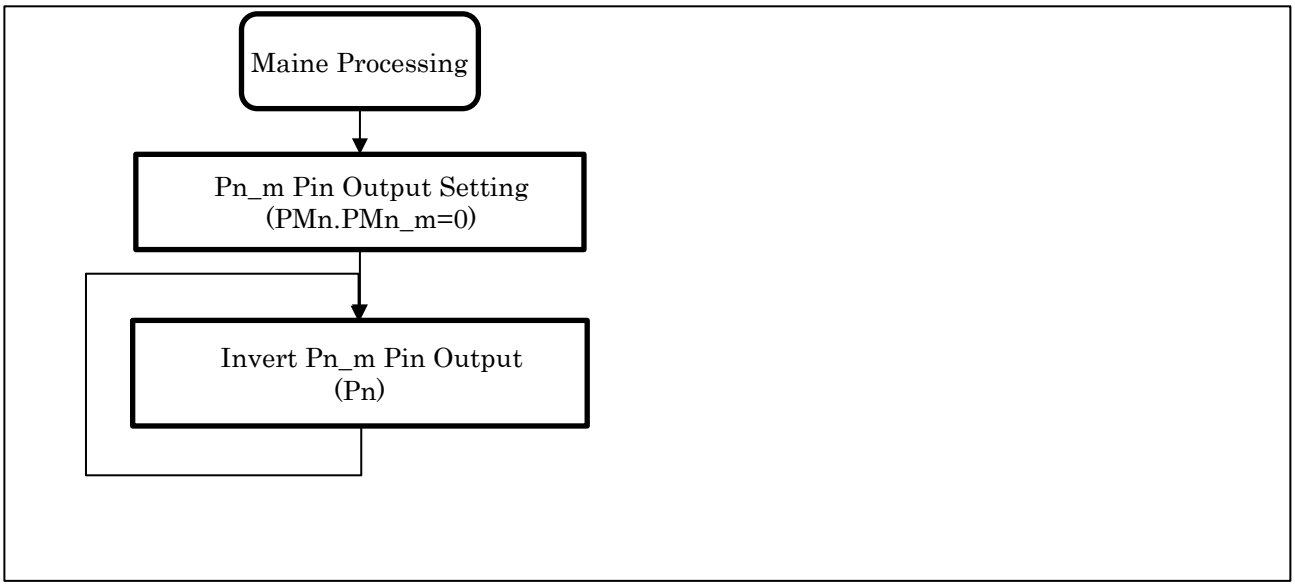

Figure 3-4 Rewrite Flow on PORT Register

3.2 Band Width Regulator (Threshold Mode)

3.2.1 Specification Overview

In this operation example, the writing for PORT register by CPU1 is controlled by the Threshold Mode of the band width regulator in QoS. The band width regulator is set in CPU0.

- Band Width Regulator
  - The bus master of the access suppression target is the CPU1 peripheral bus.
  - Set Threshold Mode for the operation mode.
  - Set 100us to the suppression period of bus access by interval mode, “PERIOD”.
  - Set 3 times to the number of bus access in the controlling period of bus access by Threshold Mode.

Refer to “*RH850/U2B User’s Manual 3.9.4.1 Bandwidth Regulator*”を for the details of band width regulator.

3.2.2 System Configuration

The following shows the system configuration in this operation example.

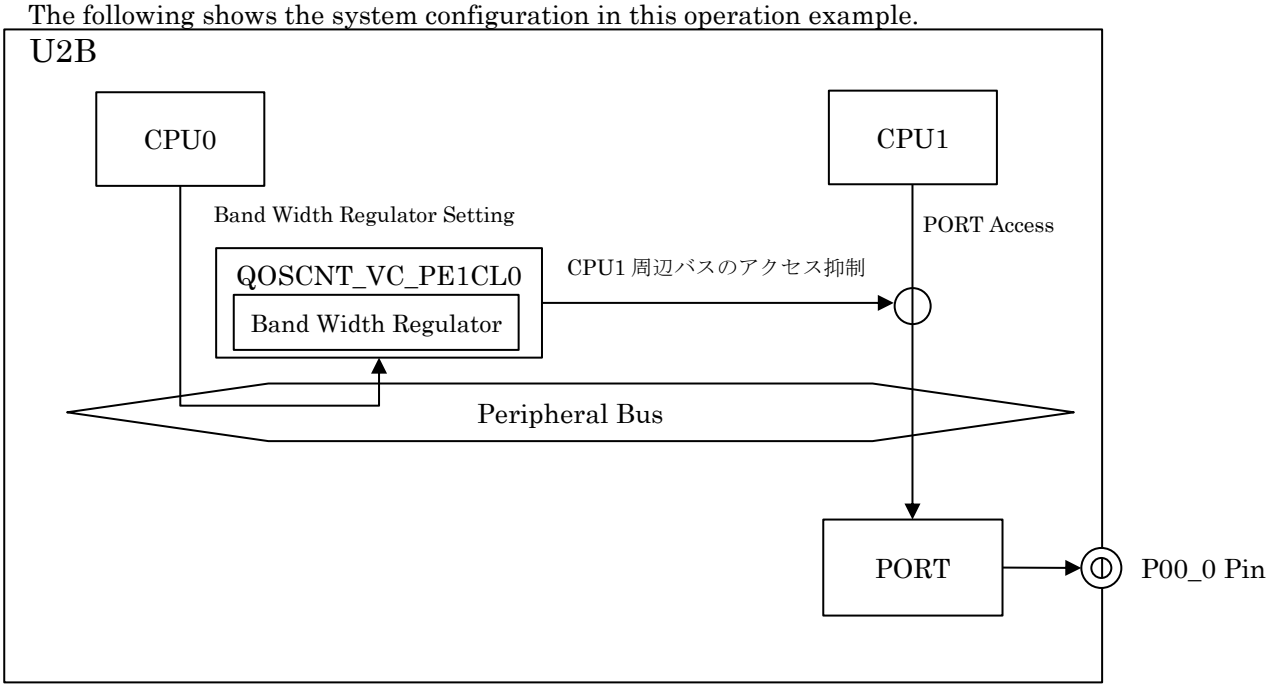

Figure 3-5 System Configuration

3.2.3 Timing Chart

The following shows the timing chart in this operation example.

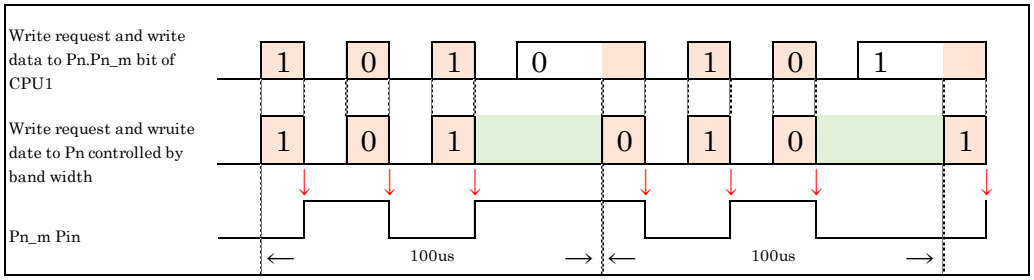

Figure 3-6 PORT Register Rewrite Control of CPU1 by Band Width Regulator (Threshold Mode)

3.2.4 Software Explanation

3.2.4.1 Module Explanation

The following shows the module list in this operation example.

Table 3-5 Module

Module Name	Function Name	Function
QoS Initial Setting Function	qos_init	Initial set QoS.
PORT Initial Setting Function	port_init	Initial set PORT. Set access permission of CPU1 since CPU0 is only accessible to PORT register after resetting

3.2.4.2 Register Setting

The following shows the register initial setting of each function in this operation example.

(a) QoS Initial Setting

Table 3-6 QoS Initial Setting

Unit Name	Register Name	Bit Name	Setting Value	Function
QOSCNT_VC_PE1CL0	BR_MODE	MODE[1:0]	0x3	Band width regulator is operated in Threshold Mode.
	BR_PERIOD	CFG[15:0]	0x9C3F	Specify the number of cycles in controlling period of band width regulator “PERIOD”. When CPU1 peripheral bus clock CLK_CPU is 400MHz, the setting value for CFG bit is calculated by the following to set the bandwidth regulator suppression period to 100us. CFG = PERIOD - 1 = 100us * f_{CLK_CPU} - 1 = 100us * 400MHz – 1 = 40,000 – 1 = 0x9C3F
	BR_ACCNTTH_W	CNT[15:0]	0x0002	Set threshold in write access count of band width regulator (CNT+1=3 times).
	BR_ACCNTTH_R	CNT[15:0]	0x0002	Set threshold in read access count of band width regulator (CNT+1=3 times).

(b) PORT Initial Setting Function

Table 3-7 PORT Initial Setting

Unit Name (PBG Group)	Register Name	Bit Name	Setting Value	Function
PBG20	PBGPROT1_12	SPID[31:0]	0x0000 0003	When SPIDm bit=1, enable to access bus master of SPIDm to port setting register categorized A. In this operation example, enable to access CPU1 for PKCPROT and PWE register setting required for register setting of PORT group.
PBG20	PBGPROT1_14	SPID[31:0]	0x0000 0003	When SPIDm bit=1, enable to access bus master of SPIDm to port setting register categorized C. In this operation example, enable to access CPU1 for PCRn_m register setting.
PBG21	PBGPROT1_4	SPID[31:0]	0x0000 0003	When SPIDm bit=1, enable to access bus master of SPIDm to port group 00 setting register categorized F. In this operation example, enable to access CPU1 (SPID0) for P00 register setting.

Refer to "*RH850/U2B User's Manual*" for the details of PORT categorization and PBG group.

- *Table 55.497 List of Peripheral Circuit Modules to be Protected*
- *Table 55.498 Relation between categories and target registers for PORT configuration registers*

3.2.4.3 Operation Flow

The following shows the flowchart in this operation example.

(a) CPU0

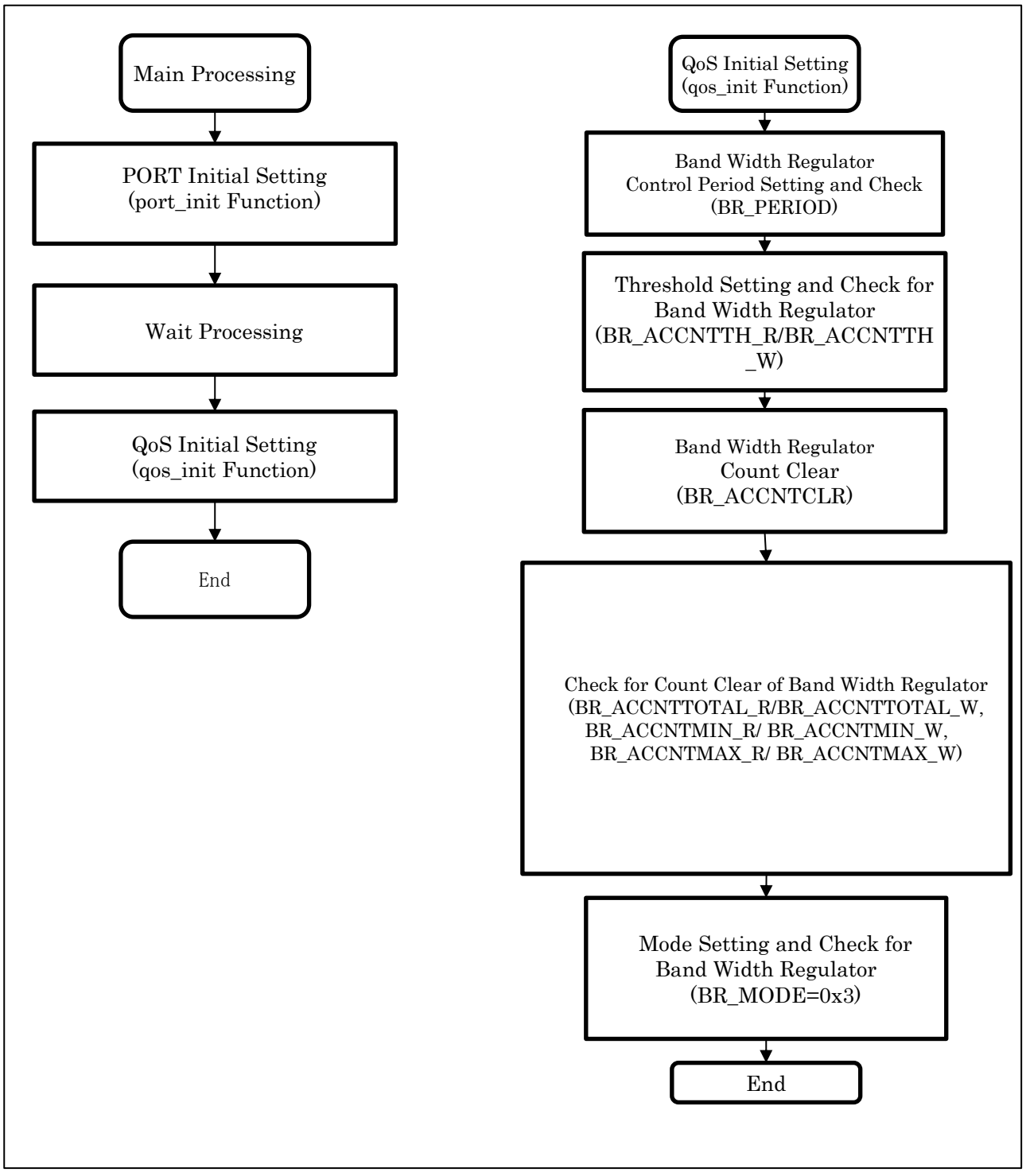

Figure 3-7 Setting Flow of PORT Register Rewrite Control by Band Width Regulator (Threshold Mode)

Refer to "*RH850/U2B User's Manual Figure 3.71 Initial setting flow of Bandwidth regulator (Threshold mode)*" for the setting flow details of Threshold Mode in Band Width Regulator.

(b) CPU1

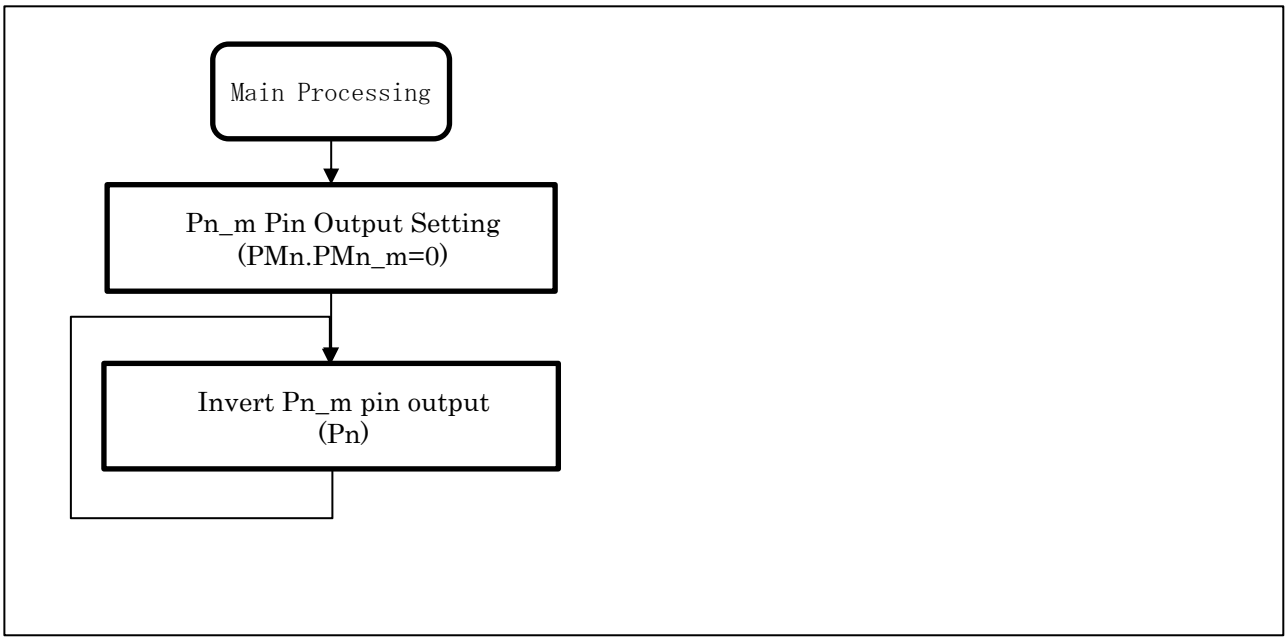

Figure 3-8 Write Flow of PORT Register

3.3 Latency Monitor

3.3.1 Specification Overview

In this operation example, monitor the latency for the PORT register writing by CPU1 with the latency monitor.

In this operation example, enhance the latency for the PORT register writing by continuously accessing the FENMIF register of the same bus group as the PORT register, and issue excessive access latency interrupts from latency monitor.

- Latency Monitor
  - Set latency monitor by CPU0.
  - The bus master of the latency monitor target is the CPU1 peripheral bus.
  - Monitor access latency in CPU1 peripheral bus by latency monitor CH0.
  - Threshold of excessive access latency is 0x30 cycle by CLK_CPU clock.
  - Threshold of number of excessive access latency detection is 2 times.
  - Bind the CPU1 peripheral bus (QoSID=4) of the latency monitor CH0 for excessive access latency detection interrupt to PORT0 (INTQOS0_4). INTQOS0_4 is specified as INTQOS0 interrupt to INTC2.
  - Filtering target of address area is the allocated address of P00 register.
  - Bus master of SPID filtering target is CPU1 (SPID=0).
- When INTQOS0 interrupt is detected, CPU0 clears the latency monitor counter and clears LM_INTFLG.FLG0 to clear the INTQOS0 interrupt. To display the interrupt timing, toggle the P2_0 pin output at the beginning and end of interrupt processing.
- CPU2 continuous accesses FENMIF register.

Refer to "*RH850/U2B User's Manual 3.9.4.2 Latency Monitor*"を for the latency monitor details.

3.3.2 System Configuration

The following shows the system configuration in this operation example.

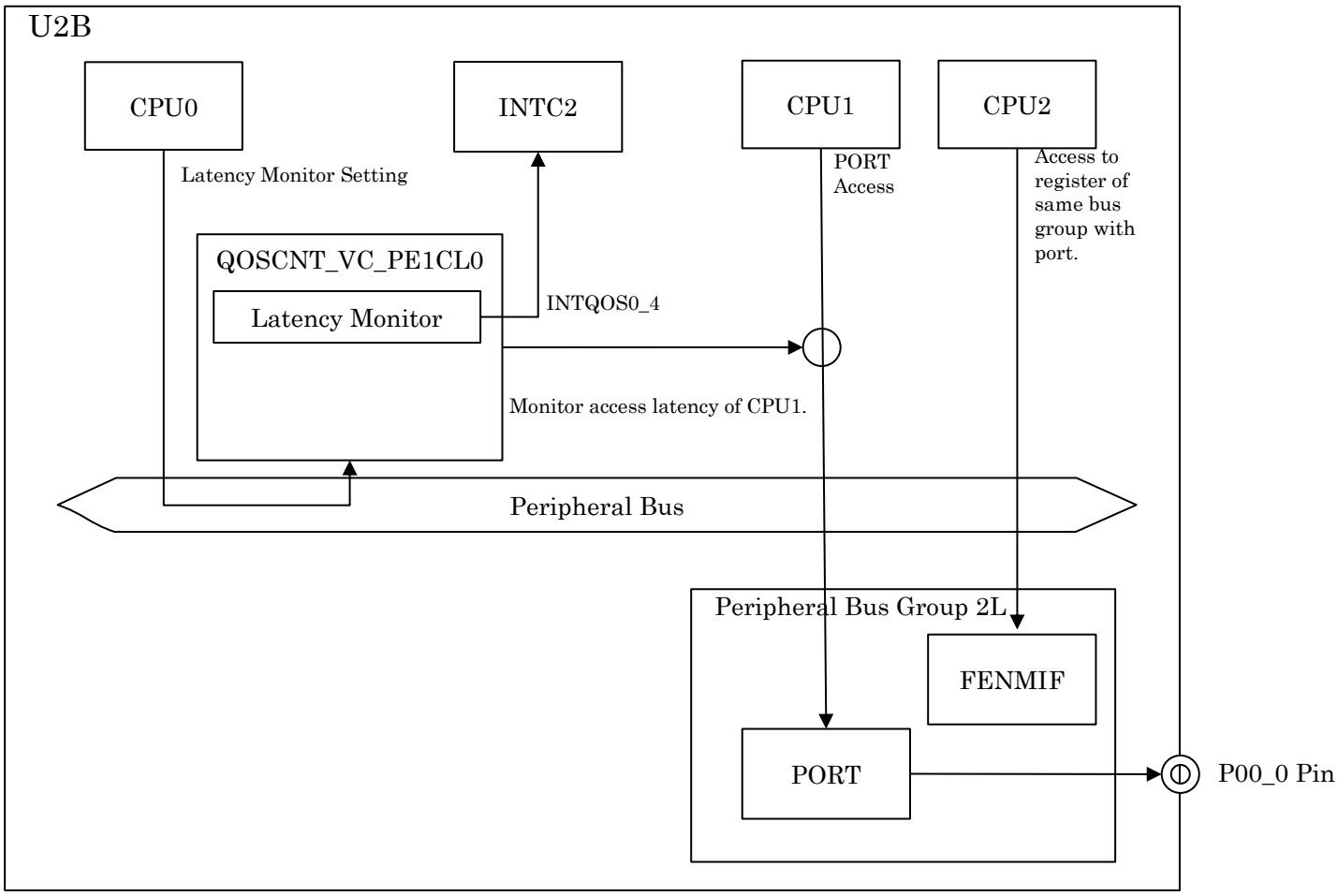

Figure 3-9 System Configuration

3.3.3 Timing Chart

The following shows the timing chart in this operation example.

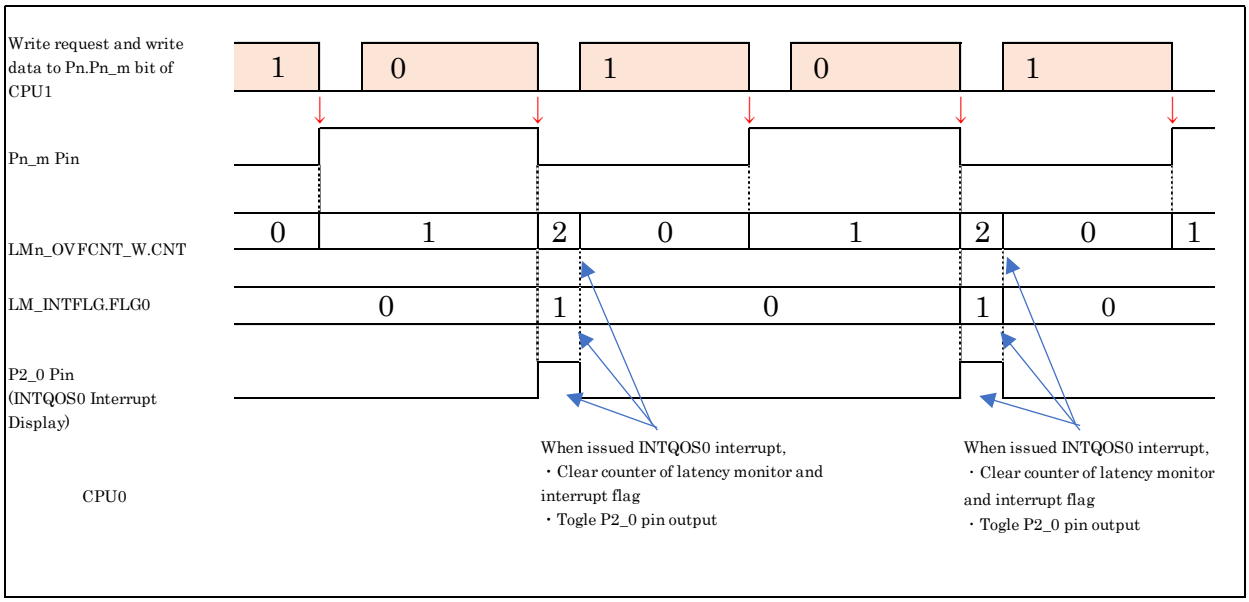

Figure 3-10 Timing Chart of Latency Monitor

3.3.1 Software Explanation

3.3.1.1 Module Explanation

The following shows the module list in this operation example.

Table 3-8 Module

Module Name	Function Name	Function
QoS Initial Setting Function	qos_init	Initial set QoS.
PORT Initial Setting Function	port_init	Initial set PORT. Set access permission of CPU1 since CPU0 is only accessible to PORT register after resetting
Interrupt Initial Setting Function	interrupt_init	Initial set interrupt.

3.3.1.2 Register Setting

The following shows the register initial setting of each function in this operation example.

(a) QoS Initial Setting

Table 3-9 QoS Initial Setting (n=0)

Unit Name	Register Name	Bit Name	Setting Value	Function
QOSCNT_VC_PE1CL0	LM_CNTSTRT	START	0x1	Latency monitor starting
	LM_INTEN	EN[7:0]	0x01	Enable PORTm (INTQOSm_x) of latency monitor in QoSID=x by ENmbit=1. In this operation example, enable PORT0 (INTQOS0_4) of latency monitor in QOSCNT_VC_PE1CL0 by EN0 bit=1.
	LMn_INTBD	INTPORT[7:0]	0x01	Transmit latency monitor of QoSID=x to PORTm of latency monitor by INTPORTm bit=1. In this operation example, transmit latency monitor of QOSCNT_VC_PE1CL0 (QoSID=4) to PORT0 of latency monitor by INTPORT0 bit=1
	LMn_LTTH_R	CYCLE[15:00]	0x0030	Set threshold (number of cycles) of read latency.
	LMn_LTTH_W	CYCLE[15:00]	0x0030	Set threshold (number of cycles) of write latency.
	LMn_OVFTH_R	CNT[15:0]	2	Set overflow count threshold (times) of read latency.
	LMn_OVFTH_W	CNT[15:0]	2	Set overflow count threshold (times) of write latency.
	LMn_LADDR0	ADDR[31:0]	0xFFD90000	Set lower-limit in address area 0 of monitor target. In this operation example, set P00 register address (0xFFD9_0000).
	LMn_UADDR0	ADDR[31:0]	0xFFD90000	Set upper-limit in address area 0 of monitor target.

				In this operation example, set P00 register address (0xFFD9_0000).
	LMn_SPID	SPID[31:0]	0x2	Set bus master of SPID=m to monitor target by SPIDm bit=1. In this operation example, monitor the access from CPU1(SPID=1).

(b) PORT Initial Setting Function

Table 3-10 PORT Initial Setting

Unit Name (PBG Group)	Register Name	Bit Name	Setting Value	Function
PBG20	PBGPROT1_12	SPID1	0x0000 0003	When SPIDm bit=1, enable to access bus master of SPIDm to port setting register categorized A. In this operation example, enable to access CPU1 for PKCPROT and PWE register setting required for register setting of PORT group.
PBG20	PBGPROT1_14	SPID1	0x0000 0003	When SPIDm bit=1, enable to access bus master of SPIDm to port setting register categorized C. In this operation example, enable to access CPU1 for PCRn_m register setting.
PBG21	PBGPROT1_4	SPID1	0x0000 0003	When SPIDm bit=1, enable to access bus master of SPIDm to port group 00 setting register categorized F. In this operation example, enable to access CPU1 (SPID0) for P00 register setting.
PORT0	PCR02_0	PM	0	Set P02_0 pin to Output Mode.

Refer to "*RH850/U2B User's Manual*" for the details of PORT categorization and protected area by PBG group.

- *Table 55.497 List of Peripheral Circuit Modules to be Protected*
- *Table 55.498 Relation between categories and target registers for PORT configuration registers*

(c) Interrupt Initial Setting Function

Table 3-11 Interrupt Initial Setting

Unit Name	Register Name	Bit Name	Setting Value	Function
INTC2	EIBD822	PEID[2:0]	0	When PEID[2:0] = m, bind interrupt to CPUm. In this operation example, bind INTQOS0 to CPU0.
	EIC822	EIMK	0	Enable INTQOS0 interrupt processing.
		EITB	1	Set INTQOS0 interrupt to table reference method.

3.3.1.3 Operation Flow

The following shows the flowchart in this operation example.

(a) CPU0

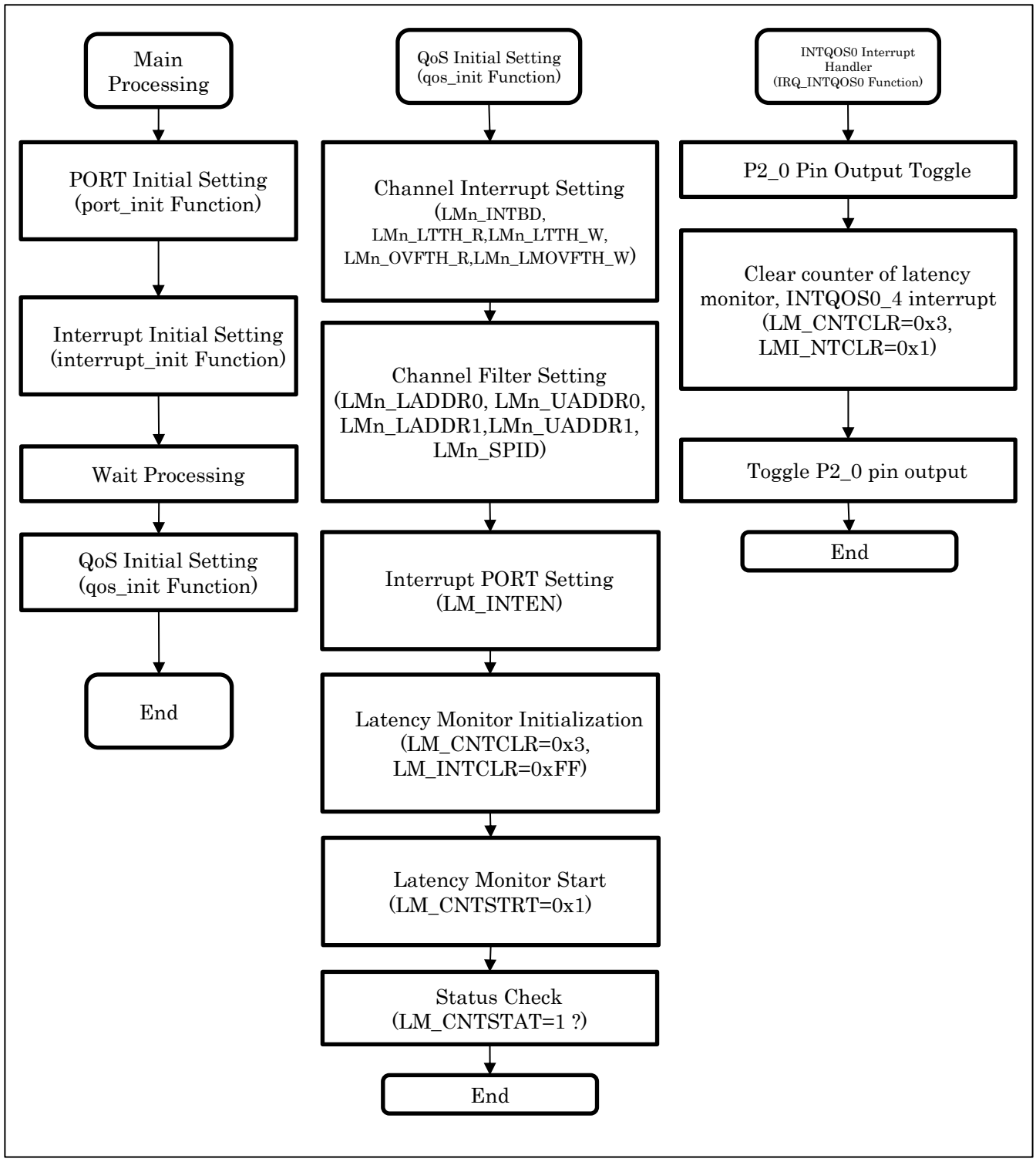

Figure 3-11 Setting Flow of Latency Monitor

Refer to "*RH850/U2B User's Manual Figure 3.73 Initial Setting of Latency Monitor*" for the setting flow details of latency monitor.

(b) CPU1

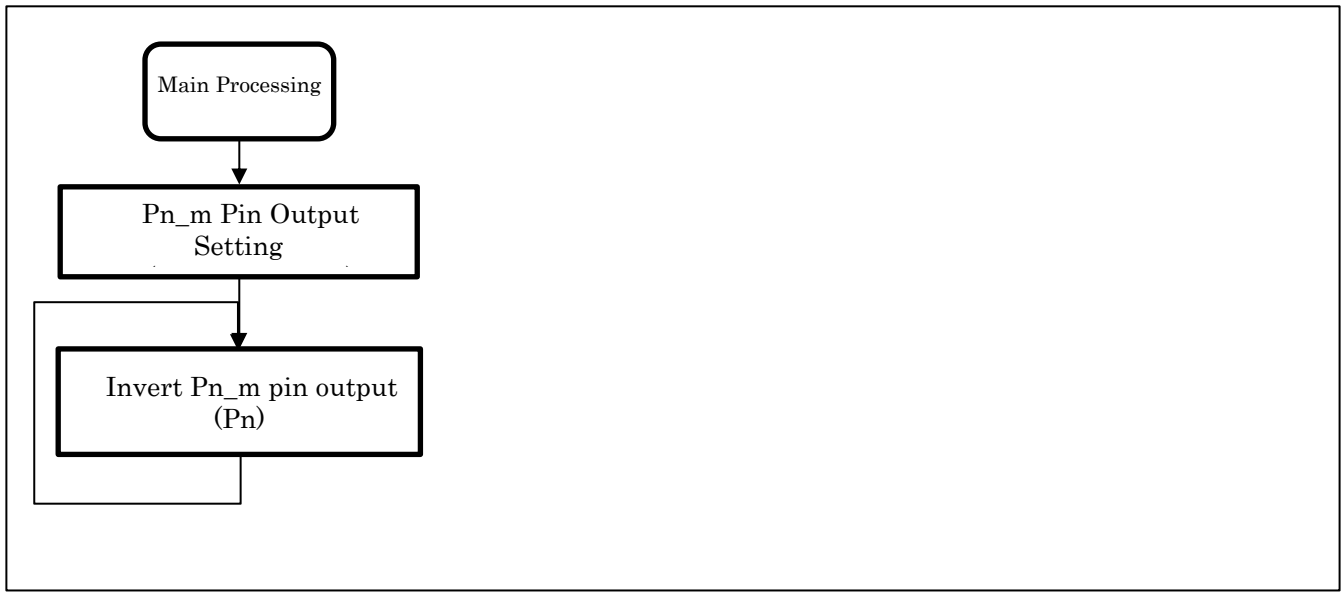

Figure 3-12 Rewrite Flow of PORT Register

(c) CPU2

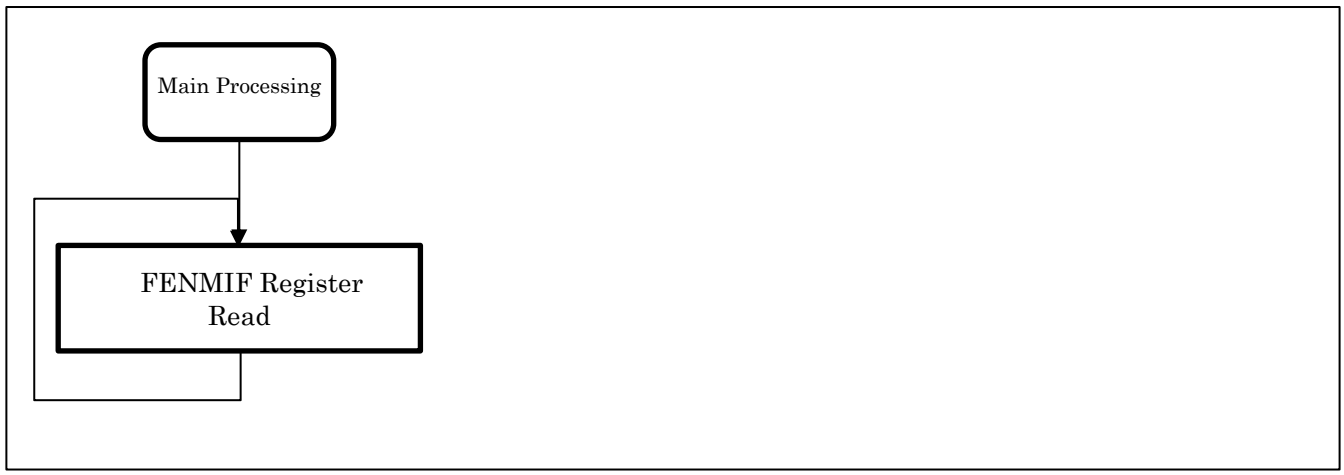

Figure 3-13 Read Flow for Register in Same Bus Group with PORT Register

Revision History

Rev.	Data	Description	
		Page	Summary
0.10	2023.12.15	All	Issue initial edition.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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