RH850/U2B Group

R01AN7075EJ0100
Rev.1.00

PSI5S Application Note

Summary

This application note summaries the operation example using the peripheral sensor interface 5S (PSI5-S) for RH850/U2Bx.

The operation example described in this application note have been confirmed to operate, be sure to confirm the operation before using it.

Summary

1. Introduction

This application note describes the creating example and the farmwear of the peripheral sensor interface 5S (PSI5-S) for RH850/U2Bx.

1.1 Used Function

The following shoes the hardware function for RH850/U2Bx used in this application note.

- Peripheral Sensor Interface 5S (PSI5-S)

2. Operation Example

2.1 Internal Loopback Communication (UART Mode)

2.1.1 Specification Overview

In this application, perform the internal loopback communication used the loopback test function of PSI5-S.

The following shows the communication specification.

- Baud rate : 4Mbps
- Number of over sample :5
- Start bit : 1 bit
- Data length : 8 bits
- Parity : Even Parity
- Stop bit : 1 bit

2.1.2 System Configuration

Figure 2-1 shows the system configuration.

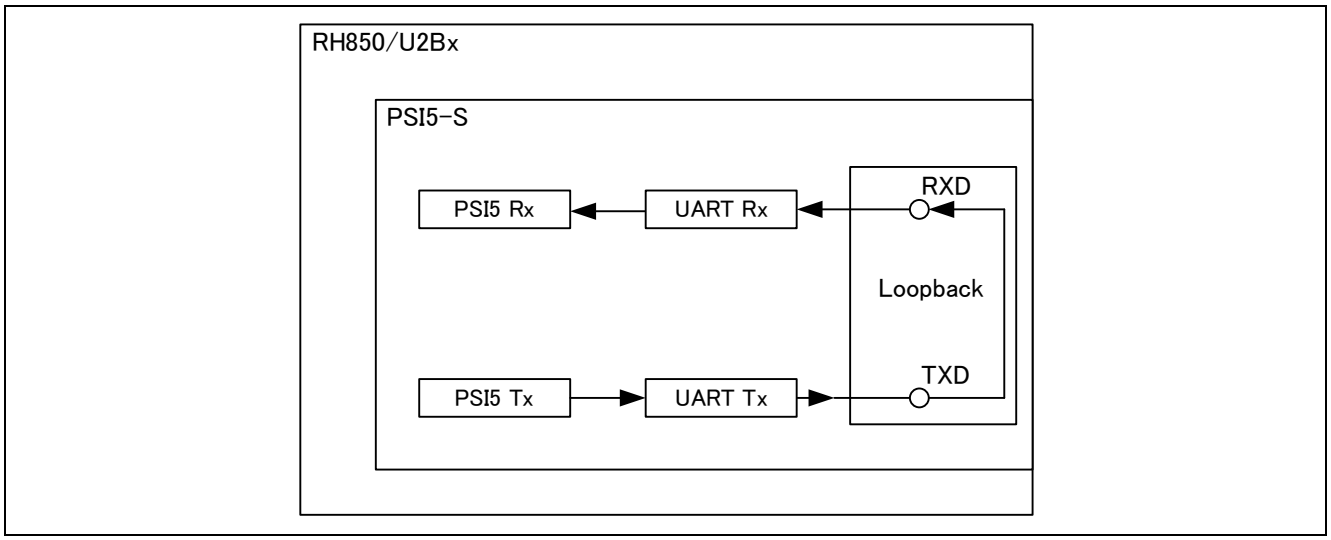

Figure 2-1 System Configuration

2.1.3 Software Explanation

- Module Explanation

The following shows the module list in this operation example.

Table 2-1 Module List

Module Name	Function Name	Feature
Main Routine	main_pe0	Perform each setting and application startup.
Module Operation Setting Routine	standby_init	Release standby of PSI5-S.
Interrupt Function Initial Setting Routine	intc_init	Perform setting of PSI5-S communication interrupt.
PSI5-S Initialization Routine	psi5s0_init	Perform initialization of PSI5-S.
Interrupt Processing Routine	psi5s0_int	Perform PSI5-S interrupt processing.

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- Register Setting

The following shows the register setting for each function in this operation example.

Table 2-2 PSI5-S ch0 Register Setting

Register Name	Setting Value	Function
PSI5SPUSWR	0x00000001	Start the software reset of PSI5-S.
PSI5SPUPTS	0x00000101	Tx parity : Even parity
		Rx parity : Even parity
PSI5SPUBPR	0x00040003	Rx over sample number : 5 samples
		Division value of clock for SCLK : 1/1
		Prescaler of SCLK : 1/4
PSI5SPUBCE	0x00000001	Clock output enable : Enable
PSI5SUCRIE	0x00000008	Interrupt enable of Rx end flag : Enable
		Interrupt enable of Rx overrun error flag : Disable
		Interrupt enable of Rx framing error flag : Disable
		Interrupt enable of Rx parity error flag : Disable
PSI5SUCTIE	0x00000002	Interrupt enable of Tx end flag : Enable
		Interrupt enable of Tx overrun error flag : Disable
PSI5SPUOMD	0x00000000	Operation mode selection : UART mode
PSI5SPUCLB	0xA7→0x58	Value of test mode
	0x01	3rd writing value enable of loopback test sequencer : Enable
PSI5SUCTD	0x000000AA	Transmit data setting : 0xAA
PSI5SPUOEB	0x00000001	Operation enable : Enable

Table 2-3 Interrupt Register Setting

Register Name	Setting Value	Function
EIBD943	0x00000000	Bind communication interrupt of PSI5-S CH0 to PE0 (CPU0).
EIC943	0x0040	Table reference/Priority level 15

- Operation Flow

The following shows the flowchart in this operation example.

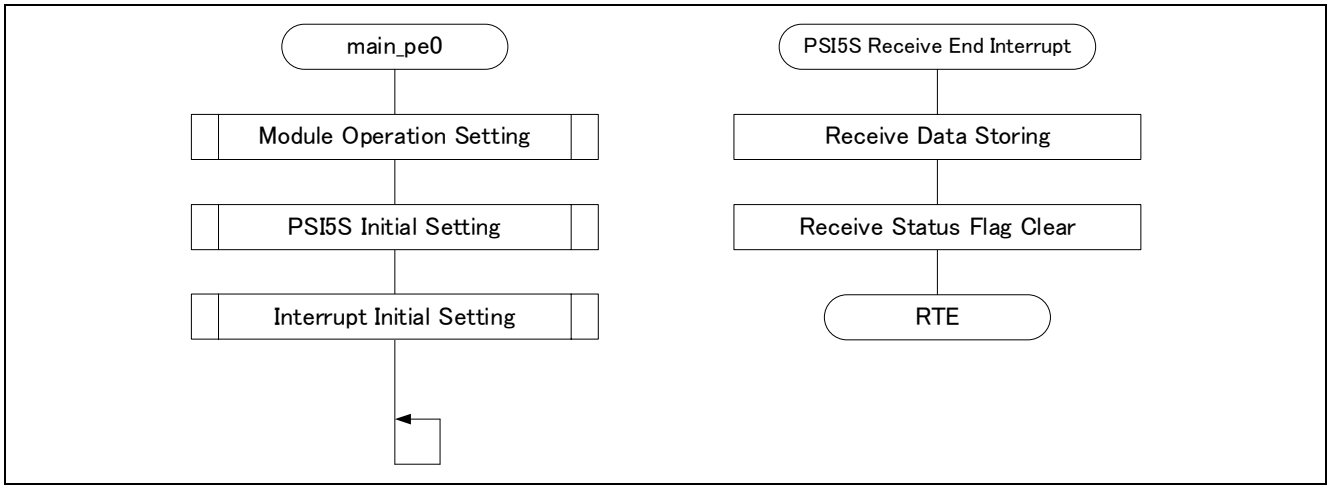

Figure 2-2 Flowchart

2.2 Receive Operation (UART Mode)

2.2.1 Specification Overview

In this operation example, perform the receive operation of inputted data from the sensor. Figure 2-3 shows the communication waveform.

The following shows the communication specification.

- Baud rate : 800Kbps
- Number of over sample : 5
- Start bit : 1 bit
- Data length : 8 bits
- Parity : No parity
- Stop bit : 1 bit

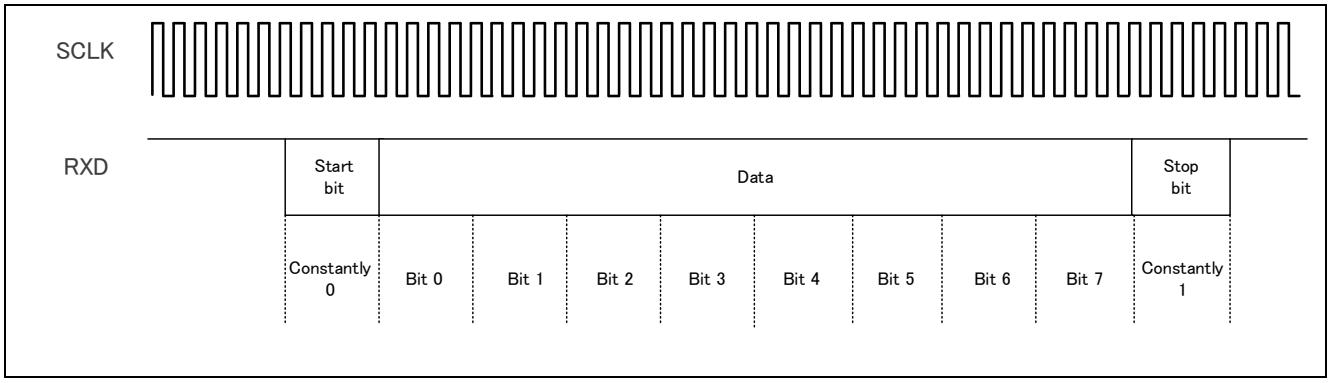

Figure 2-3 Communication Format

2.2.2 System Configuration

Figure 2-4 shows the system configuration.

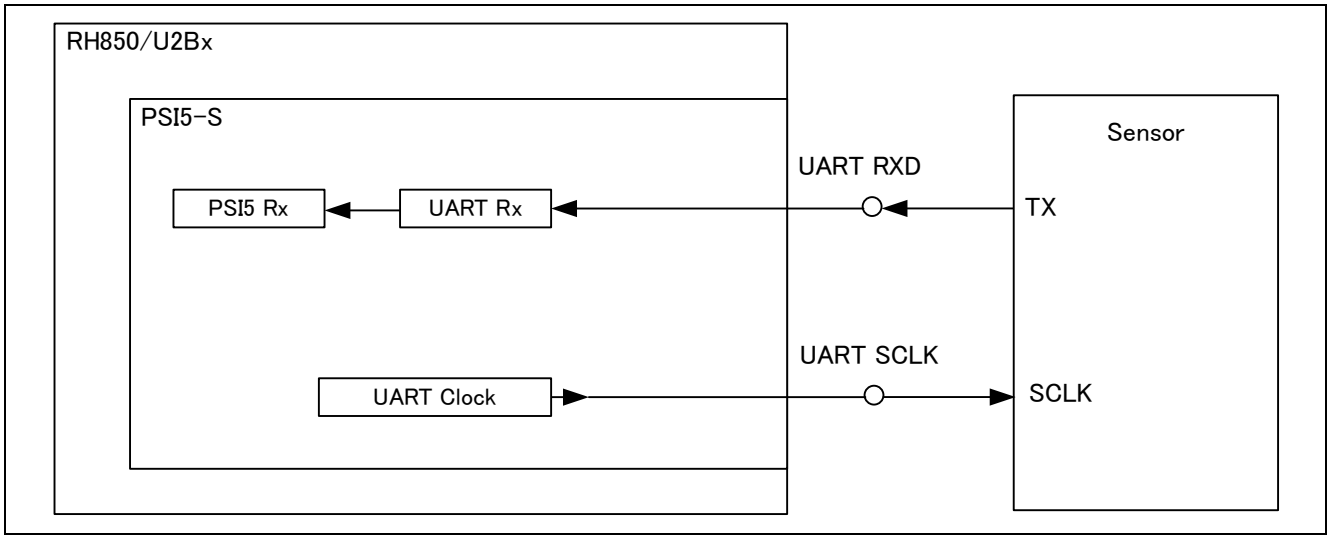

Figure 2-4 System Configuration

2.2.3 Software Explanation

- Module Explanation

The following shows the module list in this operation example.

Table 2-4 Module List

Module Name	Function Name	Feature
Main Routine	main_pe0	Perform each setting and application startup.
Module Operation Setting Routine	standby_init	Release standby of PSI5-S.
Port Initialization Routine	PORT_init	Initiarize port.
Interrupt Function Initial Setting Routine	intc_init	Perform setting of PSI5-S communication interrupt.
PSI5-S Initialization Routine	psi5s0_init	Perform initialization of PSI5-S.
Interrupt Processing Routine	psi5s0_int	Perform PSI5-S interrupt processing.

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- Register Setting

The following shows the register setting for each function in this operation example.

Table 2-5 PSI5-S ch0 Register Setting

Register Name	Setting Value	Function
PSI5SPUSWR	0x00000001	Start the software reset of PSI5-S.
PSI5SPUPTS	0x00000000	Tx parity : Even parity
		Rx parity : Even parity
PSI5SPUBPR	0x00040163	Rx over sample number : 5 samples
		Division value of clock for SCLK : 1/2
		Prescaler of SCLK : 1/100
PSI5SPUBCE	0x00000001	Clock output enable : Enable
PSI5SUCRIE	0x00000008	Interrupt enable of Rx end flag : Enable
		Interrupt enable of Rx overrun error flag : Disable
		Interrupt enable of Rx framing error flag : Disable
		Interrupt enable of Rx parity error flag : Disable
PSI5SPUOMD	0x00000000	Operation mode selection : UART mode
PSI5SPUOEB	0x00000001	Operation enable : Enable

Table 2-6 Interrupt Register Setting

Register Name	Setting Value	Function
EIBD943	0x00000000	Bind communication interrupt of PSI5-S CH0 to PE0 (CPU0).
EIC943	0x0040	Table reference/Priority level 15

- Operation Flow

The following shows the flowchart in this operation example.

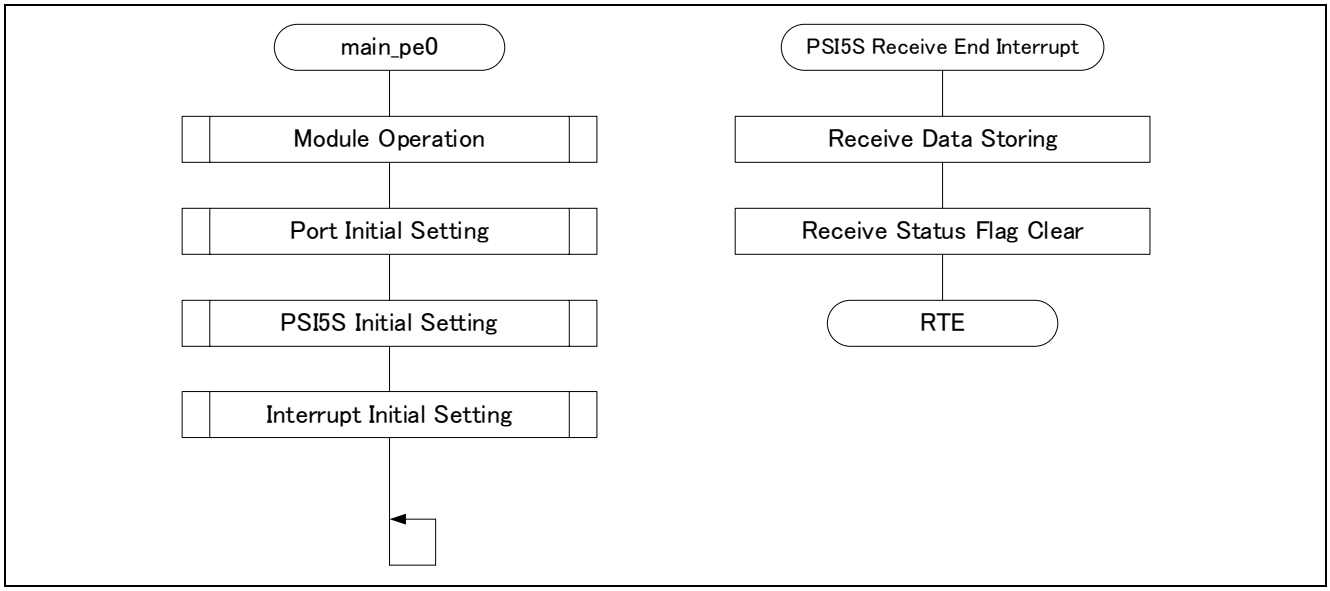

Figure 2-5 Flowchart

2.3 Internal Loopback Communication (PSI5 Mode)

2.3.1 Specification Overview

In this operation example, perform the internal loopback communication used the loopback test function of PSI5-S .

The following shows the communication specification.

- Baud rate : 10Mbps
- Frame : Frame 4
- Payload length : 8 bits
- Packet number : 4

2.3.2 System Configuration

Figure 2-6 shows the system configuration.

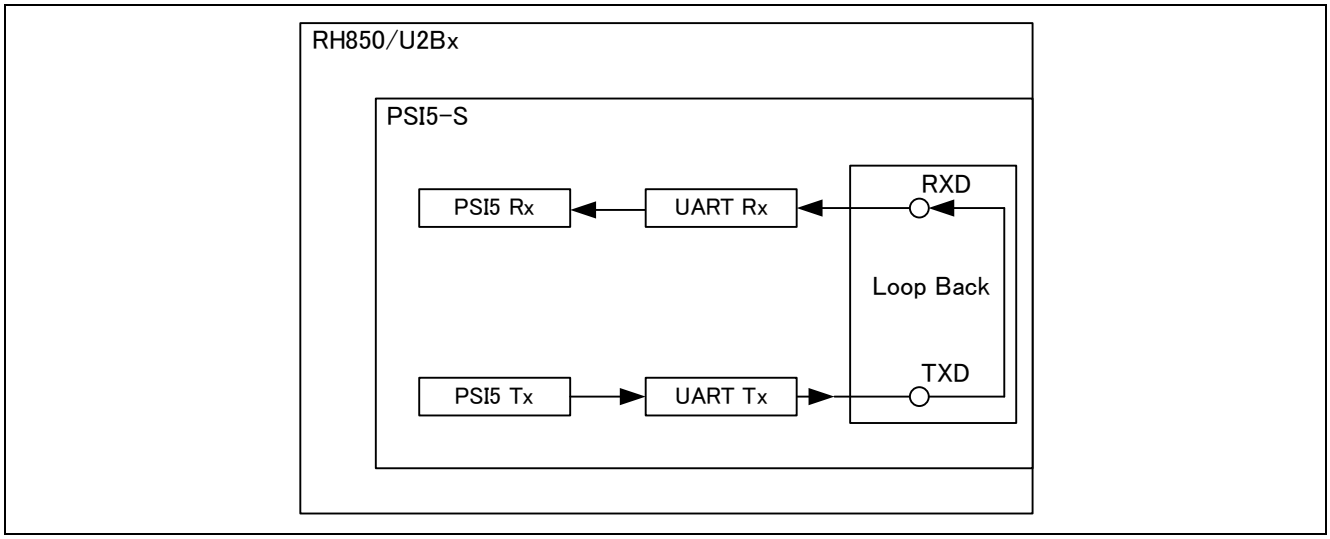

Figure 2-6 System Configuration

2.3.3 Software Explanation

- Module Explanation

The following shows the module list in this operation example.

Table 2-7 Module List

Module Name	Function Name	Feature
Main Routine	main_pe0	Perform each setting and application startup.
Module Operation Setting Routine	standby_init	Release standby of PSI5-S.
Interrupt Function Initial Setting Routine	intc_init	Perform setting of PSI5-S communication interrupt.
PSI5-S Initialization Routine	psi5s0_init	Perform initialization of PSI5-S.
Interrupt Processing Routine	psi5s0_int	Perform PSI5-S interrupt processing.

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- Register Setting

The following shows the register setting for each function in this operation example.

Table 2-8 PSI5-S ch0 Register Setting

Register Name	Setting Value	Function
PSI5SPUSWR	0x00000001	Start the software reset of PSI5-S.
PSI5SPUPTS	0x00000000	Tx parity : Even parity
		Rx parity : Even parity
PSI5SPUBPR	0x00040300	Rx over sample number : 5 samples
		Division value of clock for SCLK : 1/4
		Prescaler of SCLK : 1/1
PSI5SPUBCE	0x00000001	Clock output enable : Enable
PSI5SPRCF10	0x00000103	Frame 1 packet number : Set “4” to packet number Rx frame check sum : Select CRC Channel enable : Enable
PSI5SPRCF20	0x00000008	Frame 1 payload length : Set “8” to payload length
PSI5SPCIE0	0x00000E00	Interrupt enable of Rx packet frame completion frag : Enable
		Interrupt enable of Rx frame overrun error : Enable
		Interrupt enable of Rx frame shortage error : Enable
PSI5SPUOMD	0x00000001	Operation mode selection : PSI5 mode
PSI5SPUCLB	0xA7→0x58	Value of test mode key
	0x01	3rd writing value of loopback test sequence : Enable
PSI5SPUOEB	0x00000001	Operation enable : Enable
PSI5SPTFNM	0x00000003	4 packet transmission
PSI5SPTFD1	0x9C022800	Transmit data setting : 0x28 (CRC6 : 0x27, CRC3 : 0x2)
PSI5SPTFST	0x00000001	Transmission start
PSI5SPMB01D	-	Rx data register

Table 2-9 Interrupt Register Setting

Register Name	Setting Value	Function
EIBD943	0x00000000	Bind communication interrupt of PSI5-S CH0 to PE0 (CPU0).
EIC943	0x0040	Table reference/Priority level 15

- Operation Flow

The following shows the flowchart in this operation example.

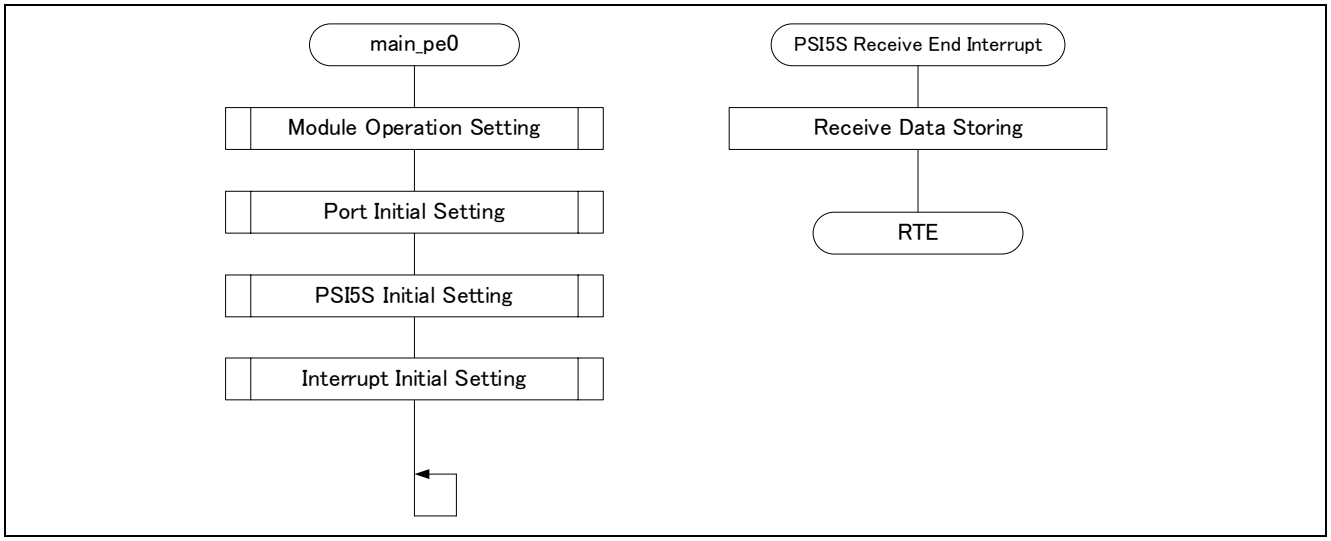

Figure 2-7 Flowchart

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2024.03.27	—	First Issue

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

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   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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