RH850/U2B Group

R01AN7074EJ0100
Rev.1.00

Gbit Ethernet Application Note

Summary

This application describes the operation example of the Gigabit Ethernet Communication that used Ethernet TSN (ETN).

The operation example described in this application note have been confirmed to operate, be sure to confirm the operation before using it.

Contents

1. Introduction

This application note describes the usage for Ethernet TSN (ETN) and the creating example for the software.

1.1 Usage Function

This following shows the hardware function of RH850/U2Bx used in this application note.

- TSNSWA
- Port (P10, P11)

1.1.1 System Configuration

Figure 1-1 shows the connection diagram with PHY.

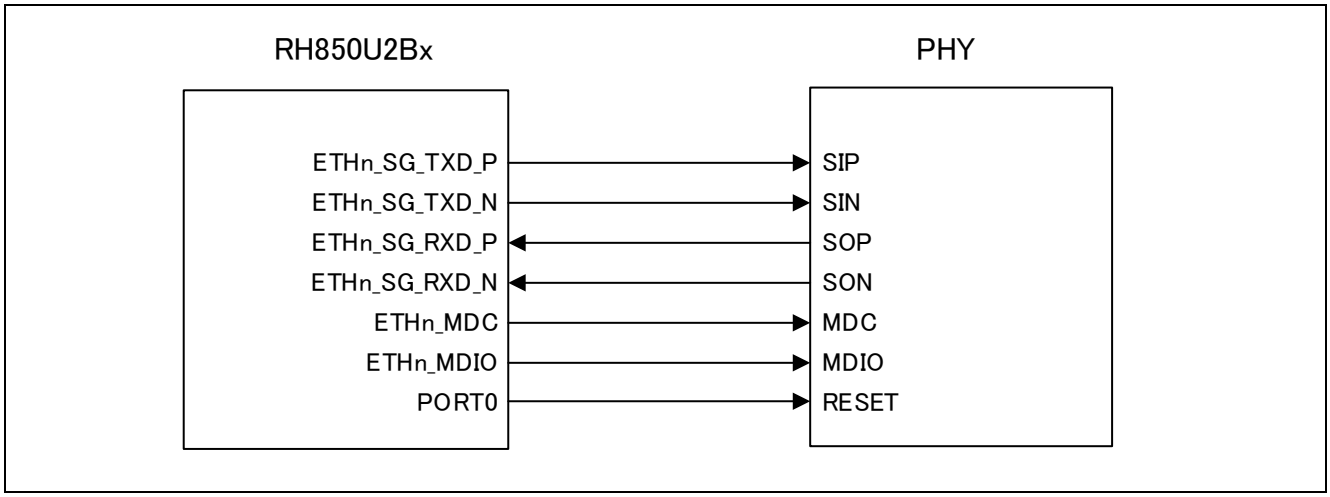

Figure 1-1 Connection Diagram between RH850/U2Bx and PHY

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1.2 TSN Overview

Figure 1-7 shows the block diagram of TSN module. In Gigabit Ethernet communication, MFWDA, GWCAA (including AXIBMI), ETHAA, RMAC System, SGMII, PWRCTL of TSNSWA are used.

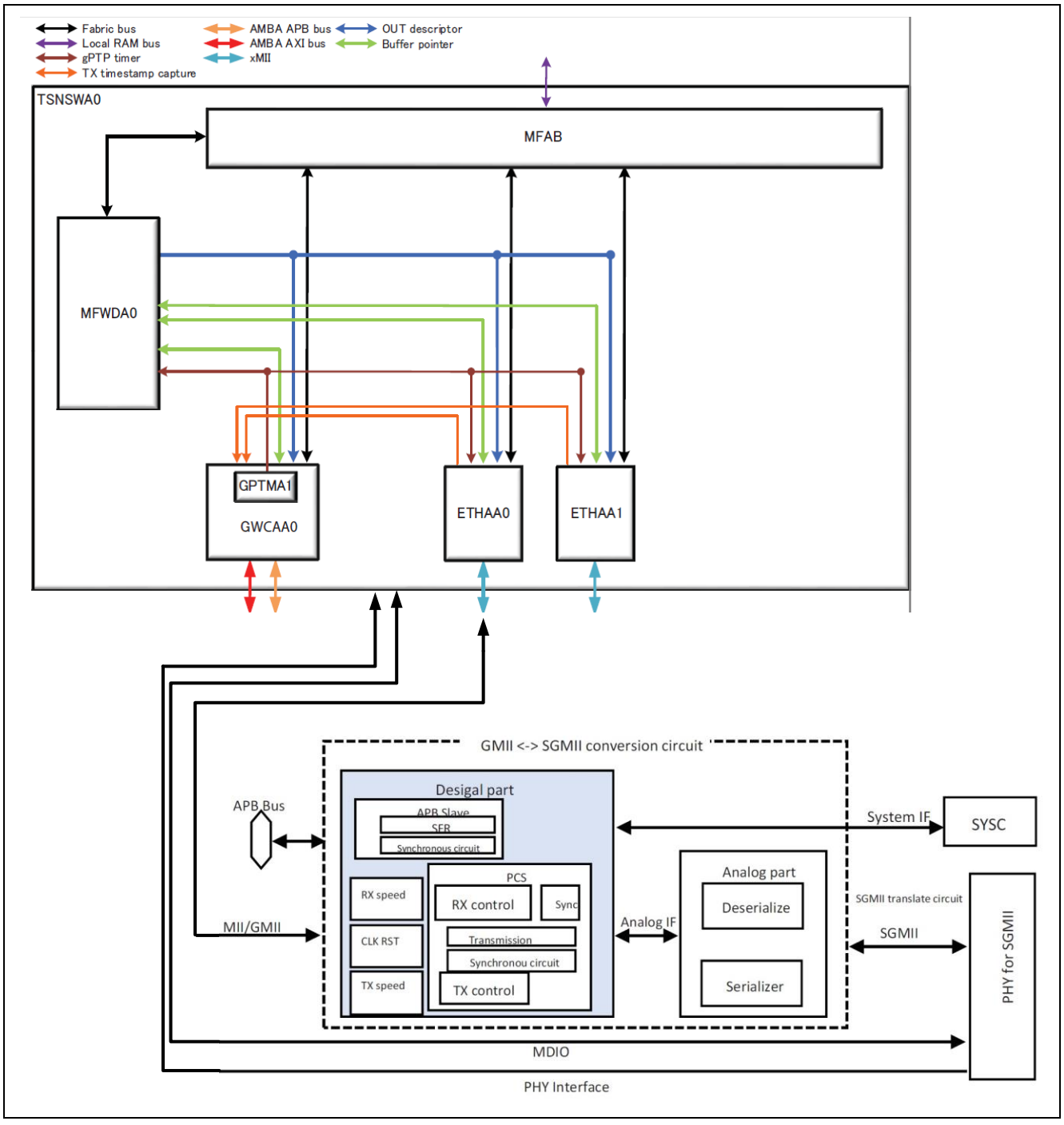

Figure 1-2 Block Diagram of TSN Module

1.2.1 Ethernet Frame Format

The frame format of Ethernet II/IEEE802.3 is supported.

1.2.2 Frame Format in Data Transmitting/Receiving

Figure 1-3 shows the frame format of Ethernet II/IEEE802.3.

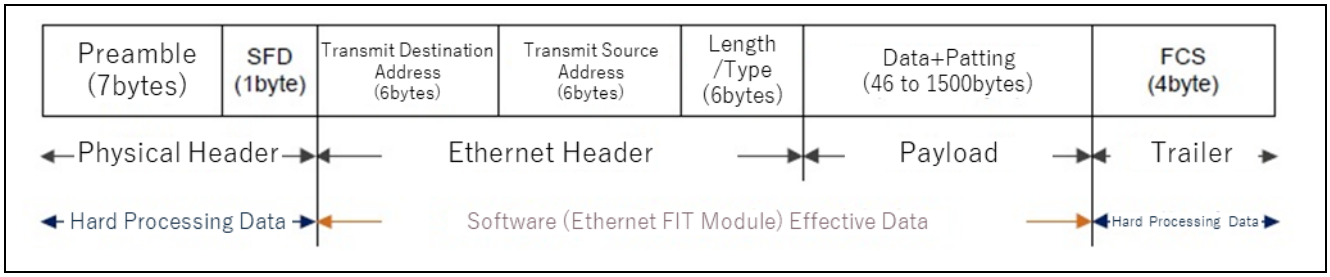

Figure 1-3 Frame Format of Ethernet II /IEEE802.3

- Preamble and SFD are the signals for singing the start of Ethernet frame. Also, in FCS, the CRC value of the ethernet frame calculated by the transmission side is stored, and the hardware similarly calculates the CRC value when receiving data and discards the Ethernet frame if it does not match.
- The effective range of the receive data in case the handwear figured the normal data is (Transmit destination address) + (Transmit source address) + (Length/Type) + (Data).

1.2.3 Frame Format of PAUSE Frame

Figure 1-4 shows the frame format of the PAUSE frame.

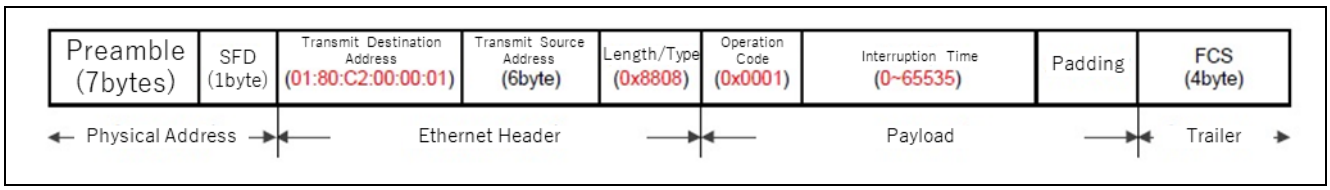

Figure 1-4 Frame Format of PAUSE Frame

- ”01:80:C2:00:00:01” (Multi cast address reserved for PAUSE frame) is specified to the transmit destination address. Also, ”0x8808” is specified to Length/Type, and “0x0001” is specified as the operation code to the header of the payload.
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1.2.4 Frame Format of Magic Packet

Figure 1-5 shows the frame format of the magic packet.

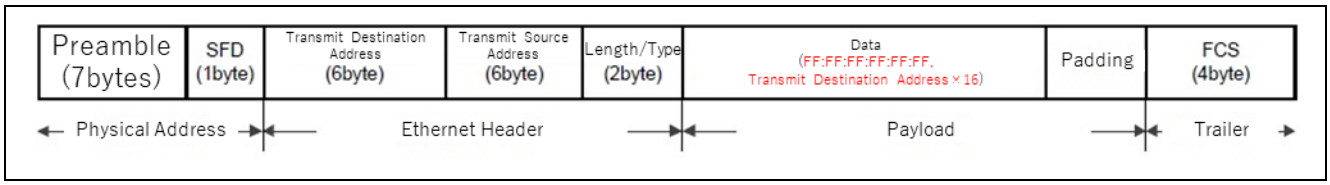

Figure 1-5 Frame Format of Magic Packet

The magic packet inserts “destination address repeated 16 times” to somewhere in the ether frame data and after “FF:FF:FF:FF:FF:FF”.

1.2.5 TSNSWA Overview

In data transmission, GWCAA and MFAB fetch and writ to the frame data allocated to the user RAM, transmit to SGMII via ETHAA, and output to PHY. In data reception, SGMII receives the frame data inputted from PHY, and transmit to the user RAM via ETHAA. Figure 1-6 shows the transmit/receive data processing.

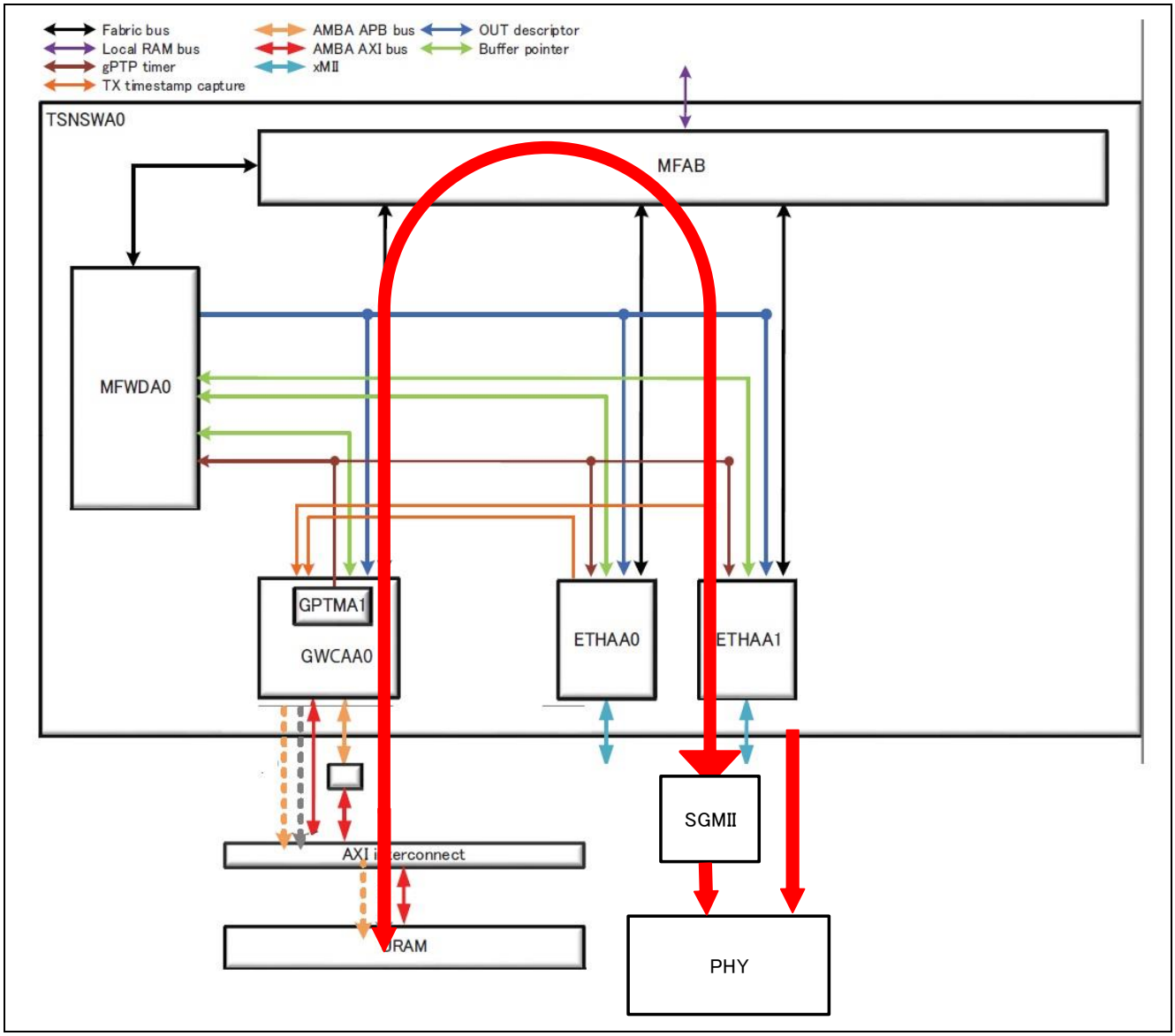

Figure 1-6 Data Processing of Transmission

1.2.6 RMAC Overview

Figure 1-7 shows the block diagram of RMAC module. Perform PHY management (reset, and internal register write/read) the linkup confirmation by using PHY MDIO interface of RMAC.

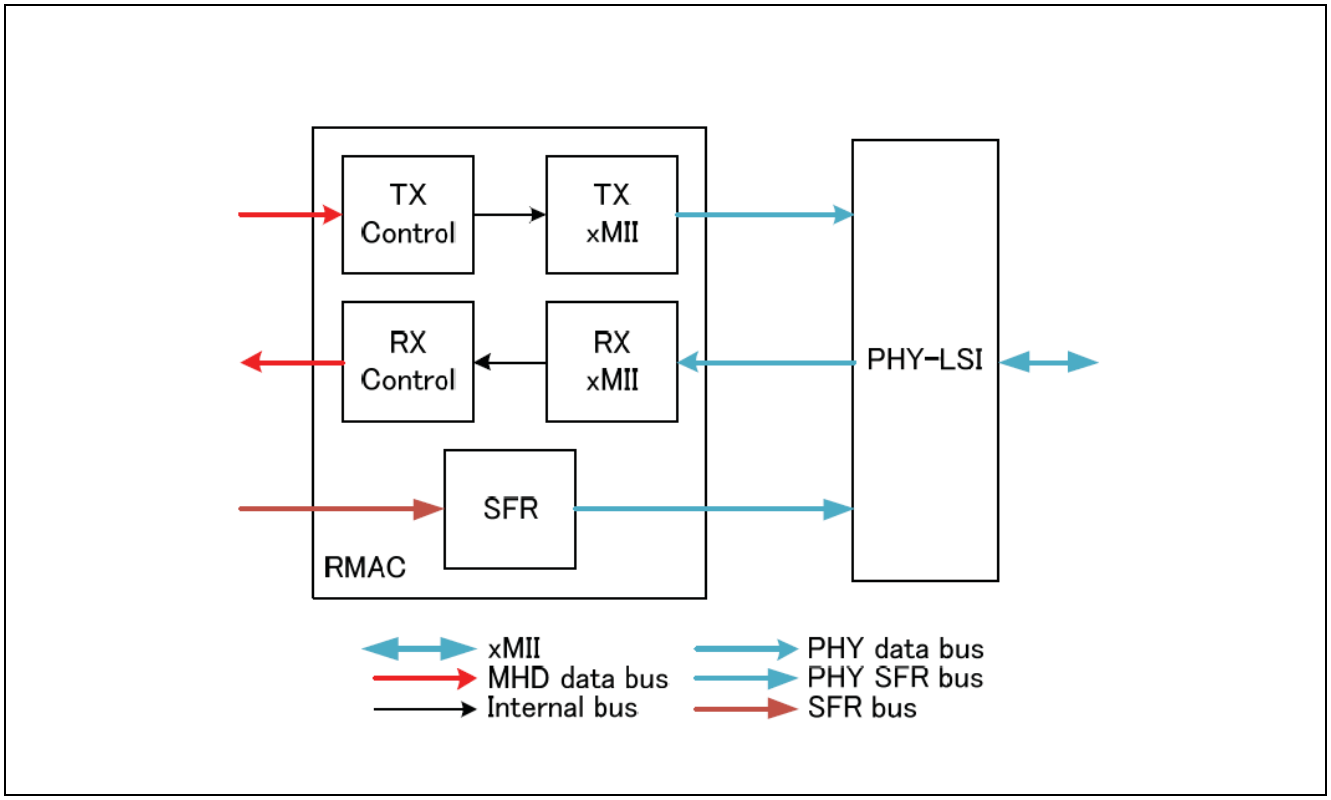

Figure 1-7 Block Diagram of RMAC

1.2.7 PHY Management and Linkup

This section explains PHY configuration function by PHY MDIO interface function.

The following show PHY specification in this operation example.

- PHY interface : SGMII
- Communication format : All duplication
- Transmission speed : 1000base
- Management data clock : 1MHz
- Management interface : Clause 22
- PHY address : 00000b

（1） Clause 45 Conversion

PHY register used in this operation example access to convert Clause 22 to Clause 45 for Clause 45 specification. Table 1-1 shows the setting value of PHY register for Clause 45 conversion.

Table 1-1 PHY Register for Clause 45 Conversion

Register Address	Bit	Setting Value
13	b15:14	11 = Data 00 = Address
	b4:0	Device address
14	b15:0	Data and address

（2） PHY Register Setting

Table 1-2 shows the setting value of PHY register (Clause 45) used in this operation example.

Table 1-2 PHY Register

Device Address	Register Address	Setting Value	Function
0x0004	0x8000	0x8000 (in resetting)	PHY reset
		0x0040 (in communicating)	1000Mbps
0x0007	0x0200	0x1200	Auto negotiation, restart auto negotiation

1.3 64 Byte Transmit/Receive Operation Example (Loopback Mode)

This operation example explains the method for transmitting and receiving the normal frame of the 64 bytes continuously 4 times by the loopback mode.

1.3.1 Communication Specification

Used channel : TSNSWA0

Frame : Normal frame (VLAN non-tagged frame)

Number of data : 64 bytes

Transmit/Receive FIFO : 64 bytes

Number of descriptor : 4

1.3.2 System Configuration

Table 1-8 shows the system configuration.

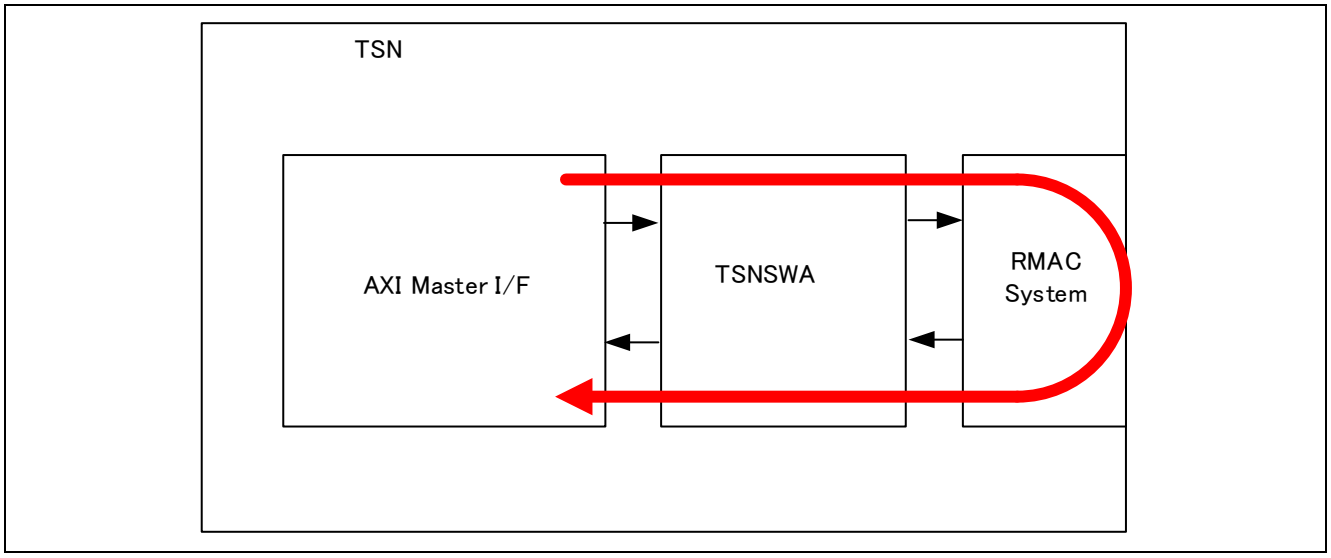

Figure 1-8 System Configuration

1.3.3 Descriptor Explanation

The storage destination (internal RAM) of the transmit/receive data and the data delivering between FIFOs in TSNSWA are performed by using the transferring information set to the descriptor. In this operation example, the format of the descriptor is the extended descriptor that is non-timestamp (16 bytes). Table 1-3 shows the setting value of the descriptor.

Table 1-3 Setting Value of Descriptor

Category	Number	Type	Data Storing Destination Address	Size
Reception	1	FEMPTY	0xFDC01000	64 bytes
	2	FEMPTY	0xFDC01040	64 bytes
	3	FEMPTY	0xFDC01080	64 bytes
	4	FEMPTY	0xFDC010C0	64 bytes
	5	EEMPTY	-	-
Transmission	1	FSINGLE	0xFDC01200	64 bytes
	2	FSINGLE	0xFDC01240	64 bytes
	3	FSINGLE	0xFDC01280	64 bytes
	4	FSINGLE	0xFDC012C0	64 bytes
	5	EEMPTY	-	-

1.3.4 MAC Address Filter

The data reception performs the filtering processing of MAC address. In this operation example, the unicast reception is enabled.

1.3.5 Software Explanation

- Module Explanation

The following shows the module list in this operation example.

Table 1-4 Module List

Module Name	Label Name	Function
Main routine	main_pe0	Perform each setting, and application booting.
Port initialization routine	port_init	Perform initial setting of port.
Ether communication start	eth_open	Perform processing of ether communication start.
Ether communication end	eth_close	Perform processing of ether communication end.
GWCAA initial setting	gwcaa	Perform initial setting of GWCAA.
AXIBMI2 initial setting	axibmi2	Perform AXIBMI2 initial setting.
RMACA2 initial setting	rmaca2	Perform RMACA2 initial setting.
ETHAA0 initial setting	ethaa0	Perform ETHAA0 initial setting.
SGMII initial setting	sgmii	Perform SGMII initial setting.
mFwd initial setting	mFwd	Perform mFwd initial setting.
Descriptor initialization	init_ethram	Initialize the descriptor.
RAM initialization	init_ram	Initialize RAM.
Data transmission	eth_write	Perform the transmit data setting and transmit start processing.
Data reception	eth_read	Perform the receive data reading and storing processes.
Transmit data setting	write_ethram	Set the transmit data to the local RAM.
Receive data setting	read_ethram	Set the receive data to the local RAM.
PHY initialization	phy_init	Perform PHY resetting.
Auto negotiation	phy_start_autonegotiate	Perform communication format, transmit speed setting, and auto-negotiation enable /execution.
PHY register read	phy_read	Specify PHY register address and read internal register.
PHY register write	phy_write	Specify PHY register address and write internal register.
Clause45 format PHY register lead	Clause45_read	Specify address PHY address in Clause 45 format, and read internal register.
Clause45 format PHY register write	Clause45_write	Specify address PHY address in Clause 45 format, and write internal register.

- Register Setting

The following shows the register setting for each function in this operation example.

Table 1-5 ETHAA0 Register Setting

Register Name	Setting Value	Function
EAMC	0x00000001	Operation mode control : Disable mode
	0x00000002	Operation mode control : Config mode
	0x00000003	Operation mode control : Operation mode
EAVTMC	0x00020001	Transmit/Receive VLAN tagging : Transmit/Receive VLAN non-tagging mode

Table 1-6 GWCAA Register Setting

Register Name	Setting Value	Function
GWRR	0x00000001	RAM Initialization
GWMC	0x00000000	Operation mode control : Disable mode
	0x00000001	Operation mode control : Config mode
	0x00000002	Operation mode control : Operation mode

Table 1-7 SGMII Register Setting

Register Name	Setting Value	Function
ETN0SGSRST	0x00000001	Software reset
ETN0SGCLKSEL	0x00000001	Reference clock selection : Internal clock (20MHz)
ETN0SGRCIE	0x01	Clock enable
ETN0SGOPMC	0x0000000B	Transfer rate : 1000Mbps, all duplication, and LSI bypass

Table 1-8 MFWDA Register Setting

Register Name	Setting Value	Function
FWSTPFC	0x00000007	Spanning tree forwarding : Port 7
FWAC	0x00000007	MAC Authentication : Port 7
FWSPBFE	0x00000007	Source port base forwarding : Port 7
FWSPBFC20	0x00000004	ag0 input/output : Port 4
FWSPBFC22	0x00000001	CPU input/output : Port 1

Table 1-9 AXIBMI2 Register Setting

Register Name	Setting Value	Function
AXIBMI2RR	0x00000003	TX descriptor address table RAM reset : Enable
		RX descriptor address table RAM reset : Enable
AXIBMI2AXIWC	0x00004411	Write RX P frame number : 4
		Write RX E frame number : 4
		Write TX P frame number : 1
		Write TX E frame number : 1
AXIBMI2AXIRC	0x00001122	Read RX P frame number : 1
		Read RX E frame number : 1
		Read TX P frame number : 2
		Read TX E frame number : 2
AXIBMI2TATLS0	0x00000002	Extended descriptor : Enable
		Normal mode : Transmit synchronization mode
AXIBMI2TATLS1	le0.txcurrent	TX descriptor address : le0.txcurrent
AXIBMI2TATLR	0x00000001	TX descriptor address education : Enable
AXIBMI2RATLS0	0x00000028	RX descriptor address wait : Enable
		RX frame size error : AXIBMI stop
		Extended descriptor : Enable
		Normal mode : receive synchronization mode
AXIBMI2RATLS1	le0.rxcurrent	RX descriptor address education：le0.rxcurrent
AXIBMI2RATLR	0x00000001	RX descriptor address education : Enable
AXIBMI2TRCR0	0x00000001	Transmit start request : Enable
AXIBMI2TDIS0	0xFFFFFFFF	Transmit completion flag : Clear
AXIBMI2RDIS0	0xFFFFFFFF	Receive completion flag : Clear

Table 1-10 RMACA2 Register Setting

Register Name	Setting Value	Function
RMACA2MRMAC1	MAC_ADDR[1] MAC_ADDR[2]	MAC lower address : MAC_ADDR[1]、MAC_ADDR[2]
RMACA2MRMAC0	MAC_ADDR[0]	MAC higher address : MAC_ADDR[0]
RMACA2MRAFC	0x00010001	p frame unicast : Enable
		E frame unicast : Enable
RMACA2MPIC	0x1209000A	Capture time correction : 1
		Hold time correction : 2
		Premble : Disable
		Clock selection : 0x0A
		Link speed : 1Gbps
		PHY I/F：SGMII
RMACA2MLBC	0x00000001	Loopback mode : Enable

RMACA2MPSM (in reading)	0x0000XX00	PHY register write : 0
		PHY register address : XX(reg_addr)
		PHY device address : 0
		Access direction : Read
		Management : Disable
	↓	↓
	0x0000XX01	PHY register write : 0
		PHY register address : XX(reg_addr)
		PHY device address : 0
		Access direction : Read
		Management : Enable
RMACA2MPSM (in writing)	0xYY00XX02	PHY register write : YY(data)
		PHY register address : XX(reg_addr)
		PHY device address : 0
		Access direction : Write
		Management : Disable
	↓	↓
	0xYY00XX03	PHY register write : YY(data)
		PHY register address : XX(reg_addr) PHY device address : 0
		Access direction : Write
		Management : Enable

Table 1-11 Port Register Setting

Register Name	Setting Value	Function
PCR10_2	0x01000046	P10_2 : ETH0_MDC
PCR10_4	0x01000077	P10_4 : ETH0_MDIO
PCR10_8	0x00001000	P10_8 : ETH0_RESET

1.3.6 Flowchart

The following shows the flowchart in this operation example.

1.3.7 Main

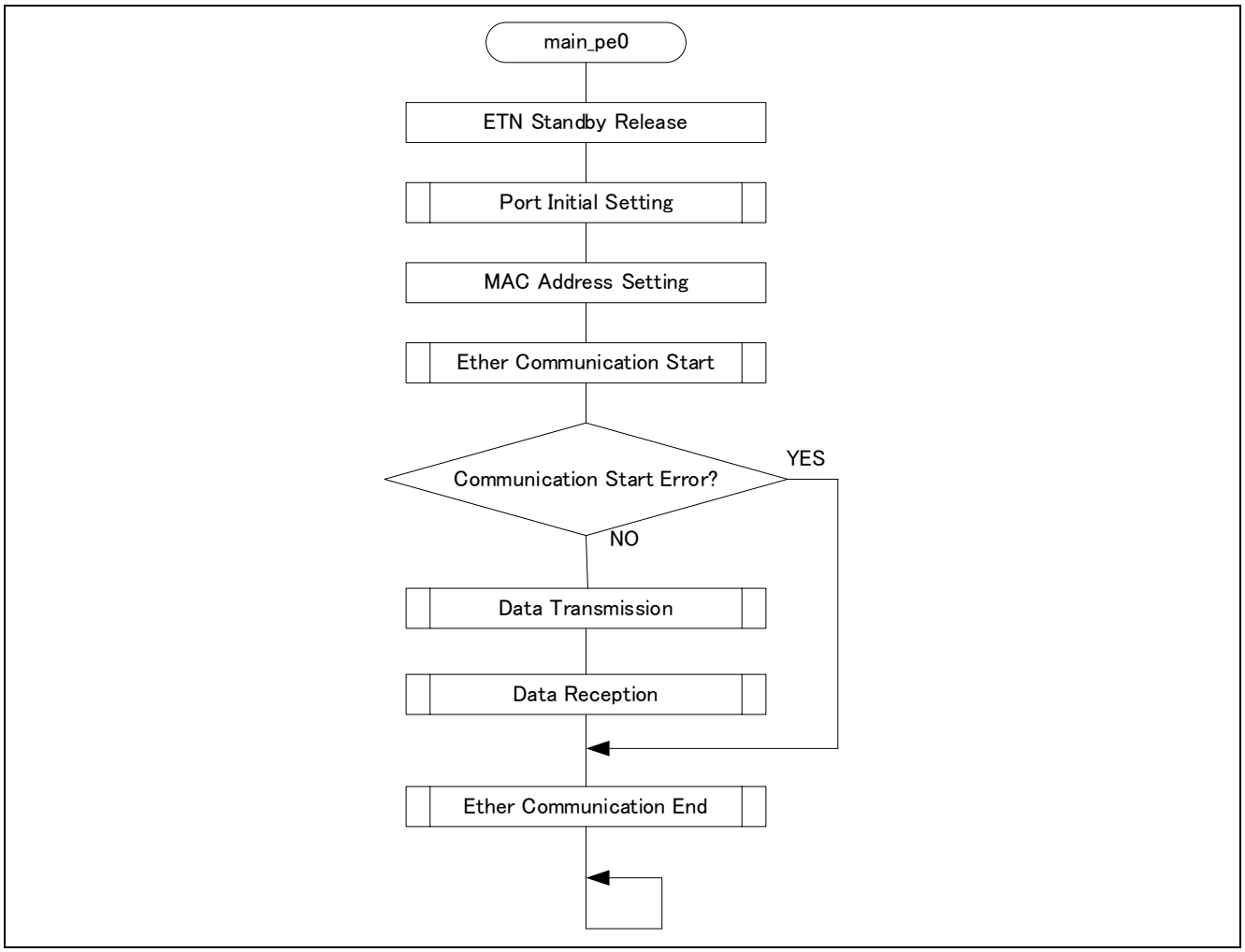

Figure 1-9 Main Module Flowchart

1.3.8 Ether Communication Start

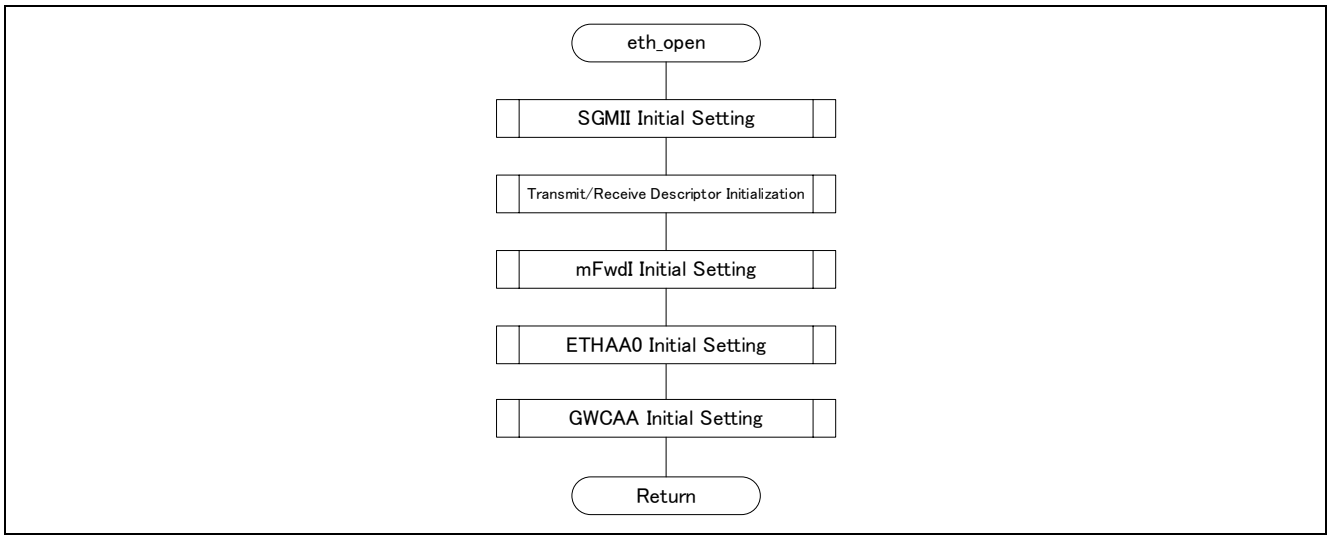

Figure 1-10 Ether Communication Module Start Flowchart

1.3.9 Ether Communication End

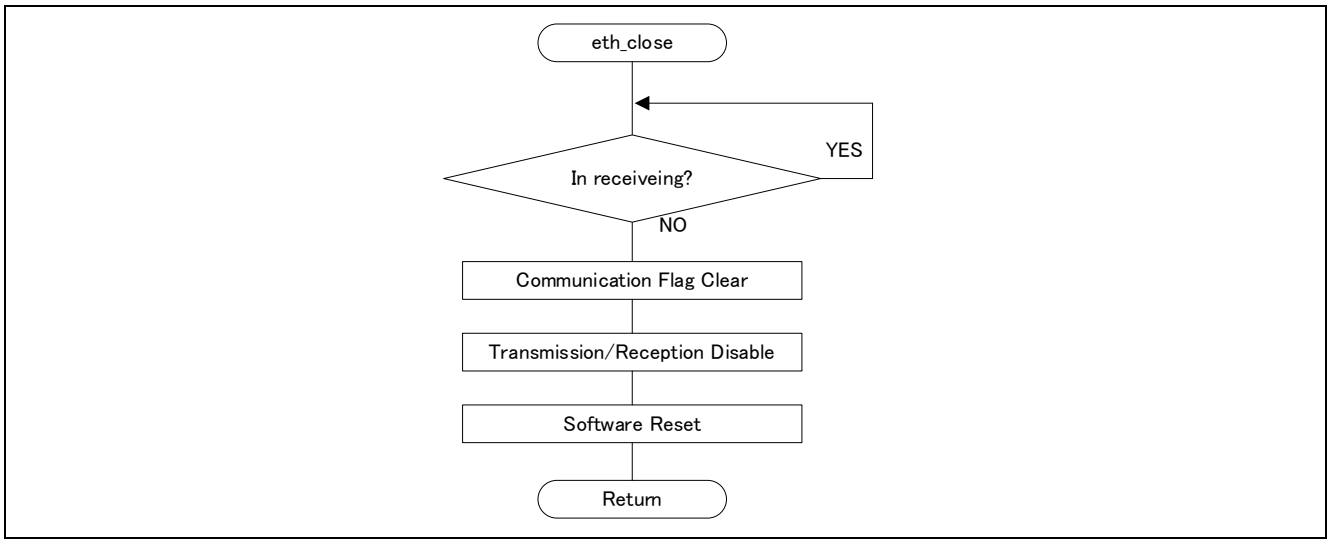

Figure 1-11 Ether Communication Module End Flowchart

1.3.10 ETHAA0 Initial Setting

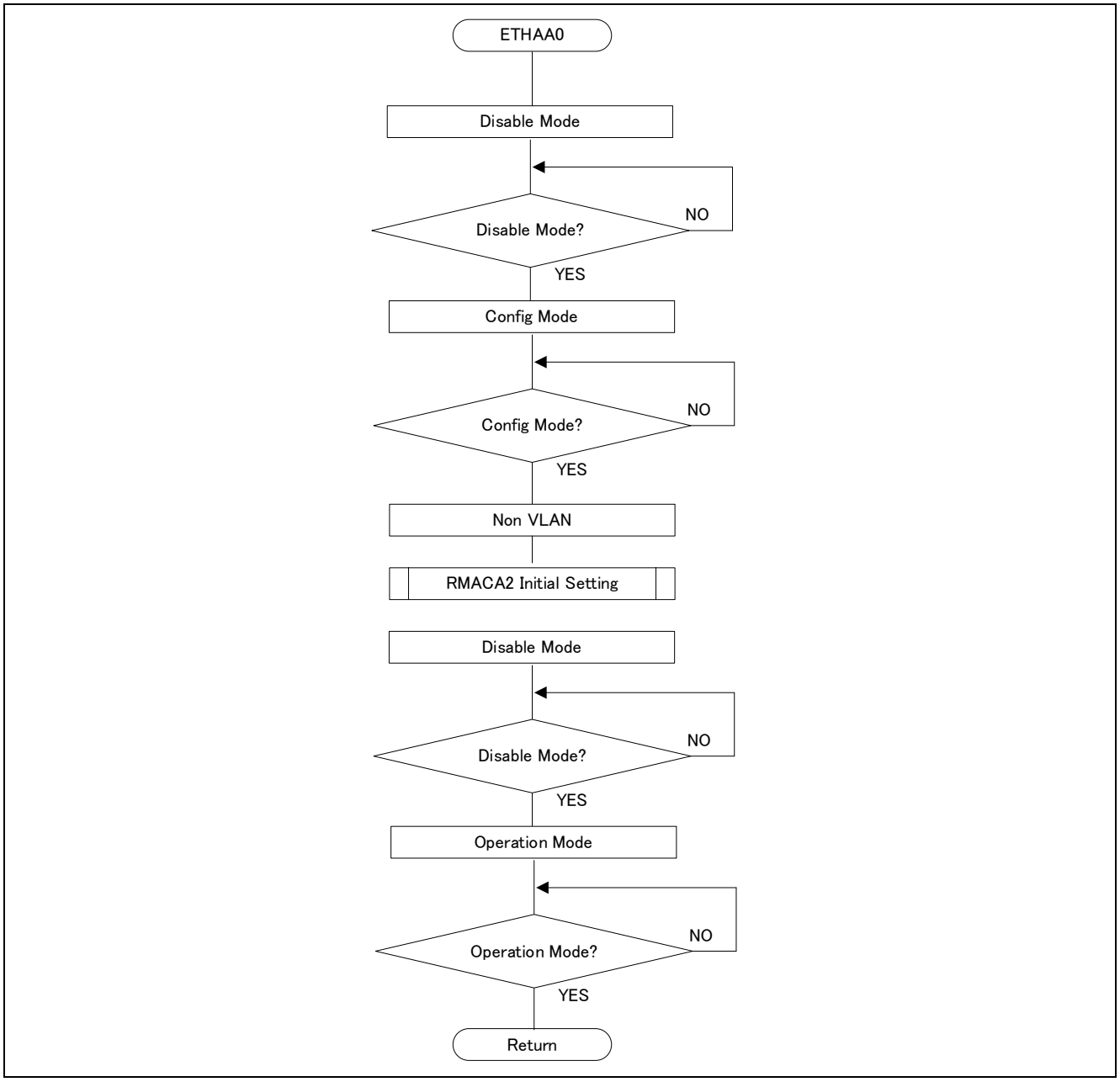

Figure 1-12 ETHAA0 Initial Setting Module Flowchart

1.3.11 GWCAA Initial Setting

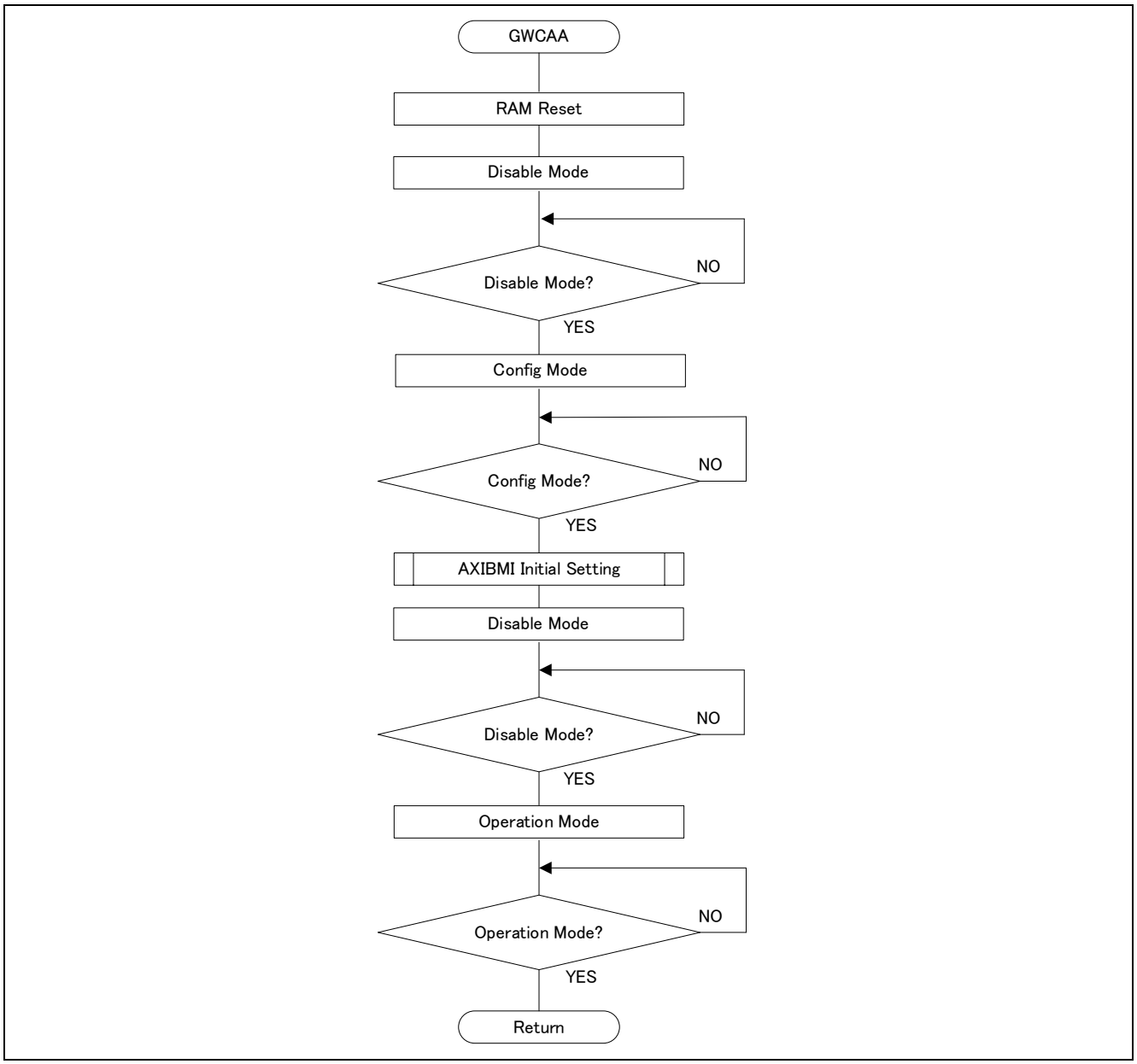

Figure 1-13 GWCAA Initial Setting Module Flowchart

1.3.12 AXIBMI2 Initial Setting

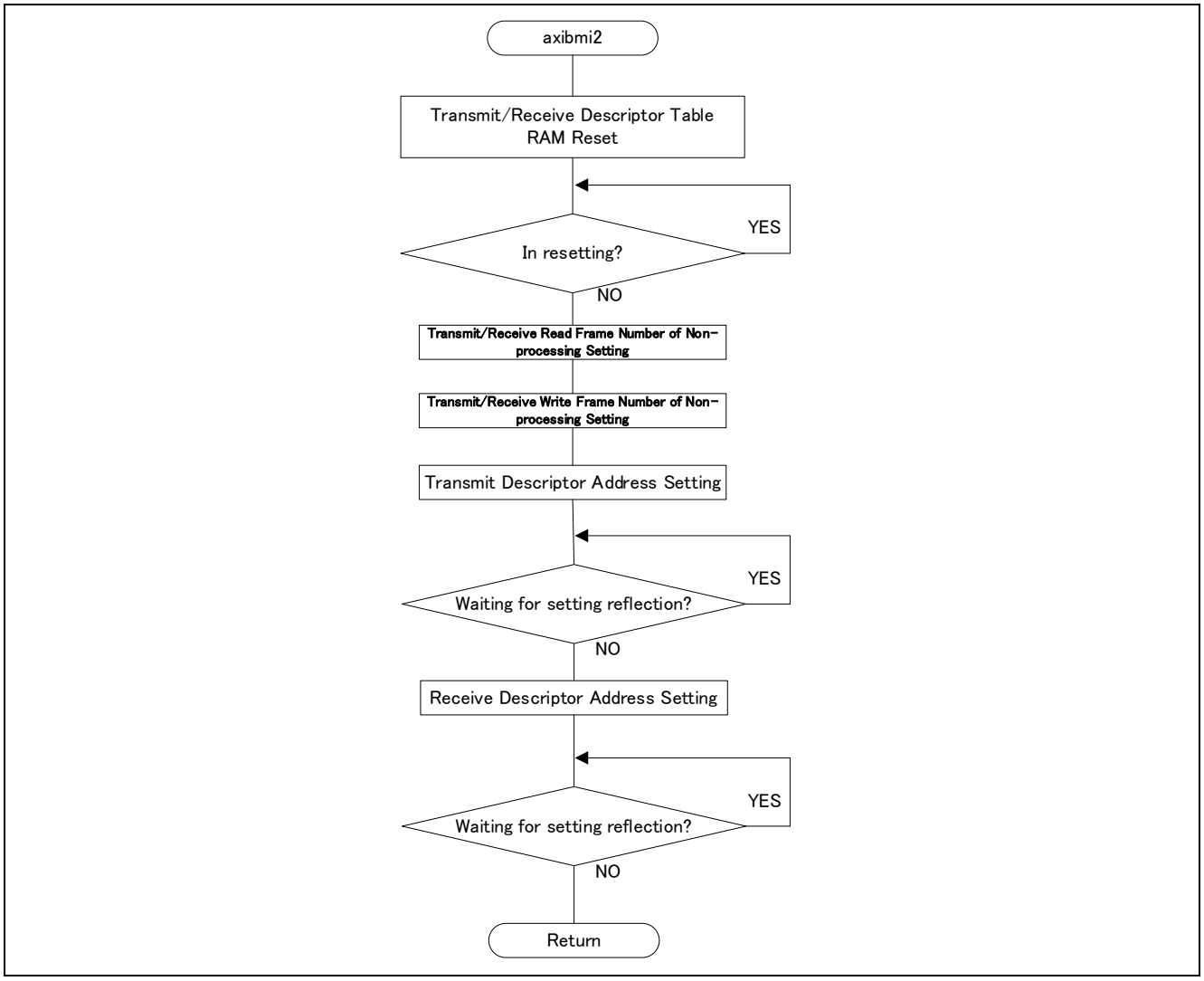

Figure 1-14 AXIBMI2 Initial Setting Module Flowchart

1.3.13 RMACA2 Initial Setting

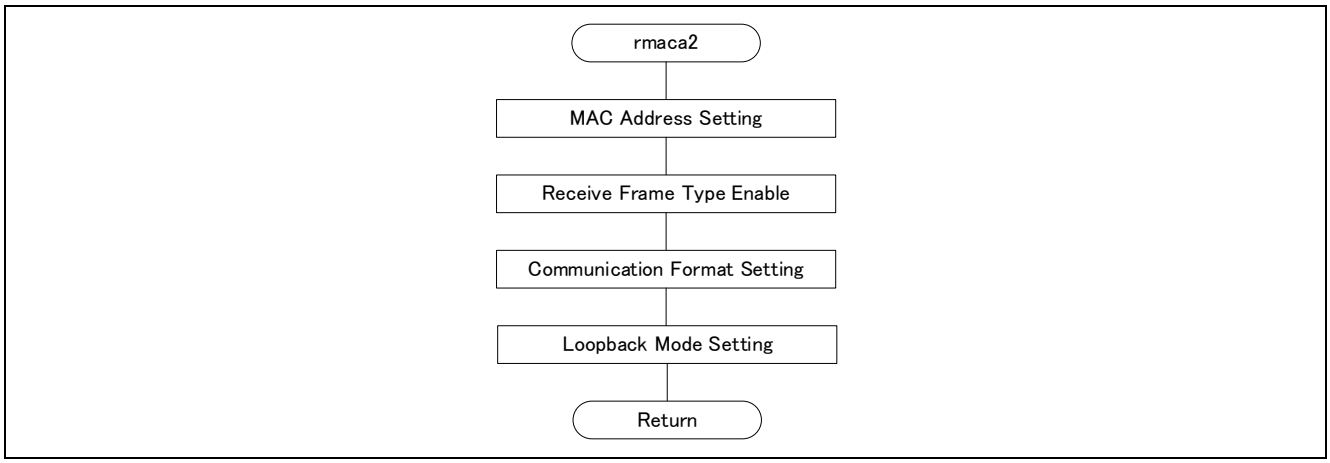

Figure 1-15 RMACA2 Initial Setting Module Flowchart

1.3.14 SGMII Initial Setting

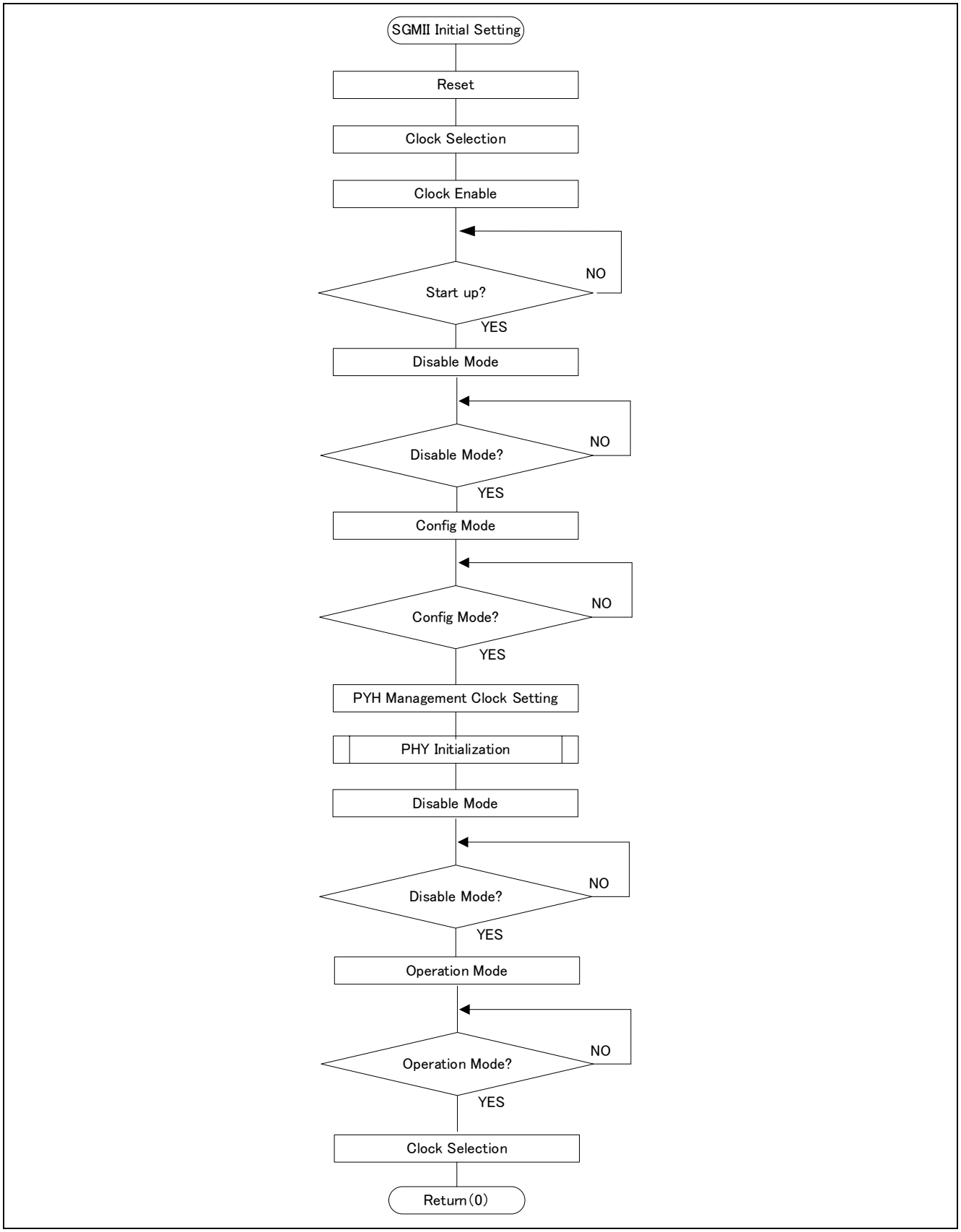

Figure 1-16 SGMII Initial Setting Module Flowchart

1.3.15 MFWDA Initialization

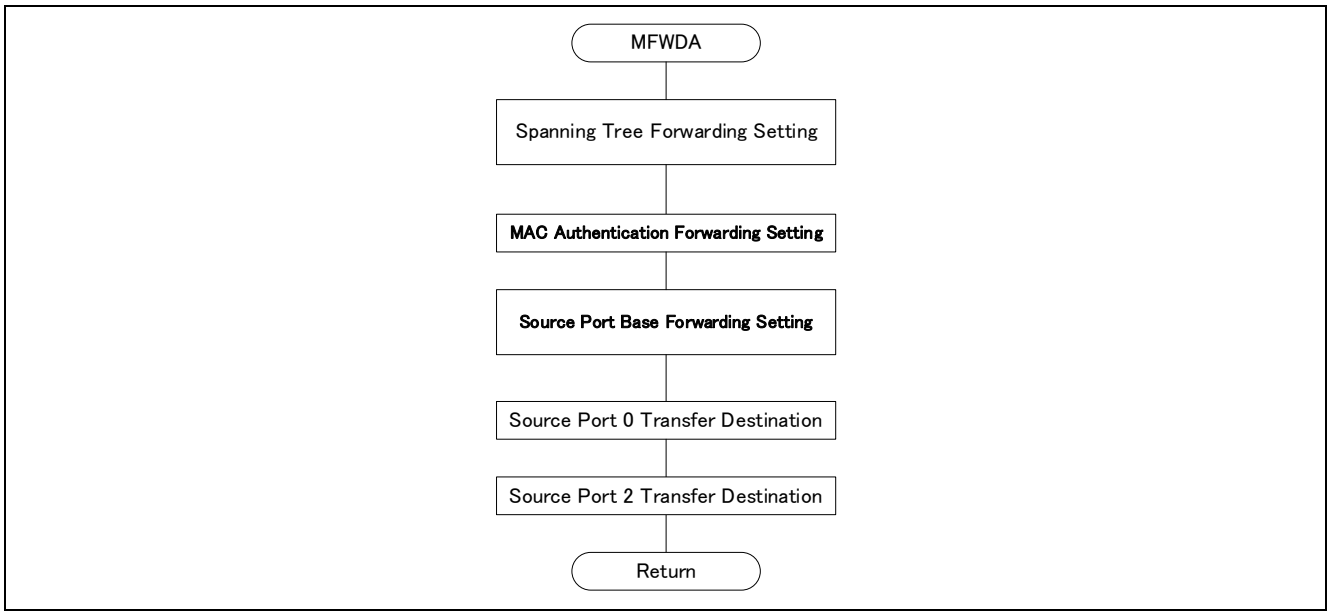

Figure 1-17 MFWDA Initialization Module Flowchart

1.3.16 Transmit/Receive Descriptor Initialization

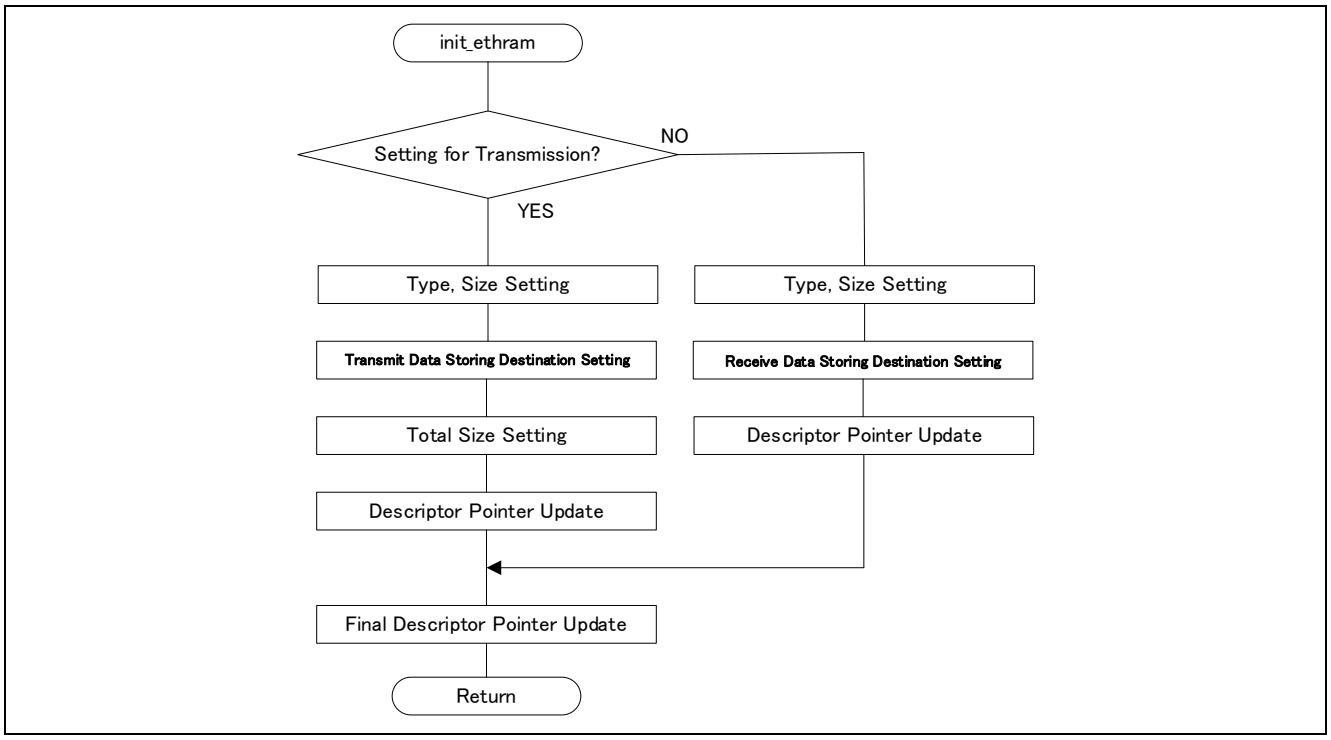

Figure 1-18 Transmit/Receive Descriptor Initialization Module Flowchart

1.3.17 Data Transmission

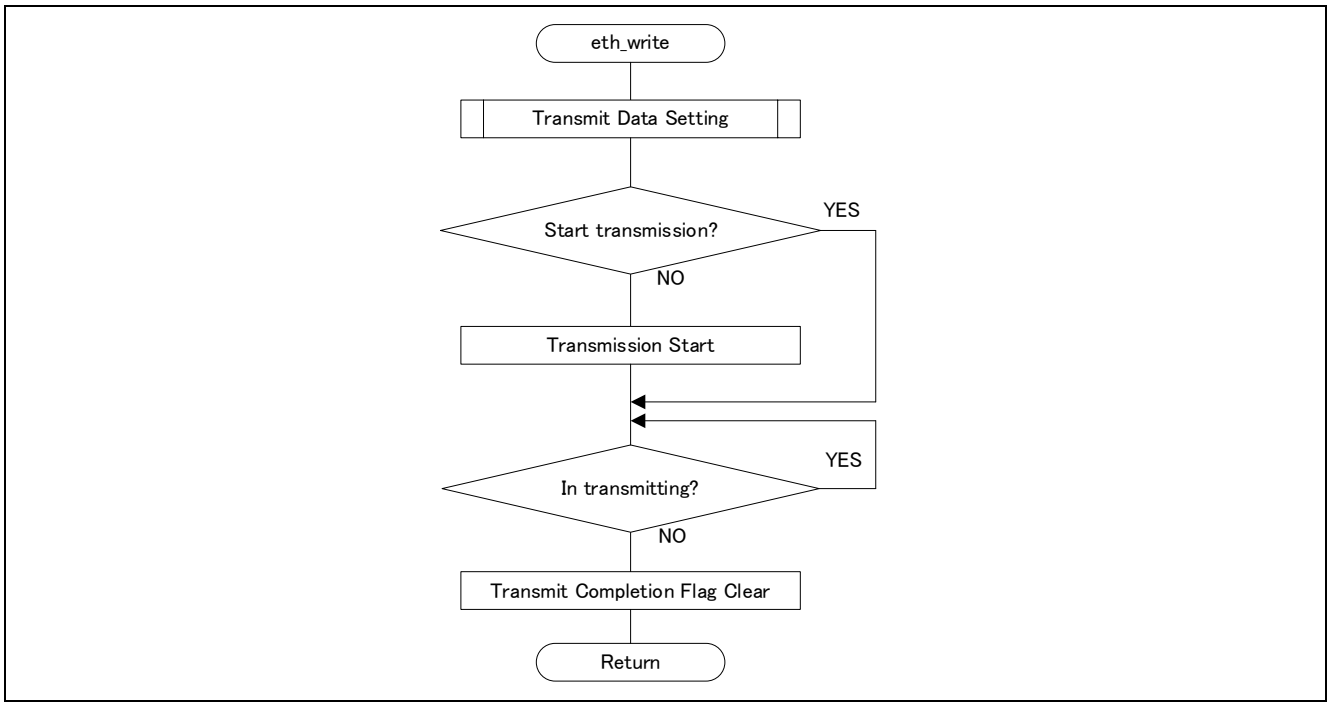

Figure 1-19 Data Transmit Module Flowchart

1.3.18 Data Reception

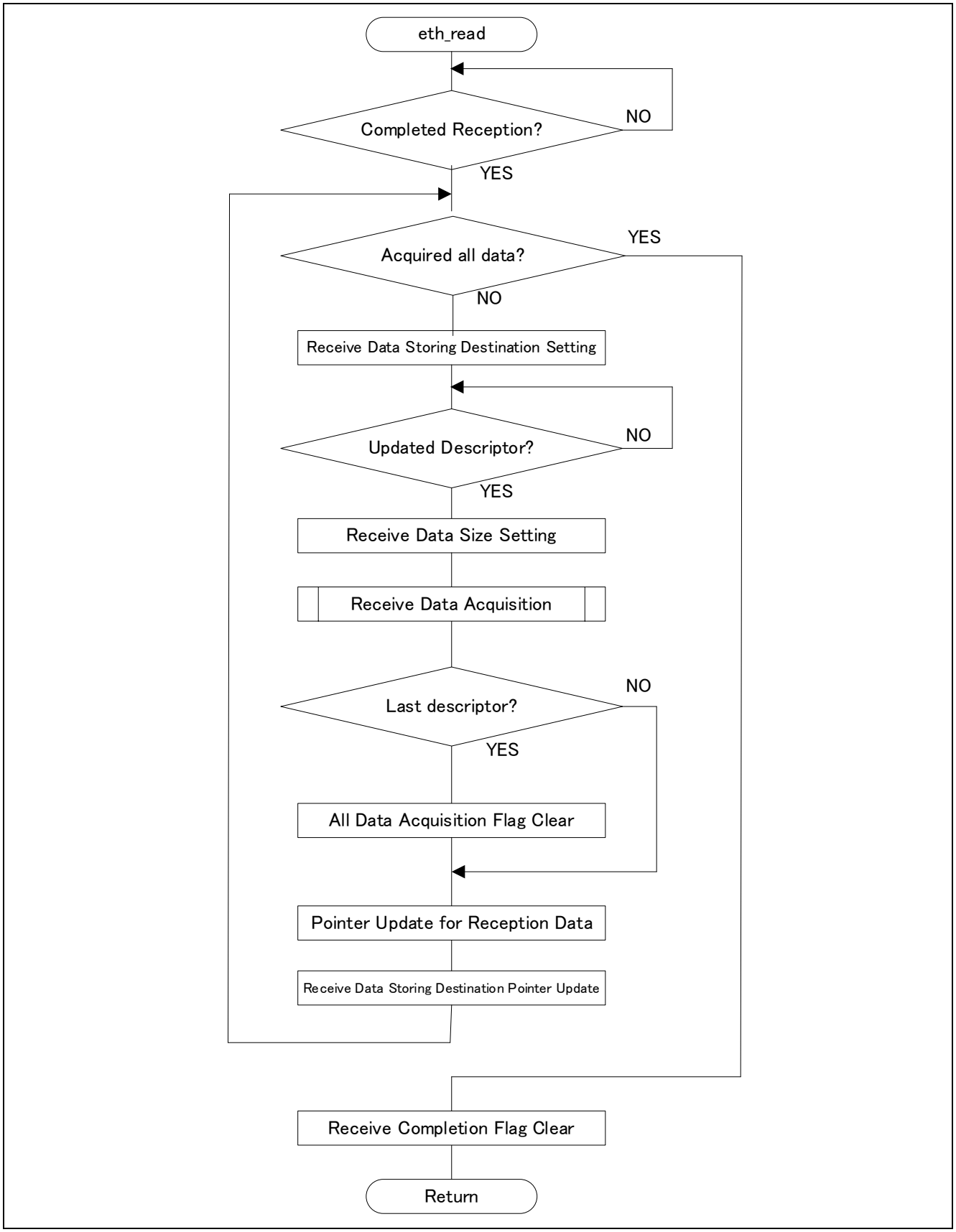

Figure 1-20 Data Receive Module Flowchart

1.3.19 Transmit Data Setting

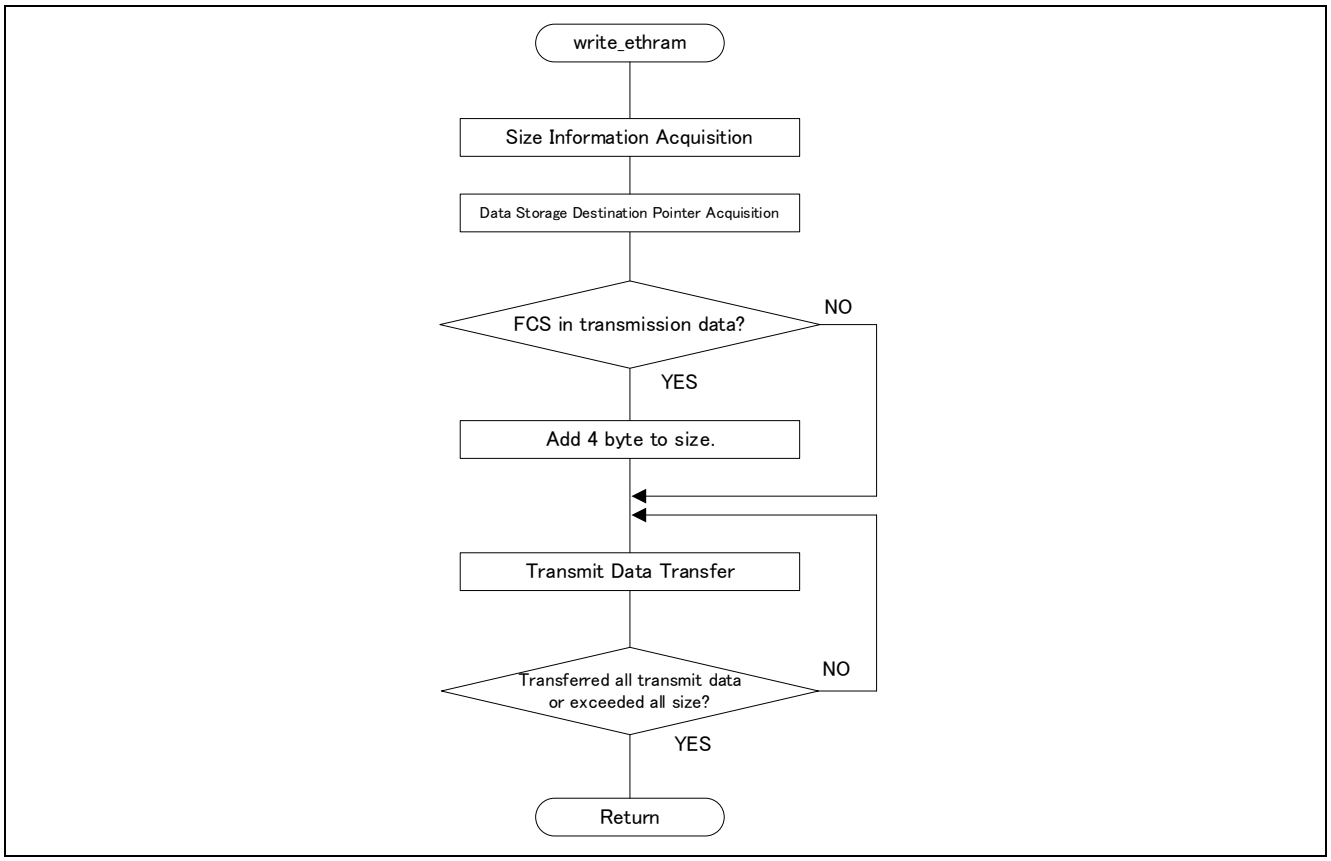

Figure 1-21 Transmit Data Setting Module Flowchart

1.3.20 Receive Data Acquisition

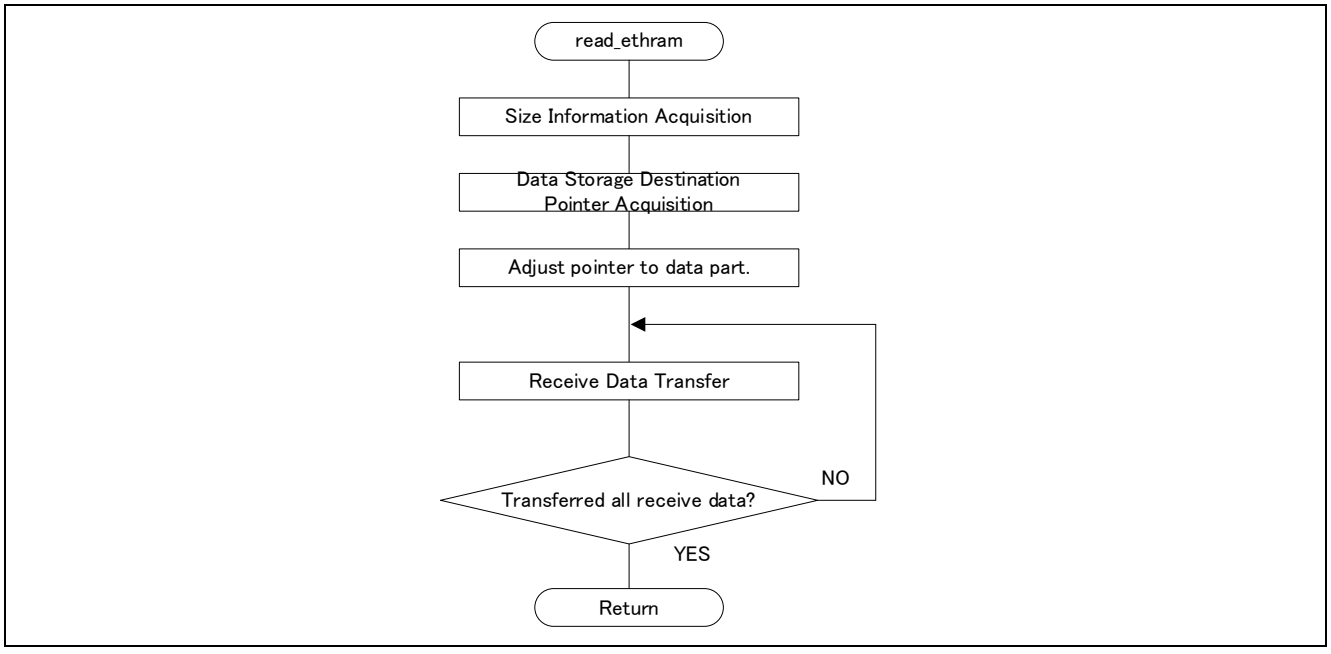

Figure 1-22 Receive Data Acquisition Module Flowchart

1.3.21 PHY Initialization

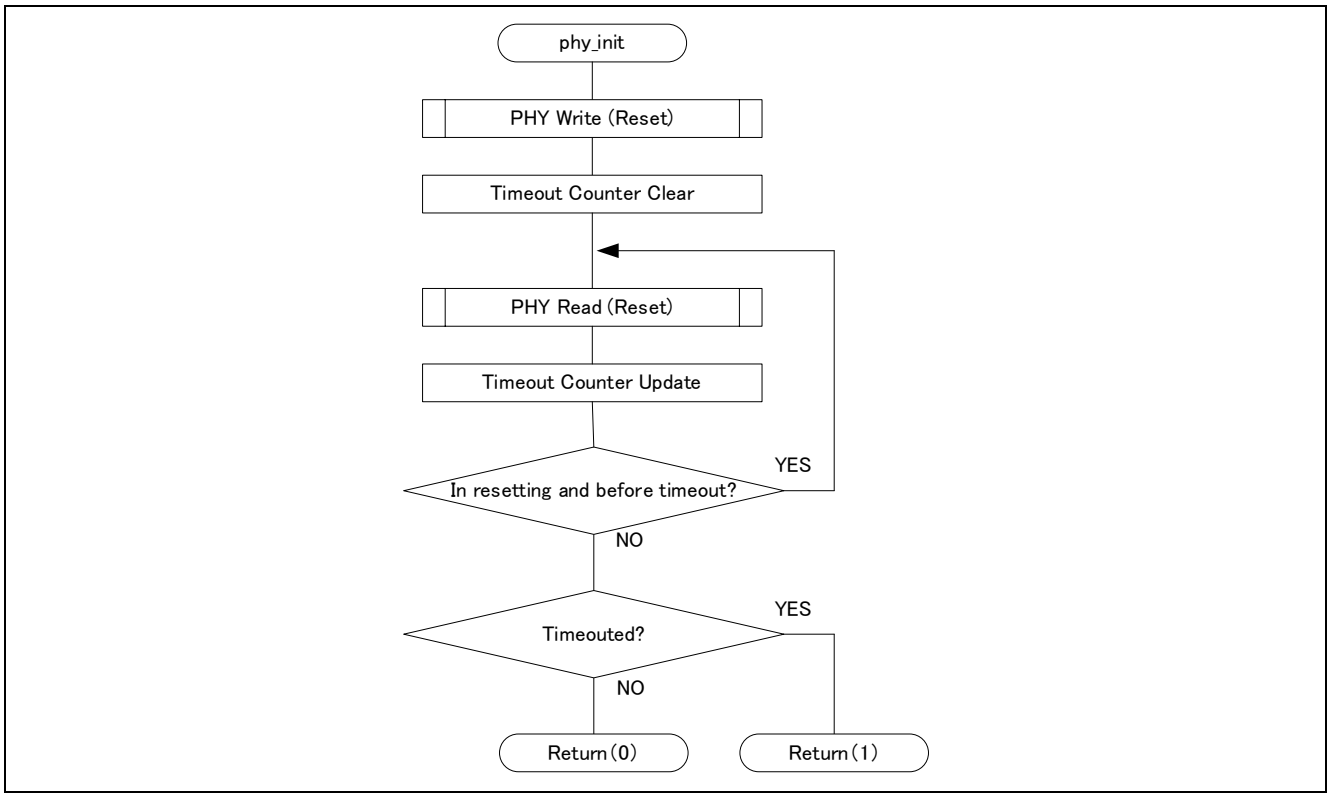

Figure 1-23 PHY Initialization Module Flowchart

1.3.22 Auto Negotiation

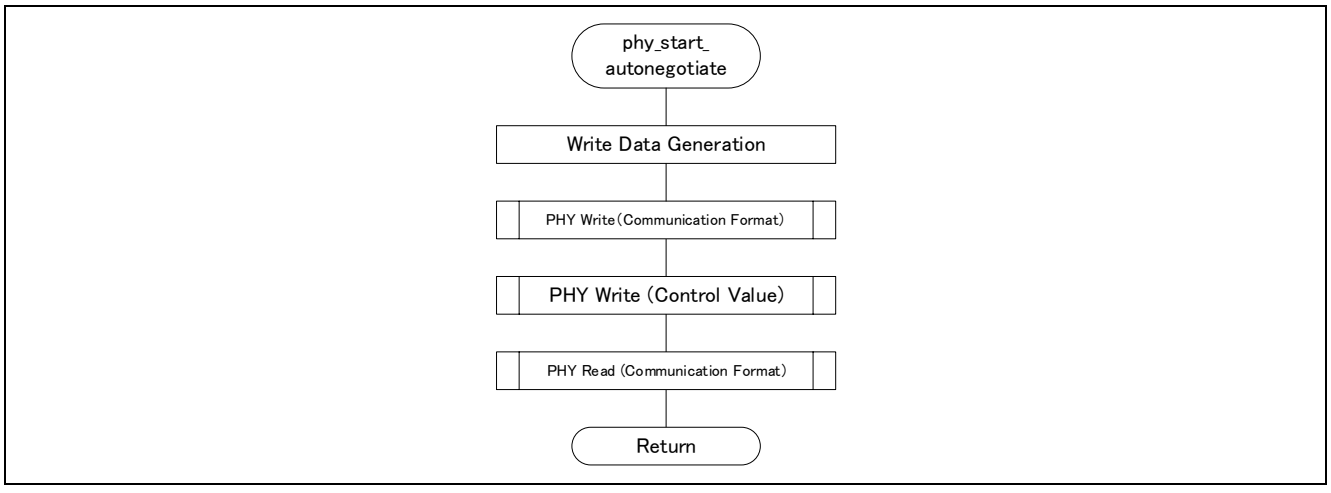

Figure 1-24 Auto Negotiation Module Flowchart

1.3.23 PHY Write

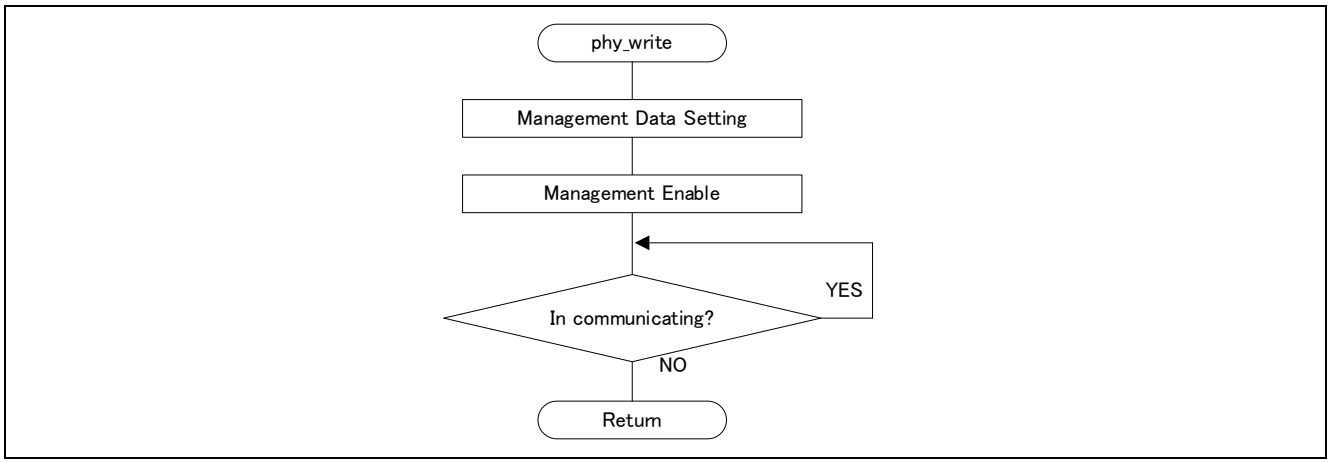

Figure 1-25 PHY Write Module Flowchart

1.3.24 PHY Read

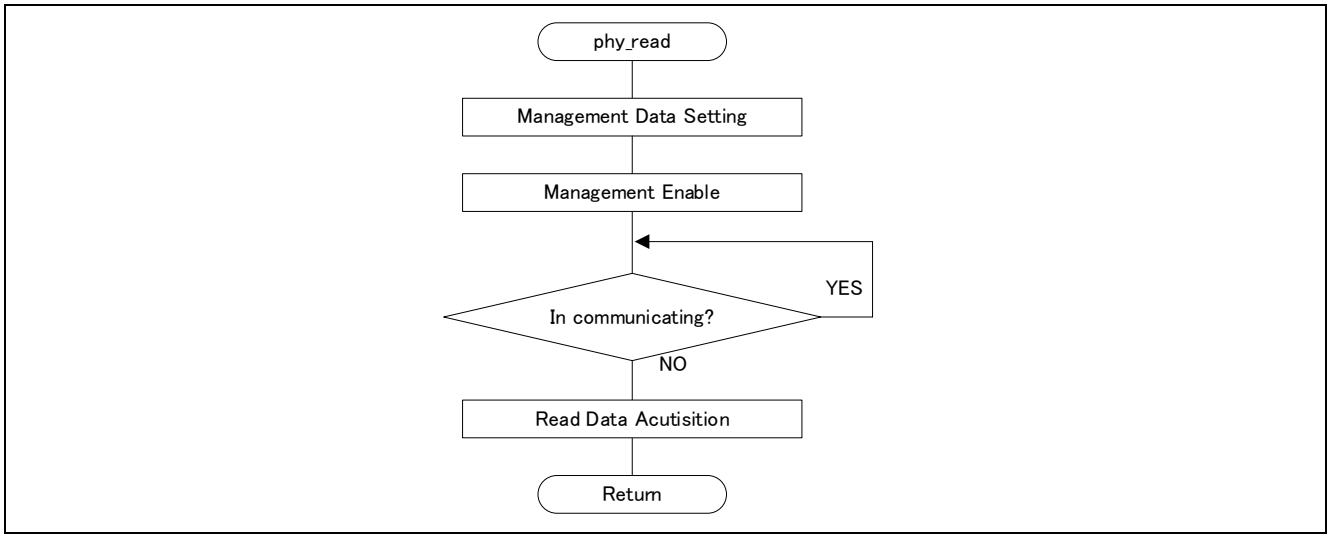

Figure 1-26 PHY Read Module Flowchart

1.3.25 Clause45 Format Write

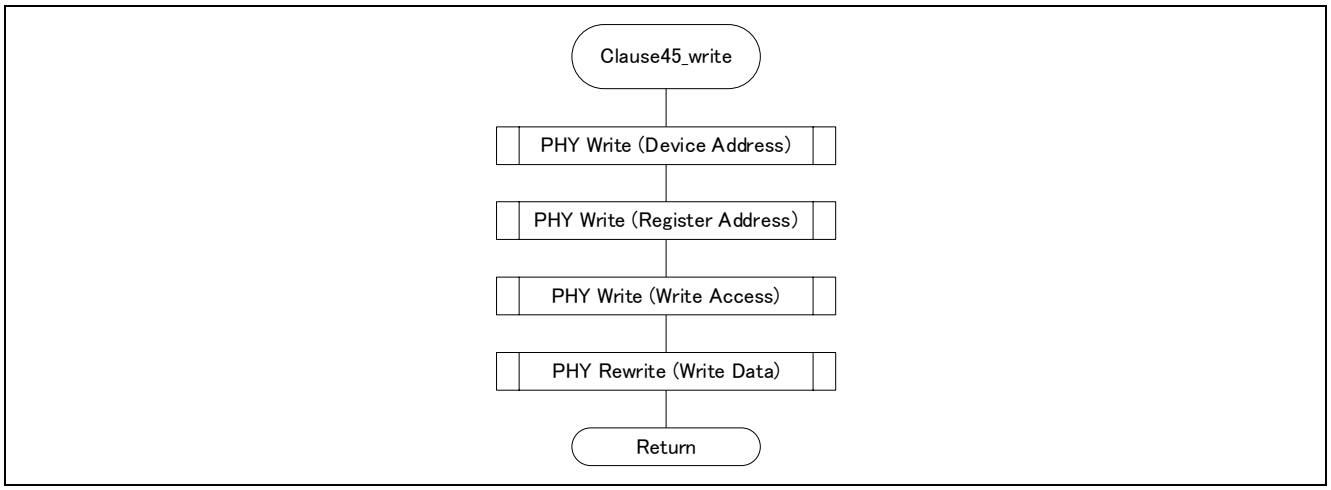

Figure 1-27 Clause45 Format Write Module Flowchart

1.3.26 Clause45 Format Read

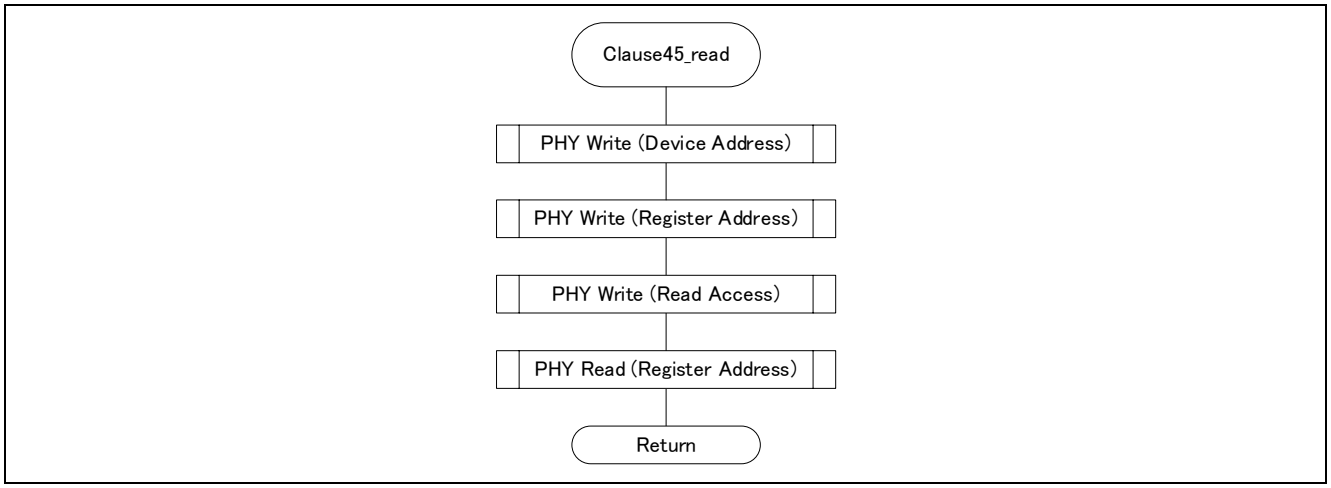

Figure 1-28 Clause45 Format Read Module Flowchart

1.4 256 Byte Transmit/Receive Operation

In this operation example, perform the transmission/reception of the 256 bytes normal frame and the transmission of the magic pocket.

1.4.1 Communication Specification

Use Channel : TSNSWA0

Frame : Normal frame, magic packet frame

Number of data : 256 Bytes

Transmit/Receive FIFO : 256 Bytes

Number of descriptors : 4

1.4.2 System Configuration

Figure 1-29 shows the system configuration.

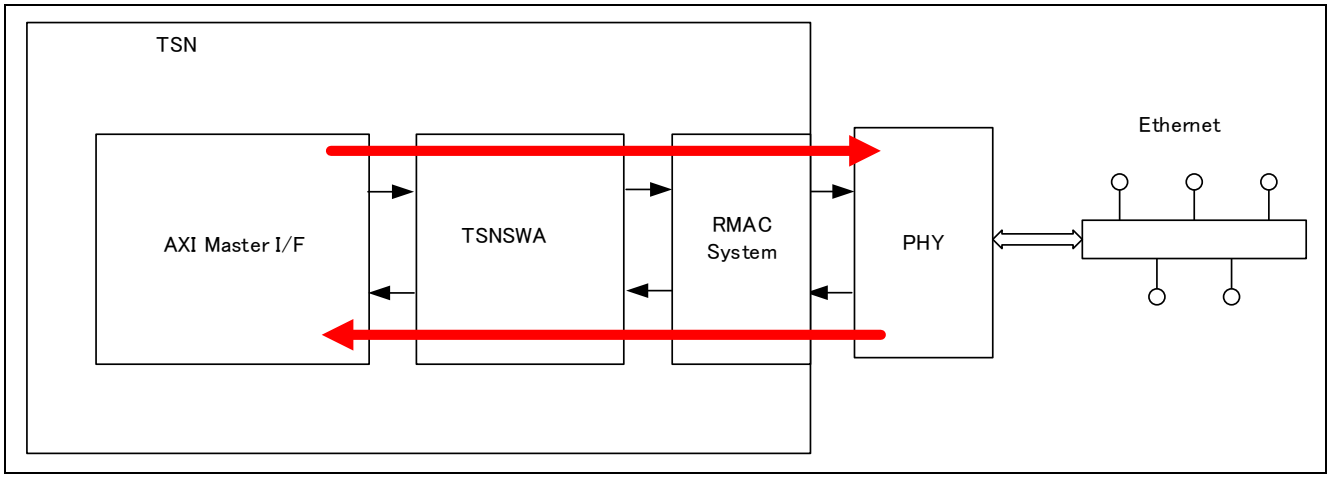

Figure 1-29 System Configuration

1.4.3 Descriptor Explanation

The storage destination (internal RAM) of the transmit/receive data and the data delivering between FIFOs in TSNSWA are performed by using the transferring information set to the descriptor. In this operation example, the format of the descriptor is the extended descriptor that is non-timestamp (16 bytes). 256 bytes of data is divided into 64 bytes and sent/received. Figure 1-3 shows the setting value of descriptor.

Table 1-12 Setting Value of Descriptor

Category	No.	Type	Data Storing Destination Address	Size
Reception	1	FEMPTY	0xFDC01000	64 bytes
	2	FEMPTY	0xFDC01040	64 bytes
	3	FEMPTY	0xFDC01080	64 bytes
	4	FEMPTY	0xFDC010C0	64 bytes
	5	EEMPTY	-	-
Transmission	1	FSTART	0xFDC01200	64 bytes
	2	FMID	0xFDC01240	64 bytes
	3	FMID	0xFDC01280	64 bytes
	4	FEND	0xFDC012C0	64 bytes
	5	EEMPTY	-	-

1.4.4 Magic Packet Reception

In this operation example, perform the reception of the magic packet. The data of the received magic packet is the following.

“0xFF,0xFF,0xFF,0xFF,0xFF,0xFF”, “0x74,0x90,0x50,0x00,0x79,0x03” ×16

1.4.5 Software Explanation

- Module Explanation

The following shows the module list in this operation example.

Table 1-13 Module List

Module Name	Rabel Name	Function
Main routine	main_pe0	Perform each setting, and application booting.
Port initialization routine	port_init	Perform initial setting of port.
Ether communication start	eth_open	Perform processing of ether communication start.
Ether communication end	eth_close	Perform processing of ether communication end.
GWCAA initial setting	gwcaa	Perform initial setting of GWCAA.
AXIBMI2 initial setting	axibmi2	Perform AXIBMI2 initial setting.
RMACA2 initial setting	rmaca2	Perform RMACA2 initial setting.
ETHAA0 initial setting	ethaa0	Perform ETHAA0 initial setting.
SGMII initial setting	sgmii	Perform SGMII initial setting.
mFwd initial setting	mFwd	Perform mFwd initial setting.
Descriptor initialization	init_ethram	Initialize the descriptor.
RAM initialization	init_ram	Initialize RAM.
Data transmission	eth_write	Perform the transmit data setting and transmit start processing.
Data reception	eth_read	Perform the receive data reading and storing processes.
Transmit data setting	write_ethram	Set the transmit data to the local RAM.
Receive data setting	read_ethram	Set the receive data to the local RAM.
PHY initialization	phy_init	Perform PHY resetting.
Auto negotiation	phy_start_autonegotiate	Perform communication format, transmit speed setting, and auto-negotiation enable /execution.
PHY register read	phy_read	Specify PHY register address and read internal register.
PHY register write	phy_write	Specify PHY register address and write internal register.
Clause45 format PHY register lead	Clause45_read	Specify address PHY address in Clause 45 format, and read internal register.
Clause45 format PHY register write	Clause45_write	Specify address PHY address in Clause 45 format, and write internal register.

- Register Setting

The following shows the register setting for each function in this operation example.

Table 1-14 ETHAA0 Register Setting

Register Name	Setting Value	Function
EAMC	0x00000001	Operation mode control : Disable mode
	0x00000002	Operation mode control : Config mode
	0x00000003	Operation mode control : Operation mode
EAVTMC	0x00020001	Transmit/Receive VLAN tagging : Transmit/Receive VLAN non-tagging mode

Table 1-15 GWCAA Register Setting

Register Name	Setting Value	Function
GWRR	0x00000001	RAM Initialization
GWMC	0x00000000	Operation mode control : Disable mode
	0x00000001	Operation mode control : Config mode
	0x00000002	Operation mode control : Operation mode

Table 1-16 SGMII Register Setting

Register Name	Setting Value	Function
ETN0SGSRST	0x00000001	Software reset
ETN0SGCLKSEL	0x00000001	Reference clock selection : Internal clock (20MHz)
ETN0SGRCIE	0x01	Clock enable
ETN0SGOPMC	0x0000000B	Transfer rate : 1000Mbps, all duplication, and LSI bypass

Table 1-17 MFWDA Register Setting

Register Name	Setting Value	Function
FWSTPFC	0x00000007	Spanning tree forwarding : Port 7
FWAC	0x00000007	MAC Authentication : Port 7
FWSPBFE	0x00000007	Source port base forwarding : Port 7
FWSPBFC20	0x00000004	ag0 input/output : Port 4
FWSPBFC22	0x00000001	CPU input/output : Port 1

Table 1-18 AXIBMI2 Register Setting

Register Name	Setting Value	Function
AXIBMI2RR	0x00000003	TX descriptor address table RAM reset : Enable
		RX descriptor address table RAM reset : Enable
AXIBMI2AXIWC	0x00004411	Write RX P frame number : 4
		Write RX E frame number : 4
		Write TX P frame number : 1
		Write TX E frame number : 1
AXIBMI2AXIRC	0x00001122	Read RX P frame number : 1
		Read RX E frame number : 1
		Read TX P frame number : 2
		Read TX E frame number : 2
AXIBMI2TATLS0	0x00000002	Extended descriptor : Enable
		Normal mode : Transmit synchronization mode
AXIBMI2TATLS1	le0.txcurrent	TX descriptor address : le0.txcurrent
AXIBMI2TATLR	0x00000001	TX descriptor address education : Enable
AXIBMI2RATLS0	0x00000028	RX descriptor address wait : Enable
		RX frame size error : AXIBMI stop
		Extended descriptor : Enable
		Normal mode : receive synchronization mode
AXIBMI2RATLS1	le0.rxcurrent	RX descriptor address education：le0.rxcurrent
AXIBMI2RATLR	0x00000001	RX descriptor address education : Enable
AXIBMI2TRCR0	0x00000001	Transmit start request : Enable
AXIBMI2TDIS0	0xFFFFFFFF	Transmit completion flag : Clear
AXIBMI2RDIS0	0xFFFFFFFF	Receive completion flag : Clear

Table 1-19 RMACA2 Register Setting

Register Name	Setting Value	Function
RMACA2MRMAC1	MAC_ADDR[1] MAC_ADDR[2]	MAC lower address : MAC_ADDR[1], MAC_ADDR[2]
RMACA2MRMAC0	MAC_ADDR[0]	MAC higher address : MAC_ADDR[0]
RMACA2MRAFC	0x00010001	p frame unicast : Enable
		E frame unicast : Enable
RMACA2MPIC	0x1209000A	Capture time correction : 1
		Hold time correction : 2
		Premble : Disable
		Clock selection : 0x0A
		Link speed : 1Gbps
		PHY I/F：SGMII
RMACA2MRGC	0x0000000F	Loopback mode : Enable
		MAC lower address : MAC_ADDR[1], MAC_ADDR[2]
		MAC higher address : MAC_ADDR[0]
		p frame unicast : Enable

RMACA2MPSM (in reading)	0x0000XX00	PHY register write : 0
		PHY register address : XX(reg_addr)
		PHY device address : 0
		Access direction : Read
		Management : Disable
	↓	↓
	0x0000XX01	PHY register write : 0
		PHY register address : XX(reg_addr)
		PHY device address : 0
		Access direction : Read
		Management : Enable
RMACA2MPSM (in writing)	0xYY00XX02	PHY register write : YY(data)
		PHY register address : XX(reg_addr)
		PHY device address : 0
		Access direction : Write
		Management : Disable
	↓	↓
	0xYY00XX03	PHY register write : YY(data)
		PHY register address : XX(reg_addr) PHY device address : 0
		Access direction : Write
		Management : Enable

Table 1-20 Port Register Setting

Register Name	Setting Value	Function
PCR10_2	0x01000046	P10_2 : ETH0_MDC
PCR10_4	0x01000077	P10_4 : ETH0_MDIO
PCR10_8	0x00001000	P10_8 : ETH0_RESET

1.4.6 Flowchart

The following shows the flowchart in this operation example.

1.4.7 Main

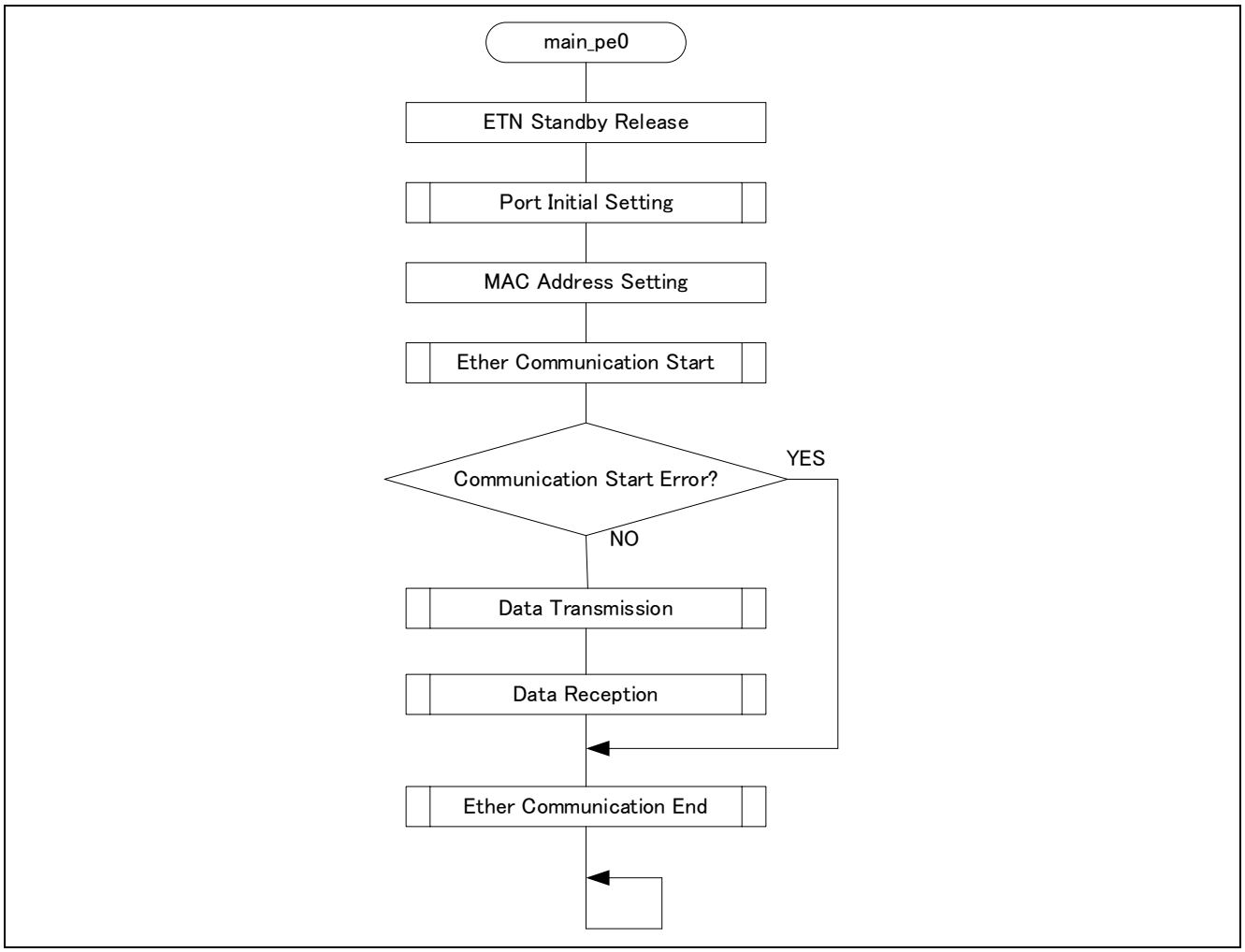

Figure 1-30 Main Module Flowchart

1.4.8 Ether Communication Start

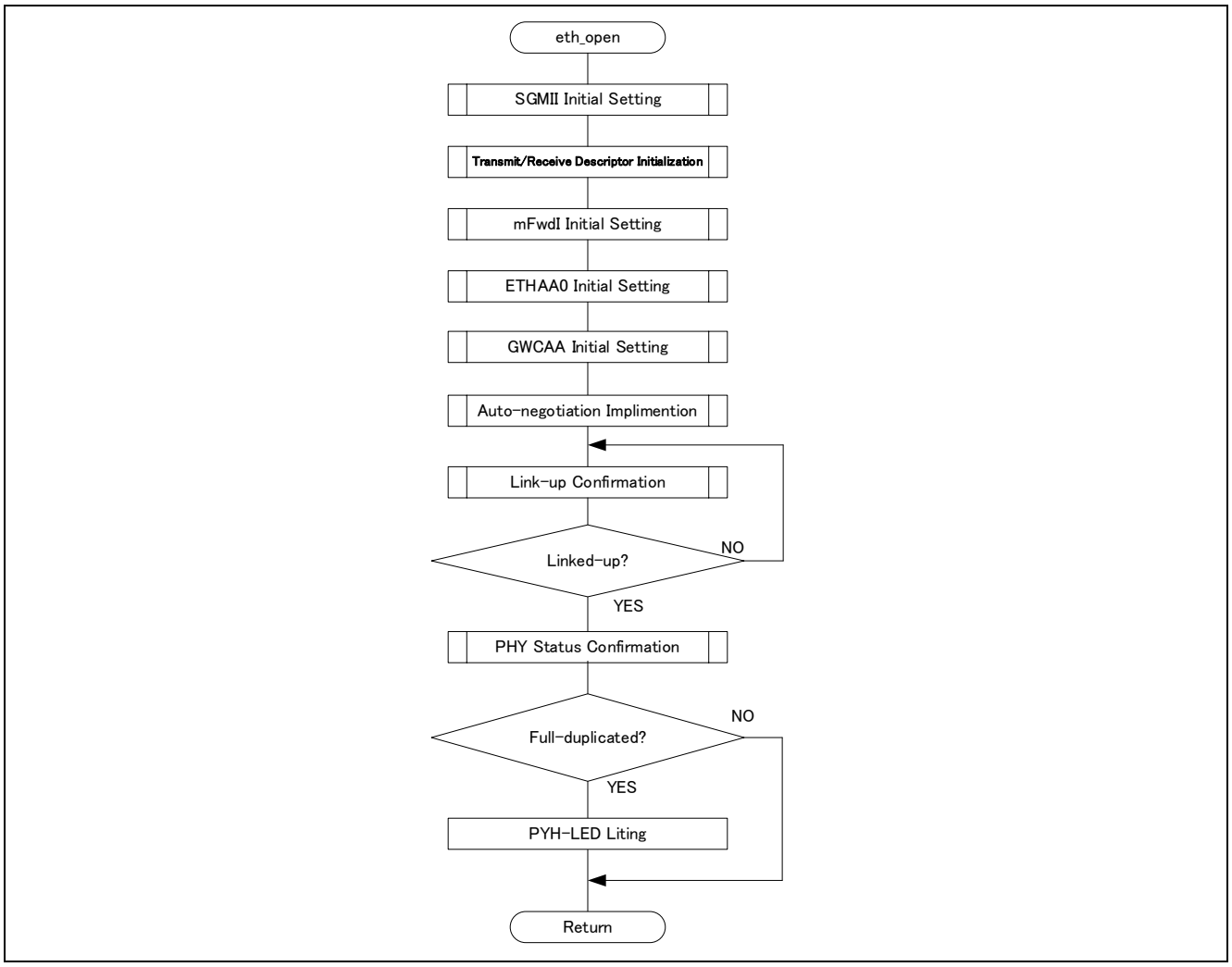

Figure 1-31 Ether Communication Strat Module Flowchart

1.4.9 Ether Communication End

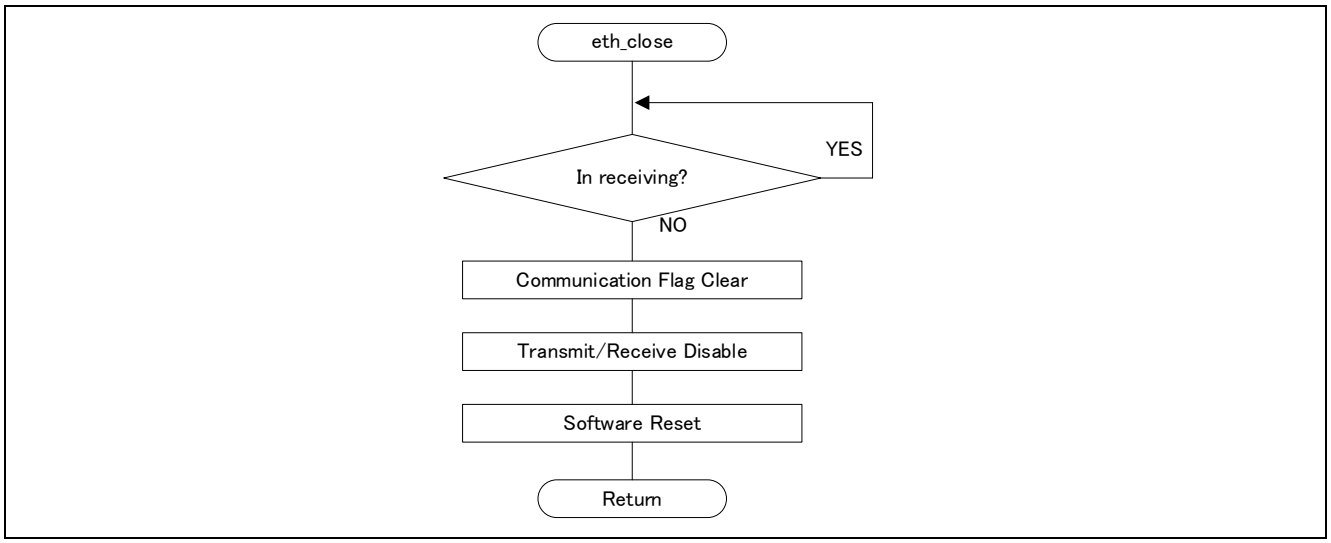

Figure 1-32 Ether Communication End Module Flowchart

1.4.10 ETHAA0 Initial Setting

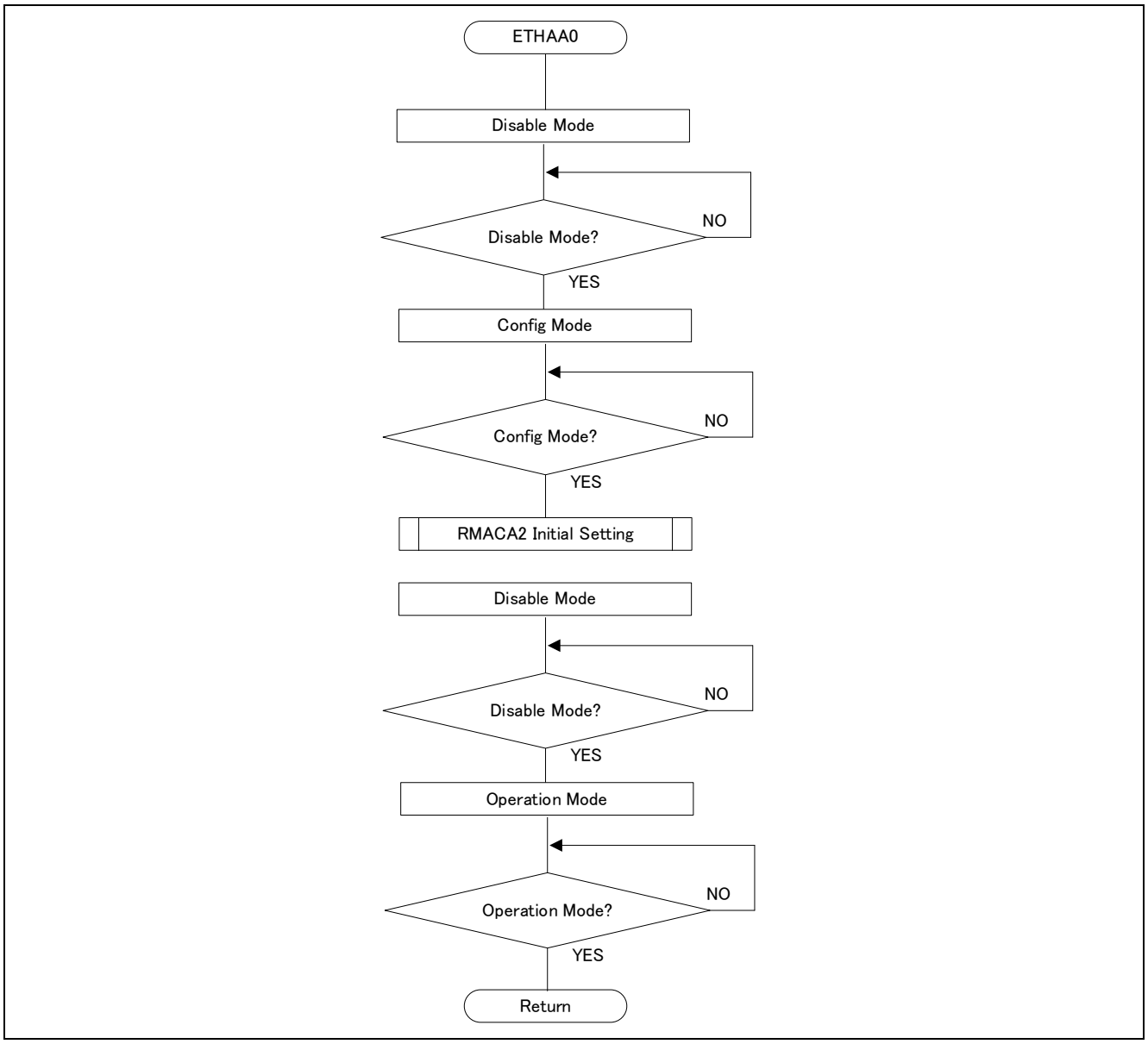

Figure 1-33 ETHAA0 Initial Setting Module Flowchart

1.4.11 GWCAA Initial Setting

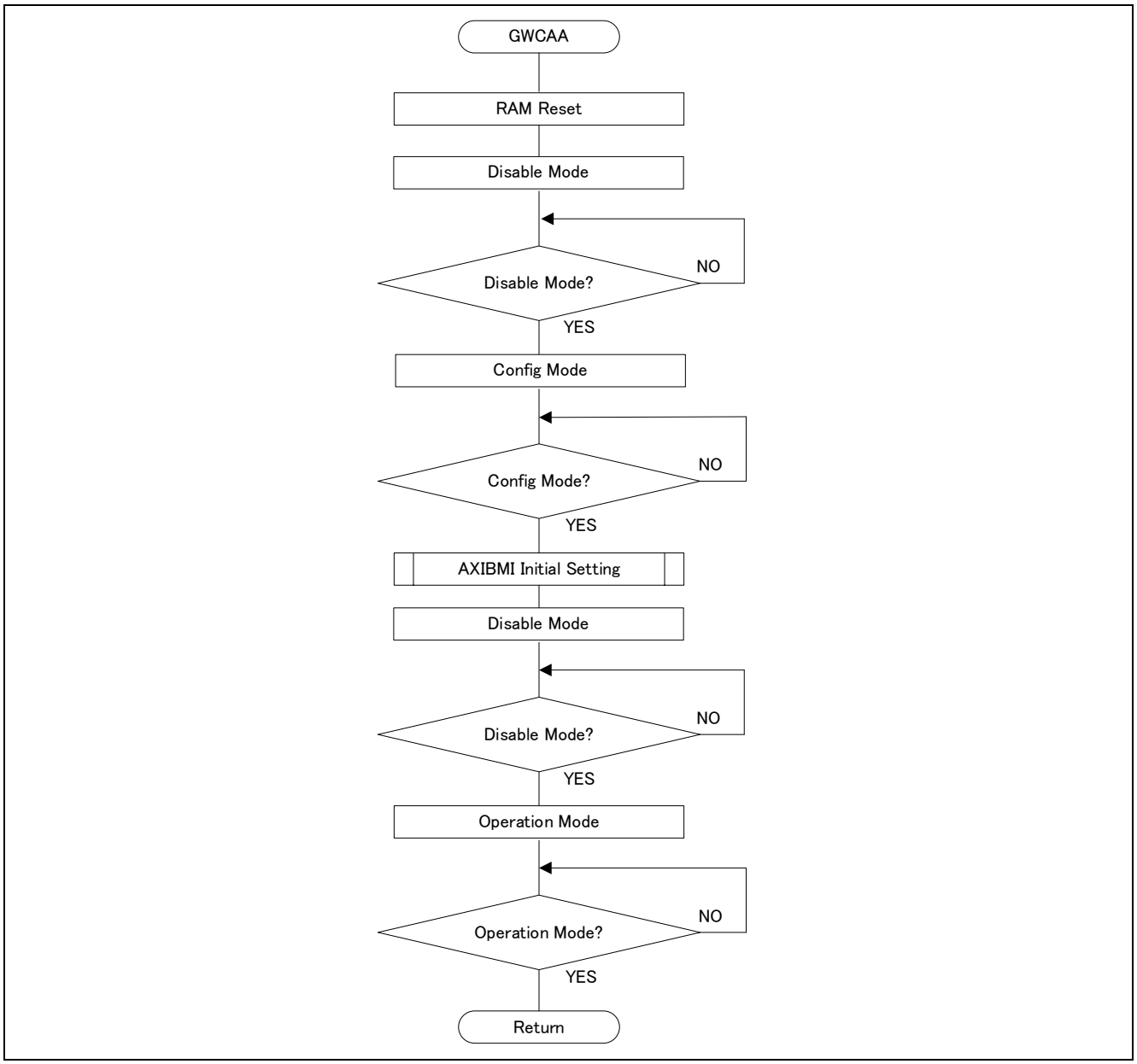

Figure 1-34 GWCAA Initial Setting Module Flowchart

1.4.12 AXIBMI2 Initial Setting

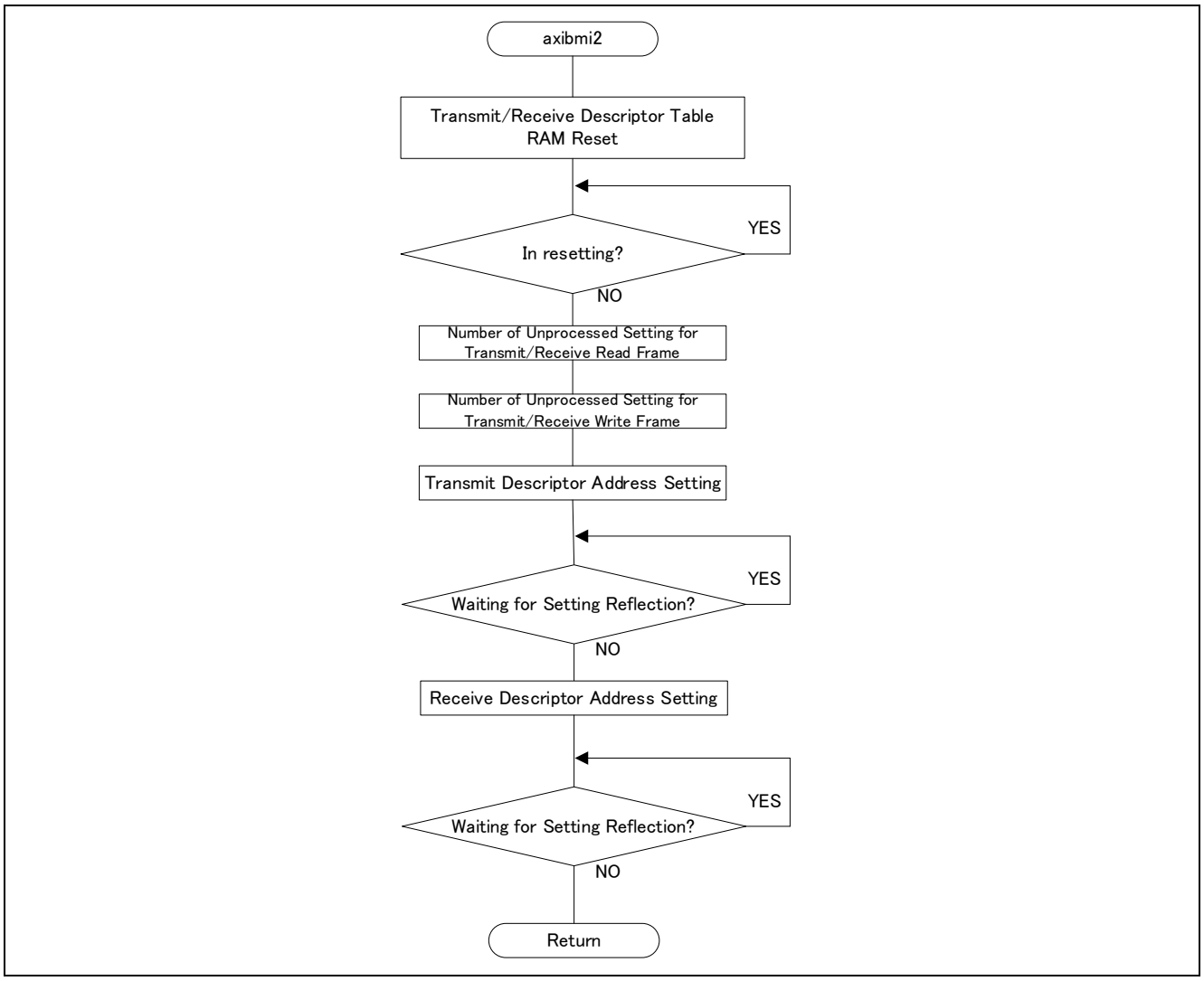

Figure 1-35 AXIBMI2 Initial Setting Module Flowchart

1.4.13 RMACA2 Initial Setting

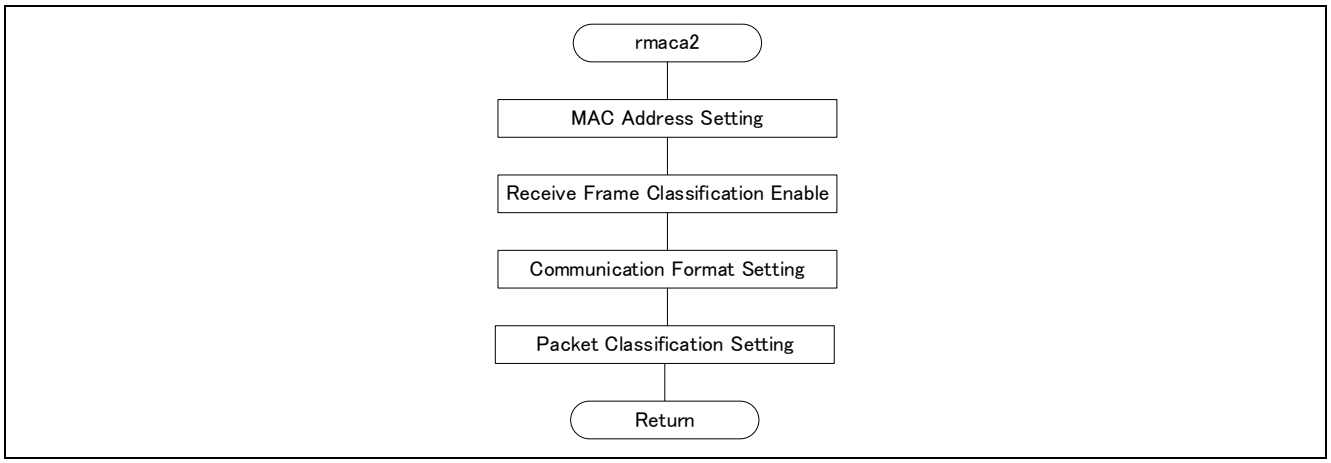

Figure 1-36 RMACA2 Initial Setting Module Flowchart

1.4.14 SGMII Initial Setting

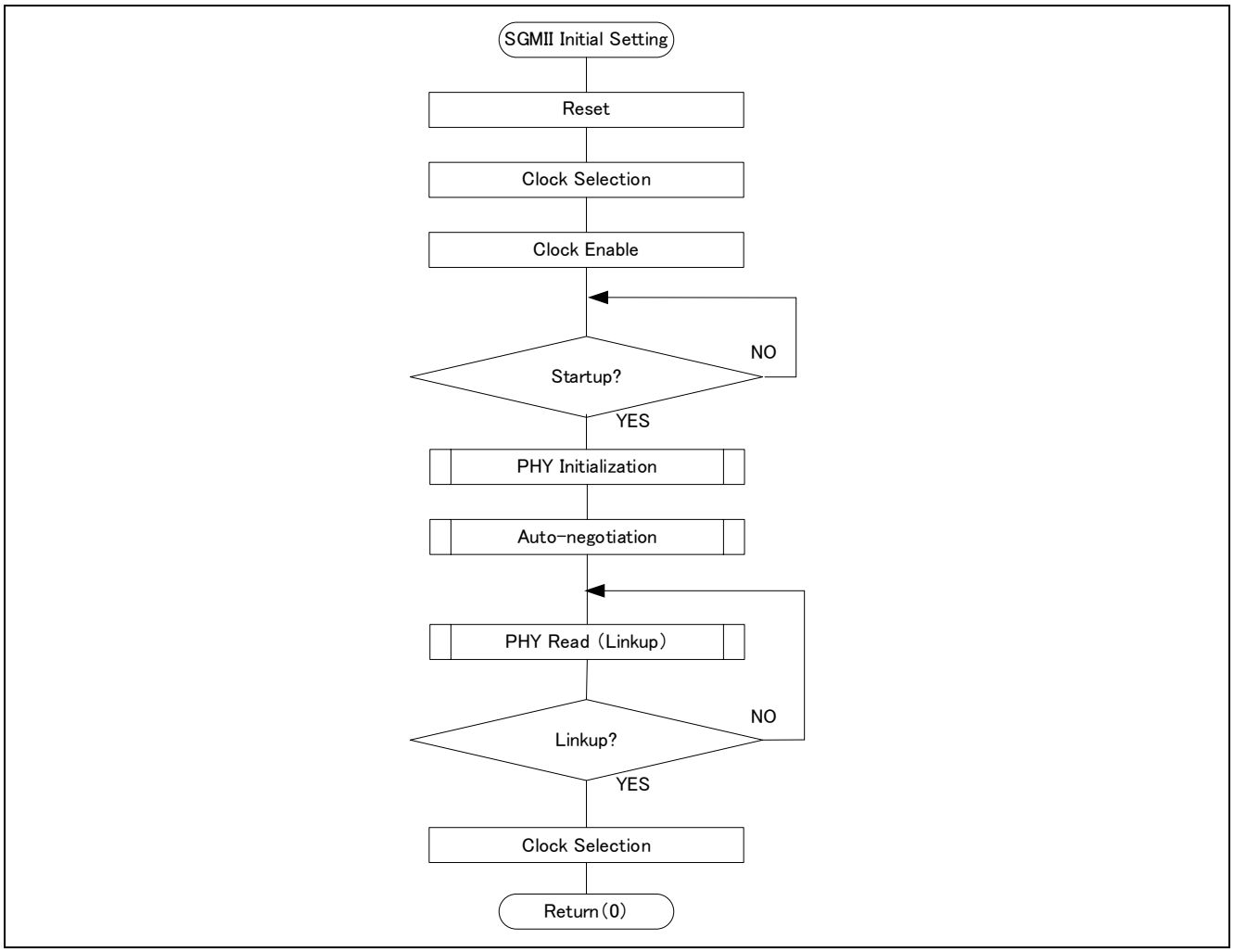

Figure 1-37 SGMII Initial Setting Module Flowchart

1.4.15 MFWDA Initialization

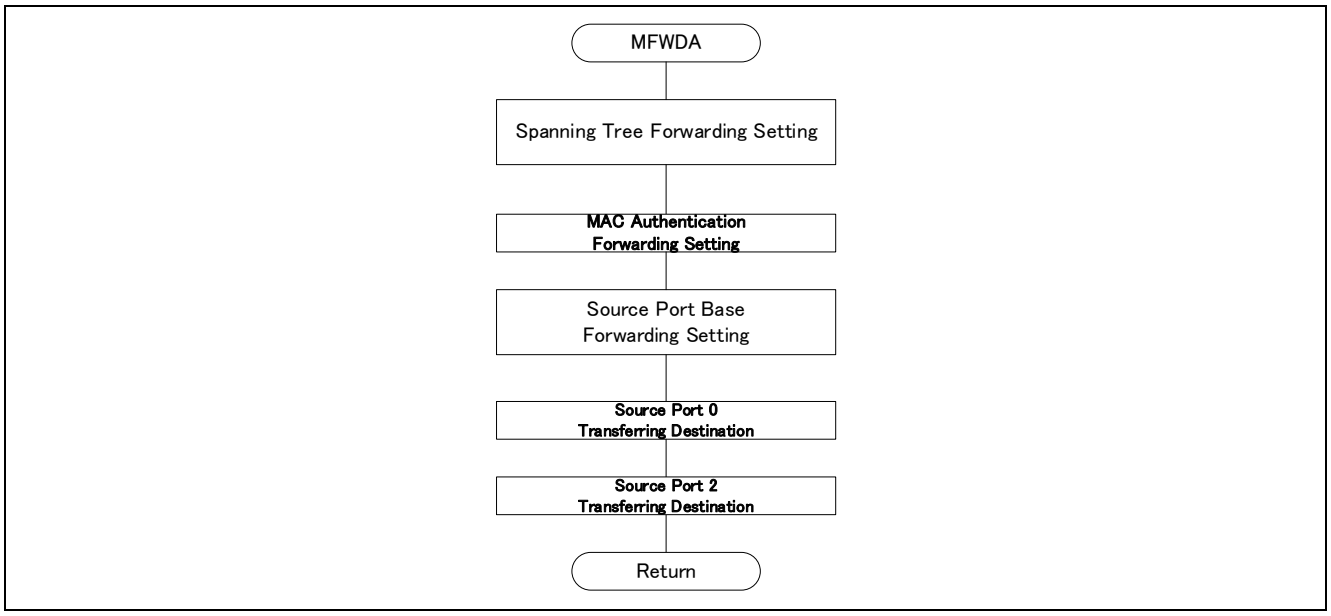

Figure 1-38 MFWDA Initialization Module Flowchart

1.4.16 Transmit/Receive Descriptor Initialization

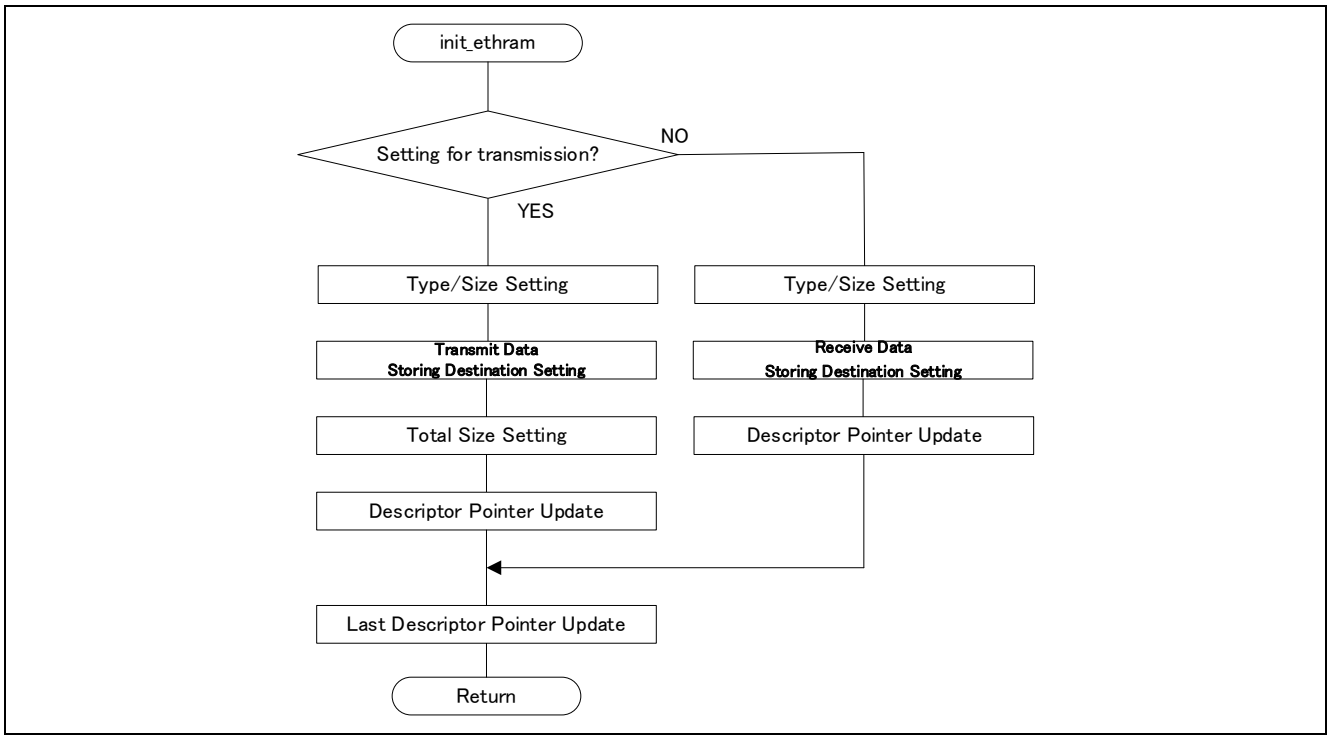

Figure 1-39 Transmit/Receive Descriptor Initialization Module Flowchart

1.4.17 Data Transmission

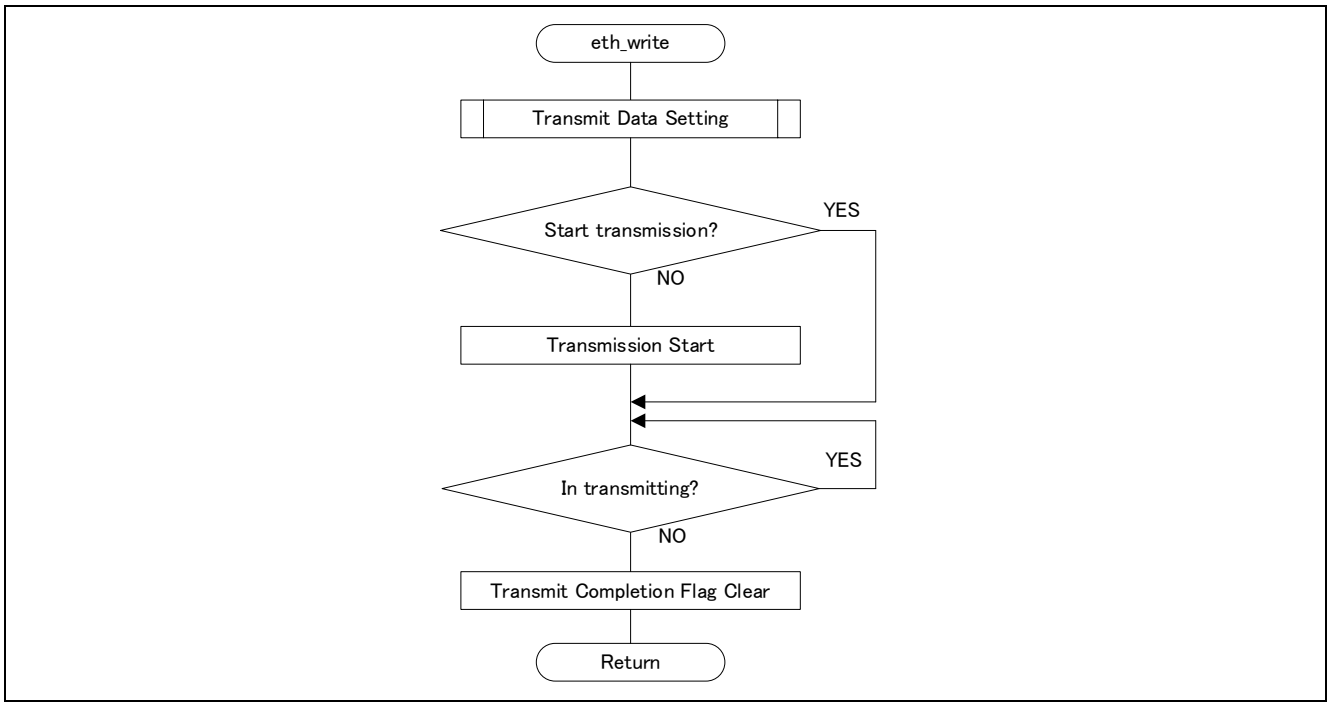

Figure 1-40 Data Transmit Module Flowchart

1.4.18 Data Reception

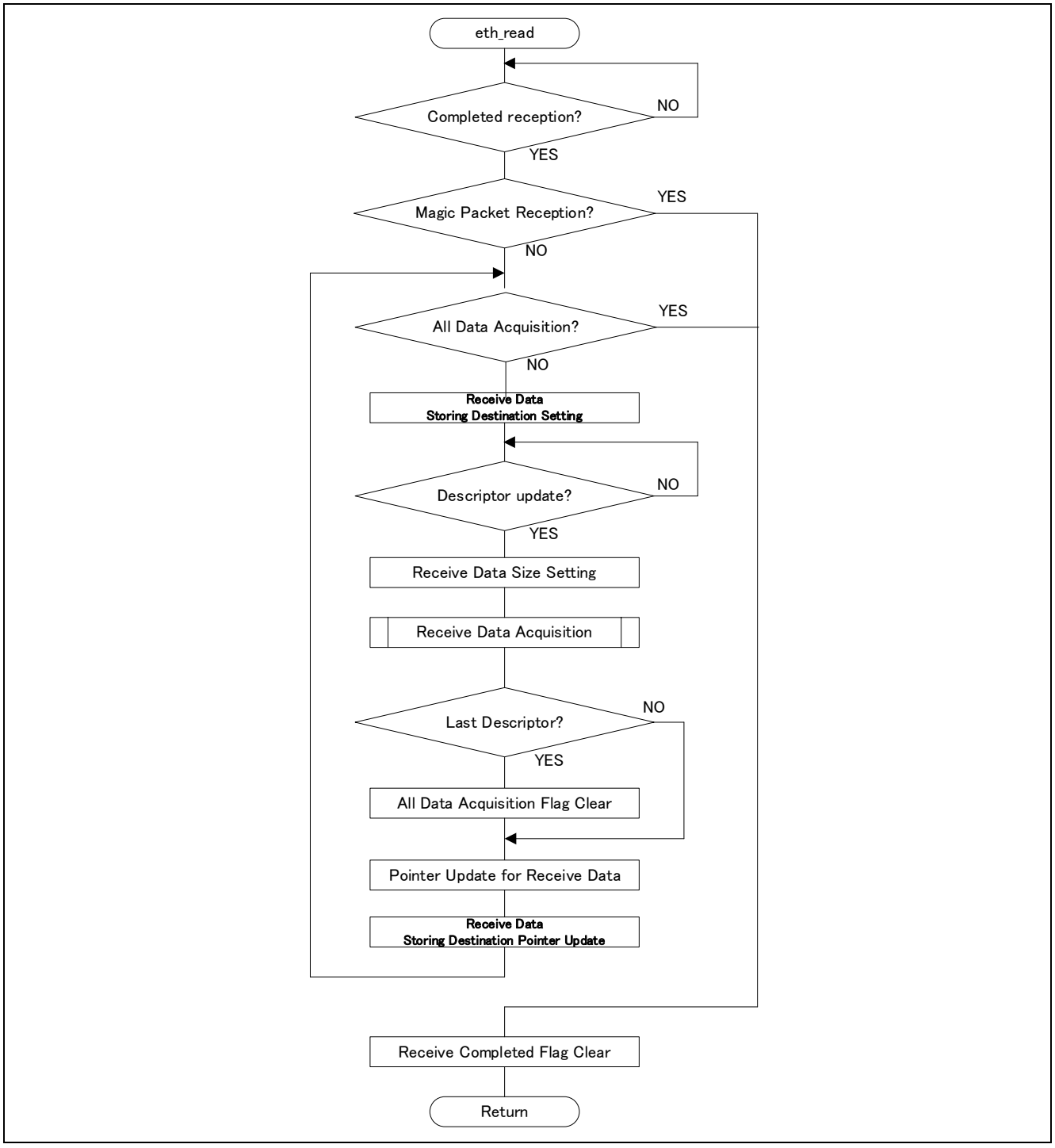

Figure 1-41 Data Receive Module Flowchart

1.4.19 Transmit Data Setting

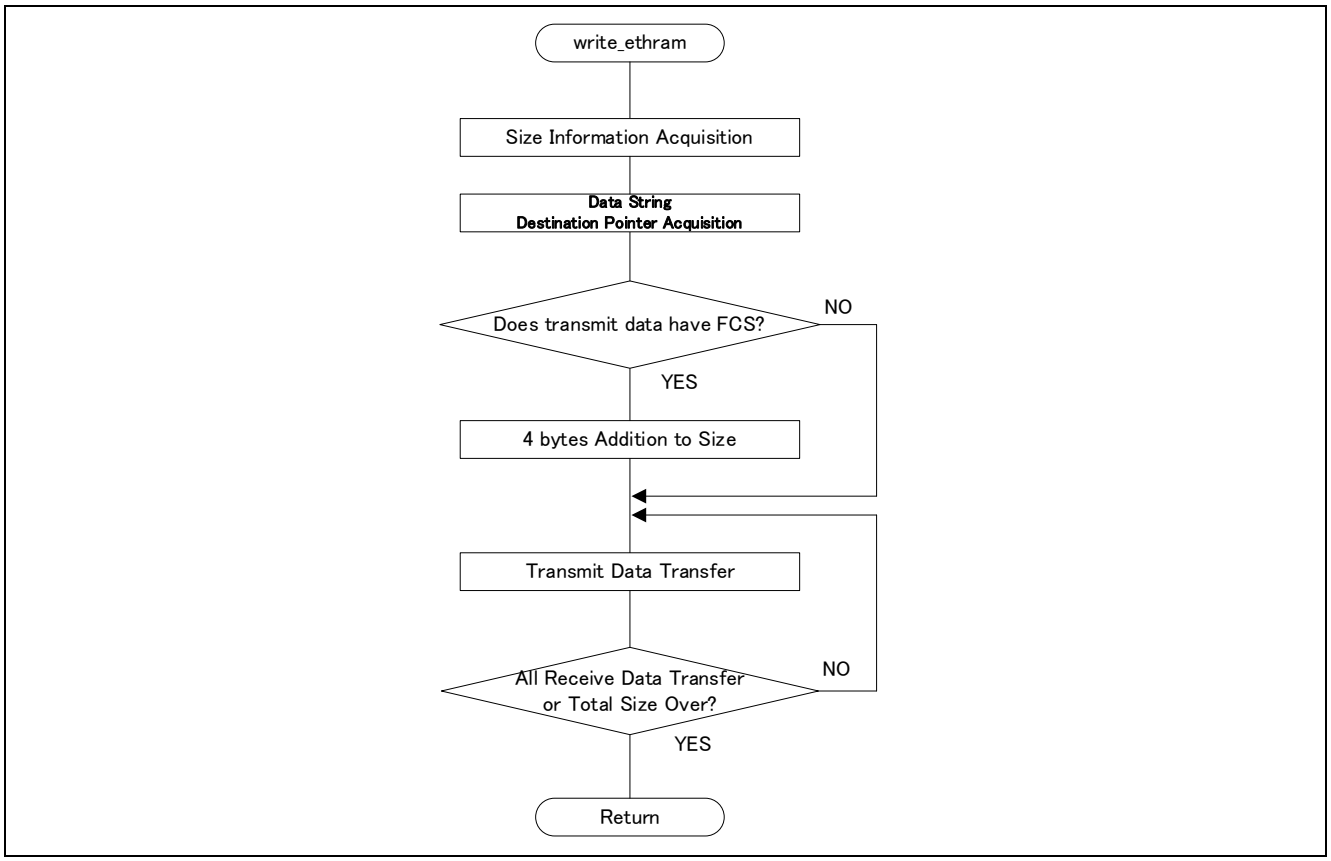

Figure 1-42 Transmit Data Setting Module Flowchart

1.4.20 Receive Data Acquisition

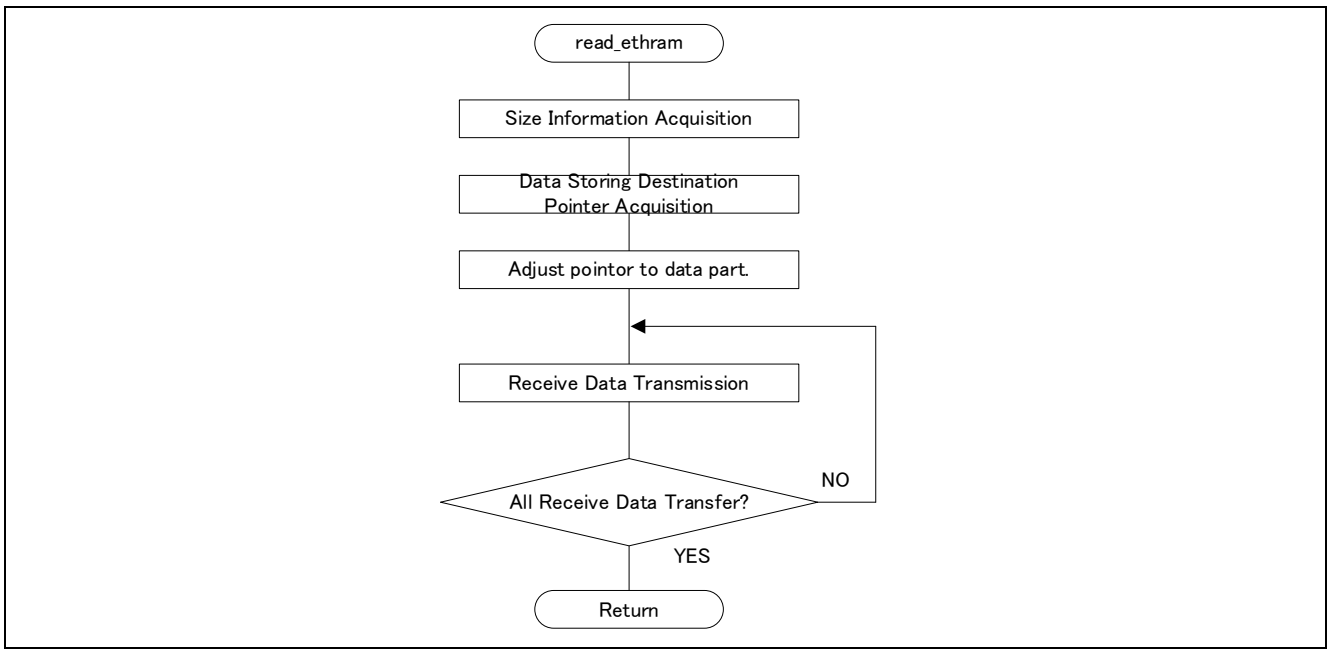

Figure 1-43 Receive Data Acquisition Module Flowchart

1.4.21 PHY Initialization

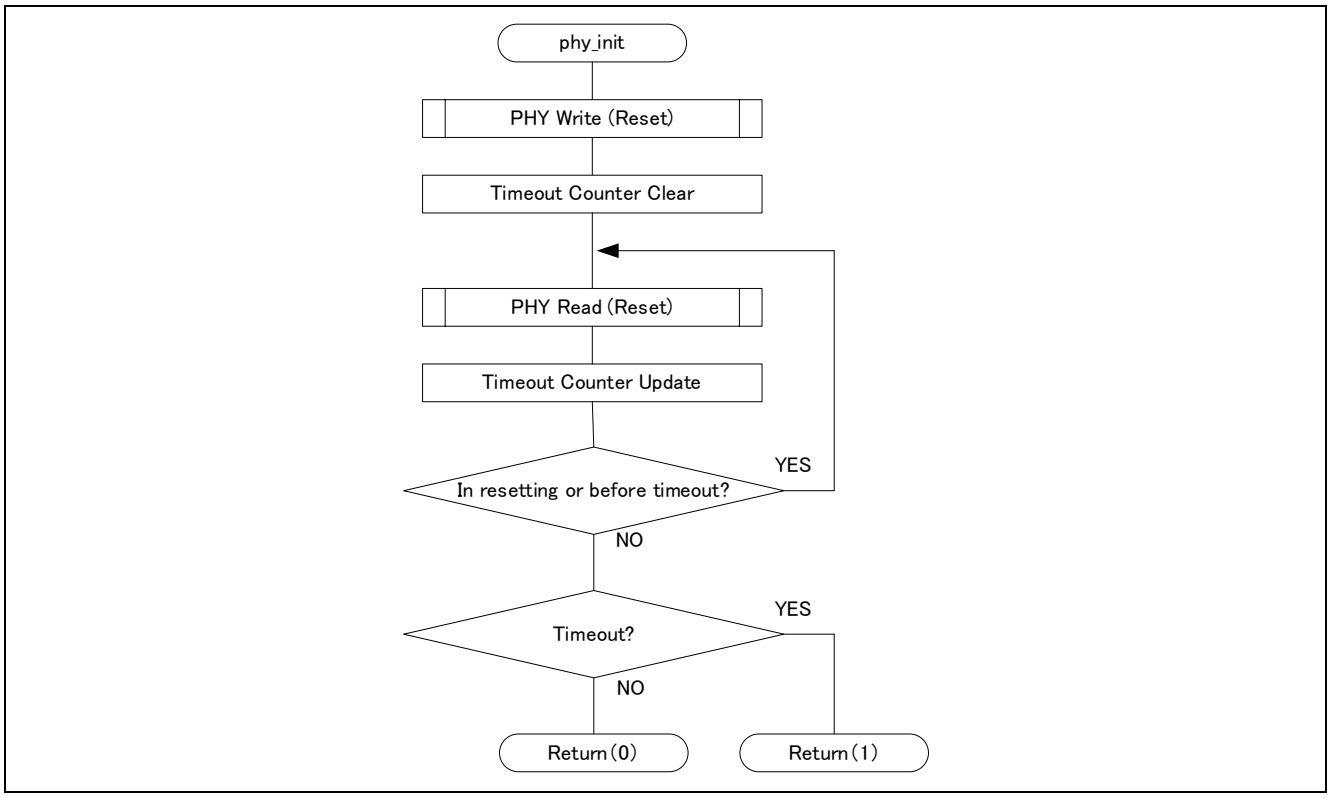

Figure 1-44 PHY Initialization Module Flowchart

1.4.22 Auto-negotiation

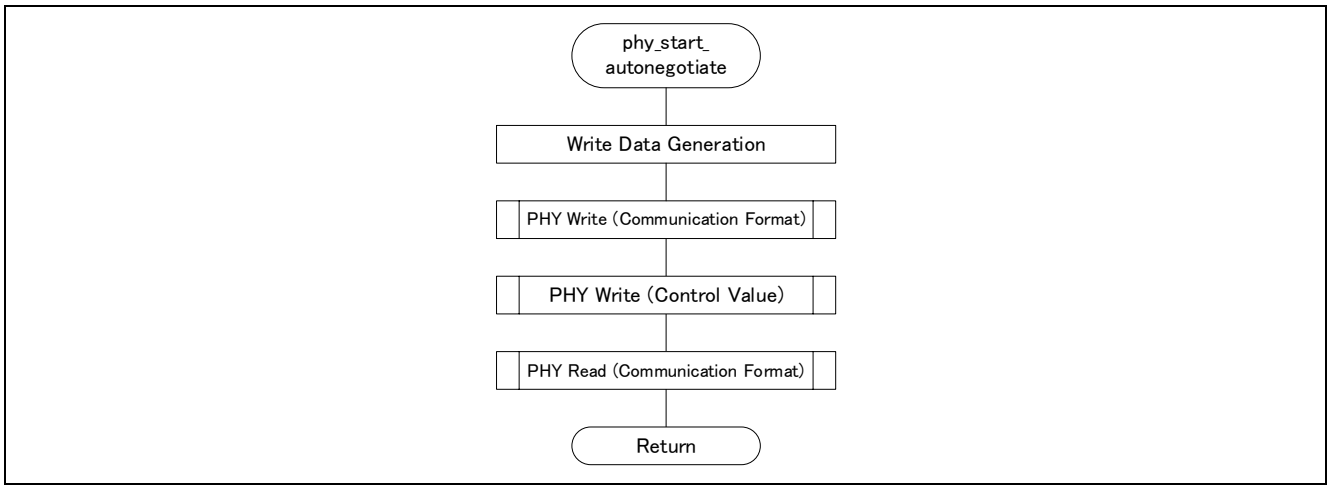

Figure 1-45 Auto-negotiation Module Flowchart

1.4.23 PHY Write

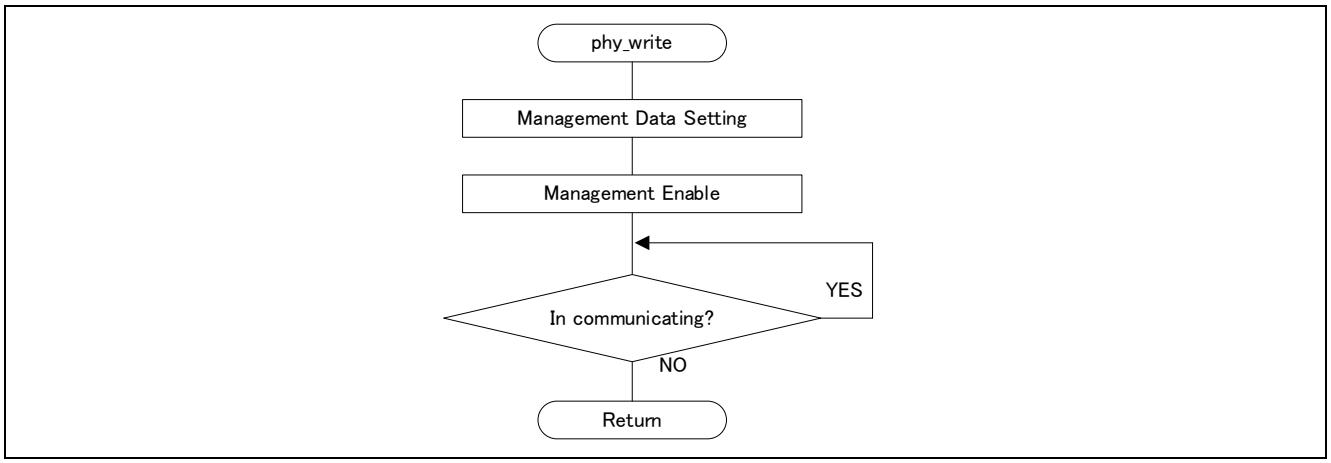

Figure 1-46 PHY Write Module Flowchart

1.4.24 PHY Read

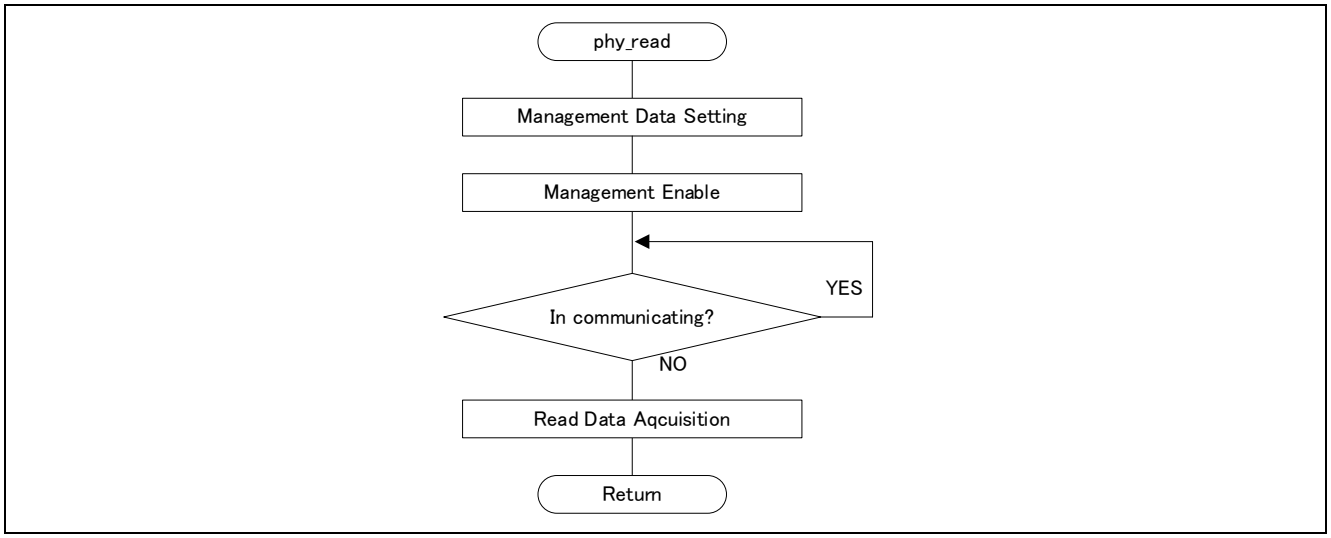

Figure 1-47 PHY Read Module Flowchart

1.4.25 Clause45 Format Write

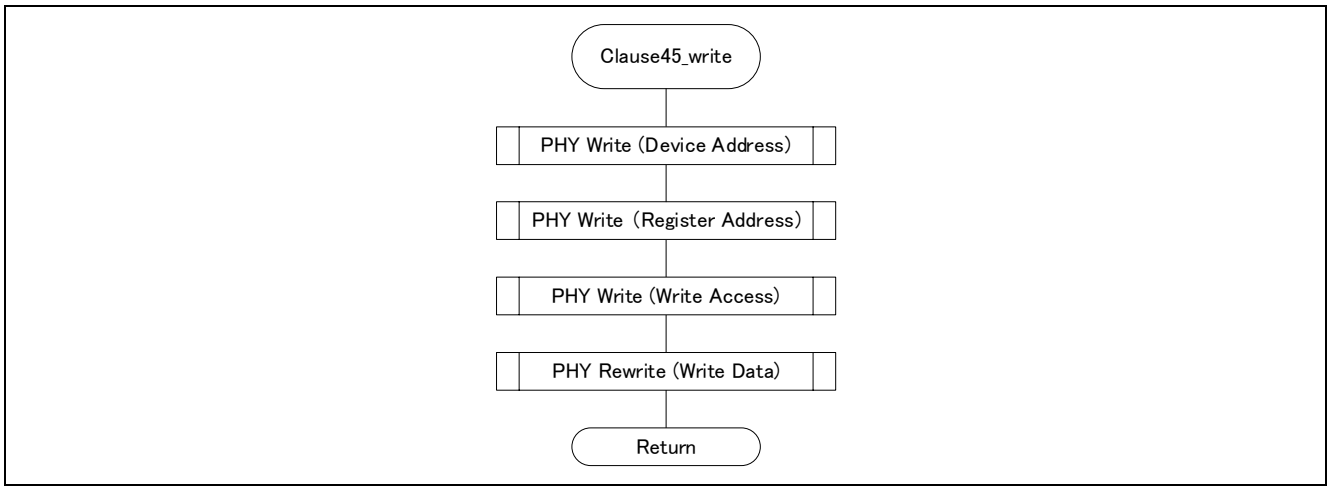

Figure 1-48 Clause45 Format Write Module Flowchart

1.4.26 Clause45 Format Read

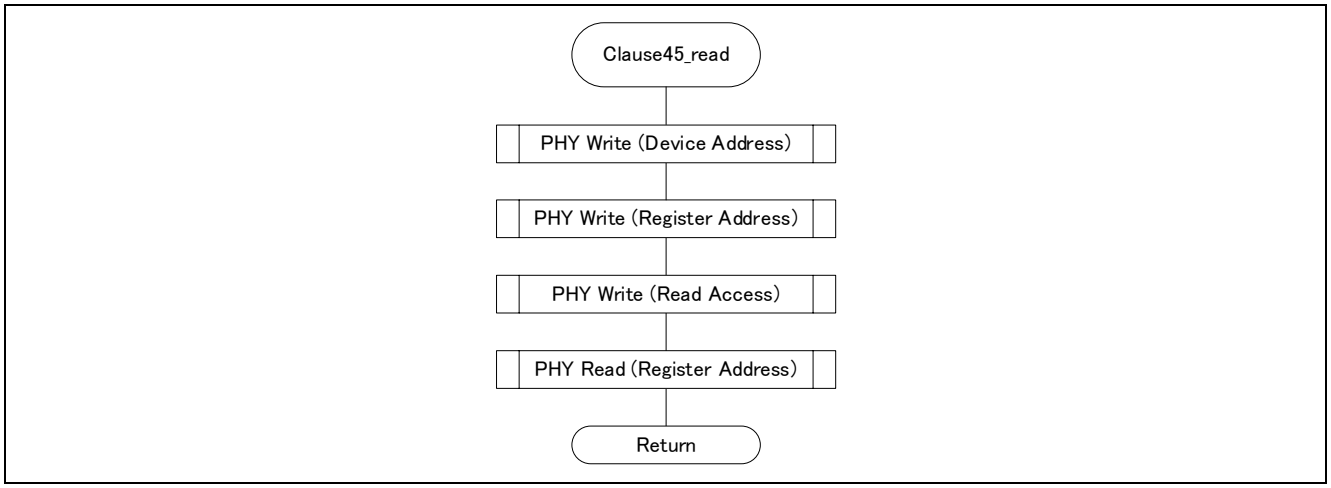

Figure 1-49 Clause45 Format Read Module Flowchart

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Revision History

Rev.	Data	Description	
		Page	Summary
1.00	2024.1.11	-	First Issue

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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