RH850/U2B Group

R01AN6330EJ0100
Rev.1.00

Gateway Procedure Application Note

Summary

This document applies to the RH850 series. This document and the program are intended to promote understanding of the installed functions in the RH850/U2B, and it is not intended for mass production. design. It also does not reflect the latest manuals, errata, technical updates, and development environment updates. When using the corresponding function, please treat this program as a reference, and use the latest documents and development environment at your own risk. RSCFDnCFD is omitted from the register name in the text.

Target Device

- • RH850/U2Bx
-

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1. Gateway Function

The functions available when using CAN gateway are shown below. For details of each processing, refer to the following chapters.

- Gateway operation
- Transmit abort function
- Interval transmission function gateway operation
- Interrupt processing of transmit/receive FIFO buffer (gateway mode)

2. Gateway Operation

When the transmit/receive FIFO buffer is set to gateway mode, the received message can be sent from any channel without going through the CPU.

When the transmit/receive FIFO buffer with the CFM [1: 0] bit of the CFCCk register set to "10_B " (gateway mode) is selected with the GAFLP1j register, the messages that have passed the receive rule filter processing are stored in the specified transmit/receive FIFO buffer and are automatically transmitted from the buffer.

The transmit/receive FIFO buffer is transmitted in order from the first stored message. In addition, priority determination is performed only for the next message to be transmitted in the transmit/receive FIFO buffer.

In gateway mode, you cannot read or write to the transmit/receive FIFO buffer, but you can check the message transmitted from the transmit/receive FIFO buffer in gateway mode by using the mirror function.

For the configuration settings for using the transmit/receive FIFO buffer in gateway mode, refer to "CAN Configuration Application Note".

Figure 2-1 shows an example of the operation of the transmit/receive FIFO buffer in gateway mode.

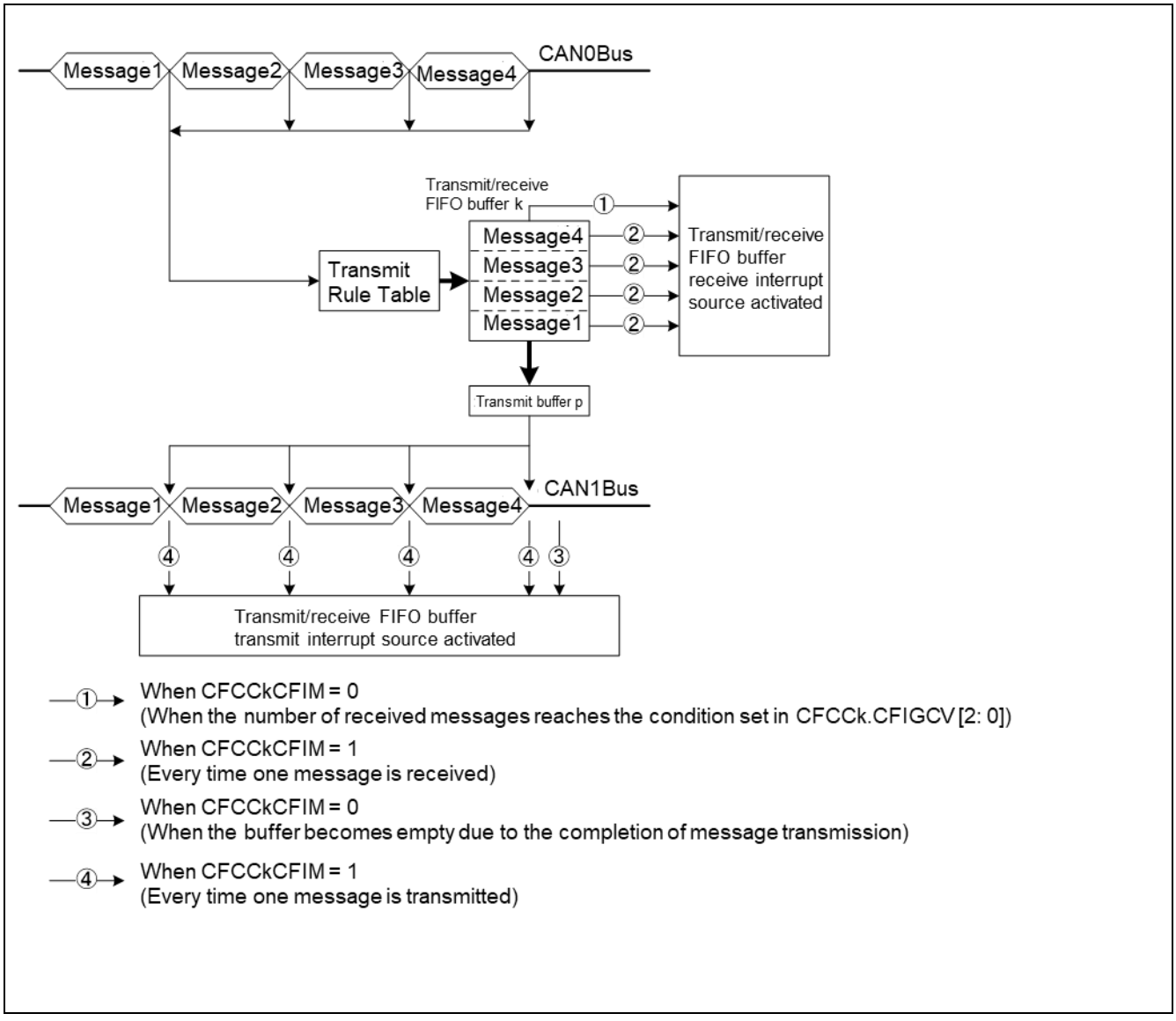
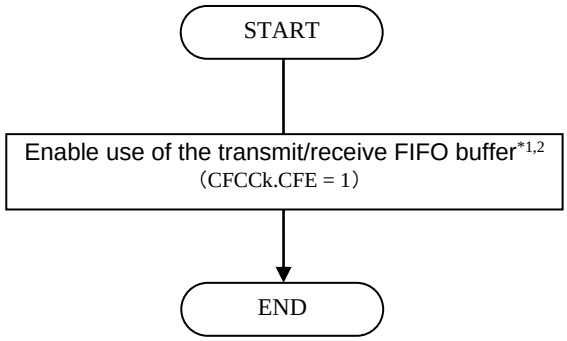


Figure 2-1 Operation Example of Transmit/Receive FIFO Buffer (Gateway Mode)

2.1 Gateway Procedure in Transmit/Receive FIFO Buffer

In gateway mode, messages are transmitted and received automatically within the RS-CANFD module, thus there is no need to perform the transmit/receive processing with the program.

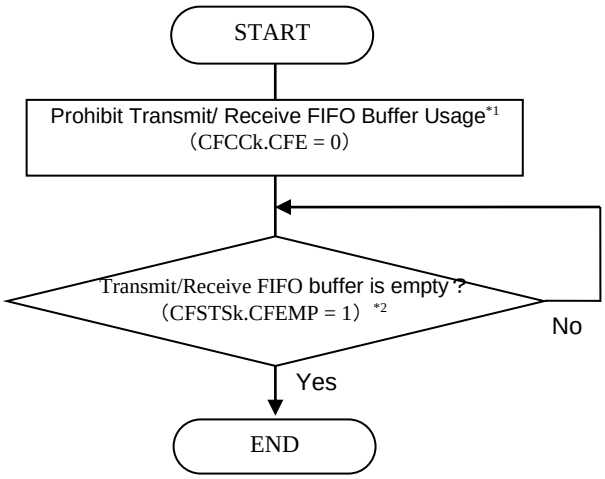
Figures 2-2 and 2-3 show the procedure for enabling and prohibiting the transmit/receive FIFO buffer.



【Note】 1. In transmit mode or gateway mode, rewrite the transmit/receive FIFO buffer usage enabling settings in channel communication mode or channel standby mode.

2. Make the configuration settings for using the transmit/receive FIFO buffer before enabling the transmit/receive FIFO buffer.

Figure 2-2 Procedure for Enabling Transmit/Receive FIFO Buffer



【Note】 1. In transmit mode or gateway mode, rewrite the transmit/receive FIFO buffer usage disabling settings in channel communication mode or channel standby mode.

2. When the transmit/receive FIFO buffer is disabled, the transmit/receive FIFO buffer empty status flag is set at the following timing.

・If a message in the transmit/receive FIFO buffer is not being transmitted and is not determined for the next transmission, it will be empty immediately.

・If the message in the transmit/receive FIFO buffer is already being transmitted or is determined to be the next transmission, it will be empty after transmission completion, CAN bus error detection, or arbitration lost.

3. Even if the use of the transmit/receive FIFO buffer is prohibited with the transmit/receive FIFO interrupt request (CFSTSk.CFTXIF = 1 or CFSTSk.CFRXIF = 1), the transmit/receive FIFO interrupt request is not automatically canceled (CFSTSk.CFTXIF = 0 or CFSTSk.CFRXIF = 0). To cancel the receive FIFO interrupt request, set it with the program.

Figure 2-3 Procedure for Prohibiting Transmit/Receive FIFO Buffer Usage

2.2 Transmit Abort Function

By disabling the transmit/receive FIFO buffer (CFCCk.CFE = 0), all messages in the transmit/receive FIFO buffer are lost, and the transmit/receive FIFO buffer empty status flag in thetransmit/receive FIFO buffer status register is set to "1" (CFSTSk.CFEMP = 1). "1" is set in the transmit/receive FIFO buffer empty status flag at the following timing. Note that no message is stored in the transmit/receive FIFO buffer when the use of the transmit/receive FIFO buffer is prohibited.

- If a message in the transmit/receive FIFO buffer is not being transmitted and is not determined for the next transmission, it will be empty immediately.
- If the message in the transmit/receive FIFO buffer is already being transmitted or is determined to be the next transmission, it will be empty after transmission completion, CAN bus error detection, or arbitration lost.

No interrupt is generated when the transmit abort of the transmit/receive FIFO buffer is completed. However, if aborted during transmission, a CANm transmit/receive FIFO transmission completion interrupt may occur due to transmission completion. For details, refer to "CAN Transmission Procedure Application Note".

For the transmit abort procedure of the transmit/receive FIFO buffer, refer to "Figure 2-3 Procedure for Prohibiting Transmit/Receive FIFO Buffer ".

2.3 Interval Transmission Function

To transmit messages continuously from the same transmit/receive FIFO buffer that is set to transmit mode or gateway mode, message transmission interval time can be set.

After thetransmit/receive FIFO buffer is enabled (CFCCk.CFE = 1) and the first message is successfully sent from the transmit/receive FIFO buffer, the interval timer starts counting (after the 7th bit of the CAN protocol EOF). After that, when the interval time elapses, the following message is sent and the interval timer is reset. The timing at which the interval timer stops is shown below.

- When the use of the transmit/receive FIFO buffer is prohibited (CFCCk.CFE = 0)
- When transitioning to channel reset mode

Table 2-1 shows the count source of the interval timer and the calculation formula of the interval timer, Figure 2-4 shows the block diagram of the interval timer, and Figure 2-5 shows the operation example of the interval timer.

Table 2-1 Interval Timer Source and Calculation Formula

CFCCk		Counter Source	Interval Timer Calculation Formula
CFITR	CFITSS		
0	0	Clock obtained by dividing pclk/2 by the value of the ITRCP [15: 0] bit of the GCFG register	$1/f_{PBA} \times 2 \times M \times N$
1	0	Clock obtained by dividing pclk/2 by the value of the ITRCP [15: 0] bits of the GCFG register x 10.	$1/f_{PBA} \times 2 \times M \times 10 \times N$
-	1	Normal CANm bit time clock	$1/f_{CANBIT} \times N$

【Note】 M: Divided value of the clock source of the interval timer for FIFO (set value of GCFG.ITRCP [15: 0])
N: Message transmission interval (set value of CFCCk.CFITT [7: 0])
f_{PBA} : pclk frequency
f_{CANBIT} : Normal CANm bit time clock frequency

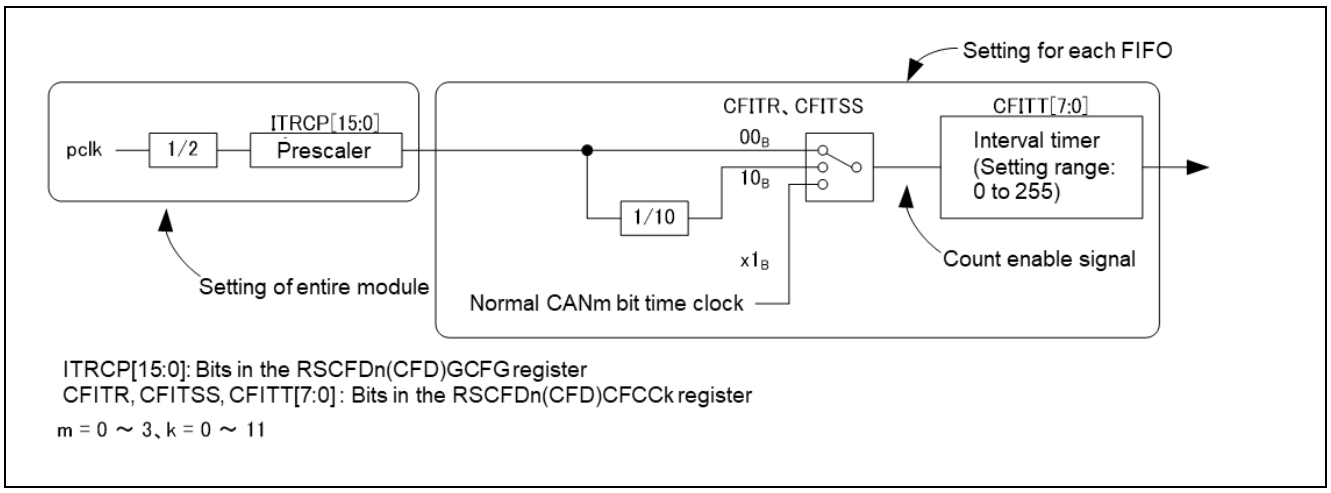
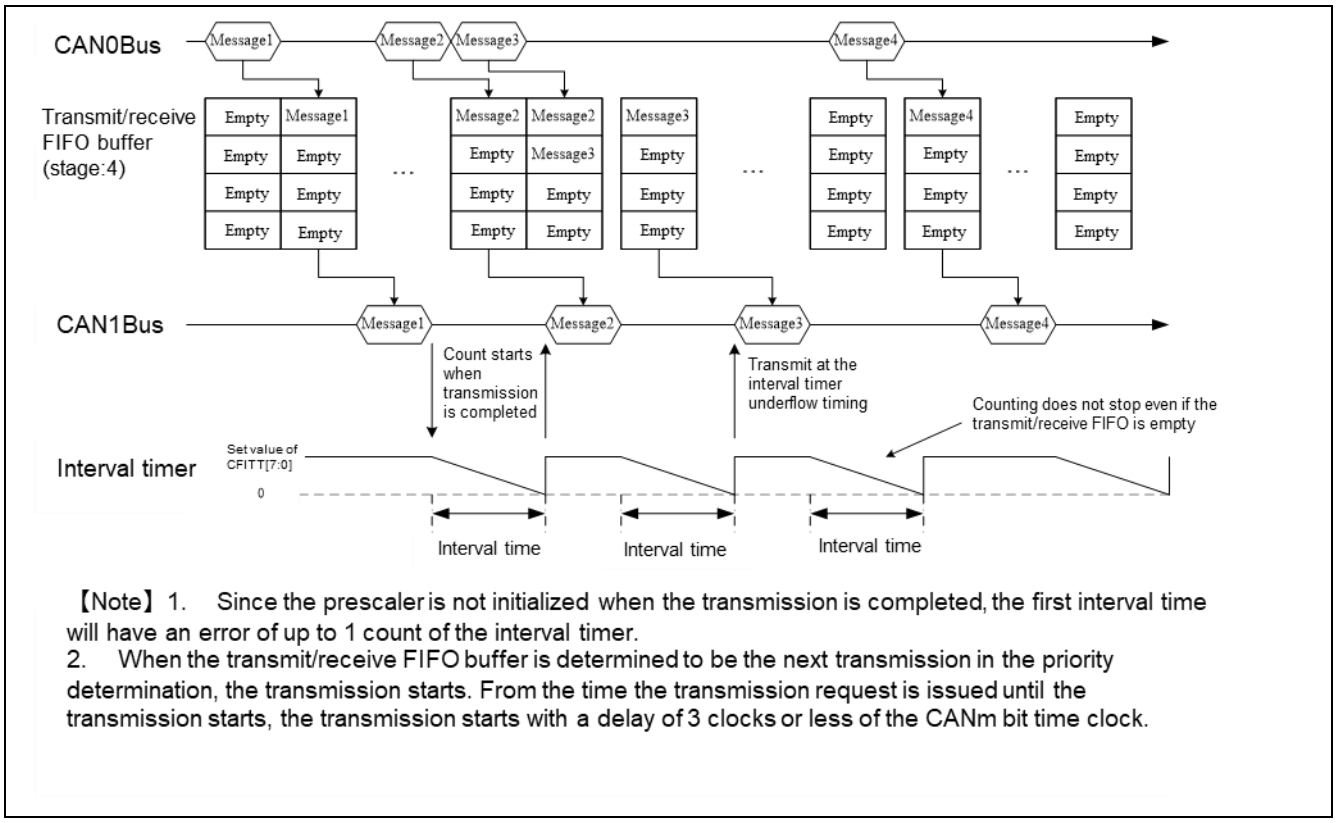


Figure 2-4 Block Diagram of Interval Timer



【Note】1. Since the prescaler is not initialized when the transmission is completed, the first interval time will have an error of up to 1 count of the interval timer.
2. When the transmit/receive FIFO buffer is determined to be the next transmission in the priority determination, the transmission starts. From the time the transmission request is issued until the transmission starts, the transmission starts with a delay of 3 clocks or less of the CANm bit time clock.

Figure 2-5 Interval Transmission Operation Example (Gateway Mode)

2.4 Transmit/Receive FIFO Buffer Interrupt Processing (Gatewat Mode)

2.4.1 Transmit/Receive FIFO Buffer Interrupt Processing

If the transmit/receive FIFO receive interrupt is enabled, the transmit/receive FIFO receive interrupt occurs when the condition selected by the CFIM bit of the CFCCk register is satisfied.

Even if the use of the transmit/receive FIFO buffer is set to be prohibited (CFCCk.CFE=0) while the transmit/receive FIFO receive interrupt request is being generated (CFSTSk.CFRXIF=1), the transmit / receive FIFO receive interrupt request is not automatically canceled (CFSTSk.CFRXIF=0). When canceling the transmit/receive FIFO receive interrupt request, please set it with the program.

Whether to enable or disable the transmit/receive FIFO receive interrupt can be set for each transmit/receive FIFO buffer by the CFRXIE bit of the CFCCk register.

The transmit/receive FIFO receive interrupt request generation condition can be selected for each transmit/receive FIFO buffer by the CFIM bit and CFIGCV bit of the CFCCk register.

Table 2-2 summarizes the sources of transmit/receive FIFO receive interrupt in gateway mode.

Table 2-2 Reception Interrupt Source of Transmit/Receive FIFO

CFCCk		Ocurrance condition of FIFO receive interrupt request	How to clear the interrupt request
CFIM	CFIGCV		
1	-	Every time one message is received	Write "0" to the CFRXIF bit of the CFSTSk register
0	000※	When a message is stored up to 1/8 in the FIFO buffer	
	001	When a message is stored up to 2/8 in the FIFO buffer	
	010※	When a message is stored up to 3/8 in the FIFO buffer	
	011	When a message is stored up to 4/8 in the FIFO buffer	
	100※	When a message is stored up to 5/8 in the FIFO buffer	
	101	When a message is stored up to 6/8 in the FIFO buffer	
	110※	When a message is stored up to 7/8 in the FIFO buffer	
	111	When the FIFO buffer is full	

* Set the number of transmit/receive FIFO buffers to 4 messages
If set to (CFCCk.CFDC [2: 0] = 001), selection is prohibited.

2.4.2 Transmit/Receive FIFO Buffer Full Interrupt

If the transmit / receive FIFO buffer full interrupt is enabled, the transmit / receive FIFO buffer full interrupt occurs when the transmit / receive FIFO buffer becomes full state.[*1]

Transmit/Receive FIFO Buffer Full interrupt enable/disable can be set for each transmit/receive FIFO buffer by the CFFIE bit of the CFCCEk register.

The transmit/receive FIFO buffer full interrupt is expected to be used in the following cases.

1. Interrupt request at the number of stages set by the CFIGCV bit of the transmit / receive FIFO buffer
2. Interrupt request when the transmit/receive FIFO buffer is full state.

These interrupt requests make facilitate data management in the transmit/receive FIFO.

2.4.3 Transmit/Receive FIFO One-frame Reception Completion Inetrrupt

If the transmit/receive FIFO one-frame interrupt is enabled, the transmit/receive FIFO one-frame interrupt occurs when the transmit/receive FIFO buffer receives the one-frame.[*1]

Transmit/Receive FIFO one-frame reception interrupt enable/disable can be set for each transmit/receive FIFO buffer by the CFOFRXIE bit of the CFCCEk register.

2.4.4 Trasmit/Receiev FIFO Trasmition Interrupt Processing

If the transmit/receive FIFO transmition interrupt is enabled, the transmit/receive FIFO transmit interrupt occurs when the condition selected by the CFIM bit of the CFCCk register is satisfied.

Even if the use of the transmit/receive FIFO buffer is set to be prohibited (CFCCk.CFE=0) while the transmit/receive FIFO receive interrupt request is being generated (CFSTSk.CFRXIF=1), the transmit/receive FIFO transmition interrupt request is not automatically canceled (CFSTSk.CFRXIF=0). When canceling the transmit/receive FIFO transmition interrupt request, please set it with the program.

Whether to enable or disable the transmit/receive FIFO transmition interrupt can be set for each transmit/receive FIFO buffer by the CFRXIE bit of the CFCCk register.

The transmit/receive FIFO transmition interrupt request generation condition can be selected for each transmit/receive FIFO buffer by the CFIM bit and CFIGCV bit of the CFCCk register.

Table 2-3 summarizes the sources of transmit/receive FIFO transmition interrupt in gateway mode.

Tbale 2-3 Trasmit/Receive FIFO Transmision Inetrrupt Source

CFIM	Ocurrance condition of FIFO transmit interrupt request	How to clear the interrupt request
1	Every time one message is transmitted	Write "0" to the CFTXI bit of the CFSTSk register
0	When the buffer becomes empty due to the completion of message transmission	

2.4.5 Transmit/Receive FIFO One-frame Transmission Interrupt Processing

If the transmit/receive FIFO one-frame transmittion interrupt is enabled, the transmit/receive FIFO one-frame interrupt occurs when the transmit/receive FIFO buffer receives the one-frame.[*1]

Transmit/Receive FIFO one-frame transmition interrupt enable/disable can be set for each transmit/receive FIFO buffer by the CFOFTXIE bit of the CFCCEk register.

2.4.6 グローバルエラー割り込み処理

2.4.7 Global Error Interrupt Processing

By enabling the FIFO message lost interrupt, a global error interrupt is generated when the message lost in the transmit/receive FIFO buffer is detected. Whether to enable or disable the FIFO message lost interrupt can be set in common for the entire module with the MEIE bit of the GCTR register.

Table 2-4 summarizes the sources of global error interrupt.

Tbale 2-4 Global Error Interrupt Source

Occurrence condition of global error interrrup request	How to clear the interrupt request
When a message lost in the transmit/receive FIFO buffer is detected	Write "0" to the CFMLT bit of the CFSTSk register*1

*1 Multiple interrupt factors can be selected for global error interrupts.

Clear the following flags to "0" according to the interrupt factor that occurred.

・Transmit history buffer overflow:

GERFL register THLES bit (THLSTSm register THLELT bit of all channels)

・DLC error: GCTR register DEIE bit

・CAN-FD message payload over write：GCTR register CMPOFIE bit

・Receive que message over write：GCTR register QOWEIE bit

・Receive que message lost：GCTR register QMEIE bit

・GW FIFO message over write：GCTR register MOWEIE bit

3. CAN-CAN FD Gateway (Only in CAN FD Mode)

When using the gateway function in CAN FD mode, the frame to be transmitted can be replaced with a classical CAN frame or a CAN FD frame.

Setting the GWEN bit of the FDCFG register to “1” enables the CAN-CAN FD gateway. You can select the FDF bit and BRS bit of the transmit frame with the GWFDF bit and GWBRS bit of the FDCFG register. If the DLC value of the received CAN frame is “1001B” or higher and the GWFDF bit is “1” (CAN FD frame), the DLC is replaced with “1000B”.

Do not route the following frames when the CAN-CAN FD gateway is enabled.

- CAN FD frame with payload length greater than 8 bytes
- Remote frame

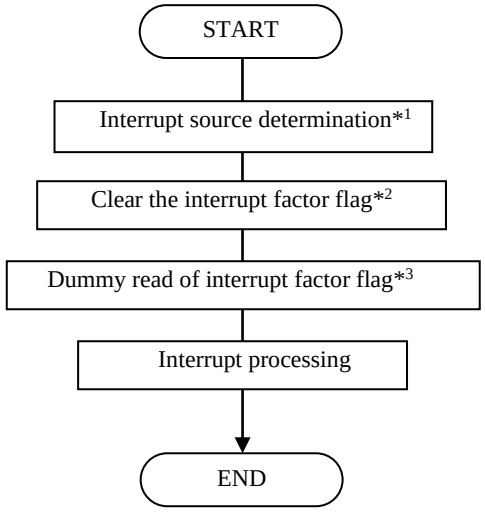
Also, when the CAN-CAN FD gateway is enabled, transmit only the following frames from the corresponding channel according to the GWFDF settings.

- GWFDF = 0 : Transmit the received frame as a classical CAN frame
- GWFDF = 1 : Transmit the received frame as a CAN FD frame

4. CAN-related Interrupt Processing

When using interrupts, the interrupt source flag must be cleared to “0”.

Figure 4-1 shows how to clear the interrupt source flag to “0” in interrupt processing.



【Note】 1. Please carry out if necessary.

2. The interrupt request flag (the EIRF bit of the EIC register) of the embedded controller cannot be cleared directly to "0" with the program. Clear the interrupt request from the peripheral function of the interrupt request source. For the process of clearing the interrupt source flag, refer to the user's manual hardware edition.
3. After clearing the interrupt source flag to "0", read the interrupt source flag after clearing to prevent accidentally accepting the interrupt source that should have been cleared.

Figure 4-1 CAN-related Interrupt Processing Procedure

5. Precautions for Processing Flow

5.1 About Functions

In this application note, there is a part that is functionalized even in the processing of single line, but this is only described as a function to clarify the processing for each function. When you actually create a program, you don't necessarily have to make it functional.

5.2 Settings for Each Channel, FIFO, and Buffer

In this application note, even if processing is required for each channel, FIFO, or buffer, only one processing is described. When actually creating a program, perform multiple processes as necessary.

5.3 Infinite Loop

To simplify the notation, there are some infinite loops in the processing flow. When actually creating a program, give each loop a time limit so that it can be exited during overtime. Figure 5-1 shows an example of processing with a loop time limit.

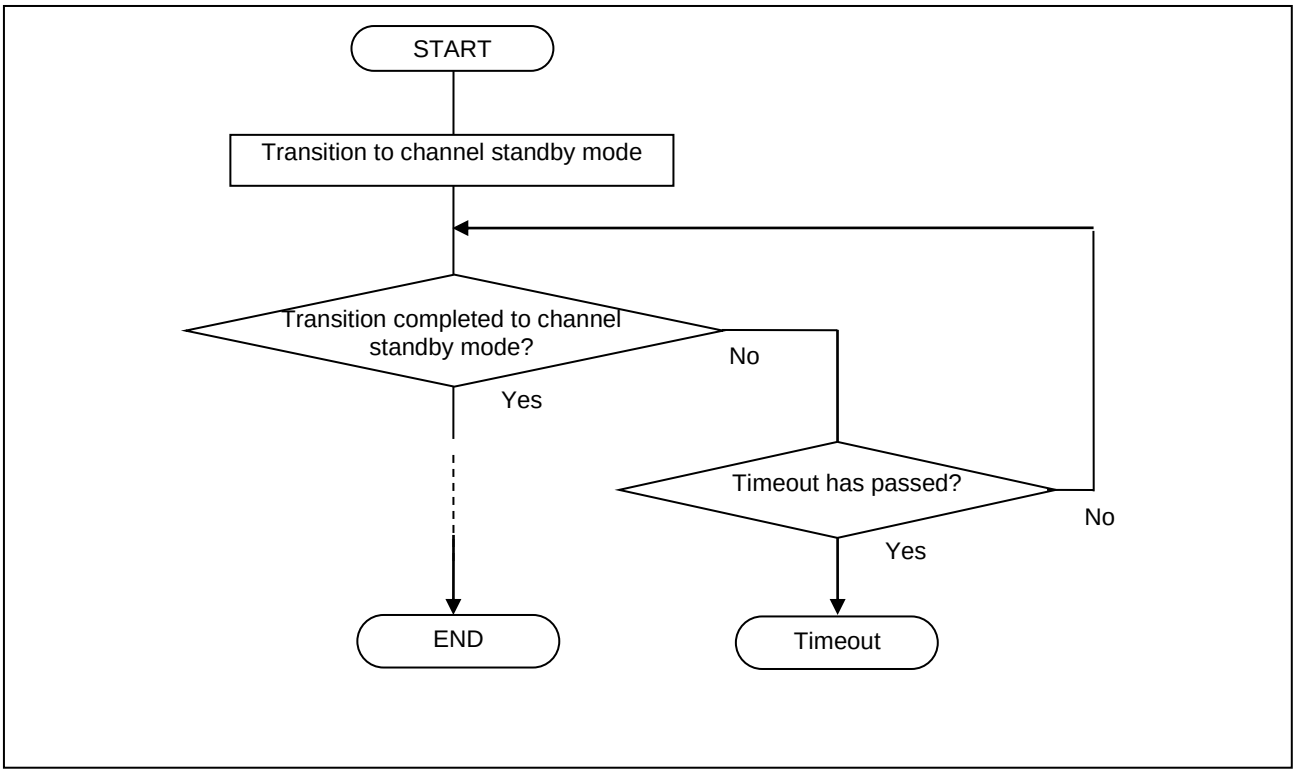


Figure 5-1 Example of Processing with Loop Time Limit

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Revision History

Rev.	Data	Description	
		Page	Summary
1.0	2023.10.5	—	Initial edition

Precautions for use of the product

This section describes the "Precautions" that apply to all microcontroller products. Please refer to this document and the Technical Update for precautions on individual products.

1. Treatment of unused pins

[Caution] Please dispose of unused pins according to "Handling of unused pins" in the text.

The impedance of the input pins of CMOS products is generally high impedance. If the unused pins are operated in an open state, noise around the LSI may be applied due to the induction phenomenon, a through current may flow inside the LSI, or it may be recognized as an input signal and malfunction may occur. Dispose of unused pins according to the instructions given in "Disposal of unused pins" in the text.

2. Treatment at power-on

[Caution] The state of the product is undefined when the power is turned on.

When the power is turned on, the state of the internal circuits of the LSI is indeterminate and the state of register settings and pins is undefined.

For products that are reset using the external reset pin, the pin state cannot be guaranteed from the time the power is supplied until the reset becomes valid.

Similarly, in the case of products that are reset using the built-in power-on reset function, the pin states cannot be guaranteed from the time the power is turned on until the voltage reaches a certain level.

3. Prohibition of Access to Reserved Addresses

[Caution] Access to reserved addresses is prohibited.

The address area has a reserved address allocated for future function expansion. The operation when these addresses are accessed cannot be guaranteed, so do not access them.

4. About clock

[Caution] When resetting, release the reset after the clock has stabilized.

When switching the clock during program execution, switch the clock after the switching destination clock is stable.

In a system that starts operating with a clock that uses an external oscillator (or external oscillator circuit) at reset, release the reset after the clock is sufficiently stable. Also, when switching to a clock that uses an external oscillator (or external oscillator circuit) in the middle of a program, make sure that the clock to be switched to is sufficiently stable before switching.

5. Differences between products

[Caution] When changing to a product with a different model name, perform a system evaluation test for each product model name.

Even if the MCUs in the same group have different model numbers, the characteristic values, operating margins, noise immunity, noise radiation, etc. may differ within the range of electrical characteristics due to differences in internal ROM and layout patterns. When changing to a product with a different model name, perform a system evaluation test for each individual product.

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