RH850/U2B Group

R01AN7090EJ0100
Rev.1.00

Function Operation Example between CPU

Summary

This application note summarizes the operation example by using the function with CPU for RH850/U2Bx.

The operation example described in this application note have been confirmed to operate, be sure to confirm the operation before using it.

Contents

1. Introduction

This operation example describes the usage of the function between CPU and the software making example for RH850/U2Bx.

1.1 Use Function

The following shows the hardware function for RH850/U2Bx using in this application note.

- Interrupt Function between Processor (IPIR)
- Barrier Synchronization Function (BARR)
- Time Protection Timer (TPTM)
- ATU-VI (Timer A)
- Port

2. Interrupt Function between Processor (IPIR)

2.1 Specification Overview

This section explains the usage for the interrupt function between the processors (IPIR).

Perform the interrupt request from CPU0 (PE0) to CPU1 (PE1) in 200ms intervals. If CPU1 (PE1) accepted the interrupt, perform the interrupt request to CPU0 (PE0). This function is continued.

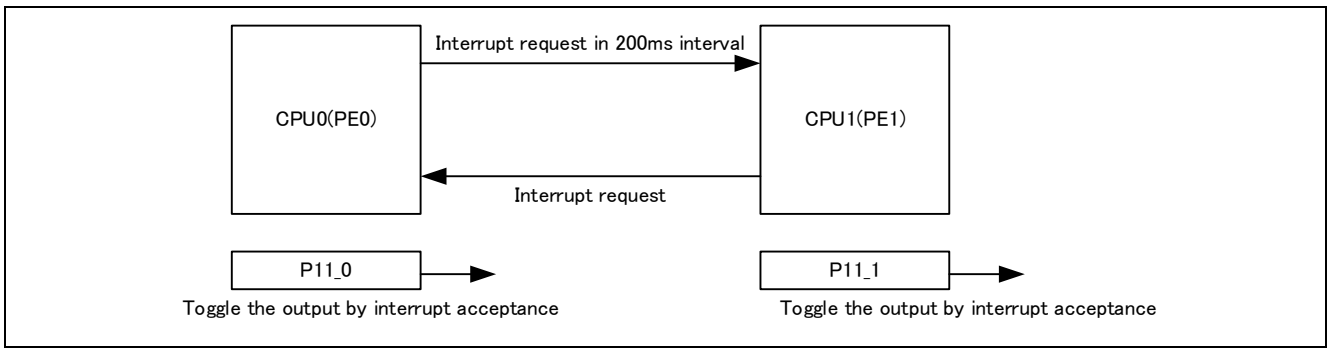

Figure 2-1 Interrupt Operation between Processor

2.2 Use Function

The following function shows the hardware function using in this operation example.

- Interrupt Function between Processors (IPIR)
- ATU-VI (Timer A)
- Port

2.3 Explanation for Operation Example

In this operation example, set enable for the interrupt function between the processors (IPIR), and alternately perform the interrupt request from each CPU. Use Timer A and 200ms interval for the interrupt request interval. Also, use the ports (P11_0 and P11_1) for checking the operation. When each CPU accepts the interrupt, the port output is toggled.

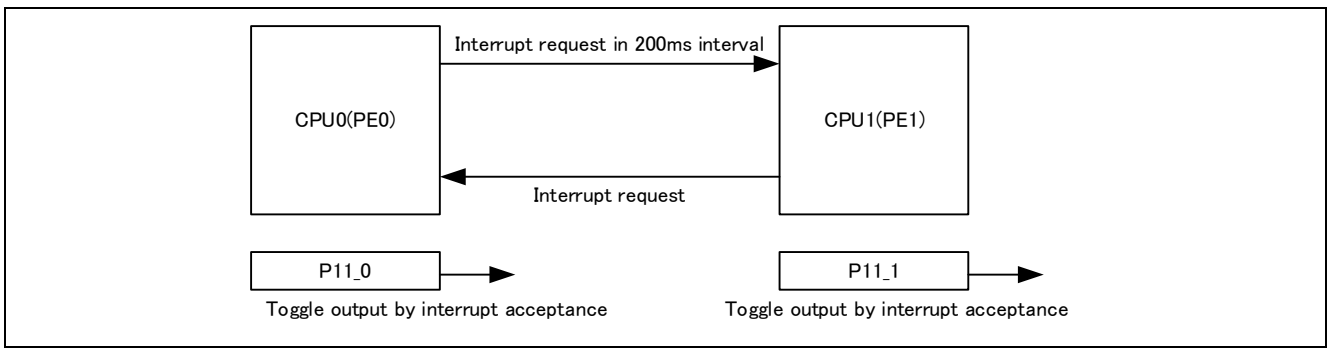

Figure 2-2 Operation Example

2.4 Software Explanation

- Module Explanation

The following shows the module list in this operation example.

Table 2-1 Module List (CPU0)

Module Name	Label Name	Function
Maine routine	main_pe0	Perform each setting and application setup.
PBG initialization routine	PBG_init	Perform PBG initial setting
Port initialization routine	port_init	Perform port initial setting.
Initialization routine of interrupt between processes	ipir_init_cpu0	Set enable for interrupt between processors.
Interrupt initialization routine	intc_init_cpu0	Perform initialization setting of interrupt function.
Software timer	Wait_Timer_CPU0	Software timer function. (200ms wait)
Interrupt processing routine	cpu0_int	Interrupt function. This clears interrupt function and toggles port output.

Table 2-2 Module List (CPU1)

Module Name	Rabel Name	Function
Maine routine	main_pe1	Perform each setting and application setup.
Initialization routine of interrupt between processes	ipir_init_cpu1	Set enable for interrupt between processors.
Interrupt initialization routine	intc_init_cpu1	Perform initialization setting of interrupt function.
Interrupt processing routine	cpu1_int	Interrupt function. This clears interrupt function and toggles port output.

- Register Setting

The following shows the register setting of each function in this operation example.

Table 2-3 Interrupt Register Setting between Processors (CPU)

Register Name	Setting Value	Function
IPI0ENS	0x02	Interrupt enable between CPUs
IPI0REQS	0x02	Request interrupt to CPU1.
IPI0FCLRS	0x02	Clear interrupt request flag.

Table 2-4 Interrupt Register Setting between Processors (CPU1)

Register Name	Setting Value	Function
IPI0ENS	0x01	Enable interrupt between CPUs.
IPI0REQS	0x01	Request interrupt to CPU0.
IPI0FCLRS	0x01	Clear interrupt request flag.

Table 2-5 Interrupt Register Setting (CPU0)

Register Name	Setting Value	Function
EIC0	0x0040	Table reference/Priority level 0

Table 2-6 Interrupt Register Setting (CPU1)

Register Name	Setting Value	Function
EIC0	0x0040	Table reference/Priority level 0

Table 2-7 Port Register Setting

Register Name	Setting Value	Function
PCR11_0	0x00000000	P11_0: Output port
PCR11_1	0x00000000	P11_1: Output port

Table 2-8 ATU-Ⅶ (Timer A) Register Setting

Register Name	Setting Value	Function
TCNTA	0xFF85EDFF	Counter initial setting (200ms)
ATUENR	0x0003	Enable Timer A count operation
		Enable clock generation of prescaler
TSCRA	0x8000	Overflow flag clear

Table 2-9 PBG Register Setting

Register Name	Setting Value	Function
PBGERRSLV20 PBGKCPROT	0xA5A5A501	Enable writing
PBG21 PBGPROT1_8	0x00000003	Enable read/write : SPID = 0 and 1

- Operation Flow

The following shows the flowchart in this operation example.

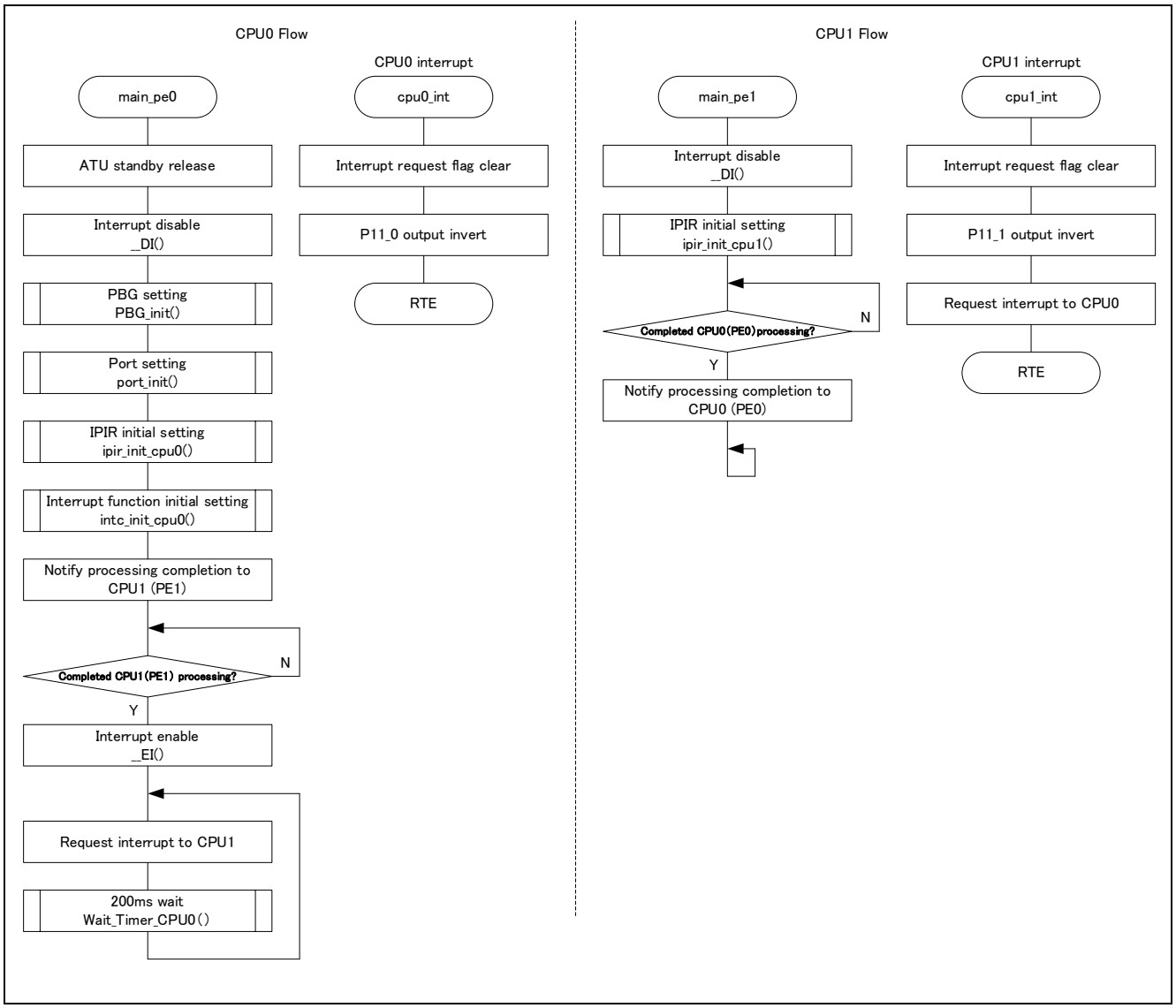

Figure 2-3 Flowchart

3. Barrier Synchronization Function (BARR)

3.1 Specification Overview

This section explains the usage of the barrier synchronization function (BARR).

When performing the parallel processing using the multicore processer, CPU is required to wait until the data required for the next process is prepared. This processing can be implemented in software, but the memory accesses, etc., may degrade the system processing performance.

The barrier synchronization function (BARR) can be detected by the processing completion of each CPU, and the synchronization can be easily realized.

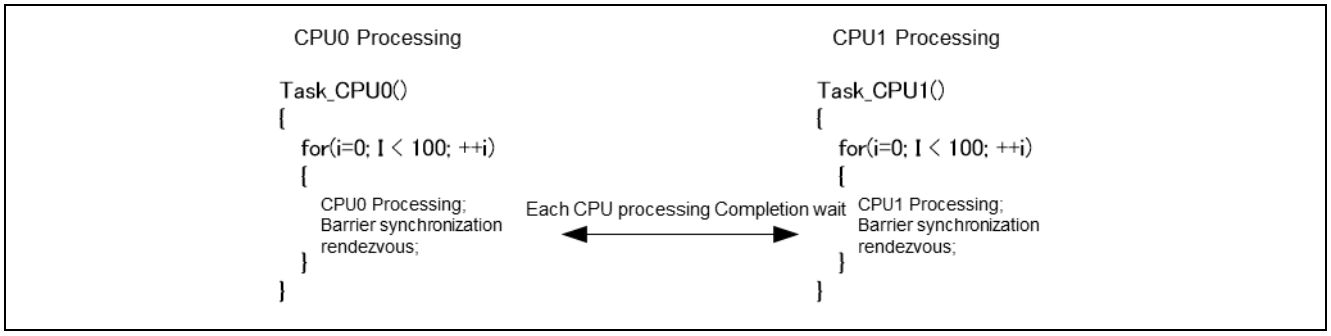

Figure 3-1 Operation of Barrier Synchronization Function

3.2 Use Function

The following shows the used hardware functions in this operation example.

- Barrier Synchronization Function (BARR)

3.3 Explanation of Operation Example

In this operation example, each CPU increments the counter variable on the memory. The increment operation is delayed to insert the wait to CPU0. By the synchronization function (BARR), it is possible to check that each counter variable value is same when the program execution is stopped.

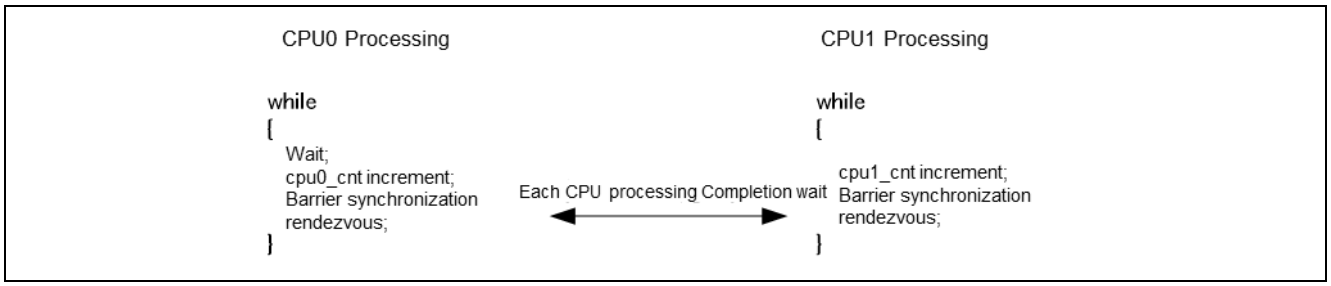

Figure 3-2 Operation Example

3.4 Software Explanation

- Module Explanation

The following shows the operation example of the module list.

Table 3-1 Module List (CPU0)

Module Name	Rabel Name	Function
Miane routine	main_pe0	Perform each setting and application booting.
BARR initialization routine	barr_init	Perform BARR initial setting.

Table 3-2 Module List (CPU1)

Module Name	Rabel Name	Function
Maine routine	main_pe1	Perform each setting and application booting.

- Register Setting

The following shows the register setting of each function in this operation example.

Table 3-3 BARR Register

Register Name	Setting Value	Function
BR0INIT	0x01	BRnCHKm register and BRnSYNCm register initialization
BR0EN	0x03	CPU0(PE0) and CPU1(PE1) barrier synchronization function enable
BR0CHKS	0x01	Notify the processing completion.
BR0SYNCS	0x00	Complete the barrier synchronization.

- Operation Flow

The following shoes the flowchart in this operation example.

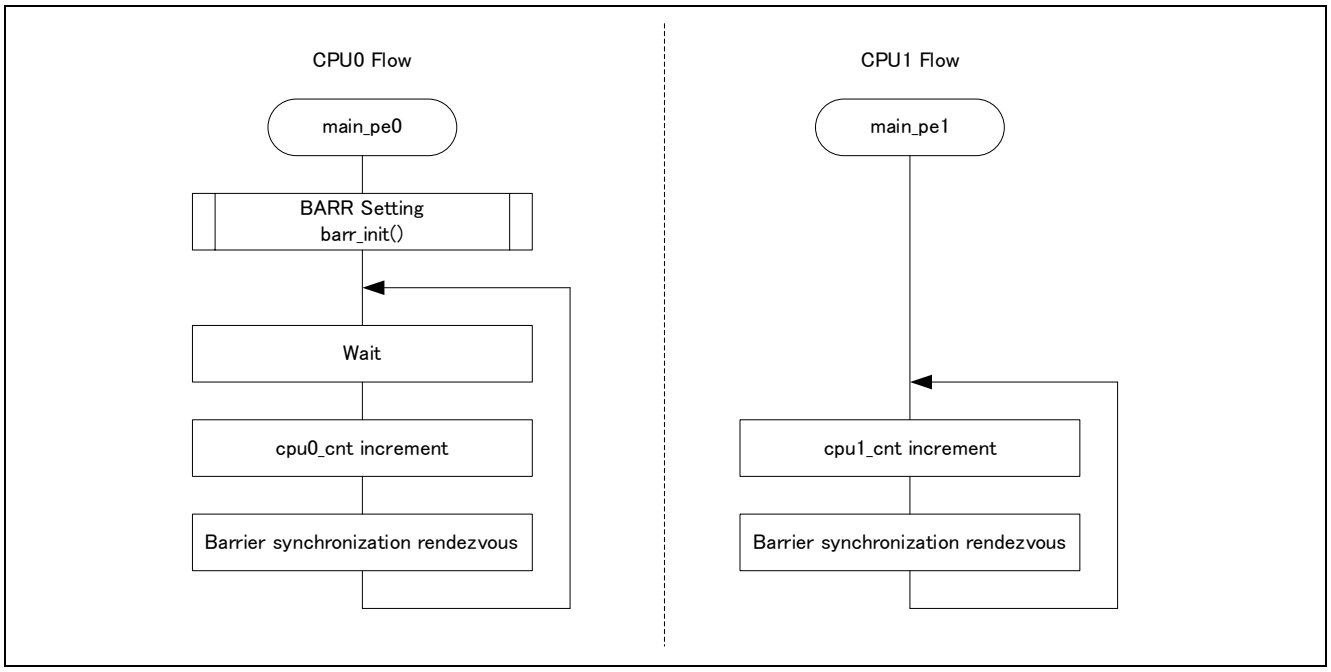

Figure 3-3 Flowchart

4. Time Protection Timer (TPTM)

4.1 Specification Overview

This example explains the use method of the time protection timer (TPTM).

The timer protection timer (TPTM) is the timer for CPU used for realizing the timing protection function. This timer is configured by the interval timer (TPTM) and the free run timer (Up counter).

In this operation example, the count value of the free run timer is acquired by the underflow interrupt of the interval timer.

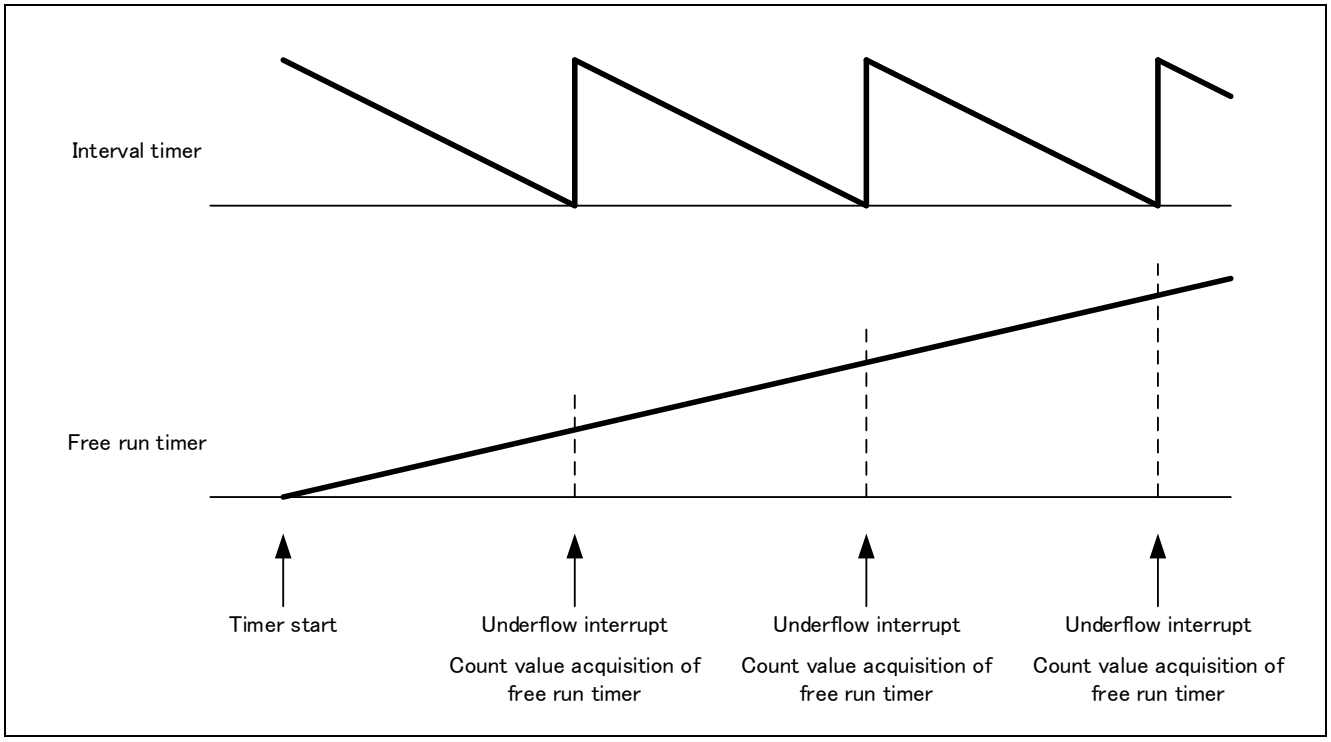

Figure 4-1 Operation of Time Protection Timer

4.2 Use Function

The following shows the used hardware function in this operation example.

- Time Protection Timer (TPTM)
- Port

4.3 Explanation for Operation Example

In this operation example, set 40MHz to the count clock of the time protection timer (TPTM), 0xFA0 (100us) to the counter load value of the interval timer, and start the count operation.

The underflow interrupt occurs every 100us, and the free run timer is stored to the count value. Also, Use the port (P11_0) for the operation check. The port output toggles every under flow interrupt occurrence.

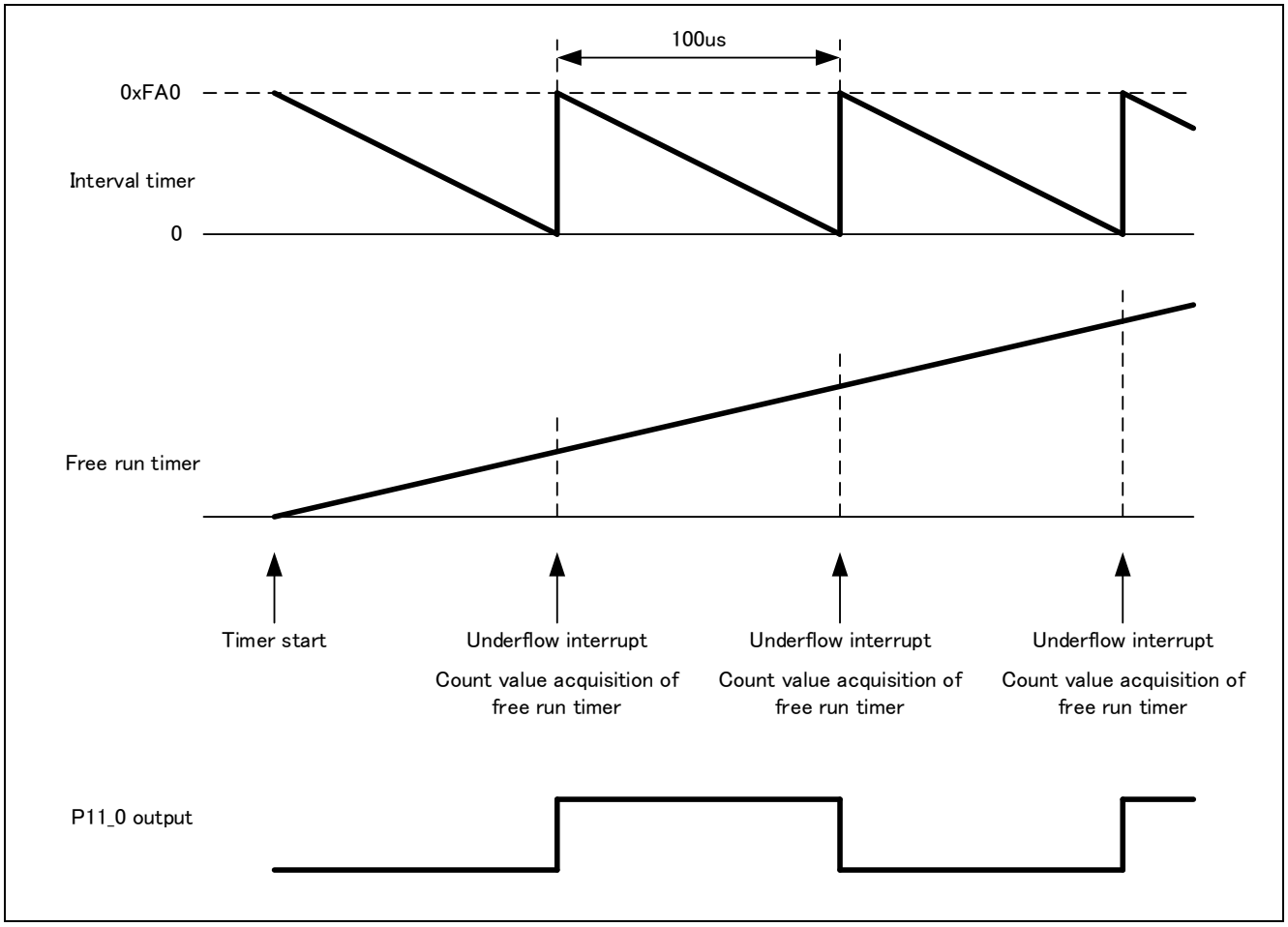

Figure 4-2 Operation Example

4.4 Software Explanation

- Module Explanation

The following shows the module list.

Table 4-1 Module List

Module Name	Label Name	Function
Maine routine	main_pe0	Perform each setting and application setup.
Port initialization routine	port_init	Perform port initial setting.
TPTM initialization routine	tptm_init	Perform TPTM initial setting.
Interrupt initialization routine	intc_init	Perform initialization setting of interrupt function.
Interrupt processing routine	tptm_int	Interrupt function. This clears interrupt function and toggles port output.

- Register Setting

The following shows the register setting of each function in this operation example.

Table 4-2 TPTM Register

Register Name	Setting Value	Function
TPTMSIIEN	0x00000001	TPTM0 channel 0 interrupt enable
TPTMSIDIV	0x00000009	Counter clock setting of interval timer CLK_CPU / 10 （40MHz）
TPTMSILD0	0x00000FA0	Counter load value of interval timer: 100us
TPTMSFDIV	0x00000009	Counter clock setting of free run timer CLK_CPU / 10 (40MHz)
TPTMSFCNT	0x00000000	Free run counter clear

Table 4-3 Interrupt Register Setting

Register Name	Setting Value	Function
EIC31	0x0040	Table reference/Priority level 0
TPTMSEL	0x00000001	Connect TPTM interrupt with EINT TPTM.

- Operation Flow

The following shows the flowchart in this operation example.

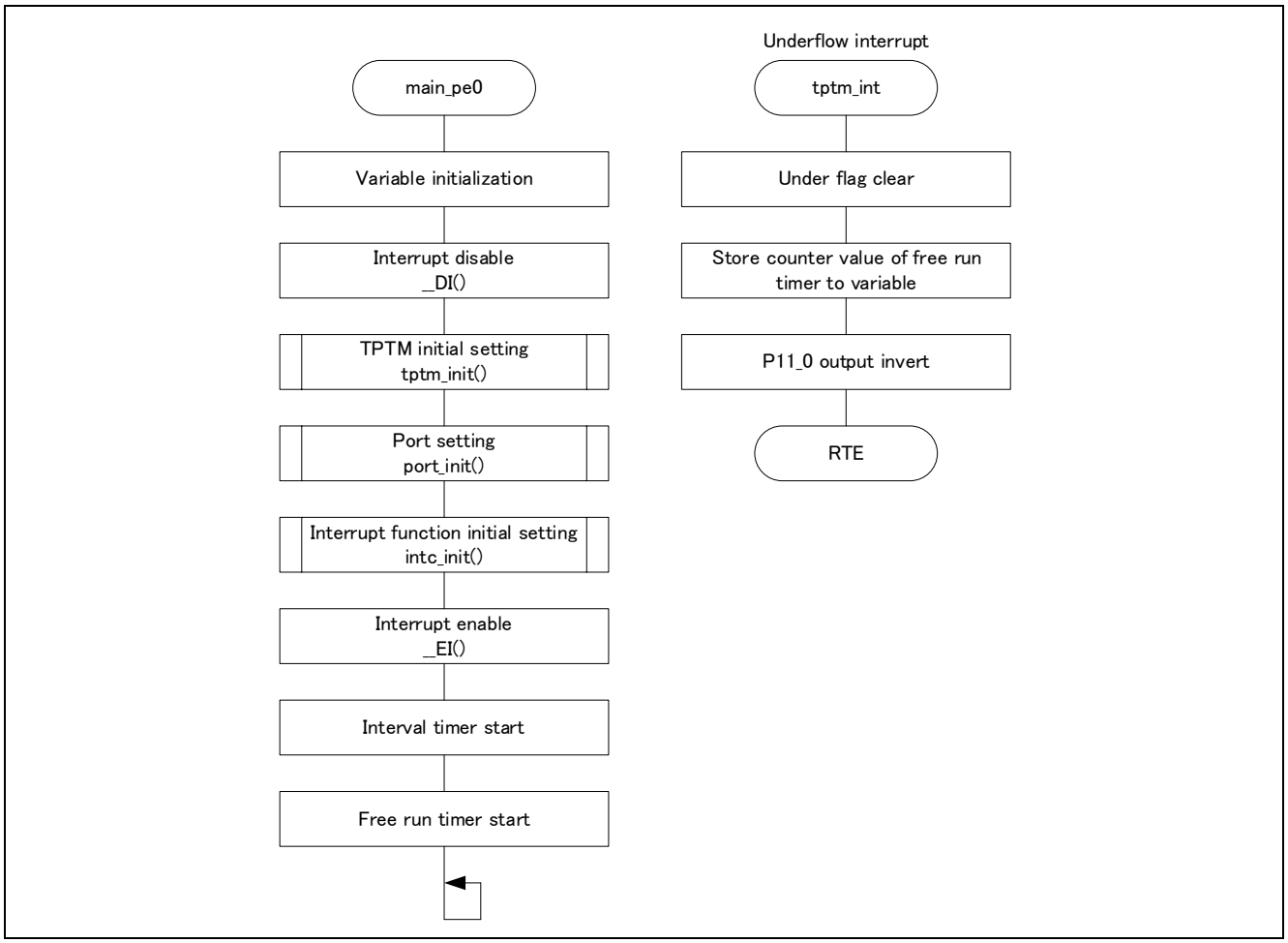

Figure 4-3 Flowchart

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Revision History

Rev.	Data	Description	
		Page	Summary
1.00	2023.10.3	-	First edition issued

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   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

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   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

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(Rev.5.0-1 October 2020)

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