RH850/U2B Group

FCMP Application Note

R01AN6593EJ0010
Rev.0.10

Summary

This application notes explains Fast Comparator (FCMP) function of automotive single-chip microcontroller RH850/U2B series for automobile (hereinafter called U2B).

Aim of this document and software is to provide supplemental information for the function on RH850/U2B. It is not intended to implement in the design for mass production.

There is no guarantee to update in this document and software to reflect the latest manual, errata, technical update and development environment. You are fully responsible for the incorporation or any other use of the information of this document in the design of your product or system, and please refer to latest manual, errata, technical update and development environment.

Target Device

- RH850/U2B Group

Target Integrated Development Environment

CS+(from RENESAS Electronics)

Version : E8.07.00g6

Device file : DR7F702Z21EDBB.DVF
DR7F702Z22EDBB.DVF

Reference Document

RH850/U2B User's Manual Hardware
For function details and electrical characteristics, please refer to "User's Manual: Hardware".

This application note is based on the following manual.

- RH850/U2B User's Manual (Rev.0.60): R01UH0923EJ0060

GTM-IP Specification

For function details of GTM mounted to the device, refer to GTM-IP specification.
This application note is based on the following specification.

- GTM IP Specification: GTM4.1−V1.00 | 2021−12−15
- GTM Specification Appendix B for Device 4185 Revision: v4.1-draft / 2020-10-28

Contents

1. Applicable

This application note describes FCMP operation example for RH850/U2B.

2. Overview

2.1 Function Overview

FCMP for U2B has the flowing functions.

- FCMP can independently control for each channel:
  - Comparison start
  - Comparison end
  - Comparison operation setting
- FCMP can concurrently control the following for multiple channels:
  - Comparison start
  - Comparison end

Each channel has the following functions:

- Access to each register depends in APB protocol:
- Conversion time: 200ns (5Msps)
- DAC data setting of 12-bits resolution DAC
- Signal Generation Function
  - Comparison result change interruption
  - Error interruption
  - Actuator current control signal output
- Analog output is selectable up to 2c[*1]:
  - Analog input is selectable from 2ch (FCMP0 or FCMP1)[*1]
  - Analog input is one (FCMP2~FCMP9) for each FCMPn[*1]
- Comparison start/Stop request
  - External trigger input
  - Software trigger
- 2 selectable comparison mode
  - Comparison mode 1: Comparison with two level (upper/lower-limit) thresholds
  - Comparison mode 2: Comparison with one level threshold
- Threshold update
  - Automatically update of threshold by convertor output
  - Threshold update by external trigger input
- Error detection
  - ID error detection
  - Parity error detection
  - Empty error detection
- Self-diagnosis

For the details, refer to "*RH850/U2B User's Manual 53.1.6 External Input/Output Signal"*.

2.1.1 Comparison Mode

The function differences between FCMP comparison mode 1 and 2 are shown below.

Table 2-1 Comparison Mode

Function		Comparison Mode 1	Comparison Mode 2
Actuator Current Control Signal Output		Output presence/absence is selectable.	—
DAC Data Update	Update Timing	● In comparison start triggering ● In external triggering ● In comparison result changing (SLSET=1)	● In comparison start triggering ● In external triggering
	Update Target	● DAC Data ● Actuator Current Control Signal	● DAC Data
Comparison Threshold		● 2 level (Upper/Lower-limit threshold) ● Selectable comparison start threshold after DAC data updating from upper/lower-limit threshold. (SLVAL bit) ● After DAC data updating, when changing comparison result, the comparison threshold before changing is upper-limit threshold or the lower threshold, automatically updated to the upper-limit threshold.	● 1 level (Selected threshold by SLVAL bit)

2.2 Block Diagram

The block diagram of FCMP is shown below.

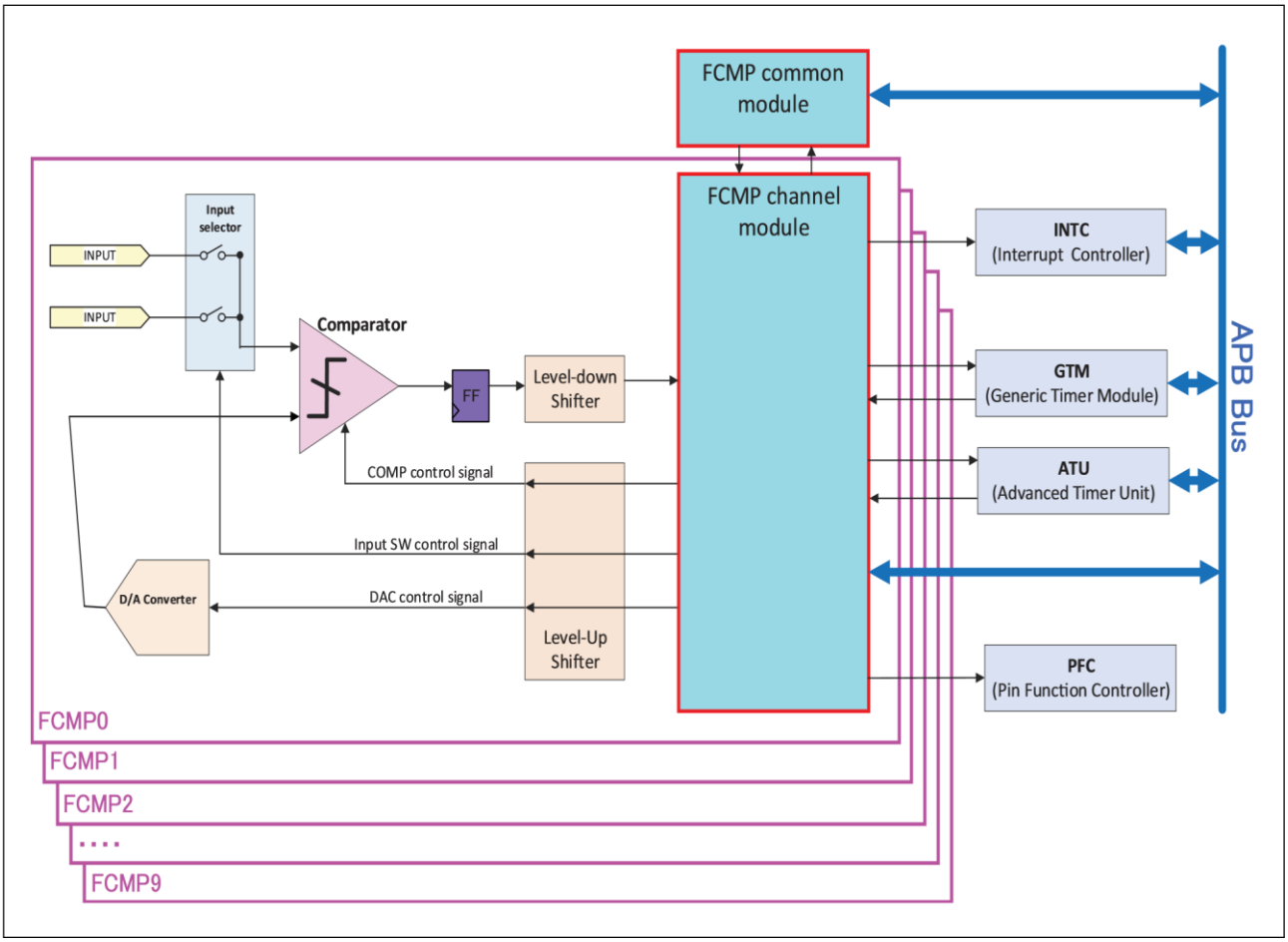


Figure 2-1 Block Diagram of FCMP

2.3 Clock Supply

Table 2-2 Clock Supply

Unit Name	Unit Clock Name	Supply Clock Name	Frequency
FCMPC	PCLK	CLK_LSB_FCOMP	40MHz
	clkcmp	CLKC_LSB_FCOMP	
FCMPn	PCLK	CLK_LSB_FCOMP	
	clkcmpu	CLKC_LSB_FCOMP	

2.4 Interrupt Request, DAM/DTS, and Error Notification

The following shows the interrupt request, DAM/DTS, and the error notification.

Table 2-3 Interrupt Request

Unit Interrupt Name	**Unit Interrupt Signal**	**Explanation**	**Connection Destination**
FCMPnINTREQ	fcmpu_int_req_n	Comparison result interrupt of channel n	INTC2
FCMPn_DACDATACHG	fcmpu_dadata_change_n	DAC data update of channel n	sDMAC, DTS
Error Notification	**Explanation**		**Connection Destination**
FCMP error	ID/Parity/Empty error of channel n (fcmpu_err_req and intc_erreq_n are same.)		ECM

2.5 External Input/Output Signal

The following shows the external output/input signal of FCMP.

Table 2-4 External Input/Output Signal

Unit Signal Name	**Explanation**	**I/O**	**Connection Destination (Combination Port Pin signal)**
AFCVCC	Power Supply Pin for Analog Part	IN	AFCVCC
AFCVSS	Grand Pin for Analog Part		AFCVSS
FCMPANn0	Analog Input Pin for Channel n		FCMPANn0
FCMPANn1	Analog Input Pin for Channel n		FCMPANn1*1
fcmpu_t1_n	Boost MOSFET Control for Channel n	OUT	FCMPUn_T1
fcmpu_t2_n	High Side MOSFET Control for Channel n		FCMPUn_T2
fcmpu_t3_n	Low Side MOSFET Control for Channel n		FCMPUn_T3

Note 1. The products other than U2B10 and U2B6 support the FCMPANn1 pin when n=0 and 1. U2B10 and U2B6 are not supported the FCMPANn1 pin.

2.6 External Input/Output Signal

The following shows the internal input/output signal of FCMP.

Table 2-5 External Input/Output Signal

Unit Signal Name	Explanation	I/O	Connection Destination
fcmpu_t1_n	Boost MOSFET Control of Channel n	OUT	PIC1
fcmpu_t2_n	High Side MOSFET Control of Channel n		
fcmpu_t3_n	Low Side MOSFET Control of Channel n		
fcmpu_cmpo_n	Comparator Output Data of Channel n	OUT	PIC2
fcmpu_int_req_n	Comparison Result Interrupt of Channel n		
fcmpu_dacdata_change_n	DAC Data Update of Channel n		
intc_erreq_n	Error Interrupt of Channel n		
ext_start_trg_n	Comparison Start Trigger from Other Module of Channel n	IN	
ext_stop_trg_n	Comparison End Trigger from Other Module of Channel n		
ext_dacdata_upda te_trg_n	DAC Data Update Request from Other Module against Channel n		

3. Operation Example

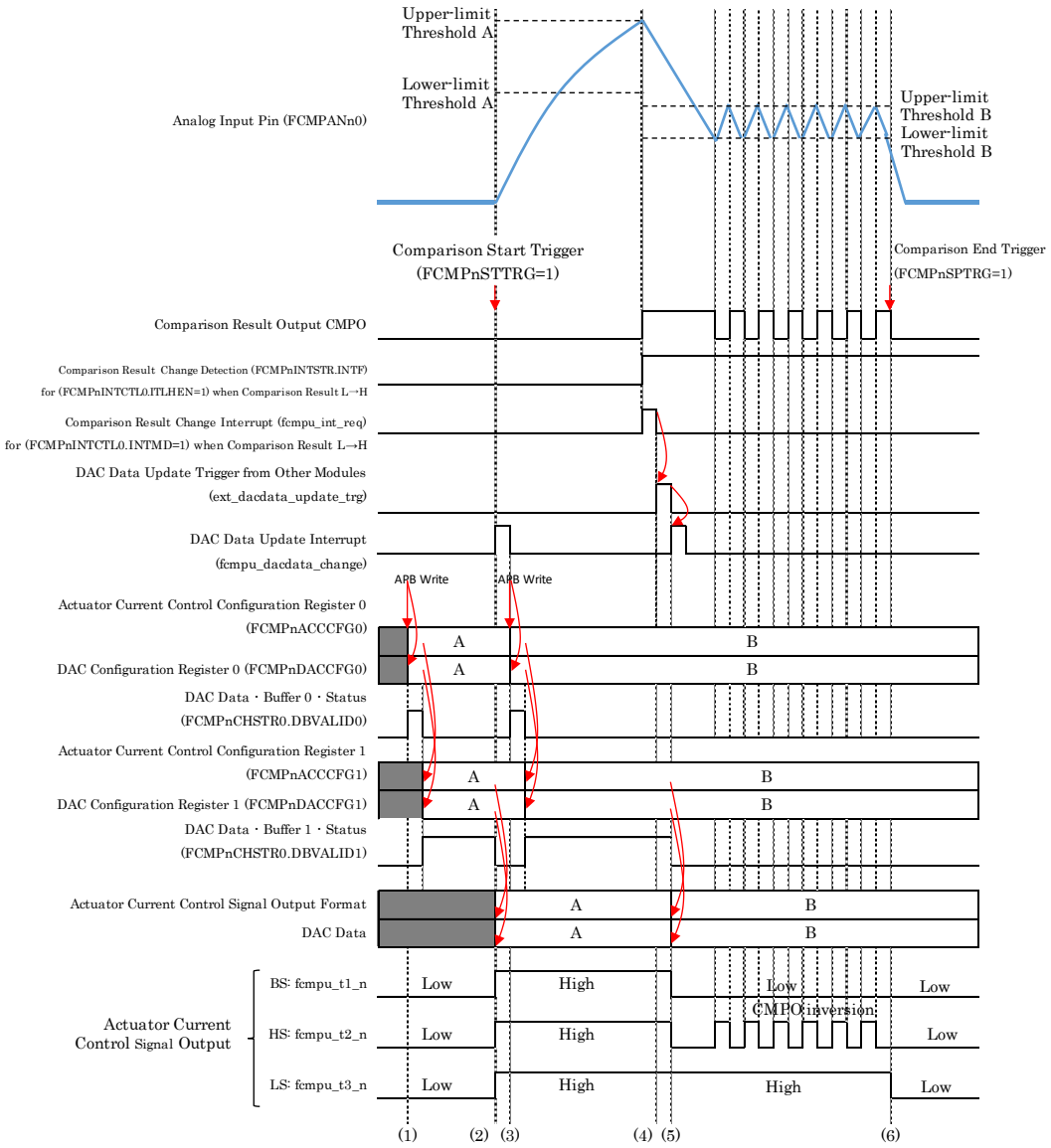
This section explains the following FCMP operation example. FCMP register, bit setting that is not in this operation example are set the bit setting after resetting the value.

- Actuator Current Control Signal Output by External Trigger
- Actuator Current Control Signal Output by Software Trigger

3.1 Actuator Current Control by External Trigger

3.1.1 Specification Overview

In this operation example, the external trigger from GTM changes by comparison threshold between the actuator current control signal output of FCMP0 and the analog input pin voltage by using GTM and FCMP0 mode1 of FCMP0. The external trigger is executed when the voltage of the analog input signal is exceeded the upper-limit threshold at the first time.



FCMPnDACCFG0 Setting Value of Threshold A
- DACVL[11:0] : Lower-limit threshold A
- DACVH[11:0] : Upper-limit threshold A
- SLSET : 0 : DAC data update disable in comparison result changing
- SLVAL : 1 : Start threshold of comparison is upper-limit

FCMPnACCCFG0 Setting Value of Actuator Current Control Signal Output Format
- SLBMTYP : 1 : BS (Boost MOFSET Signal Output) : High level
- SLHMTYP : 1 : HS (High Side MOFSET Signal Output) : High level
- SLLMTYP : 1 : LS (Low Side MOFSET Signal Output) : High level

FCMPnDACCFG0 Setting Value of Threshold B
- DACVL[11:0] : Lower-limit threshold B
- DACVH[11:0] : Upper-limit threshold B
- SLSET : 0 : DAC data update disable in comparison result changing
- SLVAL : 0 : Start threshold of comparison is lower-limit

FCMPnACCCFG0 Setting Value of Actuator Current Control Signal Output Format
- SLBMTYP : 0 : BS (Boost MOFSET Signal Output) : Low level
- SLHMTYP : 3 : HS (High side MOFSET Signal Output) : CMPO conversion level
- SLLMTYP : 1 : LS (Low side MOFSET Signal Output) : High level

Figure 3-1 Actuator Current Control by External Trigger

[Procedure]

(1) Write the actuator current control signal output format A to FCMPnACCCFG0 register and the DAC data A to FCMPnDACCFG0 register.

(2) Issue the comparison start trigger (FCMPnSTTRG=1).

In the time, FCMPn executes the follows.

- Start comparing the analog input and the upper-limit threshold of the DAC data A.
- Output the current control signal according to the actuator current control signal output format A.
- Issue the DAC data update interrupt (fcmpu_dacdata_change).

(3) By the DMA transmitting the DAC data update interrupt to the trigger, write the actuator current control signal output format B to FCMPnACCCFG0 register and the DAC data B to FCMPnDACCFG0 register.

(4) FCMPn issues the comparison result changing interrupt (fcmpu_int_req) when the voltage of the analog input pin (FCMPANn0) exceeds the upper-limit threshold of the DAC data A.

GTM triggers the DAC data update trigger (ext_dacdata_update) from the other modules after detecting the comparison result changing interrupt.

(5) FCMPn executes the follows.

- Start comparing the lower-limit threshold between the analog input and DAC data B.
- Output the current control signal according to the actuator current control signal output format B.
- Issue the data update interrupt (fcmpu_dacdata_change).

(6) Issue the comparison end trigger (FCMPnSPTRG).

The follows show the IO operation of FCMP0 and GTM and the GTM operation. The connection of internal input/output signal for FCMP0 and GTM is set by PIC register.

Table 3-1 I/O of FCMP0 and GTM and GTM Operation

FCMP0	I/O	GTM	
		ATOM/TIM	MCS
Comparison Result Interrupt (fcmpu_int_req) Issue condition: When comparison result changes low to high One-pulse high width: 25ns	→	TIM0 CH0 Input (GTM_TIM0_IN0) ・Count clock: 100MHz ・Detection edge: Falling edge ・ARU transmission: Enable	MCS0 CH0 triggers the one-shot pulse of ATOM0 CH0 after received ARU data from TIM0 CH0 (ARU address:0x1B7).
External trigger of DAC data update from another module (ext_dacdata_update_trg) Sampling clock: 40MHz	←	ATOM0 CH0 Output (GTM_ATOM0_OUT0) ・Operation mode: SOMP (One-shot mode) ・Count clock: 100MHz ・High width: 50ns (5 count @100MHz)	

In this operation example, set the follows to the upper/lower-limit threshold of DAC data A/B

DAC Data Threshold	DAC Data A	DAC Data B
Upper-limit threshold [V]	4V	3V
Lower-limit threshold [V]	2V	2V

3.1.2 System Configuration

3.1.2.1 Overview

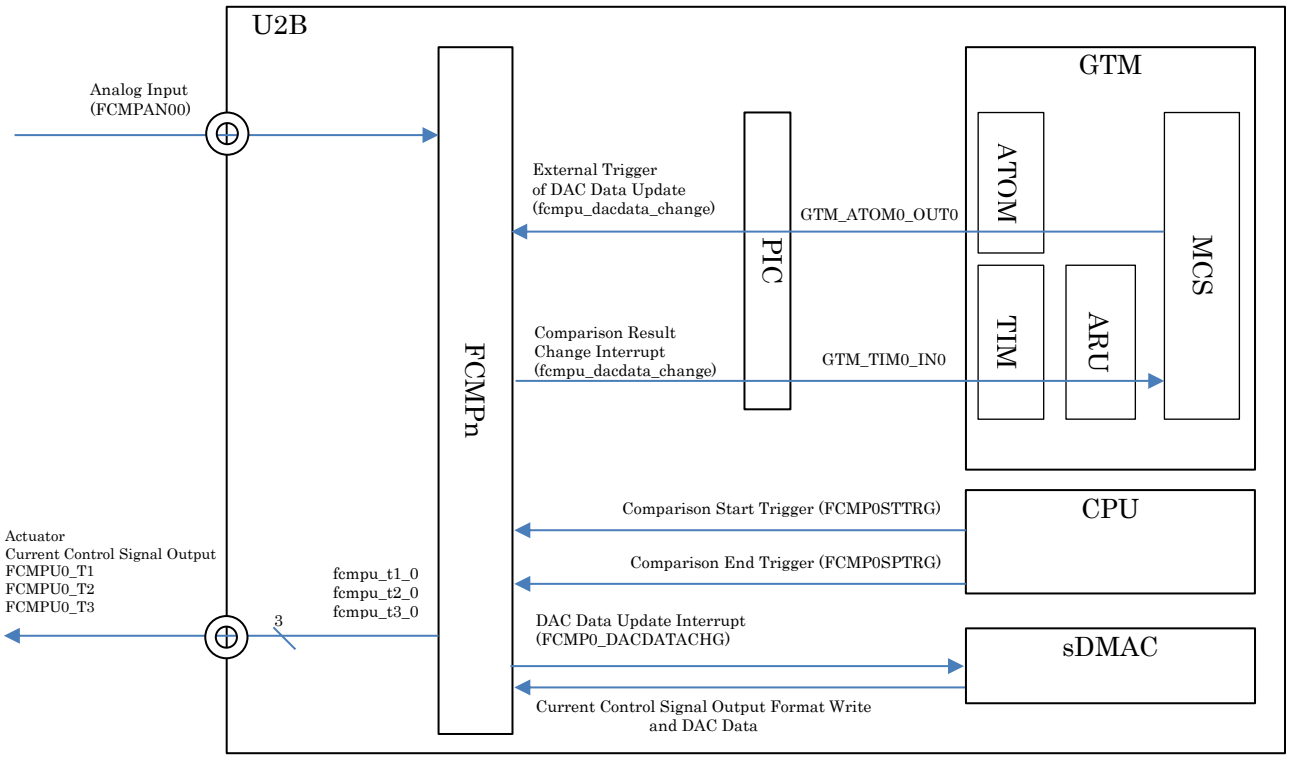


Figure 3-2 System Configuration (Whole)

3.1.2.2 PIC

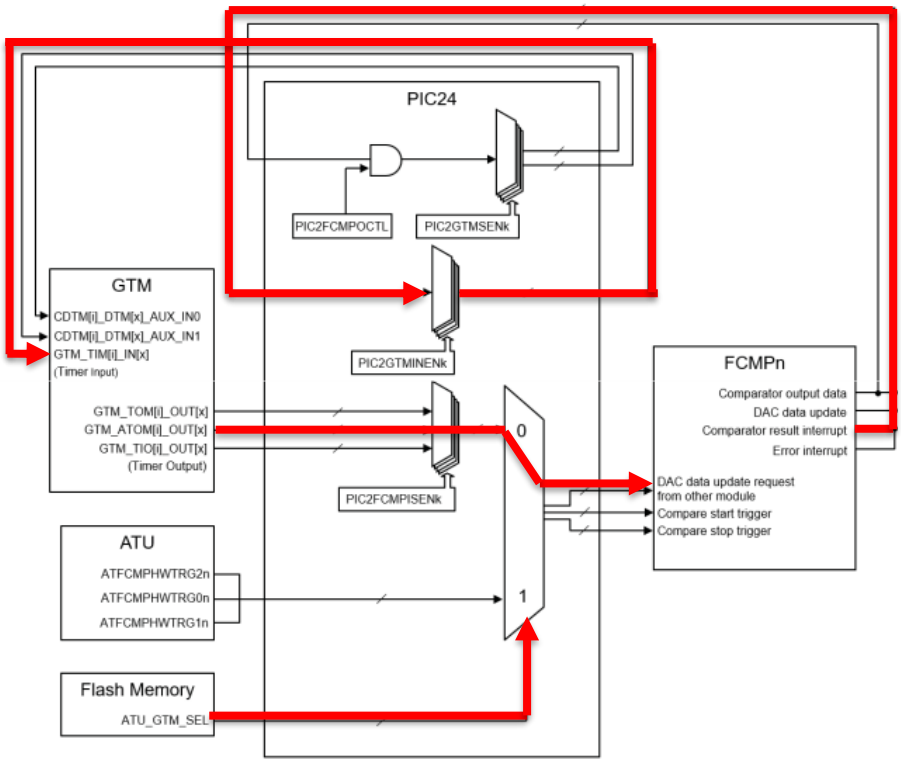


Figure 3-3 System Configuration (PIC)

3.1.3 Software Explanation

3.1.3.1 Module Explanation

The following shows the module list in this operation example.

Table 3-2 Module

Module Name	Function Name	Function
FCMP main function	fcmp_main	Execute main processing in this operation example.
FCMP initial setting function	fcmp_init	Initial set FCMP.
sDMAC initial setting function	sdmac_init	Write actuator current control signal output format and DAC data by DMA transfer in FCMPn_DACDATACHG interrupting.
PORT initial setting function	port_init	Initial set PORT.
PIC initial setting function	pic_init	Initial set PIC.
GTM initial setting function	gtm_init	Initial set GTM and copy MCS program to MCS0 RAM.

3.1.3.2 Register Setting

The following shows the register setting of each function in this operation example.

(a) FCMP Main Function

Table 3-3 FCMP Mian (n=0)

Unit Name	Register Name	Bit Name	Setting Value	Function
FCMPn	FCMPnSTTRG	CHSTRQ	1	0: No operation 1: Comparison start request
	FCMPnSPTRG	CHSPRQ	1	0: No operation 1: Comparison end request
	FCMPnDACBCLR	DACBUFCLR	1	0: No operation 1: Clear Clear the enable status (FCMPnCHSTR0.DBVALID1 and DBVALID0 bit) of FCMPnDACCFG0 and FCMPnDACCFG1.

(b) FCMP Initial Setting Function

Table 3-4 FCMP Initial Setting (n=0)

Unit Name	Register Name	Bit Name	Setting Value	Function
SYSCTRL	MSR_FCOMP	MS_FCOMP_0	0	Clock supply of FCMPC 0: Clock supply 1: Clock stop
		MS_FCOMP_1	0	Clock supply of FCMP0 0: Clock supply 1: Clock stop
	MSR_RDC	MS_RDC_2	1	Clock supply of RDC3AL0 0: Supply clock to RDC3AL0. 1: Supply clock to RDC3AL0. Set the above when using FCMP of U2B6. For the details, refer to "*RH850/U2B User's Manual 53.5.4 Notes on Using FCMP or RDC3AL*".
		MS_RDC_3	1	Clock supply of RDC3AL1 0: Supply clock to RDC3AL1. 1: Not supply clock to RDC3AL1. Set the above when using FCMP of U2B6. For the details, refer to "*RH850/U2B User's Manual 53.5.4 Notes on Using FCMP or RDC3AL*".
RDC3AL	RDC3AL0RDSTP	-	0x00000001	Stop R/D Converter. Set the above when using FCMP of U2B6. For the details, refer to "*RH850/U2B User's Manual 53.5.4 Notes on Using FCMP or RDC3AL*".
	RDC3AL1RDSTP	-	0x00000001	

Unit Name	Register Name	Bit Name	Setting Value	Function
FCMPC	FCMPCTRGCTL	STENn	1	External trigger input for comparison start (ext_start_trg_n) 0: Disable 1: Enable
	FCMPCSYSTCTL	SYSTENn	0	Synchronization comparison start request 0: Disable 1: Enable
FCMPn	FCMPnERRCTL	EMPEN	0	Empty error interrupt output (fcmpu_err_req) 0: Disable 1: Enable
		PREN	0	Parity error interrupt output (fcmpu_err_req) 0: Disable 1: Enable
		IDEN	0	ID error interrupt output (fcmpu_err_req) 0: Disable 1: Enable
	FCMPnINTCTL0	ILHEN	0	Comparison result interrupt detection when threshold exceeds comparison result. 0: Disable 1: Enable
		ILLEN	0	Comparison result interrupt detection when threshold decreases below comparison result. 0: Disable 1: Enable
		ITHLEN	0	Comparison result interrupt detection when comparison result transferring to low from high. 0: Disable 1: Enable
		ITLHEN	1	Comparison result interrupt detection when comparison result transferring to high from low. 0: Disable 1: Enable
		INTMD	1	Interrupt output mask when FCMPnINTSTR.INTF=1 0: Disable 1: Enable
		INTEN	1	Comparison result interrupt output (fcmpu_int_req) 0: Disable 1: Enable When this bit is set “1”, interrupt output is generated when either of follows is enabled. ・FCMPnILHEN bit ・FCMPnILLEN bit ・FCMPnITHLEN bit ・FCMPnITLHEN bit

<table>
<tr><th>Unit Name</th><th>Register Name</th><th>Bit Name</th><th>Setting Value</th><th>Function</th></tr>
<tr><td rowspan="6"></td><td>FCMPnINTCTL1</td><td>DACDFEN</td><td>1</td><td>DAC data update interrupt output (fcmpu_dacdata_change)
0: Disable
1: Enable</td></tr>
<tr><td>FCMPnACCCTL</td><td>ACCEN</td><td>1</td><td>Actuator current control signal output
0: Disable
1: Enable
・fcmpu_t1_n
(Boost MOSFET Control Signal)
・fcmpu_t2_n
(High Side MOSFET Control Signal)
・fcmpu_t3_n
(Low Side MOSFET Control Signal)</td></tr>
<tr><td rowspan="3">FCMPnCMPCMR</td><td>CMPWAIT[3:0]</td><td>3</td><td>Set the standby time until DAC setting time from the DAC data update timing. Calculation formula of standby time is follows.
Standby time = CMPWAIT[3:0]*200ns
CMPWAIT[3:0] is needed to set more than “3”.</td></tr>
<tr><td>DIAGMD</td><td>0</td><td>Refer to CMPMD bit</td></tr>
<tr><td>CMPCHS[2:0]</td><td>1</td><td>Analog input selection
<table>
<tr><th>Setting Value</th><th>FCMP0, FCMP1</th><th>FCMP2 to FCMP9</th></tr>
<tr><td>0</td><td colspan="2">Selection</td></tr>
<tr><td>1</td><td colspan="2">FCMPANn0</td></tr>
<tr><td>2</td><td>FCMPANn1</td><td rowspan="2">Setting Disable</td></tr>
<tr><td>Other than</td><td>Setting Disable</td></tr>
</table></td></tr>
<tr><td>FCMPnCMPSDCTL</td><td>CMPMD</td><td>0</td><td>Comparison operation mode
<table>
<tr><th>CMP MD</th><th>DIAG MD</th><th>Mode</th><th>Explanation</th></tr>
<tr><td>0</td><td>0</td><td>Comparison mode 1</td><td>Compare by the threshold of two level (Upper/Lower-limit threshold)</td></tr>
<tr><td>0</td><td>1</td><td>Setting Disable</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>Comparison mode 2</td><td>Compare by the threshold of one level (FCMPnDACCFG0.SLVAL)</td></tr>
<tr><td>1</td><td>1</td><td>Self-diagnosis mode</td><td>Self-diagnosis of six modes</td></tr>
</table></td></tr>
<tr><td rowspan="2">FCMPnCMPSDCTL</td><td>CMPRPLDN</td><td>0</td><td>Pulldown reference input of comparator for self-defense mode.
0: No operation
1: Pulldown</td></tr>
<tr><td>CMPRPLUP</td><td>0</td><td>Pullup refence input of comparator for Self-defense mode.
0: No operation
1: Pullup</td></tr>
</table>

Unit Name	Register Name	Bit Name	Setting Value	Function
		CMPIPLDN	0	Pulldown comparator input for self-reference mode. 0: No operation 1: Pulldown
		CMPIPLUP	0	Pullup comparator input of self-diagnosis. 0: No operation 1: Pullup
	FCMPnIOSDCTL	IOPLV	0	Pullup or pulldown IO self-diagnosis. 0: Pulldown 1: Pullup
	FCMPnACCCFG0	SLLMTYP[1:0]	1	Select low-side MOSFET signal output format. 0: Low level output 1: High level output 2: CMPO output 3: CMPO inversion output Use initial value “0” in comparison mode 2.
		SLHMTYP[1:0]	1	Select high-side MOSFET signal output format. 0: Low level output 1: High level output 2: CMPO output 3: CMPO inversion output Use initial value “0” in comparison mode 2.
		BMDLY[7:0]	0	Set delay time when boost MOSFET signal changed to high level from low level. Calculation formula of delay time is the following. Delay Time = BMDLY[7:0] * 25ns (clkcmp：40MHz) Use initial value “0” in comparison mode 2.
		SLBMTYP[1:0]	1	Select high-side MOSFET signal output format. 0: Low level output 1: High level output 2: CMPO output 3: CMPO inversion output Use initial value “0” in comparison mode 2.
	FCMPnDACCFG0	SLVAL	1	Start threshold of comparison 0: Lower-limit threshold DACVL[11:0] 1: Upper-limit threshold DACVH[11:0]
		DACVH	4095*4/5	Comparison operation upper-limit threshold of DAC data value.
		SLSET	0	DAC data update by comparison result changing 0: Disable 1: Enable Set “0” to SLSET bit in comparison mode 2.
		DACVL[11:0]	4095*2/5	Comparison operation lower-limit threshold of DAC data value.

Unit Name	Register Name	Bit Name	Setting Value	Function
	FCMPnDUITCTL	DACUPIT[5:0]	5	Interval time for inputting of DAC data DAC data update interval time = DACUPIT[5:0] * 200ns (Minimum: 1us, Maximum: 12.6us)

(c) PORT Initial Setting Function

Enable the actuator current control signal output pin in dual function setting of PORT. The dual-function setting is not required since the analog input pin FCMPAN00 pin is assigning to the special function of the AN250 pin.

Table 3-5 PORT Initial Setting

Unit Name	Register Name	Bit Name	Setting Value	Function
PORT0	PCR10_3	PFCEAE10_3	0	P10_3 dual pin 2 output (FCMPU0_T1)
		PFCAE10_3	0	
		PFCE10_3	1	
		PFC10_3	0	
		PM10_3	0	
	PCR10_4	PFCEAE10_4	0	P10_4 dual pin 2 output (FCMPU0_T2)
		PFCAE10_4	0	
		PFCE10_4	1	
		PFC10_4	0	
		PM10_4	0	
	PCR10_5	PFCEAE10_5	0	P10_5 dual pin 2 output (FCMPU0_T3)
		PFCAE10_5	0	
		PFCE10_5	1	
		PFC10_5	0	
		PM10_5	0	

(d) sDMAC Initial Setting Function

Table 3-6 sDMAC Initial Setting Function

Unit Name	Register Name	Bit Name	Initial Setting	Function
PBG60	PBGPROT0_9	GEN	1	Protection setting enable/disable 0: Protection disable 1: Protection enable
		DBG	1	R/W enable setting of debag master 0: Depending on other enable/disable setting 1: R/W disable
		UM	0	R/W disable setting of user mode 0: R/W disable 1: Depending on other enable/disable setting
		WG	0	Write global enable 0: In writing, use PBGPROT1_9 as determination condition 1: In writing, not use PBGPROT1_9 as determination condition
		RG	1	Read global enable 0: In reading, use PBGPROT1_9 as determination condition 1: In reading, not use PBGPROT1_9 as determination condition
	PBGPROT1_9	SPID28	1	Enable to access bus master of SPID=m by SPIDm bit=1. In this operation example, enable the accesses of bus master ・sDMAC0 (SPID=28) ・CPU0 (SPID=0)
		SPID0	1	
SDMAC0	DMA0CM_0	SPID[4:0]	0x1C	SPID=0x1C (initial value)

Unit Name	Register Name	Bit Name	Initial Setting	Function
		UM	0	0: Supervisor mode 1: User mode
	DMA0SAR_0	SAR[31:0]	Address of dacdata[0]	Transfer source address
	DMA0DAR_0	DAR[31:0]	Address of FCMP0ACCCFG0 register	Transfer source address
	DMA0TSR_0	TSR[31:0]	8	Transfer size: 4 bytes × 2 times＝8byte
	DMA0TMR_0	TRS	1	DMA Transfer Request 0: Automatic request 1: Hardware
		DM	1	Transfer destination address mode 0: Fixed 1: Increment by transfer size
		SM	0	Transfer source address mode 0: Fixed 1: Increment by transfer size
		DTS[3:0]	2	Transfer size 0000_B: 1 byte 0001_B: 2 bytes 0010_B: 4 bytes 0011_B: 8 bytes 0100_B: 16 bytes 0101_B: 32 bytes 0110_B: 64 bytes Other than: Setting disable
		STS[3:0]	3	Transfer size 0000_B: 1 byte 0001_B: 2 bytes 0010_B: 4 bytes 0011_B: 8 bytes 0100_B: 16 bytes 0101_B: 32 bytes 0110_B: 64 bytes Other than: Setting disable
	DMA0RS_0	TC[15:0]	2	Transferring times for each HW request
		TL[2:0]	1	Transferring limitation for each HW request 000: Transfer size is DMAjTMR_n.STS * DMAjRS_n.TC (When PLE = 1, setting disable) 001: Transfer size is DMAjTMR_n.DTS * DMAjRS_n.TC(when PLE = 0, setting disable) 010: Transfer size is DMAjTSR_n.TSR 011: Until DSE or TE flag is asserted 100: Until TE flag is asserted. Other than: Setting disable

Unit Name	Register Name	Bit Name	Initial Setting	Function
		FPT	0	First preload trigger 0: In DE=1 setting, first preload 1: When assert is HW request, start first preload
		PLE	1	Preload enable 0: Disable 1: Enable
		DRQI	0	DMA request initialization for descriptor setting loading 0: Initialize DRQ to disable 1: Initialize DRQ to enable
		RS[7:0]	101	DMA request source In this operation example, Set FCMP0_DACDATACHG(sDMAC transfer source no.101).
	DMA0CHFCR_0	—	0x0000320F	All flag clear
	DMA0OR	DME	1	All channel DMA transfer enable
	DMA0CHCR_0	DE	1	Transfer enable

(e) PIC Initial Setting Function

Connect the compare result interrupt (fcmpu_int_req) of FCMP0 to GTM_TIM0_IN0 inputting. Connect the compare result interrupt from other modules of FCMP to GTM_ATOM0_OUT0 output. OPBT8 is required to set in Serial Programing Mode.

Table 3-7 PIC Initial Setting

Unit Name	Register Name	Bit Name	Setting Vale	Function
PIC2	PIC2GTMINEN0	PIC2GTMINEN0[8:0]	166	Connect FCMP0 comparison result interrupt to GTM timer input signal (GTM_TIM0_IN0).
	PIC2FCMPISEN0	PIC2FCMPISEN0[7:0]	97	Connect GTM_ATOM0_OUT0 to FCMP0 DAC data update request from other modules.
FLASH	OPBT8	ATU_GTM_SEL	0	0: ATU disable, GTM enable 1: ATU enable, GTM disable

(f) GTM Initial Setting Function

Table 3-8 Operation Clock Operation Clock

Unit Name	Register Name	Bit Name	Setting Value	Function
SYSCTRL	MSR_GTM	MS_GTM_0	0	Clock supply of GTM0, E7GTmn(m=0-11,n=0,1), GTM0_1 0: Clock supply 1: Clock stop

Table 3-9 Cluster Clock

Unit Name	Register Name	Bit Name	Setting Value	Function
GTM0	GTM_CLS_CLK_CFG	CLS0_CLK_DIV	2	Set cluster clock (CLS0_CLK). 00_B: Cluster enable 01_B: Cluster enable (MainClock=200MHz) 10_B: Cluster enable(MainClock/2=100MHz)

Table 3-10 CMU

Unit Name	Register Name	Bit Name	Setting Value	Function
GTM0	CMU_GCLK_NUM	GCLK_NUM	1	CMU_CLK_RES0 = (CLS0_CLK / (GCLK_NUM / GCLK_DEN)) / (CLK_CNT+1) =100MHz
	CMU_GCLK_DEN	GCLK_DEN	1	
	CMU_CLK_0_CTRL	CLK_CNT	0	
	CMU_CLK_EN	EN_CLK0	2	CMU_CLK_RES0 enable/disable setting 00_B: Disable status (Writing is denied.) 01_B: Disabling 10_B: Enabling 11_B: Enabling status (Writing is denied.)

Table 3-11 CCM0

Unit Name	Register Name	Bit Name	Setting Value	Function
GTM0	CCM0_CMU_CLK_CFG	CLK0_SRC	0	Select clock source of CCM0_CLK_RESk. 000_B: CMU_CLK_RES0 001_B: CMU_CLK_RES8 010_B: TIM0 の TIM_EXT_CAPTURE0

Table 3-12 TBU CH0

Unit Name	Register Name	Bit Name	Setting Value	Function
GTM0	TBU_CH0_CTRL	CH_CLK_SRC	0	Select clock source of TBU CH0 000_B: CCM0_CLK_RES0 001_B: CCM0_CLK_RES1 010_B: CCM0_CLK_RES2 011_B: CCM0_CLK_RES3 100_B: CCM0_CLK_RES4 101_B: CCM0_CLK_RES5 110_B: CCM0_CLK_RES6 111_B: CCM0_CLK_RES7
		LOW_RES	0	Resolution of TBU_CH0_BASE register 0: Bit 23-0 of lower counter 1: Bit 26-3 of upper counter
	TBU_CH0_BASE	BASE[26:0]	0x0	Counter value setting of TBU CH0

Table 3-13 TBU

Unit Name	Register Name	Bit Name	Setting Value	Function
GTM0	TBU_CHEN	ENDIS_CH0	2	Disable/enable TBU CH0 00_B: Disable status (Writing is denied.) 01_B: Disable 10_B: Enable 11_B: Enable (Writing is denied.)

Table 3-14 TIM0 CH0

Unit Name	Register Name	Bit Name	Setting Value	Function
GTM0	TIM0_CH0_CTRL	CLK_SEL	0	CMU clock source selection
		ISL	0	Set edge of detection target.
		DSL	1	

CMU clock source selection

TIM0_CH0_ECTRL.ECLK_SEL	CLK_SEL	CMU Clock Source
0	000_B	CCM0_CLK_RES0
	001_B	CCM0_CLK_RES1
	010_B	CCM0_CLK_RES2
	011_B	CCM0_CLK_RES3
	100_B	CCM0_CLK_RES4
	101_B	CCM0_CLK_RES5
	110_B	CCM0_CLK_RES6
	111_B	CCM0_CLK_RES7
1	000_B	TDU_SAMPLE_EVT
	Other than	Setting disable

Set edge of detection target.

ISL	DSL	Edge of Detection Target
0	0	Falling edge
	1	Rising edge
1	X	Bothe edge

<table>
<tr><th>Unit Name</th><th>Register Name</th><th>Bit Name</th><th>Setting Value</th><th>Function</th></tr>
<tr><td rowspan="8"></td><td rowspan="8"></td><td>CNTS_SEL</td><td>0</td><td>Select storing contents of TIM0_CH0_CNTS register.
0: TIM0_CH0_CNT register
1: TIM_TBU_TS0</td></tr>
<tr><td>EGPR1_SEL</td><td>1</td><td rowspan="2">Set storing contents of GPR1 register.
<table>
<tr><th>EGPR0</th><th>GPR0_SEL</th><th>Storing Contents</th></tr>
<tr><td rowspan="4">0</td><td>00_B</td><td>TIM_TBU_TS0</td></tr>
<tr><td>01_B</td><td>TIM_TBU_TS1</td></tr>
<tr><td>10_B</td><td>TIM_TBU_TS2</td></tr>
<tr><td>11_B</td><td>TIM0_CH0_CNT</td></tr>
<tr><td rowspan="3">1</td><td>00_B</td><td>TIM0_CH0_ECNT</td></tr>
<tr><td>01_B</td><td>TIM0_INP_VAL</td></tr>
<tr><td>Other than</td><td>Setting disable</td></tr>
</table></td></tr>
<tr><td>GPR1_SEL</td><td>1</td></tr>
<tr><td>EGPR0_SEL</td><td>0</td><td rowspan="2">Set storing contents of GPR0 register.
<table>
<tr><th>EGPR0</th><th>GPR0_SEL</th><th>Storing Contents</th></tr>
<tr><td rowspan="4">0</td><td>00_B</td><td>TIM_TBU_TS0</td></tr>
<tr><td>01_B</td><td>TIM_TBU_TS1</td></tr>
<tr><td>10_B</td><td>TIM_TBU_TS2</td></tr>
<tr><td>11_B</td><td>TIM0_CH0_CNTS</td></tr>
<tr><td rowspan="3">1</td><td>00_B</td><td>TIM0_CH0_ECNT</td></tr>
<tr><td>01_B</td><td>TIM0_INP_VAL</td></tr>
<tr><td>Other than</td><td>Setting disable</td></tr>
</table></td></tr>
<tr><td>GPR0_SEL</td><td>0</td></tr>
<tr><td>TBU0_SEL</td><td>0</td><td>Select TIM_TBU_TS0 bit inputting stored to TIM0_CH0_GPR0/TIM0_CH0_GPR1.
0: TIM_TBU_TS0[23:0]
1: TIM_TBU_TS0[26:3]</td></tr>
<tr><td>CICTRL</td><td>0</td><td>Channel input control
0: TIM0 CH0 input (GTM_TIM0_IN0
1: TIM6 CH7 input (GTM_TIM6_IN7)</td></tr>
<tr><td>ARU_EN</td><td>1</td><td>ARU transfer TIM0_CH0_GPR0 and TIM0_CH0_GPR1 register value.
0: Disable
1: Enable</td></tr>
</table>

Unit Name	Register Name	Bit Name	Setting Value	Function
		TIM_MODE	2	Channel Mode 000_B : PWM Measurement Mode (TPWM) 001_B : Pulse Integration Mode (TPIM) 010_B : Input Event Mode (TIEM) 011_B : Input Prescaler Mode (TIPM) 100_B : Bit Compression Mode (TBCM) 101_B : Gated Periodic Sampling Mode (TGPS) 110_B : Serial Shift Mode (TSSM) 111_B : Setting disable
		TIM_EN	1	Channel enable/disable setting 0: Disable 1: Enable
	TIM0_CH0_ECTRL	ECLK_SEL	0	Refer to TIM0_CH0_CTRL.CLK_SEL bit.

Table 3-15 ATOM0 CH0

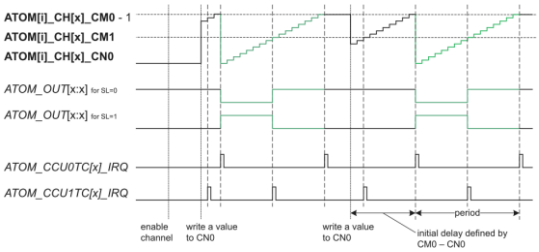
Unit Name	Register Name	Bit Name	Setting Value	Function
GTM0	ATOM0_CH0_CTRL	SOMB	0	0: SOMB mode disable 1: SOMB mode enable
		OSM	1	Set one-shot count-up mode for only soft trigger.  Refer to *GTM IP Specification Figure 98* for details.
		EXT_TRIG	0	
		OSM_TRIG	0	
		RST_CCU0	0	
		UDMODE	0	
		CLK_SRC	0	Counter clock source 0000_B: CCM0_CLK_RES0 0001_B: CCM0_CLK_RES1 0010_B: CCM0_CLK_RES2 0011_B: CCM0_CLK_RES3 0100_B: CCM0_CLK_RES4 0101_B: CCM0_CLK_RES5 0110_B: CCM0_CLK_RES6 0111_B: CCM0_CLK_RES7 1101_B: ATOM_CH_TRIGOUT[x-1] 1110_B: EXT_TRIGIN Other than: Setting disable
		SL	1	Initial signal level 0: High 1: Low
		MODE	2	Channel mode setting 0 : SOMI mode 1 : SOMC mode 2 : SOMP mode 3 : SOMS mode
	ATOM0_CH0_CM0	CM0[23:0]	5	ATOM CCU0 compare register
	ATOM0_CH0_CM1	CM1[23:0]	5	ATOM CCU1 compare register

Table 3-16 ATOM0

Unit Name	Register Name	Bit Name	Setting Value	Function
GTM0	ATOM0_AGC_OUTEN_STAT	OUTEN_STAT0	2	GTM_ATOM0_OUT0 output enable/disable 00_B: Don't care (Writing is denied.) 01_B: Output disable 10_B: Output enable 11_B: Don't care (Writing is denied.)
	ATOM0_AGC_ENDIS_STAT	ENDIS_STAT0	2	ATOM0 CH0 enable/disable Setting 00_B: Don't care (Writing is denied.) 01_B: Channel disable 10_B: Channel enable 11_B: Don't care (Writing is denied.)

Table 3-17 MCS0 CH0

Unit Name	Register Name	Bit Name	Setting Value	Function
GTM0	MCS0_CH0_PC	-	0x2000	Initial PC of MCS0 CH0 In this operation example, allocate MCS program to 0x2000 of MCS0 RAM0.
GTM0	MCS0_CH0_CTRL	EN	1	MCS0 CH0 disable/enable 0: Disable 1: Enable

3.1.3.3 Operation Flow

The following shows the flowchart in this operation example.

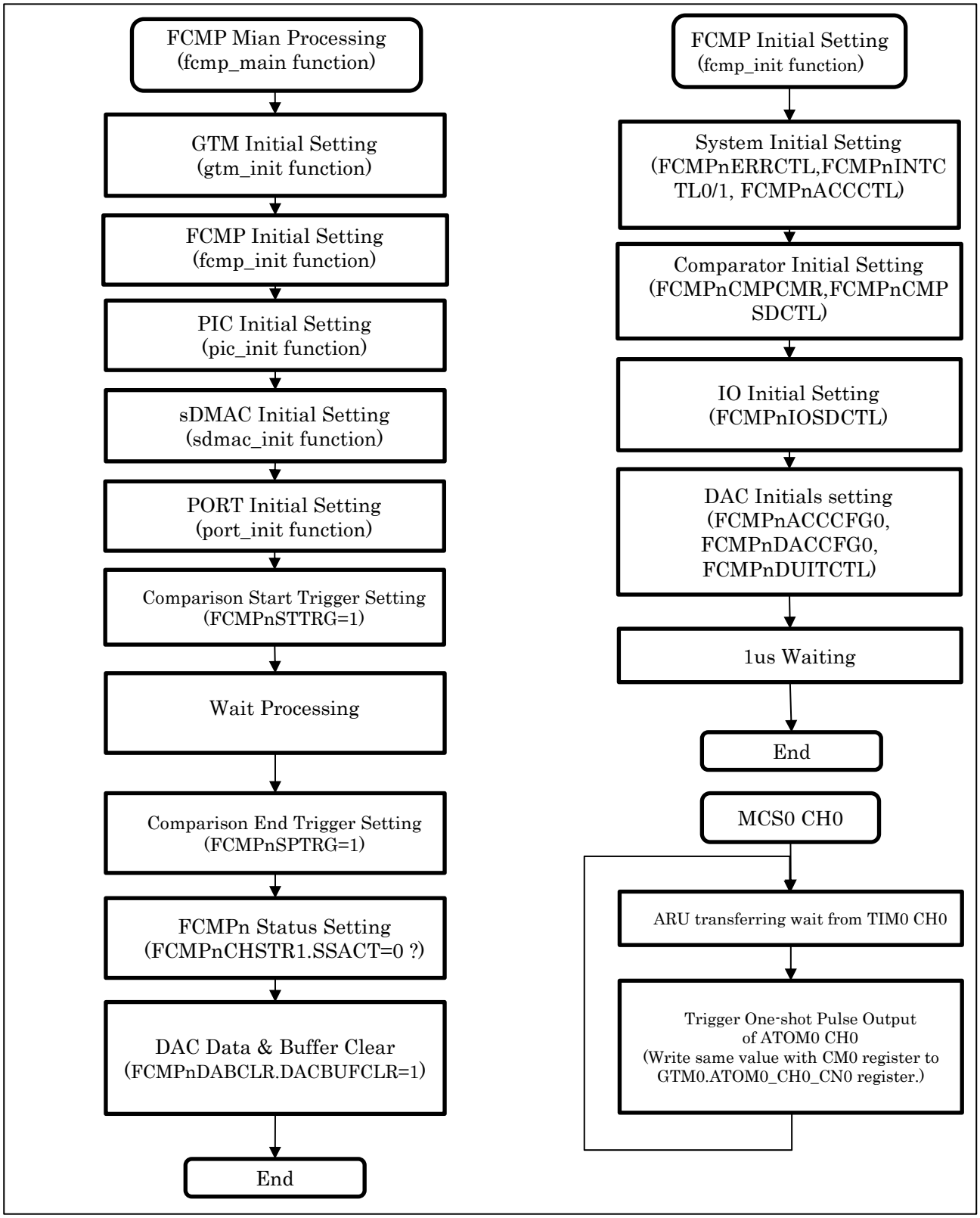
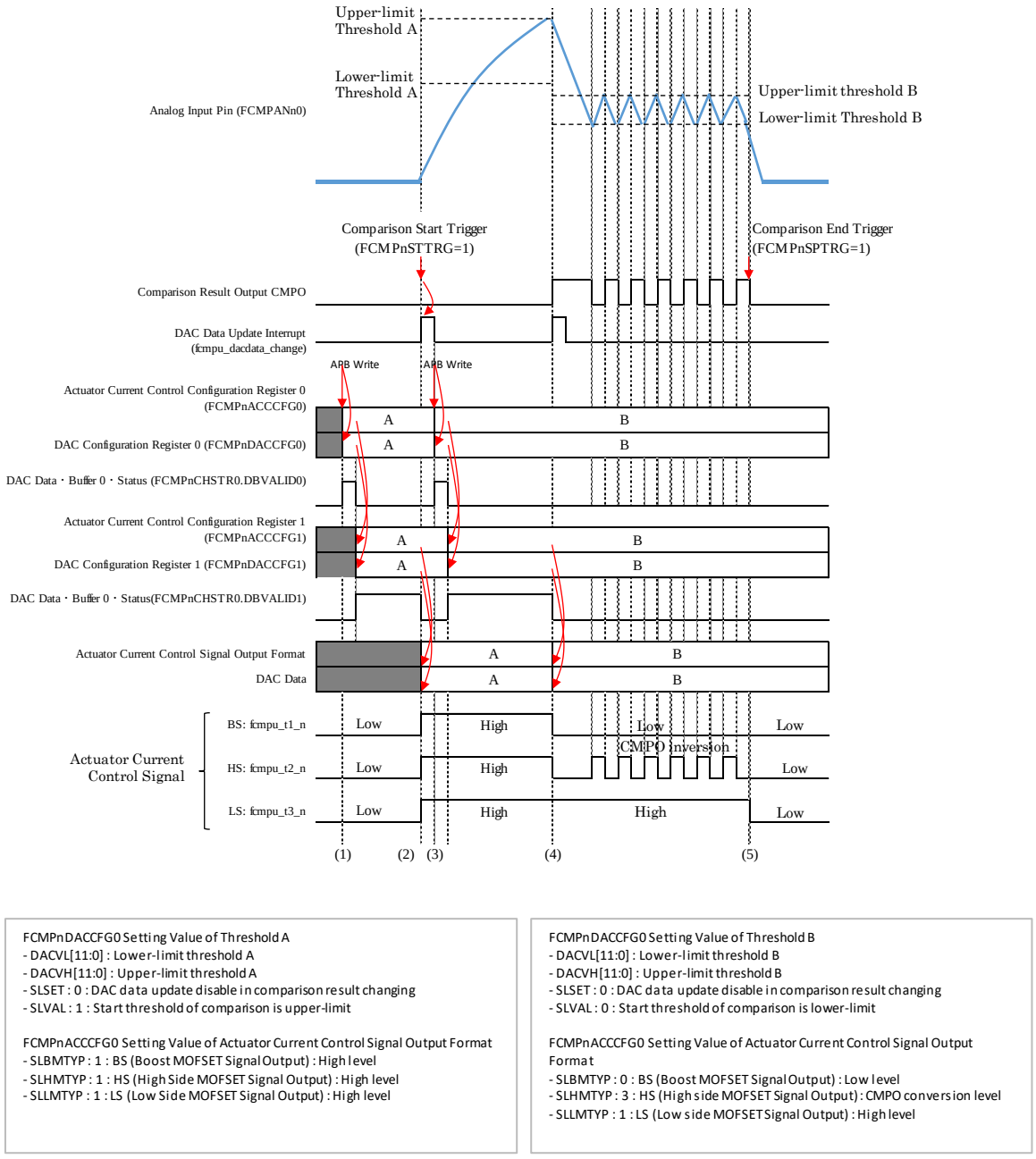


Figure 3-4 Operation Flow

3.2 Actuator Current Control by Comparator Output

3.2.1 Specification Overview

In this operation example, change the actuator current control signal output of FCMP0 by the comparator output and the comparison threshold with the analog input pin voltage by using GTM and FCMP0 mode1 of FCMP0. The comparison threshold changing is executed when the voltage of the analog input signal is exceeded the upper-limit threshold at the first time.



FCMPnDACCFG0 Setting Value of Threshold A
- DACVL[11:0] : Lower-limit threshold A
- DACVH[11:0] : Upper-limit threshold A
- SLSET : 0 : DAC data update disable in comparison result changing
- SLVAL : 1 : Start threshold of comparison is upper-limit

FCMPnACCCFG0 Setting Value of Actuator Current Control Signal Output Format
- SLBMTYP : 1 : BS (Boost MOFSET Signal Output) : High level
- SLHMTYP : 1 : HS (High Side MOFSET Signal Output) : High level
- SLLMTYP : 1 : LS (Low Side MOFSET Signal Output) : High level

FCMPnDACCFG0 Setting Value of Threshold B
- DACVL[11:0] : Lower-limit threshold B
- DACVH[11:0] : Upper-limit threshold B
- SLSET : 0 : DAC data update disable in comparison result changing
- SLVAL : 0 : Start threshold of comparison is lower-limit

FCMPnACCCFG0 Setting Value of Actuator Current Control Signal Output Format
- SLBMTYP : 0 : BS (Boost MOFSET Signal Output) : Low level
- SLHMTYP : 3 : HS (High side MOFSET Signal Output) : CMPO conversion level
- SLLMTYP : 1 : LS (Low side MOFSET Signal Output) : High level

Figure 3-5 Actuator Current Control by Comparator Output

[Procedure]

(1) Write the actuator current control signal output format A to FCMPnACCCFG0 register and the DAC data A to FCMPnDACCFG0 register.

(2) Issue the comparison start trigger (FCMPnSTTRG=1).

In the time, FCMPn executes the follows.

- Start comparing the analog input and the upper-limit threshold of the DAC data A.
- Output the current control signal according to the actuator current control signal output format A.
- Issue the DAC data update interrupt (fcmpu_dacdata_change).

(3) By the DMA transmitting the DAC data update interrupt to the trigger, write the actuator current control signal output format B to FCMPnACCCFG0 register and the DAC data B to FCMPnDACCFG0 register.

(4) When the voltage of the analog input pin (FCMPANn0) is exceeded the upper-limit threshold on the DAC data, FCMPn execute the following.

- Start comparing the lower-limit threshold between the analog input and DAC data B.
- Output the current control signal according to the actuator current control signal output format B.
- Issue the data update interrupt (fcmpu_dacdata_change).

(5) Issue the comparison end trigger (FCMPnSPTRG).

In this operation example, set the upper/lower-limit threshold of DAC data A//B.

DAC Data Threshold	DAC Data A	DAC Data B
Upper-limit threshold [V]	4V	3V
Lower-limit threshold [V]	2V	2V

3.2.2 System Configuration

3.2.2.1 Overview

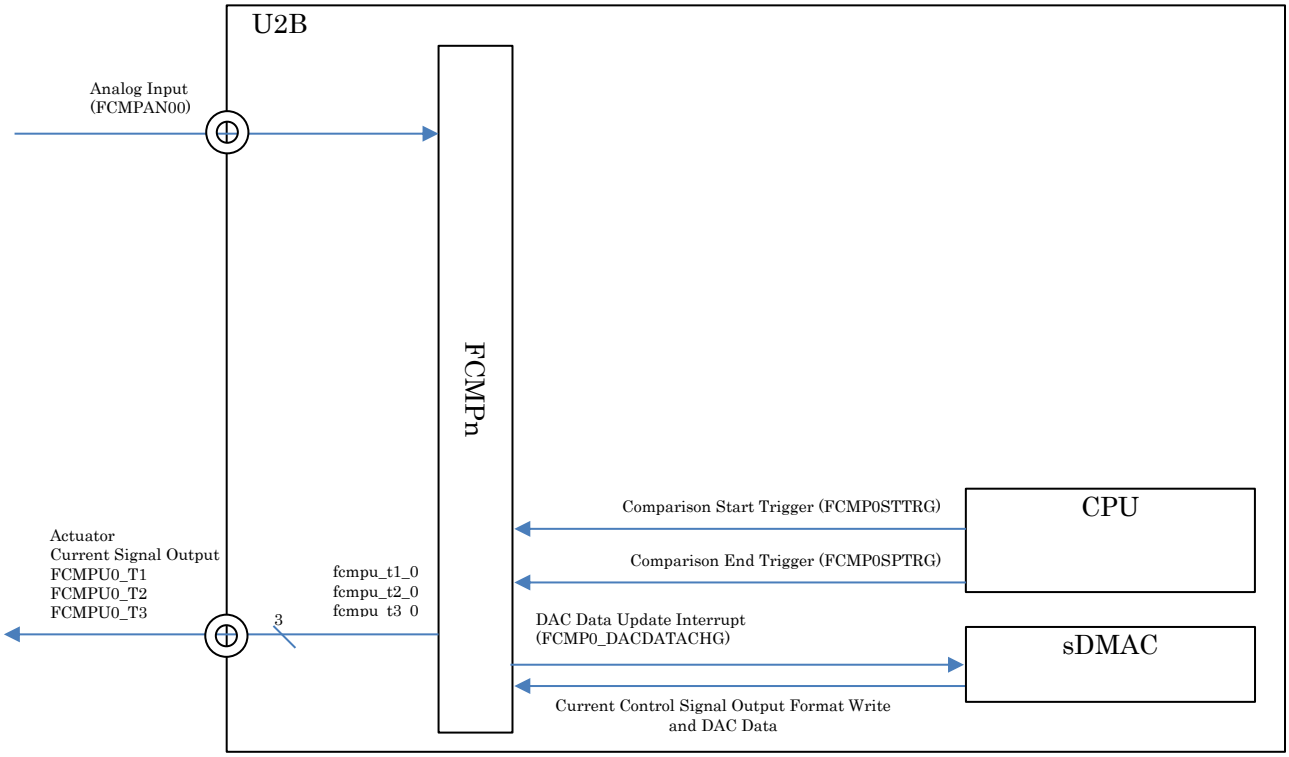


Figure 3-6 System Configuration (Overview)

3.2.3 Software Explanation

3.2.3.1 Module Explanation

The module list in this operation example is shown below.

Table 3-18 Module

Module Name	Function Name	Function
FCMP main function	fcmp_main	Execute main processing in this operation example.
FCMP initial setting function	fcmp_init	Initial set FCMP.
sDMAC initial setting function	sdmac_init	Write actuator current control signal output format and DAC data by DMA transfer in FCMPn_DACDATACHG interrupting.
PORT initial setting function	port_init	Initial set PORT.

3.2.3.2 Register Setting

The following shows the register setting for each function.

(a) FCMP Main Function

Table 3-19 FCMP Main (n=0)

Unit Name	Register Name	Bit Name	Setting Value	Function
FCMPn	FCMPnSTTRG	CHSTRQ	1	0: No operation 1: Comparison start request
	FCMPnSPTRG	CHSPRQ	1	0: No operation 1: Comparison end request
	FCMPnDACBCLR	DACBUFCLR	1	0: No operation 1: Clear Clear the enable status (FCMPnCHSTR0.DBVALID1 and DBVALID0 bit) of FCMPnDACCFG0 and FCMPnDACCFG1.

(b) FCMP Initial Setting Function

Table 3-20 FCMP Initial Setting (n=0)

Unit Name	Register Name	Bit Name	Setting Value	Function
SYSCTRL	MSR_FCOMP	MS_FCOMP_0	0	Clock Supply of FCMPC 0: Clock supply 1: Clock stop
		MS_FCOMP_1	0	Clock supply of FCMP0 0: Clock supply 1: Clock stop
	MSR_RDC	MS_RDC_2	1	Clock supply of RDC3AL0 0: Supply clock to RDC3AL0. 1: Supply clock to RDC3AL0. Set the above when using FCMP of U2B6. For the details, refer to "*RH850/U2B User's Manual 53.5.4 Notes on Using FCMP or RDC3AL*".
		MS_RDC_3	1	Clock supply of RDC3AL1 0: Supply clock to RDC3AL1. 1: Not supply clock to RDC3AL1. Set the above when using FCMP of U2B6. For the details, refer to "*RH850/U2B User's Manual 53.5.4 Notes on Using FCMP or RDC3AL*".
RDC3AL	RDC3AL0RDSTP	-	0x00000001	Stop R/D Converter. Set the above when using FCMP of U2B6. For the details, refer to "*RH850/U2B User's Manual 53.5.4 Notes on Using FCMP or RDC3AL*".
	RDC3AL1RDSTP	-	0x00000001	

Unit Name	Register Name	Bit Name	Setting Value	Function
FCMPC	FCMPCTRGCTL	STENn	0	External trigger input for comparison starts (ext_start_trg_n) 0: Disable 1: Enable
	FCMPCSYSTCTL	SYSTENn	0	Synchronization comparison start request 0: Disable 1: Enable
FCMPn	FCMPnERRCTL	EMPEN	0	Empty error interrupt output (fcmpu_err_req) 0: Disable 1: Enable
		PREN	0	Parity error interrupt output (fcmpu_err_req) 0: Disable 1: Enable
		IDEN	0	ID error interrupt output (fcmpu_err_req) 0: Disable 1: Enable
	FCMPnINTCTL0	ILHEN	0	Comparison result interrupt detection when threshold exceeds comparison result 0: Disable 1: Enable
		ILLEN	0	Comparison result interrupt detection when threshold decreases below comparison result. 0: Disable 1: Enable
		ITHLEN	0	Comparison result interrupt detection when comparison result transferring to low from high. 0: Disable 1: Enable
		ITLHEN	0	Comparison result interrupt detection when comparison result transferring to high from low. 0: Disable 1: Enable
		INTMD	0	Interrupt output mask when FCMPnINTSTR.INTF=1 0: Disable 1: Enable
		INTEN	0	Comparison result interrupt output (fcmpu_int_req) 0: Disable 1: Enable When this bit is set “1”, interrupt output is generated when either of follows is enabled. ・FCMPnILHEN bit ・FCMPnILLEN bit ・FCMPnITHLEN bit ・FCMPnITLHEN bit

<table>
<tr><th>Unit Name</th><th>Register Name</th><th>Bit Name</th><th>Setting Value</th><th>Function</th></tr>
<tr><td></td><td>FCMPnINTCTL1</td><td>DACDFEN</td><td>1</td><td>DAC data update interrupt output (fcmpu_dacdata_change)
0: Disable
1: Enable</td></tr>
<tr><td></td><td>FCMPnACCCTL</td><td>ACCEN</td><td>1</td><td>Actuator current control signal output
0: Disable
1: Enable
・fcmpu_t1_n
(Boost MOSFET Control Signal)
・fcmpu_t2_n
(High Side MOSFET Control Signal)
・fcmpu_t3_n
(Low Side MOSFET Control Signal)</td></tr>
<tr><td></td><td>FCMPnCMPCMR</td><td>CMPWAIT[3:0]</td><td>3</td><td>Set the standby time until DAC setting time from the DAC data update timing. Calculation formula of standby time is follows.
Standby time = CMPWAIT[3:0]*200ns
CMPWAIT[3:0] is needed to set more than “3”.</td></tr>
<tr><td></td><td></td><td>DIAGMD</td><td>0</td><td>Refer to CMPMD bit</td></tr>
<tr><td></td><td></td><td>CMPCHS[2:0]</td><td>1</td><td>Analog Input Selection
<table>
<tr><th>Setting Value</th><th>FCMP0, FCMP1</th><th>FCMP2 to FCMP9</th></tr>
<tr><td>0</td><td colspan="2">Selection</td></tr>
<tr><td>1</td><td colspan="2">FCMPANn0</td></tr>
<tr><td>2</td><td>FCMPANn1</td><td rowspan="2">Setting Disable</td></tr>
<tr><td>Other than</td><td>Setting Disable</td></tr>
</table></td></tr>
<tr><td></td><td></td><td>CMPMD</td><td>0</td><td>Comparison operation mode
<table>
<tr><th>CMP MD</th><th>DIAG MD</th><th>Mode</th><th>Explanation</th></tr>
<tr><td>0</td><td>0</td><td>Comparison mode 1</td><td>Compare by the threshold of two level (Upper/Lower-limit threshold)</td></tr>
<tr><td>0</td><td>1</td><td>Setting Disable</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>Comparison mode 2</td><td>Compare by the threshold of one level (FCMPnDACCFG0.SLVAL)</td></tr>
<tr><td>1</td><td>1</td><td>Self-diagnosis mode</td><td>Self-diagnosis of six modes</td></tr>
</table></td></tr>
<tr><td></td><td>FCMPnCMPSDCTL</td><td>CMPRPLDN</td><td>0</td><td>Pulldown reference input of comparator for self-defense mode.
0: No operation
1: Pulldown</td></tr>
<tr><td></td><td></td><td>CMPRPLUP</td><td>0</td><td>Pullup refence input of comparator for Self-defense mode.
0: No operation
1: Pullup</td></tr>
</table>

Unit Name	Register Name	Bit Name	Setting Value	Function
		CMPIPLDN	0	Pulldown comparator input for self-reference mode. 0: No operation 1: Pulldown
		CMPIPLUP	0	Pullup comparator input of self-diagnosis. 0: No operation 1: Pullup
	FCMPnIOSDCTL	IOPLV	0	Pullup or pulldown IO self-diagnosis. 0: Pulldown 1: Pullup
	FCMPnACCCFG0	SLLMTYP[1:0]	1	Select low-side MOSFET signal output format. 0: Low level output 1: High level output 2: CMPO output 3: CMPO inversion output Use initial value “0” in comparison mode 2.
		SLHMTYP[1:0]	1	Select high-side MOSFET signal output format. 0: Low level output 1: High level output 2: CMPO output 3: CMPO inversion output Use initial value “0” in comparison mode 2.
		BMDLY[7:0]	0	Set delay time when boost MOSFET signal changed to high level from low level. Calculation formula of delay time is the following. Delay Time = BMDLY[7:0] * 25ns (clkcmp：40MHz) Use initial value “0” in comparison mode 2.
		SLBMTYP[1:0]	1	Select high-side MOSFET signal output format. 0: Low level output 1: High level output 2: CMPO output 3: CMPO inversion output Use initial value “0” in comparison mode 2.
	FCMPnDACCFG0	SLVAL	1	Start threshold of comparison 0: Lower-limit threshold DACVL[11:0] 1: Upper-limit threshold DACVH[11:0]
		DACVH	4095*4/5	Comparison operation upper-limit threshold of DAC data value.
		SLSET	1	DAC data update by comparison result changing 0: Disable 1: Enable Set “0” to SLSET bit in comparison mode 2.
		DACVL[11:0]	4095*2/5	Comparison operation lower-limit threshold of DAC data value.

Unit Name	Register Name	Bit Name	Setting Value	Function
	FCMPnDUITCTL	DACUPIT[5:0]	5	Interval time for inputting of DAC data DAC data update interval time = DACUPIT[5:0] * 200ns (Minimum: 1us, Maximum: 12.6us)

(c) PORT Initial Setting Function

Enable the actuator current control signal output pin in dual function setting of PORT. The dual-function setting is not required since the analog input pin FCMPAN00 pin is assigning to the special function of the AN250 pin.

Table 3-21 PORT Initial Setting

Unit Name	Register Name	Bit Name	Setting Value	Function
PORT0	PCR10_3	PFCEAE10_3	0	P10_3 dual pin 2 output (FCMPU0_T1)
		PFCAE10_3	0	
		PFCE10_3	1	
		PFC10_3	0	
		PM10_3	0	
	PCR10_4	PFCEAE10_4	0	P10_4 dual pin 2 output (FCMPU0_T2)
		PFCAE10_4	0	
		PFCE10_4	1	
		PFC10_4	0	
		PM10_4	0	
	PCR10_5	PFCEAE10_5	0	P10_5 dual pin 2 output (FCMPU0_T3)
		PFCAE10_5	0	
		PFCE10_5	1	
		PFC10_5	0	
		PM10_5	0	

(d) sDMAC Initial Setting Function

Table 3-22 sDMAC Initial Setting

Unit Name	Register Name	Bit Name	Setting Value	Function
PBG60	PBGPROT0_9	GEN	1	Protection setting enable/disable 0: Protection disable 1: Protection enable
		DBG	1	R/W enable setting of debag master 0: Depending on other enable/disable setting 1: R/W disable
		UM	0	R/W disable setting of user mode 0: R/W disable 1: Depending on other enable/disable setting
		WG	0	Write global enable 0: In writing, use PBGPROT1_9 as determination condition 1: In writing, not use PBGPROT1_9 as determination condition
		RG	1	Read global enable 0: In reading, use PBGPROT1_9 as determination condition 1: In reading, not use PBGPROT1_9 as determination condition
	PBGPROT1_9	SPID28	1	Enable to access bus master of SPID=m by SPIDm bit=1. In this operation example, enable the accesses of bus master ・sDMAC0 (SPID=28) ・CPU0 (SPID=0)
		SPID0	1	
SDMAC0	DMA0CM_0	SPID[4:0]	0x1C	SPID=0x1C (initial value)

Unit Name	Register Name	Bit Name	Setting Value	Function
		UM	0	0: Supervisor mode 1: User mode
	DMA0SAR_0	SAR[31:0]	Address of dacdata[0]	Transfer source address
	DMA0DAR_0	DAR[31:0]	Address of FCMP0ACCCFG0 register	Transfer source address
	DMA0TSR_0	TSR[31:0]	8	Transfer size: 4 bytes × 2 times＝8byte
	DMA0TMR_0	TRS	1	DMA Transfer Request 0: Automatic request 1: Hardware
		DM	1	Transfer destination address mode 0: Fixed 1: Increment by transfer size
		SM	0	Transfer source address mode 0: Fixed 1: Increment by transfer size
		DTS[3:0]	2	Transfer size 0000_B: 1 byte 0001_B: 2 bytes 0010_B: 4 bytes 0011_B: 8 bytes 0100_B: 16 bytes 0101_B: 32 bytes 0110_B: 64 bytes Other than: Setting disable
		STS[3:0]	3	Transfer size 0000_B: 1 byte 0001_B: 2 bytes 0010_B: 4 bytes 0011_B: 8 bytes 0100_B: 16 bytes 0101_B: 32 bytes 0110_B: 64 bytes Other than: Setting disable
	DMA0RS_0	TC[15:0]	2	Transferring times for each HW request
		TL[2:0]	1	Transferring limitation for each HW request 000: Transfer size is DMAjTMR_n.STS * DMAjRS_n.TC (When PLE = 1, setting disable) 001: Transfer size is DMAjTMR_n.DTS * DMAjRS_n.TC(when PLE = 0, setting disable) 010: Transfer size is DMAjTSR_n.TSR 011: Until DSE or TE flag is asserted 100: Until TE flag is asserted. Other than: Setting disable

Unit Name	Register Name	Bit Name	Setting Value	Function
		FPT	0	First preload trigger 0: In DE=1 setting, first preload 1: When assert is HW request, start first preload
		PLE	1	Preload enable 0: Disable 1: Enable
		DRQI	0	DMA request initialization for descriptor setting loading 0: Initialize DRQ to disable 1: Initialize DRQ to enable
		RS[7:0]	101	DMA request source In this operation example, Set FCMP0_DACDATACHG(sDMAC transfer source no.101).
	DMA0CHFCR_0	—	0x0000320F	All flag clear
	DMA0OR	DME	1	All channel DMA transfer enable
	DMA0CHCR_0	DE	1	Transfer enable

3.2.3.3 Operation Flow

The following shows the flowchart in this operation example.

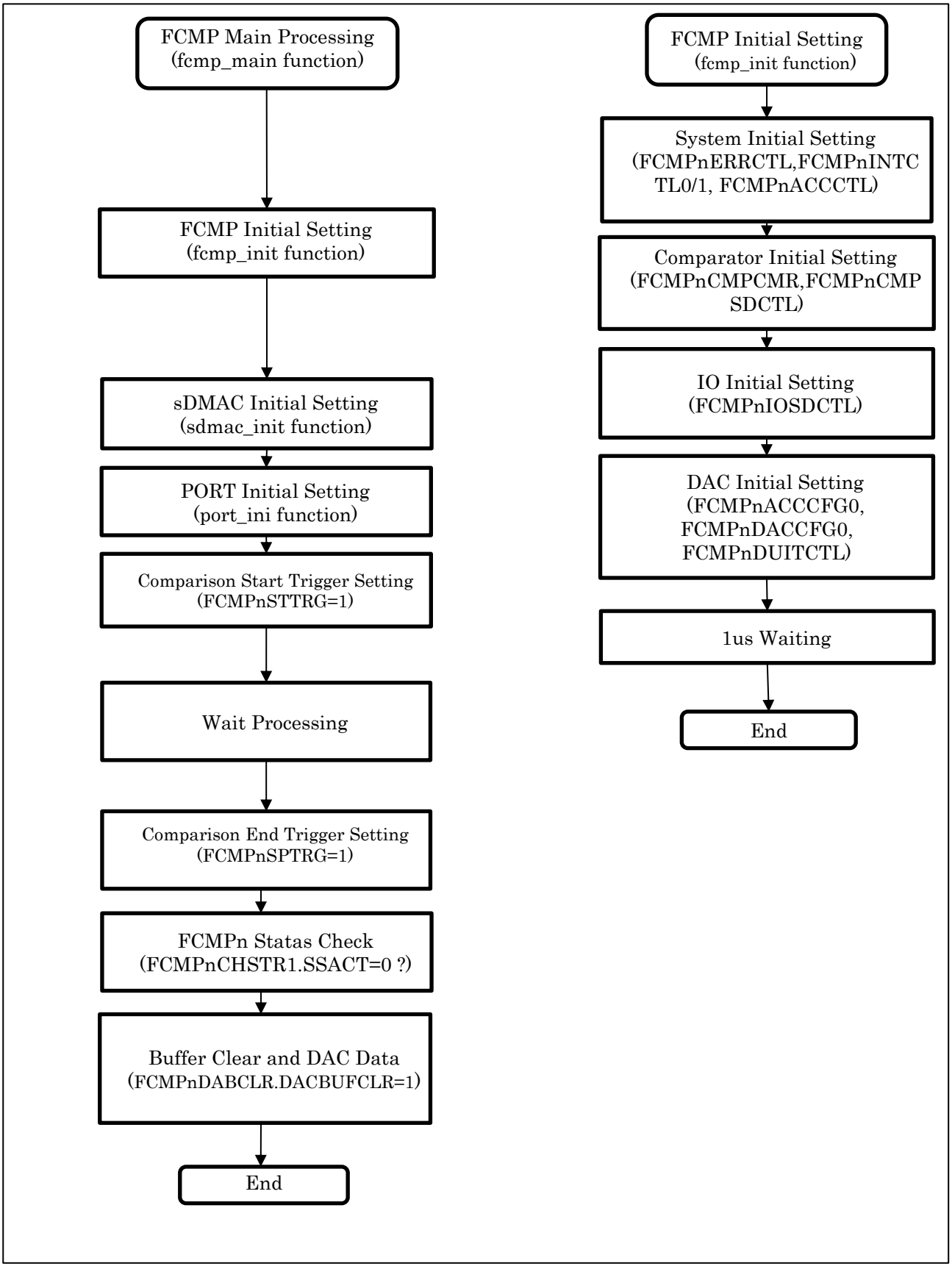


Figure 3-7 Operation Flow

Revision History

Rev.	Date	Description	
		Page	Summary
0.10	2023.12.15	All	Initial edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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